Semiconductors for Television and Video Systems

TDA4685 to μA733C

DATA HANDBOOK

BOOK IC02c 1992

Philips Semiconductors

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Semiconductors for Television and Video Systems

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TDA4660P	64 µs baseband delay line
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TDA8370	synchronization processor for TV receivers
TDA8420	hi-fi stereo audio processor; I²C-bus
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TDA9080	video control combination circuit with automatic cut-off control
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Data sheet	
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date of issue	March 1991

TDA4685

Video processor, with automatic cut-off control

FEATURES

- Operates from an 8 V DC supply
- Black level clamping of the colour-difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two analog RGB inputs, selected either by fast switch signals or the I²C-bus; brightness and contrast control of these RGB inputs
- Saturation, contrast and brightness adjustment via I²C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2- or 3-level sandcastle pulse for clamping, vertical synchronization and cut-off timing pulses
- Automatic cut-off control with picture tube leakage current compensation
- Cut-off measurement pulses after end of the vertical blanking pulse or end of an extra vertical flyback pulse
- Increased RGB signal bandwidths
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting
- PAL/SECAM or NTSC matrix selection via I²C-bus
- Emitter-follower RGB output stages to drive the video output stages
- Hue control output for the TDA4555 or TDA4650

DESCRIPTION

TDA4685 is a monolithic, integrated circuit with a colour-difference interface for video processing in TV receivers. *(continued)*

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	–	60	–	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value)	–	0.45	–	V
$V_{6(p-p)}$	-(B-Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	-(R-Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	three-level sandcastle pulse: H+V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	two-level sandcastle pulse: H+V	–	2.5	–	V
	BK	–	4.5	–	V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)	–	0.7	–	V
$V_{o(p-p)}$	RGB outputs at pins 24,22 and 20 (peak-to-peak value)	–	2.0	–	V
T_{amb}	operating ambient temperature range	0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4685	28	DIL	plastic	SOT117

Video processor, with automatic cut-off control

TDA4685

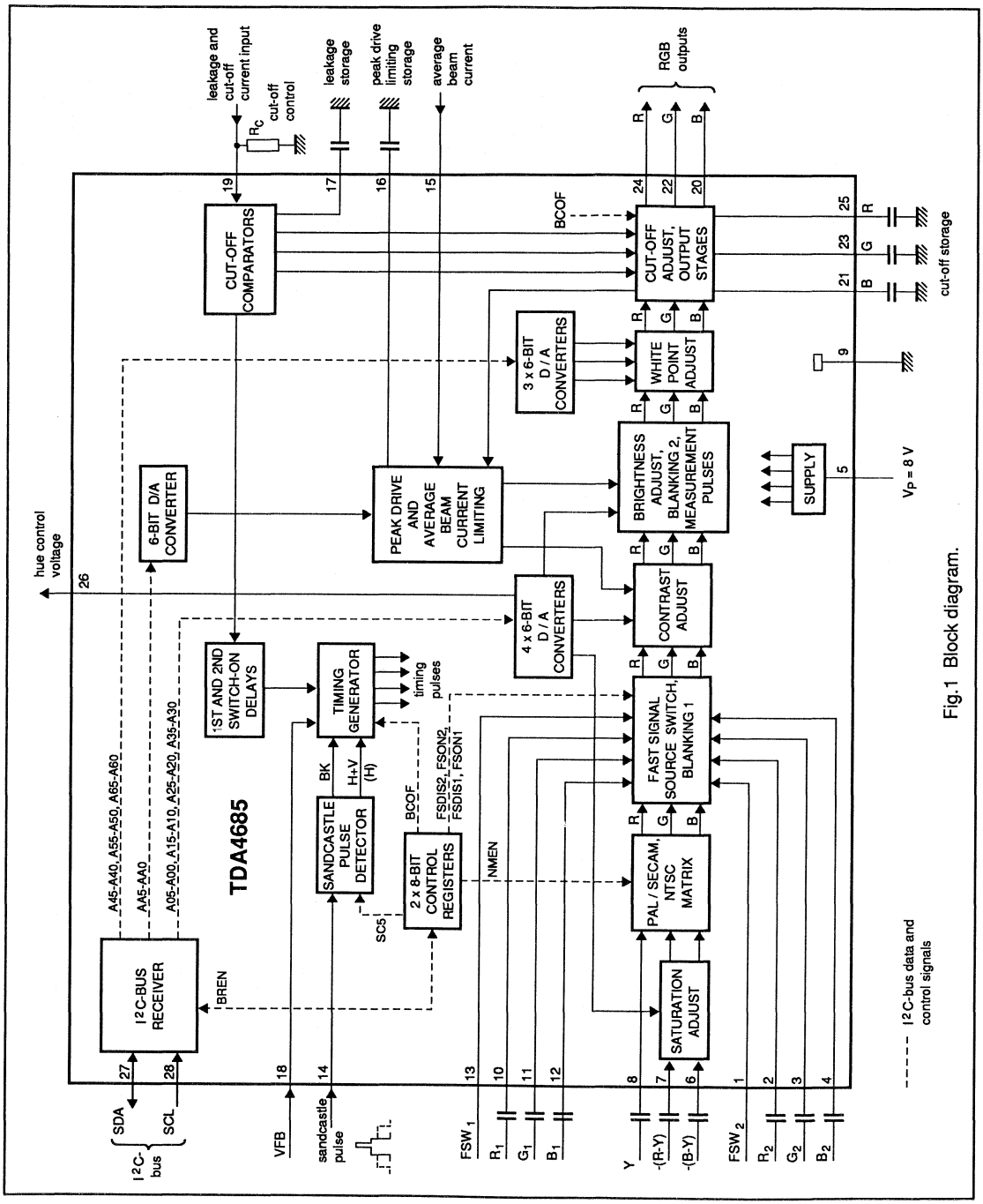


Fig.1 Block diagram.

Video processor, with automatic cut-off control

TDA4685

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
-(B-Y)	6	colour difference input -(B-Y)
-(R-Y)	7	colour difference input -(R-Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input

SYMBOL	PIN	DESCRIPTION
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current
V_{FB}	18	vertical flyback pulse input
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I^2C-bus serial data input/output
SCL	28	I^2C-bus serial clock input

DESCRIPTION (continued)

Its primary function is to process the luminance and colour-difference signals from multistandard colour decoders, TDA4650/TDA4660 or TDA4555, Colour Transient Improvement (CTI) IC, TDA4565, Picture Signal Improvement (PSI) IC, TDA4670, or from a Feature Module.

The required input signals are:

- luminance and negative colour-difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I^2C-bus data and clock signals for microprocessor control.

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector and the other from an on-screen display generator. The TDA4685 has I^2C-bus control of all parameters and functions with automatic cut-off control of the picture tube cathode currents. It provides RGB output signals for the video output stages.

The TDA4685 is a simplified, pin compatible (except pin 18) version of the TDA4680. The module address via the I^2C-bus can be used for both ICs; where a function is not included in the TDA4685 then the I^2C-bus command is not executed. The differences with the TDA4680 are:

- no automatic white level control; the white levels are determined directly by the I^2C-bus data
- RGB reference levels for automatic cut-off control are not generated
- clamping delay is fixed
- only contrast and brightness adjust for the RGB input signals
- the measurement lines are triggered either by the trailing edge of the vertical component of the sandcastle pulse or by the trailing edge of an optional external vertical flyback pulse (on pin 18), according to which occurs first.

PIN CONFIGURATION

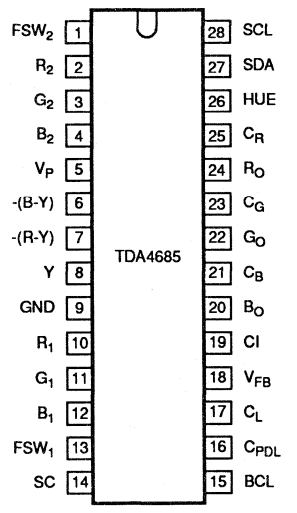


Fig.2 Pin configuration.

I²C-BUS CONTROL

The I²C-bus transmitter provides the data bytes to select and adjust the following functions and parameters:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- peak drive limiting
- selects either 3-level or 2-level (5 V) sandcastle pulse
- enables cut-off control control/ enables output clamping
- selects either PAL/SECAM or NTSC matrix
- enables/disables synchronization of the execution of the I²C-bus command with the vertical blanking interval.

I²C-BUS TRANSMITTER AND DATA TRANSFER

I²C-bus specification

The I²C-bus is a bi-directional, two-wire, serial data bus for intercommunication between ICs in an equipment. The microcontroller transmits data to the I²C-bus receiver in the TDA4685 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28). Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a start bit. A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a stop bit. Each transmission must start with a start bit and end with a stop bit. The bus is busy after a start bit and is only free again after a stop bit has been transmitted.

I²C-bus receiver

(microcontroller write mode)

Each transmission to/from the I²C-bus transceiver consists of at least three bytes following the start bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module ADdress (MAD) byte, also called slave address byte. This includes the module address, 1000100_2 for the TDA4685. The TDA4685 is a slave receiver (R/WN = 0), therefore the module address byte is 10001000_2 (88 Hex), see Fig.3.

The length of a data transmission is unrestricted, but the module address and the correct sub-address must be transmitted before the data byte(s). The order of data transmission is shown in Fig.4 and Fig.5. *Without auto-increment* (BREN = 0 or 1) the module address (MAD) byte is followed by a Sub-ADdress (SAD) byte and one data byte only (Fig.4).

Auto-increment

Auto-increment format enables quick slave receiver initialization by one transmission, when the I²C-bus control bit BREN = 0 (see control register bits of Table 1). If BREN = 1 auto-increment is not possible.

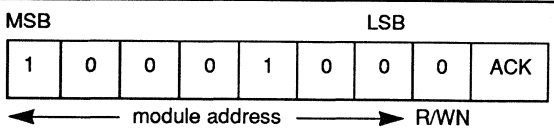


Fig.3 The module address byte.

If auto-increment format is selected the MAD byte is followed by a SAD byte and by the data bytes of consectutive sub-addresses (Fig.5).

All sub-addresses from 00 to 0F are automatically incremented, the sub-address counter wraps round from 0F to 00. Reserved sub-addresses 07, 08, 09, 0B, 0E and 0F are treated as legal but have no effect.

Sub-addresses outside the range 00 and 0F are not acknowledged by the device.

The sub-addresses are stored in the TDA4680 to address the following parameters and functions, see Table 1:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- peak drive limitting adjust
- control register functions.

The data bytes (D7-D0 of Table 1) provide the data of the parameters and functions for video processing.

Control Register 1

NMEN (NTSC - Matrix ENable):
0 = PAL/SECAM matrix
1 = NTSC matrix.

BREN (Buffer Register ENable):
0 = new data is enabled as soon as it is received
1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval. The I²C-bus transceiver does not accept any new data until this data is transferred into the data registers.

SC5 (SandCastle 5 V):
0 = 3-level sandcastle pulse
1 = 2-level (5 V) sandcastle pulse.

Control Register 2

FSON2 - Fast Switch 2 ON

FSDIS2 - Fast Switch 2 DISable

FSON1 - Fast Switch 1 ON

FSDIS1 - Fast Switch 1 DISable

Table 1 Sub-address (SAD) and data bytes

FUNCTION	SAD	MSB		DATA BYTE					LSB
	(Hex)	7	6	5	4	3	2	1	0
Brightness	00	0	0	A05	A04	A03	A02	A01	A00
Saturation	01	0	0	A15	A14	A13	A12	A11	A10
Contrast	02	0	0	A25	A24	A23	A22	A21	A20
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30
Red gain	04	0	0	A45	A44	A43	A42	A41	A40
Green gain	05	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60
Reserved	07	0	0	x	x	x	x	x	x
Reserved	08	0	0	x	x	x	x	x	x
Reserved	09	0	0	x	x	x	x	x	x
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Reserved	0B	x	x	x	x	x	x	x	x
Control Register 1	0C	SC5	x	BREN	x	NMEN	x	x	x
Control Register 2	0D	x	x	x	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Reserved	0E	x	x	x	x	x	x	x	x
Reserved	0F	x	x	x	x	x	x	x	x

The RGB input signals are selected by FSON2 and FSON1 or FSW_2 and FSW_1:
- FSON2 has priority over FSON1;
- FSW_2 has priority over FSW_1;
- FSDIS1 and FSDIS2 disable FSW_1 and FSW_2 (see Table 2).

BCOF - Black level Control OFf:
0 = automatic cut-off control enabled
1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.

When the supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage is interrupted) all data and function bits are set to 01_{Hex}.

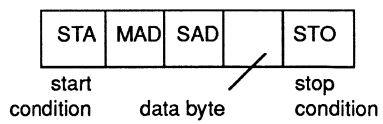


Fig.4 Data transmission without auto-increment (BREN = 0 or 1).

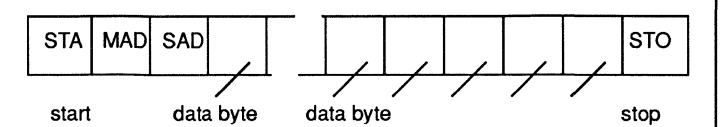


Fig.5 Data transmission with auto-increment (BREN = 0).

Table 2 Signal input selection by the fast source switches

I²C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	FSDIS2	FSON1	FSDIS1	FSW_2 (pin 1)	FSW_1 (pin 13)	RGB_2	RGB_1	Y/CD
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

Note to Table 2
Where L is a logic LOW (< 0.4 V), H is a logic HIGH (> 0.9 V), X is "don't care", and ON is the selected signal input.

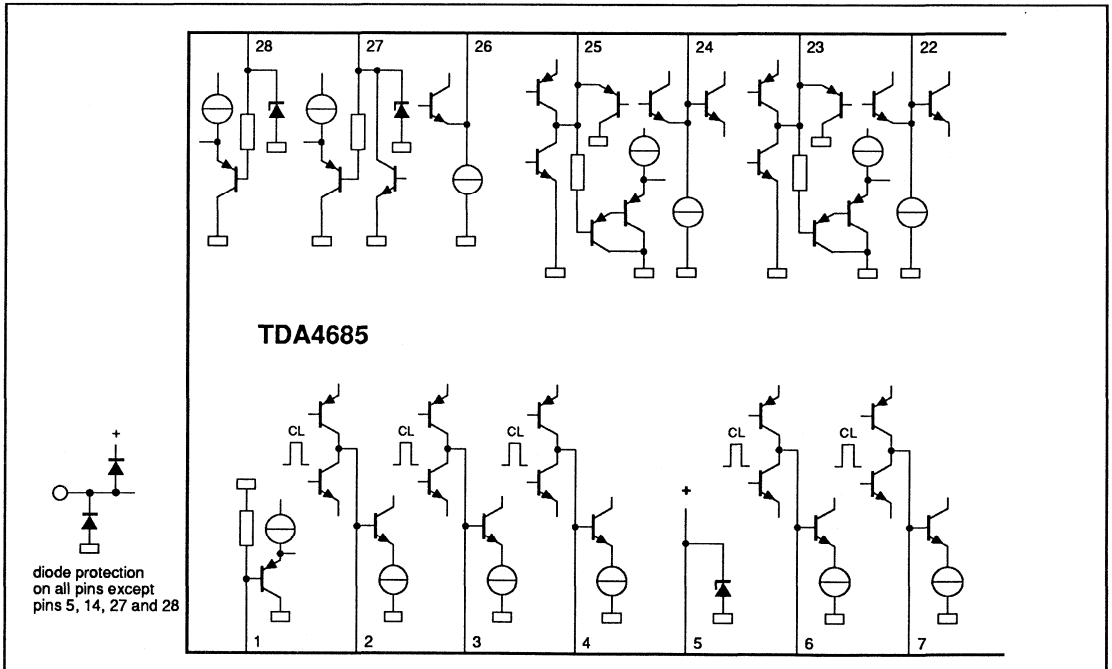


Fig.6(a) Internal circuits (continued in Fig.6b).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	–	8.8	V
V_I	voltage range (pins 1 to 8, 10 to 13, 16, 21, 23, 25, 27 and 28)	–0.1	V_P	V
	voltage range (pins 15, 18 and 19)	–0.7	V_P + 0.7	V
V_{14}	sandcastle pulse voltage range	–0.7	V_P + 5.8	V
I_{AV}	current range (pins 20, 22 and 24)	4	–10	mA
I_M	peak current range (pins 20, 22 and 24)	4	–20	mA
I_{26}	output current range	0.6	–8	mA
T_{stg}	storage temperature range	–20	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
P_{tot}	total power dissipation	–	1.2	W

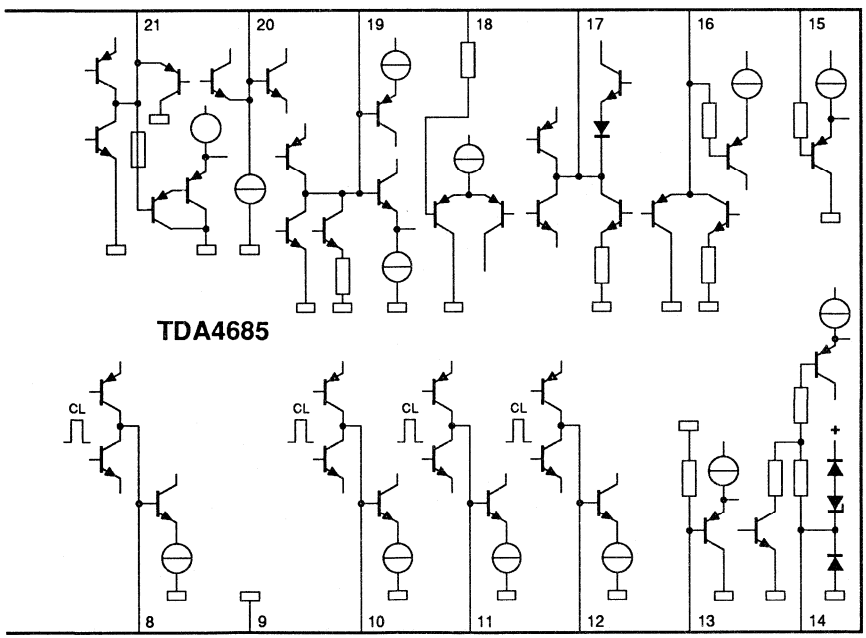


Fig.6(b) Internal circuits (continued from Fig.6a).

CHARACTERISTICS

All voltages are measured in test circuit of Fig.7 with respect to GND (pin 9); V_P = 8.0 V; T_{amb} = 25 °C:
- at nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20,
- at nominal settings of brightness, contrast, saturation and white level control,
- without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		–	60	–	mA
Colour-difference inputs						
$V_{6(p-p)}$	-(B-Y) input (peak-to-peak value)	note 1 and note 2	–	1.33	–	V
$V_{7(p-p)}$	-(R-Y) input (peak-to-peak value)	note 1 and note 2	–	1.05	–	V
$I_{6,7}$	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
$R_{6,7}$	input resistance		10	–	–	MΩ
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	4.1	–	V
Luminance/sync (VBS)						
$V_{i(p-p)}$	luminance input at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
V_8	internal DC bias voltage	at black level clamping	–	4.1	–	V
I_8	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
R_8	input resistance		10	–	–	MΩ
R_1, G_1 and B_1 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{10/11/12}$	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
$R_{10/11/12}$	input resistance		10	–	–	MΩ
R_2, G_2 and B_2 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{2/3/4}$	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
$R_{2/3/4}$	input resistance		10	–	–	MΩ
PAL/SECAM and NTSC matrix (see note 3)						
	PAL/SECAM matrix	control bit NMEN = 0				
	NTSC matrix	control bit NMEN = 1				

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast signal switch FSW_1 to select Y, CD or R_1, G_1, B_1 inputs control bits FSDIS1, FSON1 (see table 2)						
V_{13}	voltage to select Y and CD		–	–	0.4	V
	voltage range to select R_1, G_1, B_1		0.9	–	3.0	V
R_{13}	internal resistance to ground		–	4.0	–	kΩ
Fast signal switch FSW_2 to select Y, CD / R_1, G_1, B_1 or R_2, G_2, B_2 inputs control bits FSDIS2, FSON2 (see table 2)						
V_1	voltage to select Y, CD/R_1, G_1, B_1		–	–	0.4	V
	voltage range to select R_2, G_2, B_2		0.9	–	3.0	V
R_1	internal resistance to ground		–	4.0	–	kΩ
Saturation adjust acts on -(R-Y) and -(B-Y) signals under I^2C-bus control, sub-address 01_{Hex} (bit resolution 1.5 % of maximum saturation); data byte $3F_{Hex}$ for maximum saturation; data byte 23_{Hex} for nominal saturation; data byte 00_{Hex} for minimum saturation						
d_s	saturation below maximum	at 23_{Hex}	–	5	–	dB
		at 00_{Hex}; f = 100 kHz	–	50	–	dB
Contrast adjust acts on internal RGB signals under I^2C-bus control, sub-address 02_{Hex} (bit resolution 1.5 % of maximum contrast); data byte $3F_{Hex}$ for maximum contrast; data byte 22_{Hex} for nominal contrast; data byte 00_{Hex} for minimum contrast						
d_c	contrast below maximum	at 22_{Hex}	–	5.0	–	dB
		at 00_{Hex}	–	22	–	dB
Brightness adjust acts on internal RGB signals under I^2C-bus control, sub-address 00_{Hex} (bit resolution 1.5 % of maximum brightness); data byte $3F_{Hex}$ for maximum brightness; data byte 26_{Hex} for nominal brightness; data byte 00_{Hex} for minimum brightness						
d_{br}	black level shift of nominal signal amplitude referred to cut-off measurement level	at $3F_{Hex}$	–	30	–	%
		at 00_{Hex}	–	–50	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
White potentiometers, under I²C-bus control, sub-addresses 04_{Hex} (red), 05_{Hex} (green) and 06_{Hex} (blue); see note 4. data byte $3F_{Hex}$ for maximum gain data byte 19_{Hex} for nominal gain data byte 00_{Hex} for minimum gain						
ΔG_v	relative to nominal gain: increase of gain	at $3F_{Hex}$	–	50	–	%
	decrease of gain	at 00_{Hex}	–	50	–	%
RGB outputs pins 24, 22 and 20 (positive going output signals); see note 5.						
$V_{o(b-w)}$	nominal output signal amplitudes (black-to-white value)		–	2	–	V
	maximum output signal amplitudes (black-to-white value)		3.0	–	–	V
ΔV_o	spread between RGB output signals		–	–	10	%
V_o	minimum output voltages		–	–	0.8	V
	maximum output voltages		6.8	–	–	V
$V_{24,22,20}$	voltage of cut-off measurement line	BCOF = 1 (output clamping)	2.3	2.5	2.7	V
I_{int}	internal current sources		–	5.0	–	mA
R_o	output resistance		–	20	–	Ω
Frequency response						
d	frequency response of Y path (from pin 8 to pins 24, 22, 20)	f = 10 MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	f = 8 MHz;	–	–	3	dB
	frequency response of RGB_1 path (from pins 10 to 24, 11 to 22 and 12 to 20)	f = 10 MHz	–	–	3	dB
	frequency response of RGB_2 path (from pins 2 to 24, 3 to 22 and 4 to 20)	f = 10 MHz	–	–	3	dB
Sandcastle pulse detector (control bit SC5 = 0) three level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for H pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses (clamping)		7.6	–	V_P + 5.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse detector (control bit SC5 = 1) two level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	burst key pulses		4.0	4.5	V_P + 5.8	V
Sandcastle pulse detector						
I_{14}	output current	V_{14} = 0 V	–	–	–100	µA
t_d	leading edge delay of the clamping pulse		–	1.5	–	µs
VFB (note 7)						
V_{18}	vertical flyback pulse	for LOW	–	–	2.5	V
		for HIGH	4.5	–	–	V
	internal voltage	pin 18 open (note 8)	–	5.0	–	V
I_{18}	input current		–	–	5	µA
Average beam current limiting (note 9)						
$V_{c(15)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(15)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(15)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(15)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Peak drive limiting voltage (note 10) internal peak drive limiting level (V_{pdl}) acts on RGB outputs under I^2C-bus control, sub-address $0A_{Hex}$						
$V_{20/22/24}$	level for minimum RGB outputs	at byte 00_{Hex}	–	–	3.0	V
	level for maximum RGB outputs	at byte $3F_{Hex}$	7.0	–	–	V
I_{16}	charge current		–	–1	–	µA
	discharge current	during peak white	–	5	–	mA
V_{16}	internal voltage limitation		4.5	–	–	V
$V_{c(16)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(16)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(16)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(16)}$	voltage difference for full brightness reduction		–	–1.6	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic cut-off control (notes 7, 11, 12 and 13) see Fig.9						
V_{19}	cut-off measurement voltage (V_{MEAS})		–	–	V_P –1.4	V
I_{19}	output current		–	–	–60	µA
	input current		150	–	–	µA
	additional input current	switch-on delay 1	–	0.5	–	mA
$V_{24,22,20}$	monitor pulse amplitude (under I^2C-bus control, sub-address $0A_{Hex}$)	switch-on delay 1 (note 14)	–	V_{pdl} –0.1	–	V
V_{19}	voltage threshold for picture tube cathode warm-up	switch-on delay 1	–	4.5	–	V
	internally controlled voltage (V_{REF})	during leakage measurement period	–	2.7	–	V
ΔV_{19}	voltage difference between V_{MEAS} and V_{REF}		–	1.0	–	V
Cut-off storage						
$I_{21/23/25}$	charge and discharge currents	during cut-off measurement lines	–	± 0.3	–	mA
	current	outside measurement	–	–	± 0.1	µA
Leakage storage						
I_{17}	charge and discharge currents	during leakage measurement period	–	± 0.4	–	mA
	current	outside measurement	–	–	± 0.1	µA
V_{17}	voltage for reset to switch-on below		–	2.5	–	V
Hue control (note 14) under I^2C-bus control, sub-address 03_{Hex} data byte $3F_{Hex}$ for maximum voltage data byte 20_{Hex} for nominal voltage data byte 00_{Hex} for minimum voltage						
V_{26}	output voltage	at byte $3F_{Hex}$	4.8	–	–	V
		at byte 20_{Hex}	–	3.0	–	V
		at byte 00_{Hex}	–	–	1.2	V
I_{int}	current of the internal current source at pin 26		500	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus receiver clock SCL (pin 28)						
f_{SCL}	input frequency range		0	–	100	kHz
V_{IL}	input voltage LOW		–	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	–	V
I_{IL}	output current LOW		–	–	–10	μA
I_{IH}	input current HIGH		–	–	10	μA
t_d	pulse time LOW		4.7	–	–	μs
	pulse time HIGH		4.0	–	–	μs
t_r	rise time		–	–	1.0	μs
t_f	fall time		–	–	0.3	μs
I²C-bus receiver data input/output SDA (pin 27)						
V_{IL}	input voltage LOW		–	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	–	V
I_{IL}	output current LOW		–	–	–10	μA
I_{IH}	input current HIGH		–	–	10	μA
I_{OL}	output current LOW		3.0	–	–	mA
t_r	rise time		–	–	1.0	μs
t_f	fall time		–	–	0.3	μs
$t_{su;DAT}$	data set-up time		0.25	–	–	μs

Notes to the characteristics

1. The values of the -(B-Y) and -(R-Y) colour-difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600 Ω.
3. PAL/SECAM signals are matrixed by the equation:

   $$V_{G-Y} = -0.51\ V_{R-Y} - 0.19\ V_{B-Y}$$

   NTSC signals are matrixed by the equations (hue phase shift of −5 degrees):

   $$V_{R-Y}^* = 1.57\ V_{R-Y} - 0.41\ V_{B-Y}$$
   $$V_{G-Y}^* = -0.43\ V_{R-Y} - 0.11\ V_{B-Y}$$
   $$V_{B-Y}^* = V_{B-Y}$$

   In the matrix equations:
   V_{R-Y} and V_{B-Y} are for conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator.

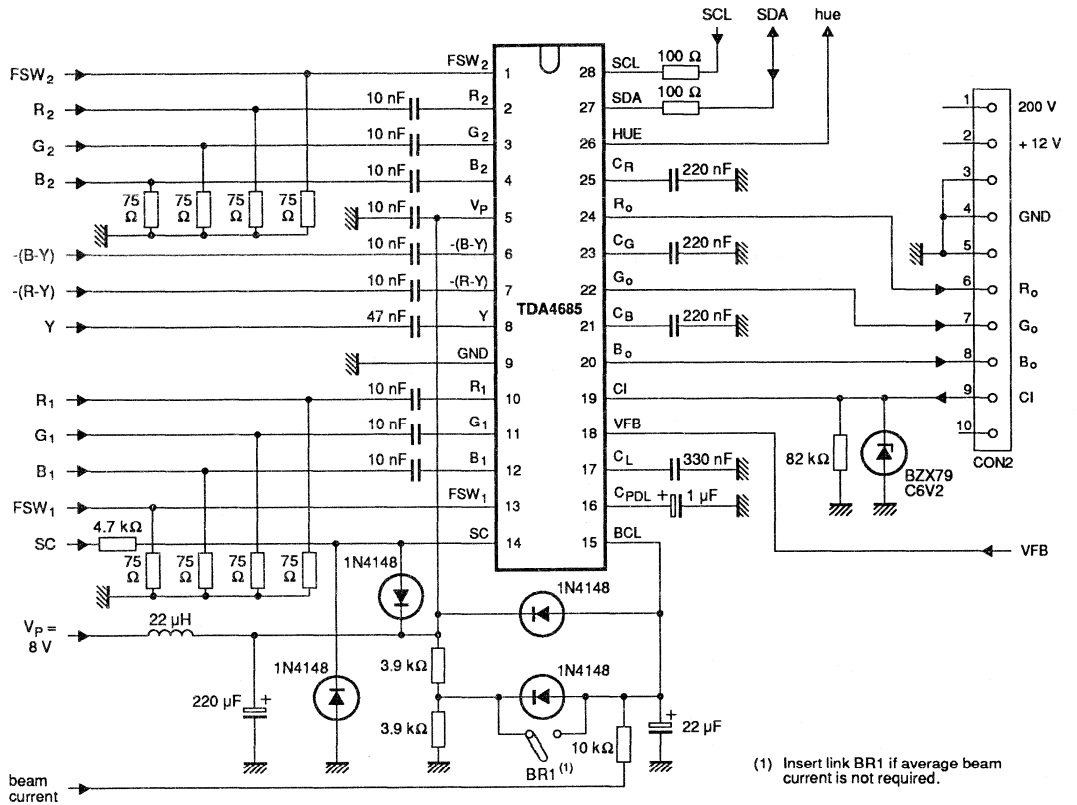
   V_{G-Y}^*, V_{R-Y}^* and V_{B-Y}^* are the NTSC-modified colour-difference signals; this is equivalent to the following demodulator axes and amplification factors:

	NTSC	PAL
(B-Y)* demodulator axis	0°	0°
(R-Y)* demodulator axis	115°	90°
(R-Y)* amplification factor	1.97	1.14
(B-Y)* amplification factor	2.03	2.03

   $V_{G-Y}^* = -0.27\ V_{R-Y}^* - 0.22\ V_{B-Y}^*$.
4. The white potentiometers affect the amplitudes of the RGB output signals.
5. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.
6. Sandcastle pulses are compared with internal threshold voltages independent from V_P. The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage. The internal threshold voltages (control bit SC5 = 0) are:
   1.5 V for horizontal and vertical blanking pulses (H and V blanking pulses),
   3.5 V for horizontal pulses,
   6.5 V for the burst key pulse.
   The internal threshold voltages, control bit SC5 = 1, are:
   1.5 V for horizontal and vertical blanking pulses,
   3.5 V for the burst key pulse.
7. Vertical signal blanking is determined by the vertical component of the sandcastle pulse. The leakage and the RGB cut-off measurement lines are positioned in the first four complete lines after the end of the vertical component. In this case, the RGB output signals are blanked until the end of the last measurement line; see Fig.9(a). If an extra vertical flyback pulse VFB is applied to pin 18, the four measurement lines start in the first complete line after the end of the VFB pulse; see Fig.9(b). In this case the output signals are blanked either until the end of the last measurement line or until the end of the vertical component of the sandcastle pulse, according to which occurs last.
8. If no VFB pulse is applied, pin 18 can be left open or connected to V_P.
9. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
10. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I^2C-bus under sub-address $0A_{Hex}$. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.
11. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Fig.8 and Fig.9).
12. During picture cathode warm-up (first switch-on delay) the RGB outputs (pins 24,22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitoring pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 4.5 V, the monitor pulse is switched off and cut-off control is activated (second switch-on delay). As soon as cut-off control stabilize, RGB output blanking is removed.
13. The cut-off measurement level range at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
14. The hue control output at pin 26 is an emitter follower with current source.

Video processor, with automatic cut-off control

TDA4685



(1) Insert link BR1 if average beam current is not required.

Fig.7 Test and application circuit.

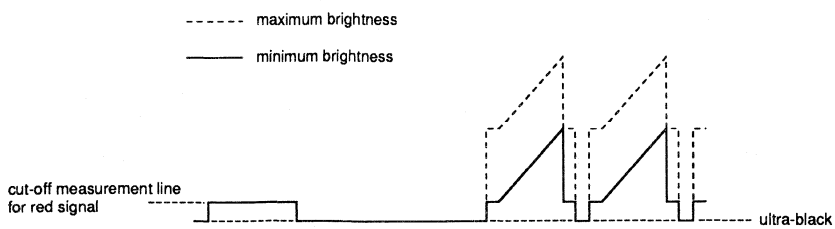


Fig.8 Cut-off measurement pulse.

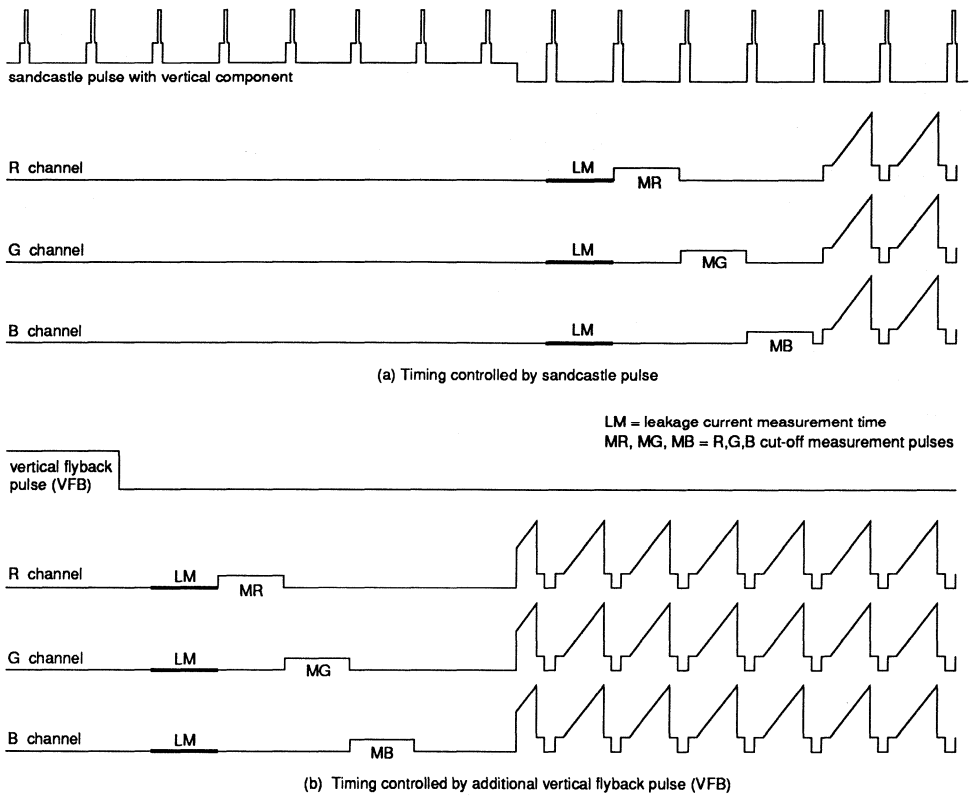


Fig.9 Leakage and cut-off current measurement timing diagram.

Purchase of Philips I²C components conveys a license under the Philips I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Philips Semiconductors

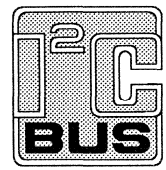
Data sheet	
status	Preliminary specification
date of issue	August 1991

TDA4686

Video processor, with automatic cut-off control

FEATURES

- Intended for double line frequency application (100/120 Hz)
- Operates from an 8 V DC supply
- Black level clamping of the colour-difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two analog RGB inputs, selected either by fast switch signals or the I²C-bus; brightness and contrast control of these RGB inputs
- Saturation, contrast and brightness adjustment via I²C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2- or 3-level sandcastle pulse for clamping, vertical synchronization and cut-off timing pulses
- Automatic cut-off control with picture tube leakage current compensation
- Cut-off measurement pulses after end of the vertical blanking pulse or end of an extra vertical flyback pulse
- Increased RGB signal bandwidths
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting
- PAL/SECAM or NTSC matrix selection via I²C-bus
- Emitter-follower RGB output stages to drive the video output stages
- Hue control output for the TDA4555 or TDA4650
- No delay of clamping pulse
- Large luminance, colour difference and RGB bandwidth



QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	–	60	–	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value)	–	0.45	–	V
$V_{6(p-p)}$	-(B-Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	-(R-Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	three-level sandcastle pulse: H+V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	two-level sandcastle pulse: H+V	–	2.5	–	V
	BK	–	4.5	–	V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)	–	0.7	–	V
$V_{o(p-p)}$	RGB outputs at pins 24,22 and 20 (peak-to-peak value)	–	2.0	–	V
T_{amb}	operating ambient temperature range	0	–	+ 70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4686	28	DIL	plastic	SOT117

Video processor, with automatic cut-off control

TDA4686

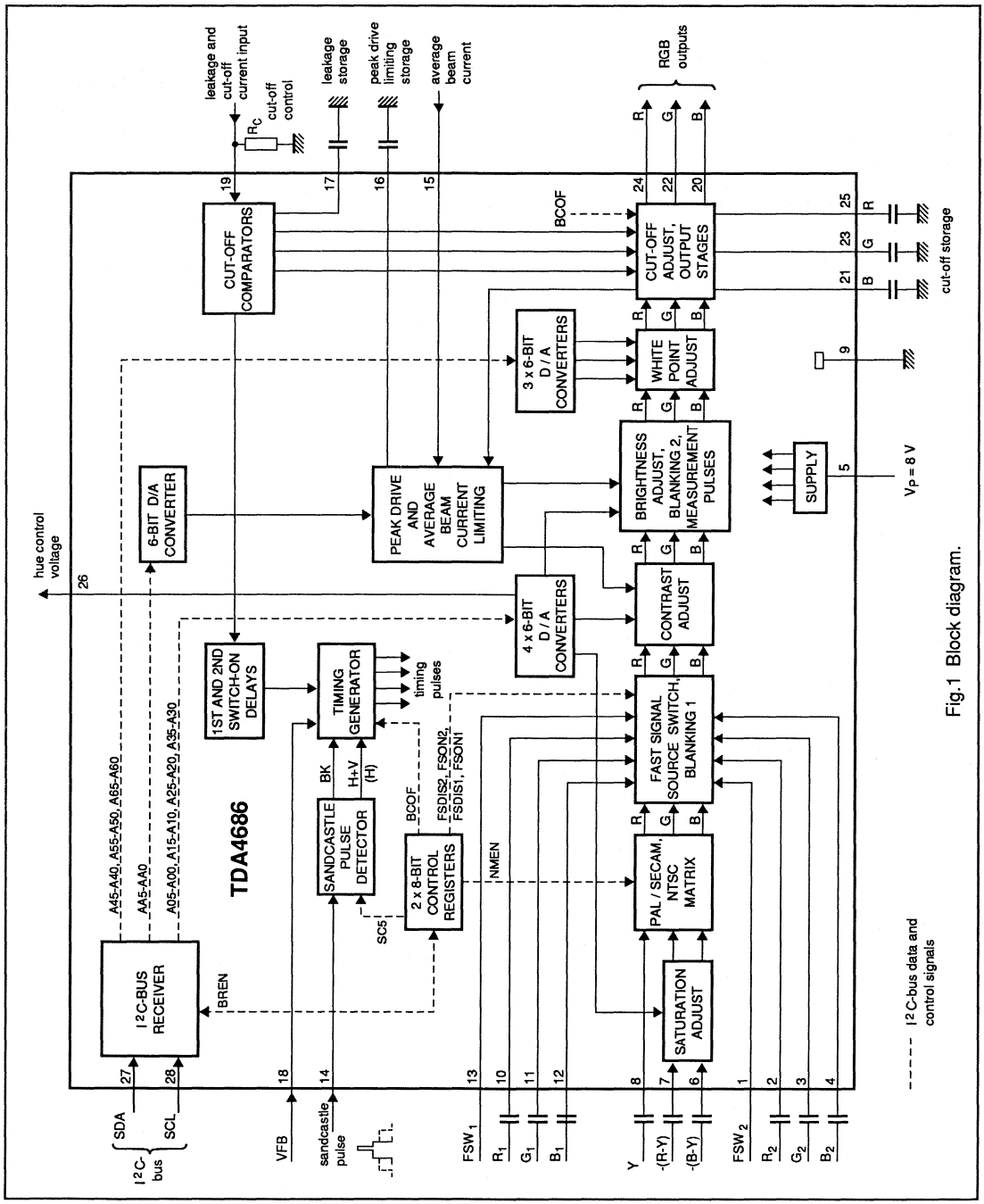


Fig.1 Block diagram.

Video processor, with automatic cut-off control

TDA4686

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
-(B-Y)	6	colour difference input -(B-Y)
-(R-Y)	7	colour difference input -(R-Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input

SYMBOL	PIN	DESCRIPTION
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current
V_{FB}	18	vertical flyback pulse input
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I^2C-bus serial data input/output
SCL	28	I^2C-bus serial clock input

DESCRIPTION

TDA4686 is a monolithic, integrated circuit with a colour-difference interface for video processing in TV receivers. Its primary function is to process the luminance and colour-difference signals from multistandard colour decoders, TDA4650/TDA4660 or TDA4555, Colour Transient Improvement (CTI) IC, TDA4565, Picture Signal Improvement (PSI) IC, TDA4670, or from a Feature Module.

The required input signals are:

- luminance and negative colour-difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I^2C-bus data and clock signals for microprocessor control.

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector and the other from an on-screen display generator. The TDA4685 has I^2C-bus control of all parameters and functions with automatic cut-off control of the picture tube cathode currents. It provides RGB output signals for the video output stages.

The TDA4686 is a simplified, pin compatible (except pin 18) version of the TDA4680. The module address via the I^2C-bus can be used for both ICs; where a function is not included in the TDA4686 then the I^2C-bus command is not executed. The differences with the TDA4680 are:

- no automatic white level control; the white levels are determined directly by the I^2C-bus data
- RGB reference levels for automatic cut-off control are not generated
- clamping delay is fixed
- only contrast and brightness adjust for the RGB input signals
- the measurement lines are triggered either by the trailing edge of the vertical component of the sandcastle pulse or by the trailing edge of an optional external vertical flyback pulse (on pin 18), according to which occurs first.

PIN CONFIGURATION

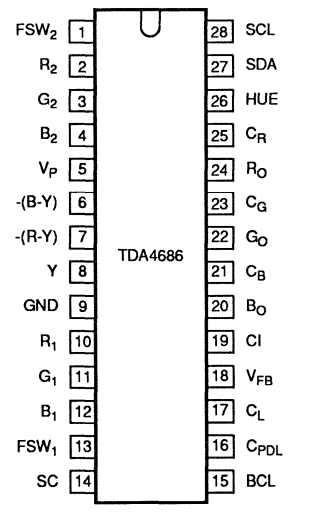


Fig.2 Pin configuration.

I²C-BUS CONTROL

The I²C-bus transmitter provides the data bytes to select and adjust the following functions and parameters:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- peak drive limiting
- selects either 3-level or 2-level (5 V) sandcastle pulse
- enables cut-off control control/ enables output clamping
- selects either PAL/SECAM or NTSC matrix
- enables/disables synchronization of the execution of the I²C-bus command with the vertical blanking interval.

I²C-BUS TRANSMITTER AND DATA TRANSFER

I²C-bus specification

The I²C-bus is a bi-directional, two-wire, serial data bus for intercommunication between ICs in an equipment. The microcontroller transmits data to the I²C-bus receiver in the TDA46865 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28). Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a start bit. A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a stop bit. Each transmission must start with a start bit and end with a stop bit. The bus is busy after a start bit and is only free again after a stop bit has been transmitted.

I²C-bus receiver

(microcontroller write mode)

Each transmission to/from the I²C-bus transceiver consists of at least three bytes following the start bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module ADdress (MAD) byte, also called slave address byte. This includes the module address, 1000100_2 for the TDA4685. The TDA4686 is a slave receiver (R/WN = 0), therefore the module address byte is 10001000_2 (88 Hex), see Fig.3.

The length of a data transmission is unrestricted, but the module address and the correct sub-address must be transmitted before the data byte(s). The order of data transmission is shown in Fig.4 and Fig.5. *Without auto-increment* (BREN = 0 or 1) the module address (MAD) byte is followed by a Sub-ADdress (SAD) byte and one data byte only (Fig.4).

Auto-increment

Auto-increment format enables quick slave receiver initialization by one transmission, when the I²C-bus control bit BREN = 0 (see control register bits of Table 1). If BREN = 1 auto-increment is not possible.

If auto-increment format is selected the MAD byte is followed by a SAD byte and by the data bytes of consectutive sub-addresses (Fig.5).

All sub-addresses from 00 to 0F are automatically incremented, the sub-address counter wraps round from 0F to 00. Reserved sub-addresses 07, 08, 09, 0B, 0E and 0F are treated as legal but have no effect.

Sub-addresses outside the range 00 and 0F are not acknowledged by the device.

The sub-addresses are stored in the TDA4686 to address the following parameters and functions, see Table 1:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- peak drive limitting adjust
- control register functions.

The data bytes (D7-D0 of Table 1) provide the data of the parameters and functions for video processing.

Control Register 1

NMEN (NTSC - Matrix ENable):
- 0 = PAL/SECAM matrix
- 1 = NTSC matrix.

BREN (Buffer Register ENable):
- 0 = new data is enabled as soon as it is received
- 1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval. The I²C-bus transceiver does not accept any new data until this data is transferred into the data registers.

SC5 (SandCastle 5 V):
- 0 = 3-level sandcastle pulse
- 1 = 2-level (5 V) sandcastle pulse.

Control Register 2

FSON2 - Fast Switch 2 ON

FSDIS2 - Fast Switch 2 DISable

FSON1 - Fast Switch 1 ON

FSDIS1 - Fast Switch 1 DISable

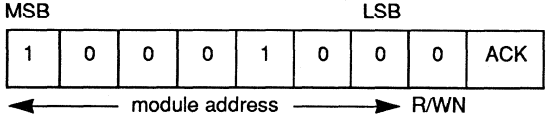


Fig.3 The module address byte.

Table 1 Sub-address (SAD) and data bytes

FUNCTION	SAD	MSB		DATA BYTE					LSB
	(Hex)	7	6	5	4	3	2	1	0
Brightness	00	0	0	A05	A04	A03	A02	A01	A00
Saturation	01	0	0	A15	A14	A13	A12	A11	A10
Contrast	02	0	0	A25	A24	A23	A22	A21	A20
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30
Red gain	04	0	0	A45	A44	A43	A42	A41	A40
Green gain	05	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60
Reserved	07	0	0	x	x	x	x	x	x
Reserved	08	0	0	x	x	x	x	x	x
Reserved	09	0	0	x	x	x	x	x	x
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Reserved	0B	x	x	x	x	x	x	x	x
Control Register 1	0C	SC5	x	BREN	x	NMEN	x	x	x
Control Register 2	0D	x	x	x	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Reserved	0E	x	x	x	x	x	x	x	x
Reserved	0F	x	x	x	x	x	x	x	x

The RGB input signals are selected by FSON2 and FSON1 or FSW_2 and FSW_1:
- FSON2 has priority over FSON1;
- FSW_2 has priority over FSW_1;
- FSDIS1 and FSDIS2 disable FSW_1 and FSW_2 (see Table 2).

BCOF - Black level Control OFf:
0 = automatic cut-off control enabled
1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.

When the supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage is interrupted) all data and function bits are set to 01_{Hex}.

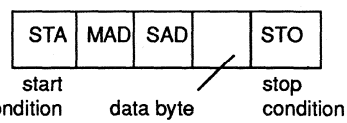


Fig.4 Data transmission without auto-increment (BREN = 0 or 1).

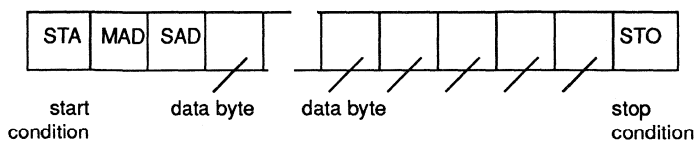


Fig.5 Data transmission with auto-increment (BREN = 0).

Table 2 Signal input selection by the fast source switches

I^2C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	FSDIS2	FSON1	FSDIS1	FSW_2 (pin 1)	FSW_1 (pin 13)	RGB_2	RGB_1	Y/CD
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

Note to Table 2

Where L is a logic LOW (< 0.4 V), H is a logic HIGH (> 0.9 V), X is "don't care", and ON is the selected signal input.

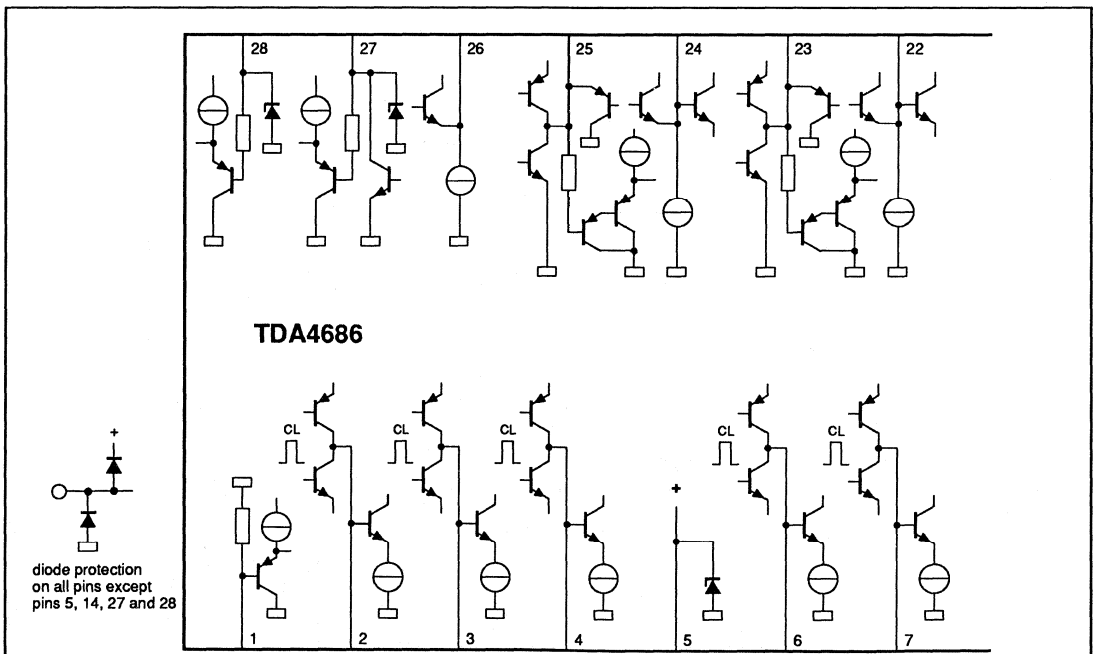


Fig.6(a) Internal circuits (continued in Fig.6b).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	–	8.8	V
V_I	voltage range (pins 1 to 8, 10 to 13, 16, 21, 23, 25, 27 and 28)	–0.1	V_P	V
	voltage range (pins 15, 18 and 19)	–0.7	V_P + 0.7	V
V_{14}	sandcastle pulse voltage range	–0.7	V_P + 5.8	V
I_{AV}	current range (pins 20, 22 and 24)	4	–10	mA
I_M	peak current range (pins 20, 22 and 24)	4	–20	mA
I_{26}	output current range	0.6	–8	mA
T_{stg}	storage temperature range	–20	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
P_{tot}	total power dissipation	–	1.2	W

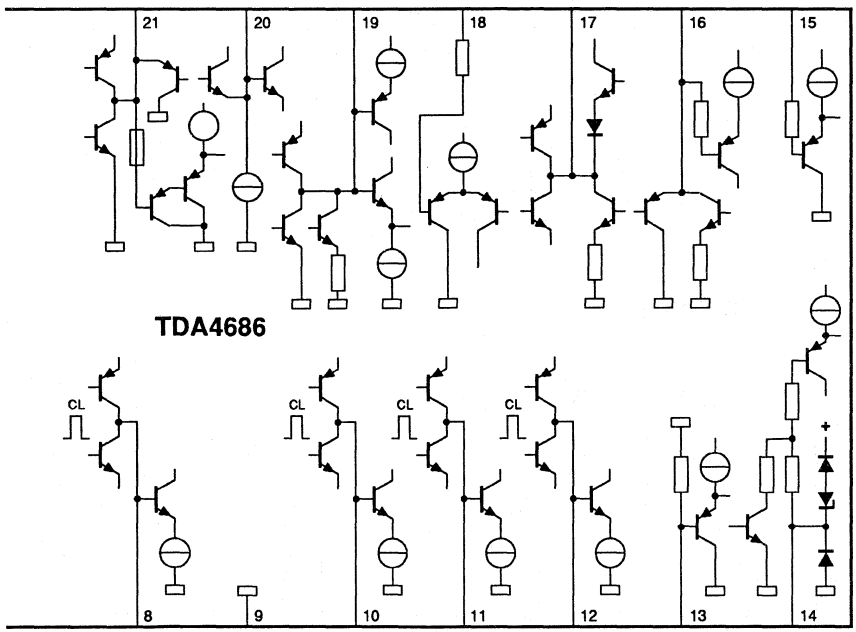


Fig.6(b) Internal circuits (continued from Fig.6a).

CHARACTERISTICS

All voltages are measured in test circuit of Fig.7 with respect to GND (pin 9); V_P = 8.0 V; T_{amb} = 25 °C:
- at nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20,
- at nominal settings of brightness, contrast, saturation and white level control,
- without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		–	60	–	mA
Colour-difference inputs						
$V_{6(p-p)}$	-(B-Y) input (peak-to-peak value)	note 1 and note 2	–	1.33	–	V
$V_{7(p-p)}$	-(R-Y) input (peak-to-peak value)	note 1 and note 2	–	1.05	–	V
$I_{6,7}$	input current	during line scan	–	–	± 0.1	μA
		at black level clamping	± 100	–	–	μA
$R_{6,7}$	input resistance		10	–	–	MΩ
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	4.1	–	V
Luminance/sync (VBS)						
$V_{i(p-p)}$	luminance input at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
V_8	internal DC bias voltage	at black level clamping	–	4.1	–	V
I_8	input current	during line scan	–	–	± 0.1	μA
		at black level clamping	± 100	–	–	μA
R_8	input resistance		10	–	–	MΩ
R_1, G_1 and B_1 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{10/11/12}$	input current	during line scan	–	–	± 0.1	μA
		at black level clamping	± 100	–	–	μA
$R_{10/11/12}$	input resistance		10	–	–	MΩ
R_2, G_2 and B_2 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{2/3/4}$	input current	during line scan	–	–	± 0.1	μA
		at black level clamping	± 100	–	–	μA
$R_{2/3/4}$	input resistance		10	–	–	MΩ
PAL/SECAM and NTSC matrix (see note 3)						
	PAL/SECAM matrix	control bit NMEN = 0				
	NTSC matrix	control bit NMEN = 1				

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast signal switch FSW_1 to select Y, CD or R_1, G_1, B_1 inputs control bits FSDIS1, FSON1 (see table 2)						
V_{13}	voltage to select Y and CD		–	–	0.4	V
	voltage range to select R_1, G_1, B_1		0.9	–	3.0	V
R_{13}	internal resistance to ground		–	4.0	–	kΩ
Fast signal switch FSW_2 to select Y, CD / R_1, G_1, B_1 or R_2, G_2, B_2 inputs control bits FSDIS2, FSON2 (see table 2)						
V_1	voltage to select Y, CD/R_1, G_1, B_1		–	–	0.4	V
	voltage range to select R_2, G_2, B_2		0.9	–	3.0	V
R_1	internal resistance to ground		–	4.0	–	kΩ
Saturation adjust acts on -(R-Y) and -(B-Y) signals under I^2C-bus control, sub-address 01_{Hex} (bit resolution 1.5 % of maximum saturation); data byte $3F_{Hex}$ for maximum saturation; data byte 23_{Hex} for nominal saturation; data byte 00_{Hex} for minimum saturation						
d_s	saturation below maximum	at 23_{Hex}	–	5	–	dB
		at 00_{Hex}; f = 100 kHz	–	50	–	dB
Contrast adjust acts on internal RGB signals under I^2C-bus control, sub-address 02_{Hex} (bit resolution 1.5 % of maximum contrast); data byte $3F_{Hex}$ for maximum contrast; data byte 22_{Hex} for nominal contrast; data byte 00_{Hex} for minimum contrast						
d_c	contrast below maximum	at 22_{Hex}	–	5.0	–	dB
		at 00_{Hex}	–	22	–	dB
Brightness adjust acts on internal RGB signals under I^2C-bus control, sub-address 00_{Hex} (bit resolution 1.5 % of maximum brightness); data byte $3F_{Hex}$ for maximum brightness; data byte 26_{Hex} for nominal brightness; data byte 00_{Hex} for minimum brightness						
d_{br}	black level shift of nominal signal amplitude referred to cut-off measurement level	at $3F_{Hex}$	–	30	–	%
		at 00_{Hex}	–	–50	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
White potentiometers, under I^2C-bus control, sub-addresses 04_{Hex} (red), 05_{Hex} (green) and 06_{Hex} (blue); see note 4. data byte $3F_{Hex}$ for maximum gain data byte 19_{Hex} for nominal gain data byte 00_{Hex} for minimum gain						
ΔG_v	relative to nominal gain: increase of gain	at $3F_{Hex}$	–	50	–	%
	decrease of gain	at 00_{Hex}	–	50	–	%
RGB outputs pins 24, 22 and 20 (positive going output signals); see note 5.						
$V_{o(b-w)}$	nominal output signal amplitudes (black-to-white value)		–	2	–	V
	maximum output signal amplitudes (black-to-white value)		3.0	–	–	V
ΔV_o	spread between RGB output signals		–	–	10	%
V_o	minimum output voltages		–	–	0.8	V
	maximum output voltages		6.8	–	–	V
$V_{24,22,20}$	voltage of cut-off measurement line	BCOF = 1 (output clamping)	2.3	2.5	2.7	V
I_{int}	internal current sources		–	5.0	–	mA
R_o	output resistance		–	20	–	Ω
Frequency response						
d	frequency response of Y path (from pin 8 to pins 24, 22, 20)	f = 14 MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	f = 12 MHz;	–	–	3	dB
	frequency response of RGB_1 path (from pins 10 to 24, 11 to 22 and 12 to 20)	f = 22 MHz	–	–	3	dB
	frequency response of RGB_2 path (from pins 2 to 24, 3 to 22 and 4 to 20)	f = 22 MHz	–	–	3	dB
Sandcastle pulse detector (control bit SC5 = 0) three level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for H pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses (clamping)		7.6	–	V_P + 5.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse detector (control bit SC5 = 1) two level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	burst key pulses		4.0	4.5	V_P + 5.8	V
Sandcastle pulse detector						
I_{14}	output current	V_{14} = 0 V	–	–	–100	µA
t_d	leading edge delay of the clamping pulse		–	0	–	µs
VFB (note 7)						
V_{18}	vertical flyback pulse	for LOW	–	–	2.5	V
		for HIGH	4.5	–	–	V
	internal voltage	pin 18 open (note 8)	–	5.0	–	V
I_{18}	input current		–	–	5	µA
Average beam current limiting (note 9)						
$V_{c(15)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(15)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(15)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(15)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Peak drive limiting voltage (note 10) internal peak drive limiting level (V_{pdl}) acts on RGB outputs under I^2C-bus control, sub-address $0A_{Hex}$						
$V_{20/22/24}$	level for minimum RGB outputs	at byte 00_{Hex}	–	–	3.0	V
	level for maximum RGB outputs	at byte $3F_{Hex}$	7.0	–	–	V
I_{16}	charge current		–	–1	–	µA
	discharge current	during peak white	–	5	–	mA
V_{16}	internal voltage limitation		4.5	–	–	V
$V_{c(16)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(16)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(16)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(16)}$	voltage difference for full brightness reduction		–	–1.6	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic cut-off control (notes 7, 11, 12 and 13) see Fig.9						
V_{19}	cut-off measurement voltage (V_{MEAS})		–	–	V_P –1.4	V
I_{19}	output current		–	–	–60	µA
	input current		150	–	–	µA
	additional input current	switch-on delay 1	–	0.5	–	mA
$V_{24,22,20}$	monitor pulse amplitude (under I²C-bus control, sub-address $0A_{Hex}$)	switch-on delay 1 (note 14)	–	V_{pdl} –0.1	–	V
V_{19}	voltage threshold for picture tube cathode warm-up	switch-on delay 1	–	4.5	–	V
	internally controlled voltage (V_{REF})	during leakage measurement period	–	2.7	–	V
ΔV_{19}	voltage difference between V_{MEAS} and V_{REF}		–	1.0	–	V
Cut-off storage						
$I_{21/23/25}$	charge and discharge currents	during cut-off measurement lines	–	± 0.3	–	mA
	current	outside measurement	–	–	± 0.1	µA
Leakage storage						
I_{17}	charge and discharge currents	during leakage measurement period	–	± 0.4	–	mA
	current	outside measurement	–	–	± 0.1	µA
V_{17}	voltage for reset to switch-on below		–	2.5	–	V
Hue control (note 14) under I²C-bus control, sub-address 03_{Hex} data byte $3F_{Hex}$ for maximum voltage data byte 20_{Hex} for nominal voltage data byte 00_{Hex} for minimum voltage						
V_{26}	output voltage	at byte $3F_{Hex}$	4.8	–	–	V
		at byte 20_{Hex}	–	3.0	–	V
		at byte 00_{Hex}	–	–	1.2	V
I_{int}	current of the internal current source at pin 26		500	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus receiver clock SCL (pin 28)						
f_{SCL}	input frequency range		0	–	100	kHz
V_{IL}	input voltage LOW		–	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	–	V
I_{IL}	output current LOW		–	–	–10	µA
I_{IH}	input current HIGH		–	–	10	µA
t_d	pulse time LOW		4.7	–	–	µs
	pulse time HIGH		4.0	–	–	µs
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
I²C-bus receiver data input/output SDA (pin 27)						
V_{IL}	input voltage LOW		–	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	–	V
I_{IL}	output current LOW		–	–	–10	µA
I_{IH}	input current HIGH		–	–	10	µA
I_{OL}	output current LOW		3.0	–	–	mA
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
$t_{su;DAT}$	data set-up time		0.25	–	–	µs

Notes to the characteristics

1. The values of the -(B-Y) and -(R-Y) colour-difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600 Ω.
3. PAL/SECAM signals are matrixed by the equation:

   $$V_{G-Y} = -0.51\ V_{R-Y} - 0.19\ V_{B-Y}$$

   NTSC signals are matrixed by the equations (hue phase shift of −5 degrees):

   $$V_{R-Y}^* = 1.57\ V_{R-Y} - 0.41\ V_{B-Y}$$
   $$V_{G-Y}^* = -0.43\ V_{R-Y} - 0.11\ V_{B-Y}$$
   $$V_{B-Y}^* = V_{B-Y}$$

   In the matrix equations:
   V_{R-Y} and V_{B-Y} are for conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator.

   V_{G-Y}^*, V_{R-Y}^* and V_{B-Y}^* are the NTSC-modified colour-difference signals; this is equivalent to the following demodulator axes and amplification factors:

	NTSC	PAL
(B-Y)* demodulator axis	0°	0°
(R-Y)* demodulator axis	115°	90°
(R-Y)* amplification factor	1.97	1.14
(B-Y)* amplification factor	2.03	2.03

   $V_{G-Y}^* = -0.27\ V_{R-Y}^* - 0.22\ V_{B-Y}^*$.
4. The white potentiometers affect the amplitudes of the RGB output signals.
5. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.
6. Sandcastle pulses are compared with internal threshold voltages independent from V_P. The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage. The internal threshold voltages (control bit SC5 = 0) are:
   1.5 V for horizontal and vertical blanking pulses (H and V blanking pulses),
   3.5 V for horizontal pulses,
   6.5 V for the burst key pulse.
   The internal threshold voltages, control bit SC5 = 1, are:
   1.5 V for horizontal and vertical blanking pulses,
   3.5 V for the burst key pulse.
7. Vertical signal blanking is determined by the vertical component of the sandcastle pulse. The leakage and the RGB cut-off measurement lines are positioned in the first four complete lines after the end of the vertical component. In this case, the RGB output signals are blanked until the end of the last measurement line; see Fig.9(a). If an extra vertical flyback pulse VFB is applied to pin 18, the four measurement lines start in the first complete line after the end of the VFB pulse; see Fig.9(b). In this case the output signals are blanked either until the end of the last measurement line or until the end of the vertical component of the sandcastle pulse, according to which occurs last.
8. If no VFB pulse is applied, pin 18 can be left open or connected to V_P.
9. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
10. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I^2C-bus under sub-address $0A_{Hex}$. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.
11. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Fig.8 and Fig.9).
12. During picture cathode warm-up (first switch-on delay) the RGB outputs (pins 24,22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitoring pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 4.5 V, the monitor pulse is switched off and cut-off control is activated (second switch-on delay). As soon as cut-off control stabilize, RGB output blanking is removed.
13. The cut-off measurement level range at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
14. The hue control output at pin 26 is an emitter follower with current source.

Video processor, with automatic cut-off control

TDA4686

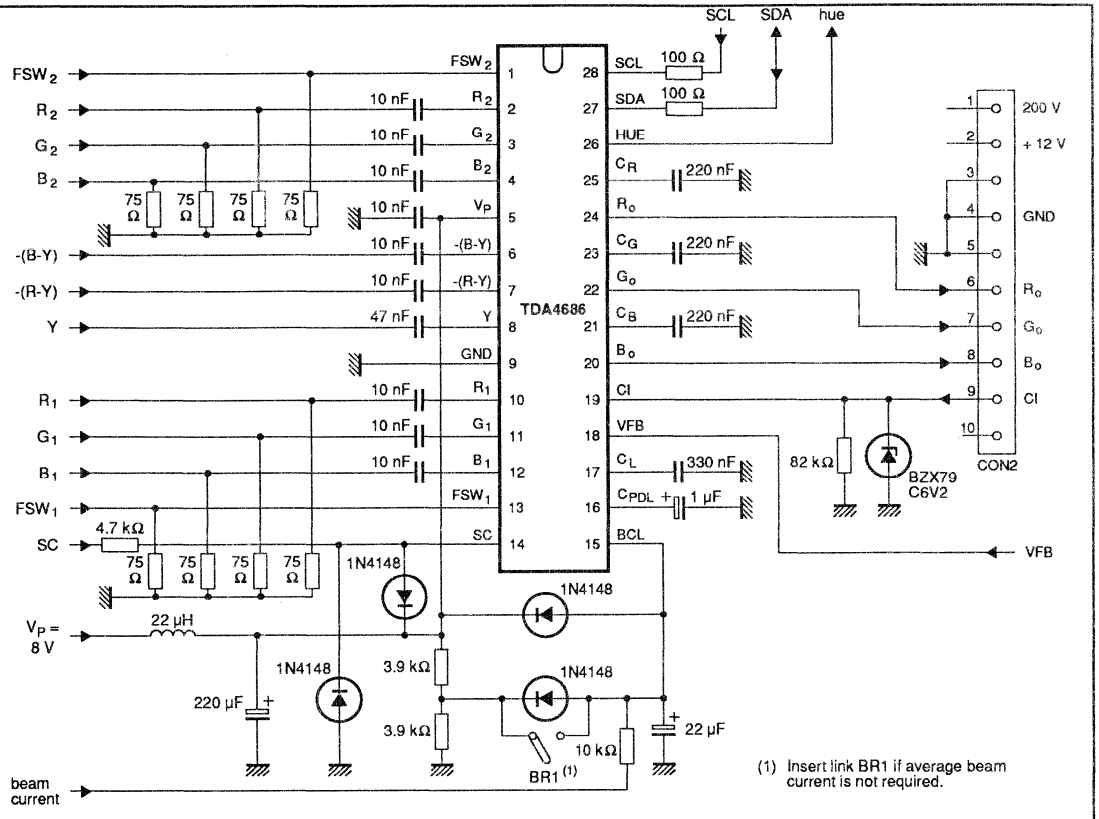


Fig.7 Test and application circuit.

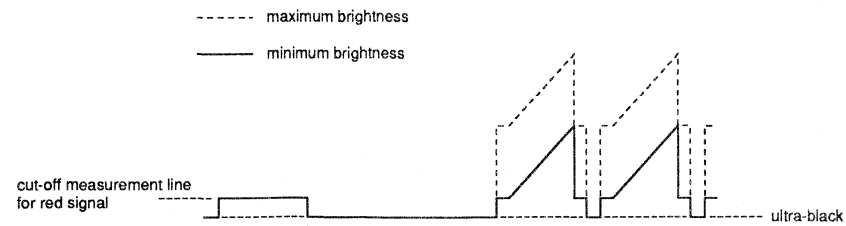


Fig.8 Cut-off measurement pulse.

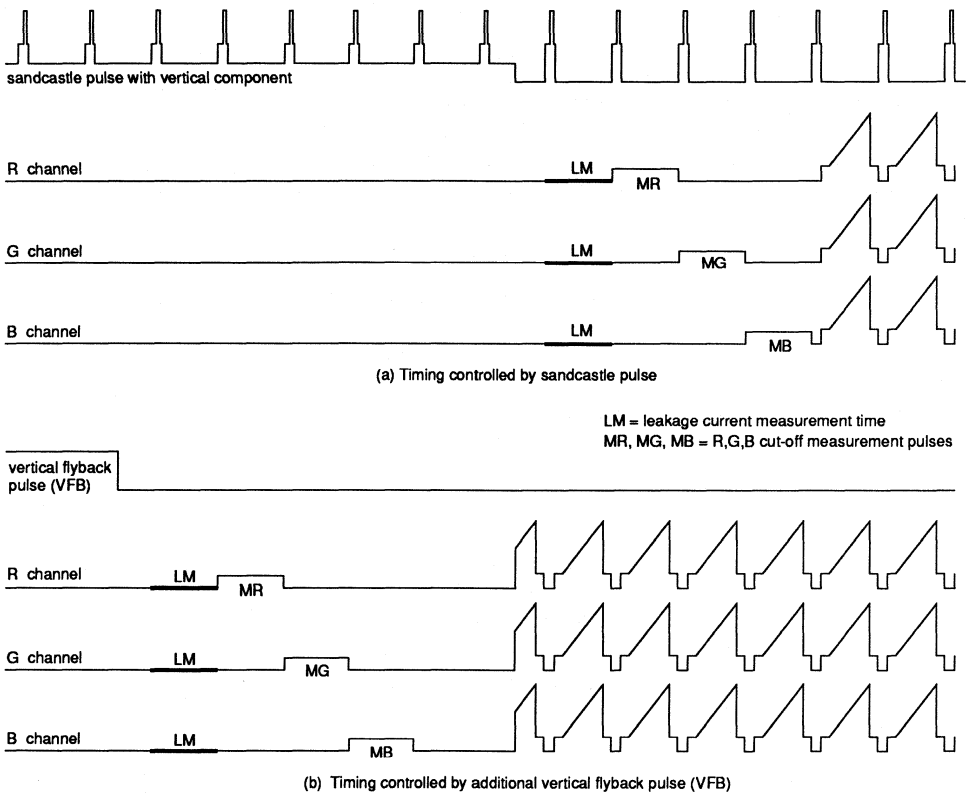


Fig.9 Leakage and cut-off current measurement timing diagram.

Purchase of Philips I²C components conveys a license under the Philips I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA4710H

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

GENERAL DESCRIPTION

The TDA4710 is an integrated circuit for VHS PAL, SECAM ME or NTSC chrominance and synchronization processing in (S) VHS cassette recorders.

FEATURES

Chrominance

- 4.43/3.58 MHz chrominance output with colour-killer for record, electronic-to-electronic (e.g. direct to a SCART connector) and playback modes
- 627/629 kHz chrominance output with colour-killer
- 8.86/7.16 MHz crystal oscillator (voltage controlled oscillator in record mode and fixed frequency oscillator during playback mode)
- Separate automatic gain control (AGC) for record and playback (two channel hold capacity)
- Burst pre-emphasis/de-emphasis selection input (for NTSC)
- Subcarrier phase rotion and head-pulse input
- PAL error detector and correction circuit for longplay multispeed (LP MS)
- Test picture generator

Synchronization

- Phase-locked loop (PLL) with coincidence detector and mute output stage for the line frequency
- Sandcastle output signal

Additional features

- Standard/longplay multispeed mode selection
- 32 µs SKEW detector and output stage
- Selectable burst pulse insert for longplay feature mode (PAL)
- NTS to PAL-M transcoder at playback

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4710H	48	QFP48	plastic	SOT196A

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	supply voltage					
V_{17-19}	digital part		-	5	-	V
V_{41-43}	analog part		-	5	-	V
$I_{17}+I_{41}$	supply current		-	45	-	mA
V_{20-19}	sync input signal slicing level		-	1.5	-	V
V_{23-19}	sandcastle output signal		-	4	-	V
V_{16-19}	test picture output signal		-	1	-	V
$V_{31(p-p)}$	4.43/3.58MHz subcarrier output (peak-to-peak value)		-	400	-	mV
Record (PAL) note 1						
$V_{48(p-p)}$	composite video input signal (peak-to-peak value)		-	450	-	mV
$V_{44(p-p)}$	AGC chrominance input signal (peak-to-peak value)		10	-	210	mV
$V_{37(p-p)}$	627 kHz subcarrier mixer output signal (peak-to-peak value)		-	1.06	-	V
Playback (PAL) note 1						
$V_{42(p-p)}$	627kHz chrominance input signal (peak-to-peak value)		-	24	-	mV
$V_{8(p-p)}$	4.43MHz chrominance output signal (peak-to-peak value)		-	420	-	mV
Playback (SECAM) note 2						
$V_{8(p-p)}$	chrominance output signal (peak-to-peak value)		-	200	-	mV

Notes to the quick reference data

1. PAL signal (red) with 75% saturation, –9 dB bandpath (pins 44 to 46), 6 dB trap pins 2 to 4 and chrominance-to-burst ratio of 2.2:1.
2. All SECAM amplitudes are frequency values (red). Amplitude depends on the start moment of the signal frequency.

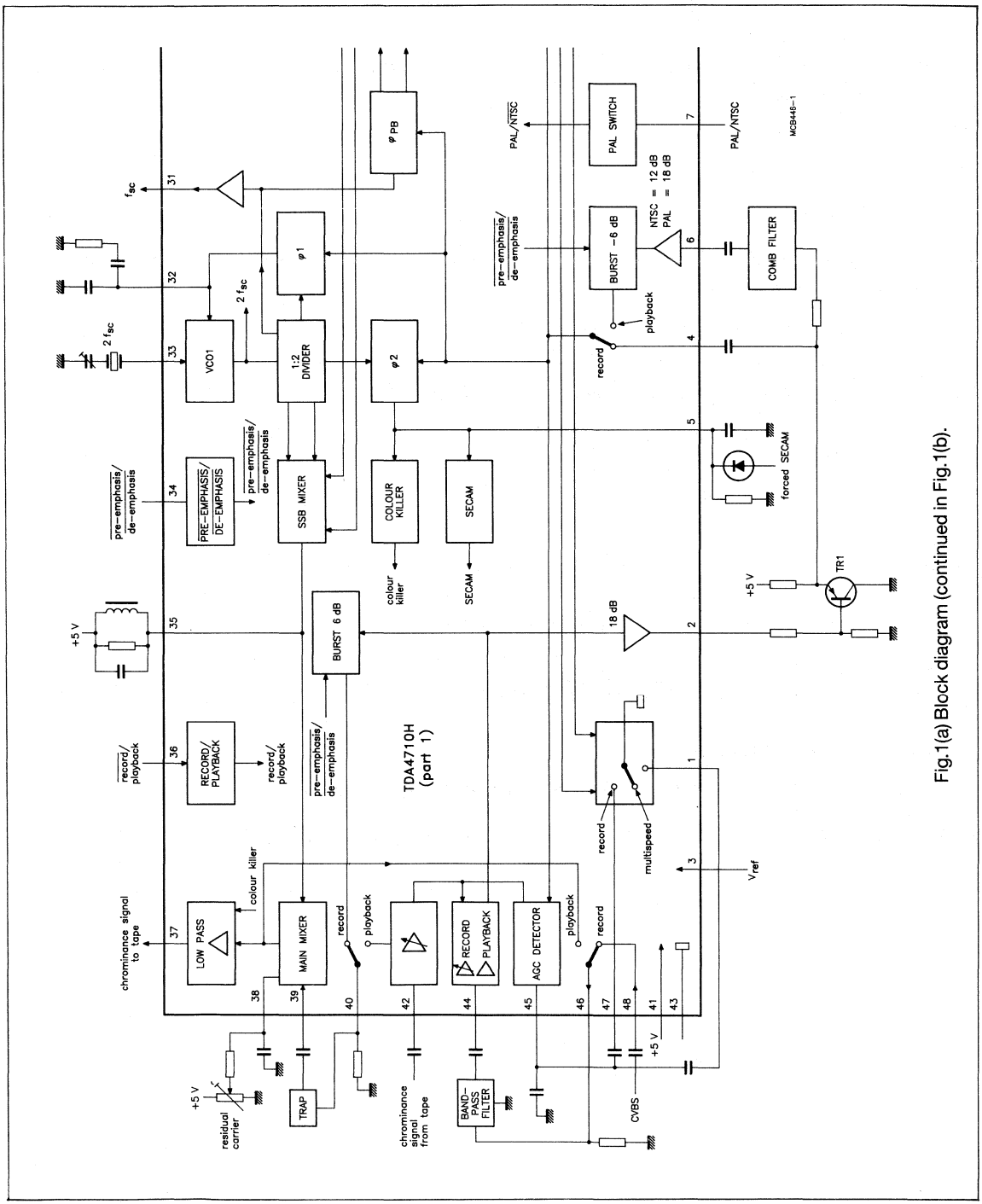


Fig.1(a) Block diagram (continued in Fig.1(b).

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

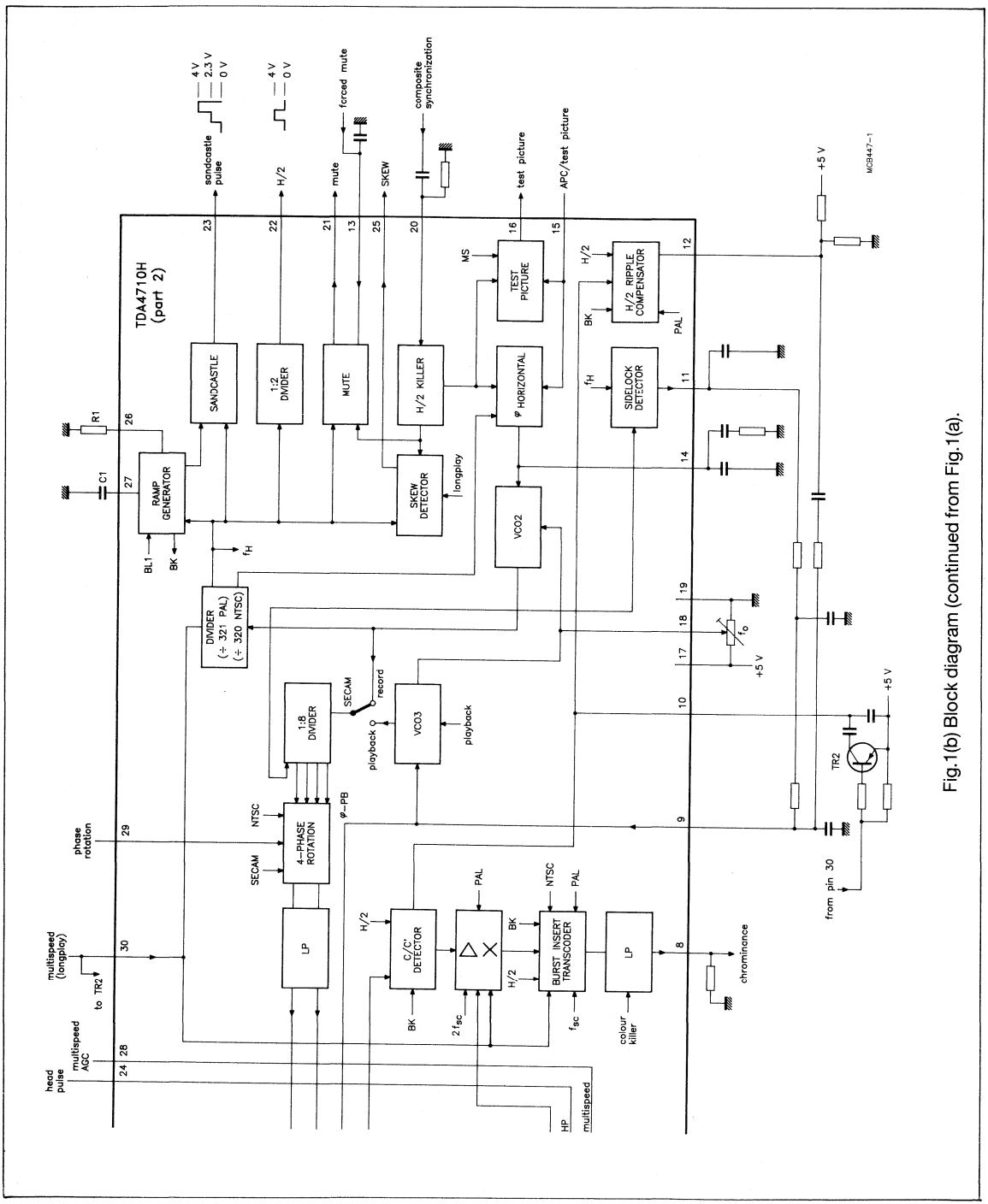


Fig.1(b) Block diagram (continued from Fig.1(a).

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

PINNING

PIN	DESCRIPTION
1	connection for an external capacitor, required for the AGC channel 2
2	chrominance/AGC output (record/playback)
3	reference voltage input
4	chrominance input (record)
5	colour-killer input/output, select colour ON, OFF or SECAM-BG mode
6	chrominance de-emphasis input (playback)
7	PAL/NTSC switch
8	chrominance output (to TV)
9	voltage controlled oscillator 3 (playback)
10	PAL sequence error detector output
11	sidelock detector output (playback)
12	H/2 ripple compensation output (playback)
13	connection for an external capacitor, required for the mute timing constant
14	voltage controlled oscillator 2
15	automatic phase correction (APC)/test picture input switch
16	test picture output
17	supply voltage, digital part
18	frequency adjustment for voltage controlled oscillator 2 and 3
19	ground, digital part
20	synchronization input
21	mute detector output
22	H/2 output
23	sandcastle pulse output
24	head-pulse input

PINNING (continued)

PIN	DESCRIPTION
25	SKEW detector output
26	sawtooth generator timing resistor
27	sawtooth generator timing capacitor
28	multispeed input switch (AGC)
29	phase rotation control input
30	multispeed input switch (longplay)
31	4.43/3.58 MHz subcarrier output
32	voltage controlled oscillator 1
33	crystal oscillator (8.86/7.16 MHz)
34	burst de-emphasis/pre-emphasis input switch
35	subcarrier resonance input (5.06 MHz, PAL; 4.21 MHz, NTSC)
36	record/playback input switch
37	627/629 kHz chrominance output signal to tape
38	main mixer balance capacitor
39	main mixer input
40	chrominance output signal
41	supply voltage, analog part
42	chrominance input signal from tape
43	ground, analog part
44	chrominance/AGC input (playback/record)
45	connection for an external capacitor, required for the AGC timing constant
46	chrominance selector output
47	connection for an external capacitor, required for the AGC channel 1
48	composite video blanking signal (CVBS) input

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	supply voltage				
V_{17-19}	digital part		-	6	V
V_{41-43}	analog part		-	6	V
	input voltage				
V_{13-19}			1	V_P	V
V_{18-19}			0	4	V
V_n	other voltages		0	V_P	V
	output currents				
$-I_{2,8,37,40,46}$			-	2	mA
$-I_{21,22,31}$			-	1	mA
$-I_{23}$			-	1	mA
$I_{1,25,47}$	other currents		-	3	mA
T_{amb}	operating ambient temperature range		0	70	°C
T_{stg}	storage temperature range		−25	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$R_{th\ j-a}$	junction-to-ambient		-	92	K/W

Table 1 Abbreviations used in the characteristics tables

ABBREVIATION	DESCRIPTION
f_{sc}	chrominance sub-carrier frequency: PAL, 4.433619 MHz; NTSC, 3.579545 MHz
f_H	line frequency: PAL, 15.625 kHz; NTSC, 15.73426 kHz
LP	longplay mode: PAL, 1.17 cm/s; NTSC, 1.667 cm/s
$N \times f_H$	PAL: $40.125 \times f_H = 626.953$ kHz NTSC: $40 \times f_H = 629.370$ kHz
MS	multispeed mode
V_T	temperature voltage (26 mV at 25 °C) generated at the emitter follower
I_C	collector current
C	PAL chrominance signal
C' (conjugate)	Complex PAL chrominance signal

CHARACTERISTICS

V_p = 5 V; V_{ref} = 1.4 V; burstkey duration = 4.0 µs; VCO 1 frequency = 4.433619/3.579545 MHz (PAL/NTSC) at pin 31 during playback mode; VCO 2 frequency = 15.625/1573426 kHz (PAL/NTSC) at pin 16 during test picture mode; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
	supply voltage range					
$V_P = V_{17-19}$	digital		4.5	5.0	5.5	V
$V_P = V_{41-43}$	analog		4.5	5.0	5.5	V
$V_{ref} = V_{3-43}$	reference input voltage		1.3	1.4	1.5	V
	input current without load					
I_{17}	digital		-	31	38	mA
I_{41}	analog		-	14	17	mA
PAL/NTSC SWITCH						
	input voltage					
V_{7-43}	PAL		3	-	V_P	V
V_{7-43}	NTSC		0	-	1.5	V
$\pm I_7$	input current		-	-	50	µA
RECORD/PLAYBACK SWITCH						
	input voltage					
V_{36-43}	record mode		0	-	3	V
V_{36-43}	playback mode		3.5	-	V_P	V
$\pm I_{7,36}$	input current		-	-	50	µA
COLOUR-KILLER (see note 1)						
	input voltage					
V_{5-43}	colour OFF		0	-	1	V
V_{5-43}	colour ON	no SECAM	2.5	-	3	V
V_{5-43}	SECAM ON (colour ON)		3.5	-	4.5	V
Record mode (see note 2)						
CONTROLLED CHROMINANCE AMPLIFIER SIGNAL						
$V_{48(P-p)}$	composite video signal input (peak-to-peak value)		-	450	-	mV
R_{48-43}	input resistance		14	20	26	kΩ
V_{48-43}	DC input voltage		-	2	-	V
$V_{40(p-p)}$	controlled output signal (peak-to-peak value)		-	335	-	mV
R_{40-43}	output resistance	note 3	-	$-V_T/I_C$	-	Ω
V_{40-43}	DC output voltage		-	3.1	-	V
BURST PRE-EMPHASIS						
	input voltage pre-/de-emphasis					
V_{34-43}	ON		0	-	0.8	V
V_{34-43}	OFF		1.5	-	V_P	V
$\pm I_{34}$	input current		-	-	50	µA
ΔV_{37-43}	burst pre-emphasis		5	6	7	dB

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHROMINANCE SELECTOR OUTPUT						
$V_{46(p-p)}$	output signal (peak-to-peak value)		-	450	-	mV
R_{46-43}	output resistance		-	$-V_T/I_C$	-	Ω
V_{46-43}	DC output voltage	note 3	-	2	-	V
CHROMINANCE INPUT SIGNAL						
$V_{44(p-p)}$	input signal (peak-to-peak value)		10	106	200	mV
R_{44-43}	input resistance		7	10	13	kΩ
V_{44-43}	DC input voltage		-	2.3	-	V
AGC OUTPUT						
	chrominance output	note 4				
$V_{2(p-p)}$	PAL, NTSC		-	840	-	mV
$V_{2(p-p)}$	SECAM		-	290	-	mV
R_{46-43}	output resistance		-	$-V_T/I_C$	-	Ω
V_{46-43}	DC output voltage	note 3	-	2	-	V
PHASE SYNC						
	chrominance input signal (peak-to-peak value)					
$V_{4(p-p)}$	PAL, NTSC		-	420	-	mV
$V_{4(p-p)}$	SECAM	note 4	-	145	-	mV
R_{4-43}	input resistance		14	20	26	kΩ
V_{4-43}	DC input voltage		-	2	-	V
627/629 kHz MIXER						
$V_{39(p-p)}$	input signal (peak-to-peak value)		-	335	-	mV
R_{39-43}	input resistance		-	2	-	kΩ
V_{39-43}	DC level		-	1.6	-	V
	output signal (peak-to-peak value)					
$V_{37(p-p)}$	PAL, NTSC		-	1.06	-	V
$V_{37(p-p)}$	SECAM	note 4	-	365	-	mV
R_{8-43}	output resistance	note 3	-	$-V_T/I_C$	-	Ω
	signal suppression					
α_{37}		$f_{sc} + N \times f_H$	35	-	-	dB
α_{37}		f_{sc}	40	-	-	dB
α_{37}		$2 \times N \times f_H$	30	-	-	dB
α_{37}		$3 \times N \times f_H$	35	-	-	dB
α_{37}		colour OFF	40	-	-	dB
CHROMINANCE OUTPUT						
	output signal (peak-to-peak value)					
$V_{8(p-p)}$	PAL, NTSC		-	420	-	mV
$V_{8(p-p)}$	SECAM	note 2	-	150	-	mV
V_{8-43}	DC output voltage		-	1.8	-	V
α_{CK}	signal suppression	colour OFF	35	-	-	dB

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{sc} PLL AND VC01						
V_{32-43}	DC voltage		-	2.7	-	V
V_{33-43}	DC voltage		-	1.8	-	V
R_{33-43}	input resistance		300	-	-	Ω
R_{VCO1}	crystal resistance	series	-	70	-	Ω
C_{33-43}	input capacitance		-	10	-	pF
Δf	oscillator lock-in frequency range	note 5	-	500	-	Hz
$\pm\Delta\varphi$	static phase error between reference and burst signal	$\Delta f = 400$ Hz	-	5	-	deg
TC	oscillator temperature coefficient		-	-	3	Hz/K
Playback mode (see notes 2 and 6)						
CHROMINANCE AGC						
$V42_{(p-p)}$	input signal (peak-to-peak value)		4.8	24	48	mV
R_{42-43}	input resistance		7	10	13	kΩ
V_{42-43}	DC input voltage		-	2.4	-	V
$V_{40(p-p)}$	output signal (peak-to-peak value)		-	237	-	mV
R_{40-43}	output resistance	note 3	-	$-V_T/I_C$	-	kΩ
V_{40-43}	DC output voltage		-	2.3	-	V
4.43/3.58 MHz MIXER						
V_{39-43}	input signal		-	237	-	mV
V_{39-43}	input resistance		-	2	-	kΩ
V_{39-43}	DC input voltage		-	1.6	-	V
$V_{46(p-p)}$	output signal (peak-to-peak value)	note 7	-	150	-	mV
R_{46-43}	output resistance	note 3	-	V_T/I_C	-	Ω
	signal suppression	note 8				
α_{46}		$f_{sc} + N \times f_H$	35	-	-	dB
α_{46}		$f_{sc} - N \times f_H$	35	-	-	dB
α_{46}		$f_{sc} - (2 \times N \times f_H)$	30	-	-	dB
CHROMINANCE AMPLIFIER						
$V_{44(p-p)}$	input signal (peak-to-peak value)		-	53	-	mV
R_{44-43}	input resistance		7	10	13	kΩ
V_{44-43}	DC input voltage		-	2.3	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHROMINANCE DE-EMPHASIS						
	input signal (peak-to-peak value)					
$V_{6(p-p)}$	PAL		-	53	-	mV
$V_{6(p-p)}$	NTSC		-	106	-	mV
R_{6-43}	input resistance		3.5	5.0	6.5	kΩ
V_{6-43}	DC input voltage		-	1.6	-	V
	output signal (peak-to-peak value)					
$V_{8(p-p)}$	PAL, NTSC		-	420	-	mV
$V_{8(p-p)}$	SECAM		-	150	-	mV
ΔV_{8-43}	burst de-emphasis	$V_{34-43} \leq 0.8$ V	–4.5	–5.5	–6.5	dB
R_{8-43}	output resistance	note 3	-	$-V_T/I_C$	-	Ω
V_{8-43}	DC output voltage		-	1.8	-	V
AGC CAPACITOR SWITCH $V_{28-43} \leq 1.5$ V; see note 9						
$I_{1,47-43}$	saturation voltage	$I_{1,47} = 1$ mA	-	-	500	mV
	headpulse input voltage	conductive				
V_{24-43}		pin 47	-	-	1.5	V
V_{24-43}		pin 1	3	-	-	V
V_{24-23}	input threshold voltage for blanking and burstkey suppression	note 10	1.5	2.5	3.0	V
$\pm I_{24}$	input current		-	-	50	µA
MULTI-SPEED AGC INPUT						
V_{28-43}	input voltage	normal mode; note 9	0	-	1.5	V
	input voltage for picture search					
V_{28-43}	normal sync		2	-	3	V
V_{28-43}	super sync		3.5	-	V_P	V
$\pm I_{28}$	input current		-	-	50	µA
PLAYBACK PHASE CONTROL - VCO3						
V_{9-43}	PLL DC voltage	locked	-	2.5	-	V
R_9	source resistance during burstkey suppression		-	40	-	kΩ
G	loop gain		-	800[3]	-	s
Δf	oscillator deviation with respect to f_{sc}		-	76	-	kHz/V
Δf	pull-in range with respect to f_{sc}		38	-	-	kHz

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder — TDA4710H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL SEQUENCE ERROR DETECTION						
	output voltage	see note 11				
V_{10-43}	HIGH		3.2	-	-	V
V_{10-43}	LOW		-	-	1.0	V
I_{10}	output current during burstkey		-	100	-	μA
$-\Delta I_{10}$	demodulated burst	polarity equal to H/2 signal	-	100	-	μA
$-\Delta I_{10}$	demodulated burst	polarity unequal to H/2 signal	-	100	-	μA
SIDELOCK DETECTOR						
$\pm I_{11}$	output current	sidelock detection	-	300	-	μA
t_p	pulse duration		-	64	-	μs
H/2 RIPPLE COMPENSATION						
$\pm I_{12}$	output current during burstkey		-	150	-	μA
V_{12-43}	DC range for linear operation		1.8	-	3.2	V
VC02 AND VCO3 f_O FREQUENCY CONTROL						
V_{18-43}	DC voltage		-	2	-	V
	nominal frequency					
f_{PAL}	PAL		-	5.016	-	MHz
f_{NTSC}	NTSC		-	4.208	-	MHz
$-I_{18}$	input current		-	100	-	μA
APC/TEST PICTURE (see note 12)						
	input voltage					
V_{15-43}	APC ON		0	-	1.4	V
V_{15-43}	APC OFF	test picture with white signal	2.7	-	3.4	V
V_{15-43}	APC OFF	test picture with white signal	4.3	-	V_P	V
$\pm I_{15}$	input current		-	-	50	μA
N x f_H PLL (VC02)						
V_{14-43}	PLL DC voltage	locked	-	1	-	V
R_{14-43}	source resistance during sync pulse		-	40	-	kΩ
G	loop gain		-	380	-	10^3/s
Δf	oscillator deviation related to f_H		-	900	-	Hz/V
Δf	pull-in range related to f_H		800	-	-	Hz

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital part						
TEST PICTURE OUTPUT (see note 13)						
	output voltage					
V_{16-19}	white level		-	2.1	-	V
V_{16-19}	black level		-	1.4	-	V
V_{16-19}	sync level		-	1.1	-	V
V_{16-19}	super sync level		-	-	0.25	V
R_{16-19}	source resistance		-	10	-	kΩ
SYNC INPUT SIGNAL						
V_{20-19}	sync input voltage		2.2	4.0	V_P	V
H/2 OUTPUT						
	output voltage					
V_{22-19}	HIGH	$-I_{22}$ = 0.5 mA	2.5	-	-	V
V_{22-19}	LOW	$-I_{22}$ = 0.5 mA	-	-	0.8	V
SANDCASTLE OUTPUT (see note 10)						
	output voltage					
V_{23-19}	LOW	I_{23} = 1 mA	-	-	0.5	V
V_{23-19}	MEDIUM	$-I_{23}$ = 0.5 mA	2.0	2.3	2.7	V
V_{23-19}	HIGH	$-I_{23}$ = 1 mA	3.75	4.0	-	V
BURSTKEY STAGE (see note 14)						
R_{26-19}	resistor R1		-	47	-	kΩ
t_p	burstkey pulse duration		-	4	-	µs
HEAD-PULSE INPUT FOR 4 PHASE ROTATION (see note 15)						
	input voltage					
V_{29-19}	channel 1		0	-	1.5	V
V_{29-19}	channel 2		3	-	V_P	V
$\pm I_{29}$	input current		-	-	50	µA
LP MS INPUT (see note 16)						
	input voltage					
V_{30-19}	normal mode		0	-	1.5	V
V_{30-19}	LPS MG		2	-	3	V
V_{30-19}	LPS MS	auto-burst				
V_{30-19}	NTSC, PAL-M	insertion	3.5	-	V_P	V
		transcoding	3.5	-	V_P	V
SEARCH CONTROL (SKEW) (see note 17)						
	output voltage					
V_{25-19}	LOW	I_{25} = 0.5 mA	-	-	0.8	V
V_{25-19}	HIGH	$-I_{25}$ = 20 µA	4	-	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital part (continued)						
MUTE FUNCTION						
	detector output voltage					
V_{21-19}	LOW	N x f_H; PLL locked, I_{21} = 0.5 mA	-	-	0.8	V
V_{21-19}	HIGH	N x f_H; PLL unlocked, I_{21} = 0.5 mA	2.5	-	-	V
	mute voltage					
V_{13-19}	LOW		3.5	-	-	V
V_{13-19}	HIGH	active	-	-	1.5	V
V_{13-19}	forced mute		1	-	1.5	V
f_{sc} SUB-CARRIER OUTPUT						
V_{31-19}	output signal		-	400	-	mV
R_{31-19}	output resistance		-	V_T/I_C	-	Ω
V_{31-19}	DC output voltage		-	1.2	-	V

Notes to the characteristics

1. SECAM-ON switching voltage is provided by the TDA4720(T).
2. PAL signal (red) with 75% saturation, 9 dB bandpath (pins 44 to 46), 6 dB trap (pin 2 to 4) and chrominance-to-burst ratio of 2.2:1.
3. NPN open emitter output.
4. All SECAM amplitudes are frequency values (red). Amplitude depends on the start moment of the frequency signal.
5. VCO1 operates as a fixed frequency oscillator during SECAM-mode.
6. Comb filter attenuations: PAL = 18 dB and NTSC = 12 dB.
7. Selective measurement of the f_{sc} component.
8. Measured at $V_{42-43(p-p)}$ = 12 mV.
   The signal suppression can be balanced at pin 38 (see Fig.1(a)).
9. During playback mode, the open collector output is conductive at the upper threshold and non-conductive at the lower threshold of the head pulse. The open collector output of pin 47 is conductive at the lower threshold and non-conductive at the upper threshold of the head pulse. During LP MS mode, pins 1 and 47 are simultaneously conductive independent of the head pulse.

Notes to the Characteristics (continued)

10. When the threshold of pin 24 is passed the upper part of the sandcastle pulse (pin 23) is suppressed 11 times and the chrominance output signals (pins 8 and 37) are colour killed for 13 lines.

11. Only active in PAL mode:
    - Output is HIGH, if the polarity of the demodulated burst is equal to the H/2 signal. In LP MS mode (pin 30 = HIGH) C/C' mixer is active.
    - Output voltage is LOW, if the polarity of the demodulated burst is unequal to the H/2 signal. In LP MS mode (pin 30 = HIGH) C/C' amplifier is active.

12. If APC = OFF, the mute output (pin 21) is switched to forced HIGH (used for automatic test picture insertion).

13. Test picture output signals depend on the control voltages at pins 15 and 28 as shown in Table 2. V_{ref} at pin 3 is loaded by the output current I_{16}.

Table 2 Control of test picture output signals

CONDITION	PIN 15 (V)	PIN 28 (V)	SEE FIG.2
APC OFF, test picture without white signal	2.7 to 3.4	<3	2(b)
APC OFF, test picture with white signal	>4.3	<3	2(a)
APC ON	<1.4	<3	2(b)
APC ON, super sync ON	<1.4	>3.5	2(c)

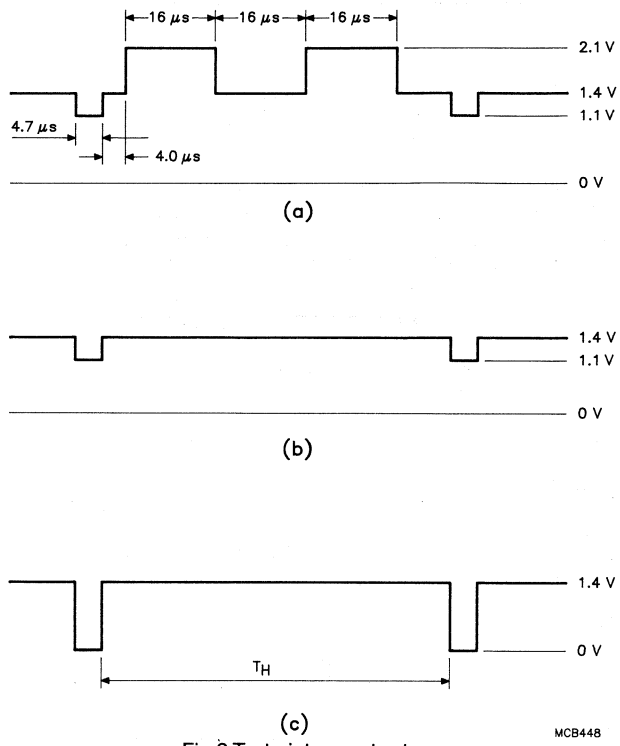

Fig.2 Test picture output.

Notes to the characteristics

14. Values refer to Fig.3 (R1 is the resistor from pin 26 to ground, C1 is the capacitor from pin 27 to ground):

- t_1 = 0.305 ms; R1C1
- t_2 = < 0.210 ms; R1C1
- t_3 = 0.1 ms; R1C1
- $t_4 1$ = 0.367 ms;

15. Phase rotation:

MODE	CHANNEL 1($V_{29\text{-}19}$ = LOW)	CHANNEL 2 (V29-19 = HIGH)
PAL	0°	–90°
NTSC	+90°	–90°
SECAM	0°	0°

16. Switching to LP MS mode activates the $2f_H$ mode of the VCO2 PLL, automatic SKEW detection and automatic PAL sequence error correction.

17 If the video head changes from one track to another during LP MS mode, the 32 µs time shifted sync pulse occurs. This shift is recognized by the SKEW detector.

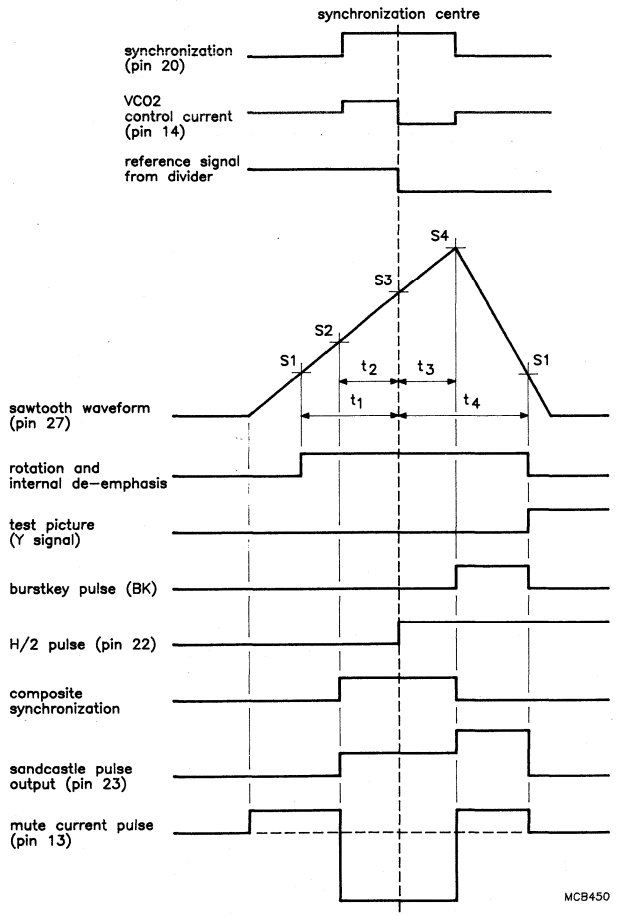

Fig.3 Timing diagram.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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APPLICATION INFORMATION

(Figs 4 to 39 show equivalent internal circuit configurations. All circuits are ESD protected).

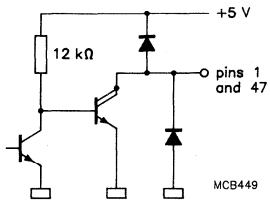


Fig.4 AGC switch output.

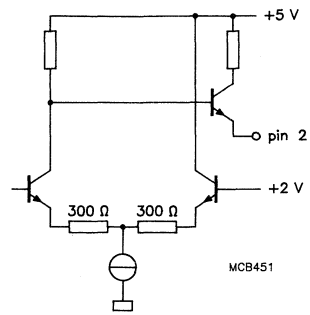


Fig.5 Chrominance output.

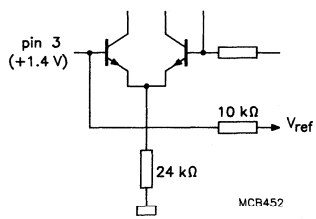


Fig.6 Voltage reference input.

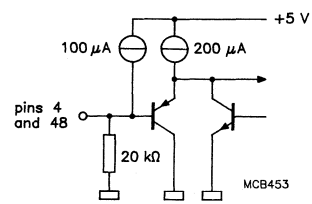
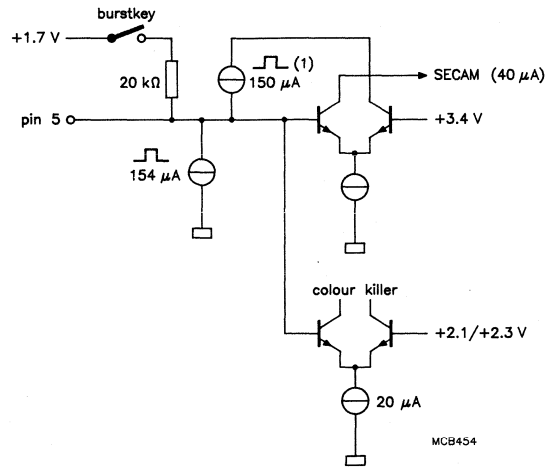


Fig.7 Chrominance/CVBS input.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H



(1) with an applied burst of 166 μA.

Fig.8 Colour-killer and SECAM switch input.

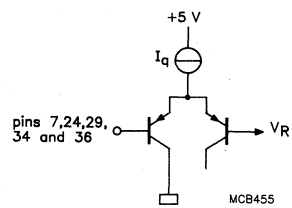


Fig.9 PAL/NTSC switch input (see Table 4).

Table 4 Switch characteristics

PIN	SIGNAL	QUIESCENT CURRENT (μA)	V(R) VOLTAGE (V)
7	PAL/NTSC switch input	20	2.5
24	HP input	30	2.5
29	phase rotation switch input	30	2.5
34	de/pre-emphasis switch input	30	1.1
36	record/playback switch input	20	3.3

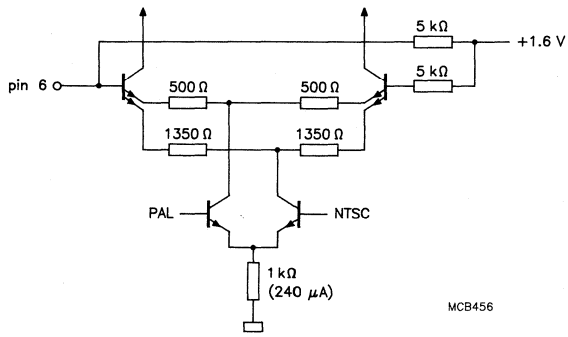


Fig.10 De-emphasis input.

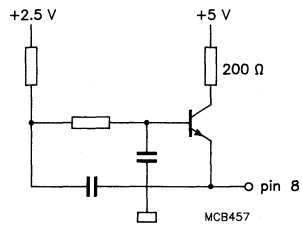


Fig.11 Chrominance output (pin 8).

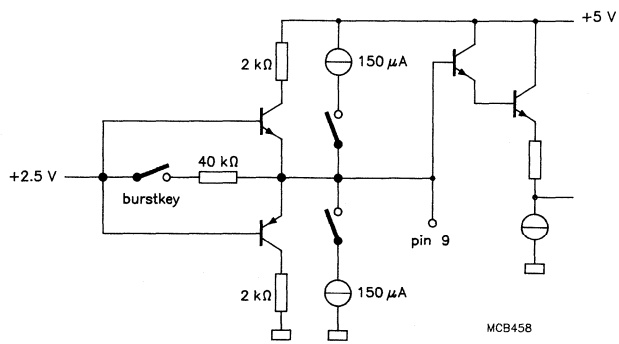


Fig.12 VCO3 control input.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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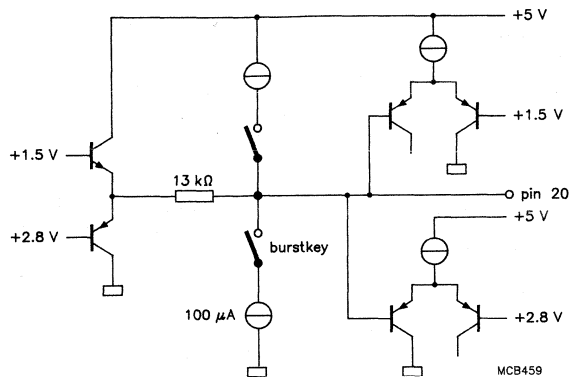

Fig.13 Sequence error detector.

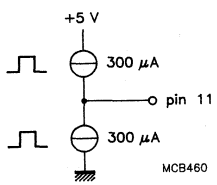

Fig.14 Sidelock detector output.

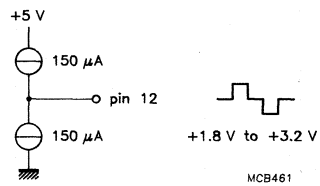

Fig.15 H/2 ripple coupling output.

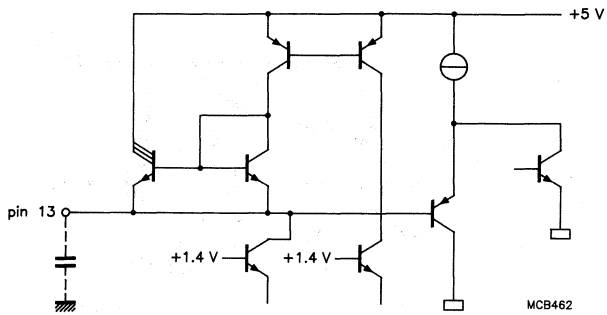

Fig.16 Mute timing input.

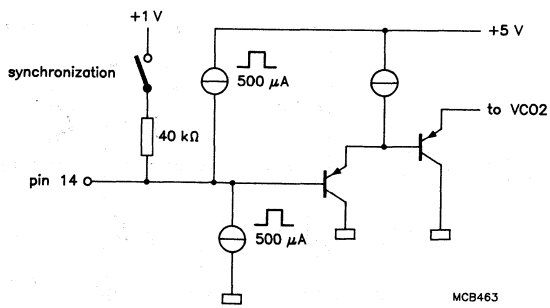

Fig.17 VCO2 control input.

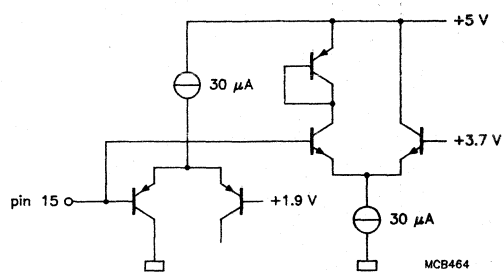

Fig.18 APC/test picture switch input.

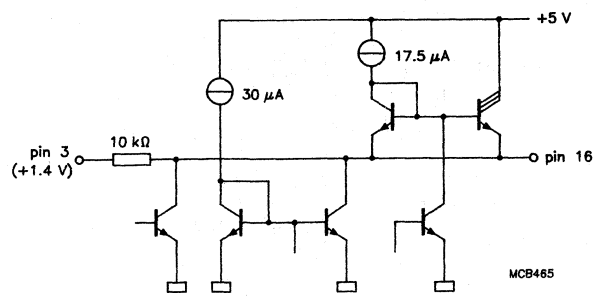

Fig.19 Test picture output.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

TDA4710H

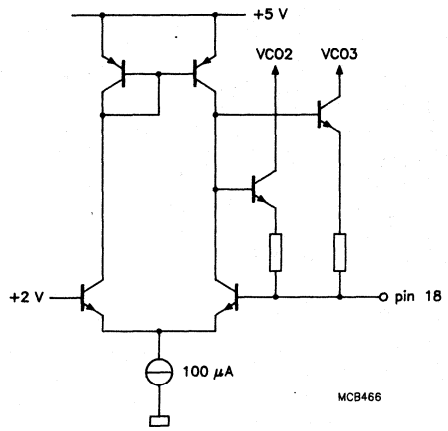

Fig.20 VCO2/VCO3 adjustment input.

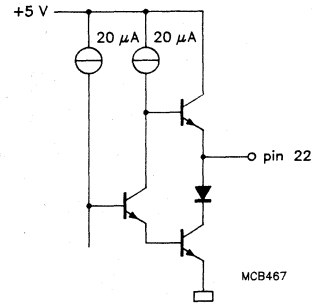

Fig.21 H/2 output.

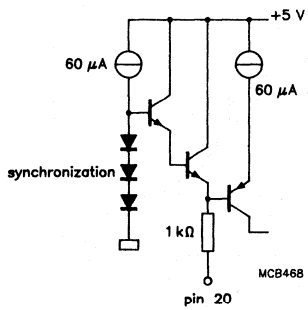

Fig.22 Synchronization input.

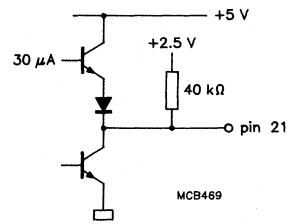

Fig.23 Mute detector output.

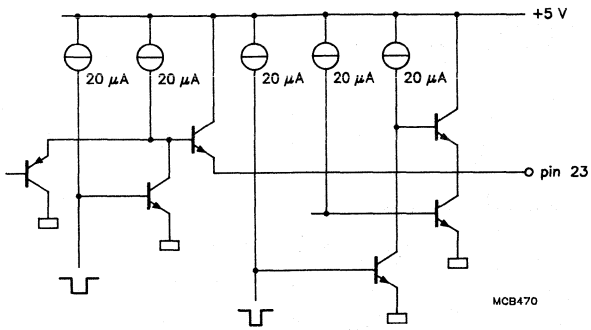

Fig.24 Sandcastle pulse output.

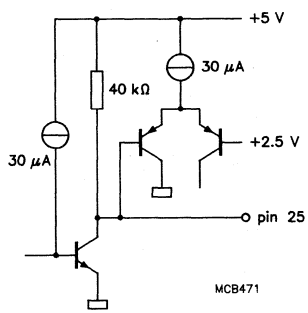

Fig.25 Skew detector output.

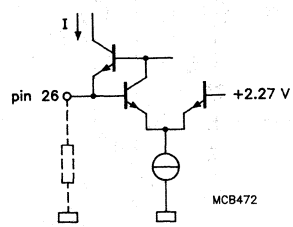

Fig.26 Reference current input for the sawtooth generator.

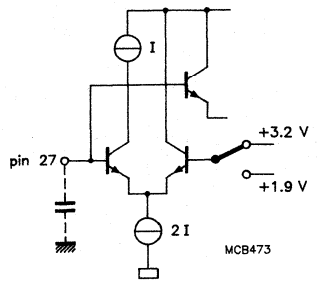

Fig.27 Sawtooth generator.

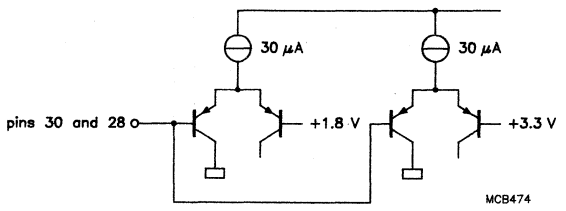

Fig.28 Multispeed AGC/LP input.

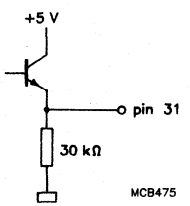

Fig.29 Subcarrier signal output.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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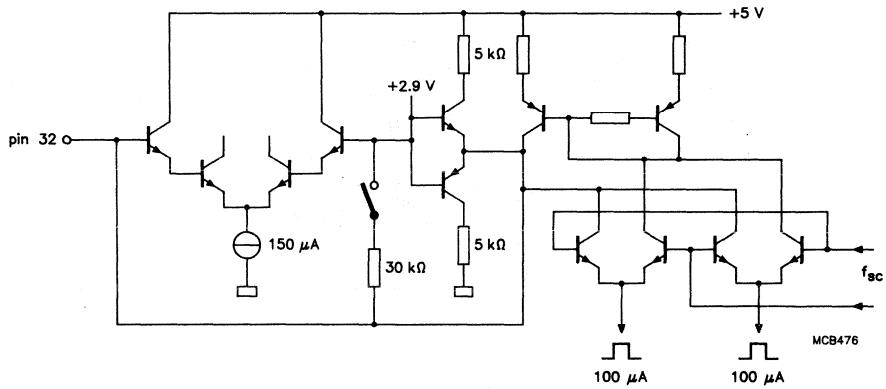

Fig.30 VCO1 control input.

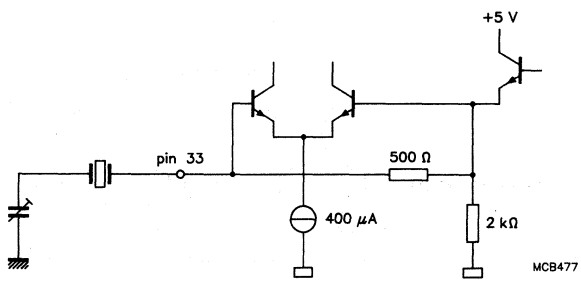

Fig.31 Oscillator input.

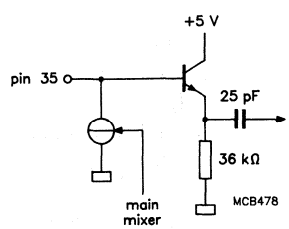

Fig.32 Subcarrier resonance output.

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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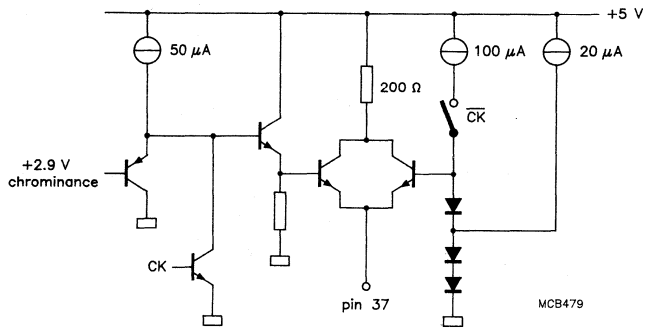

Fig.33 Chrominance signal output.

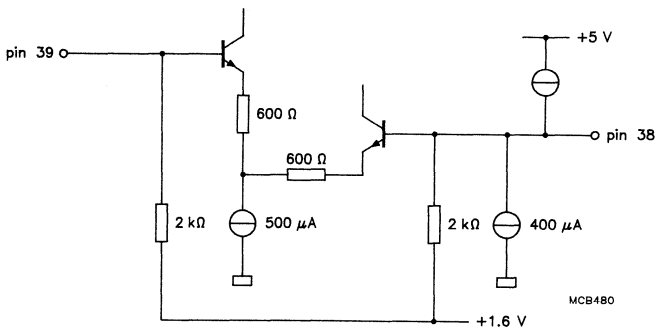

Fig.34 Main mixer input/balance circuit.

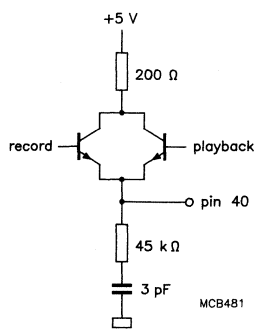

Fig.35 Chrominance output.

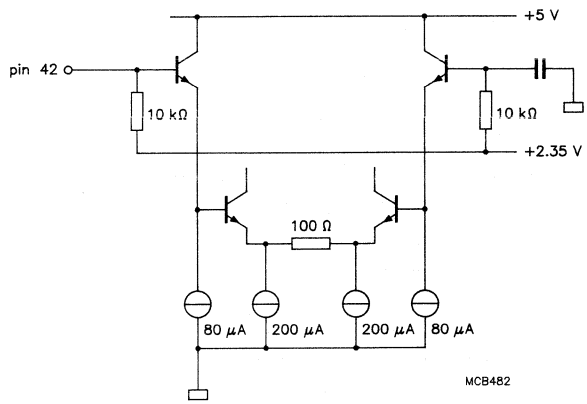

Fig.36 Chrominance input.

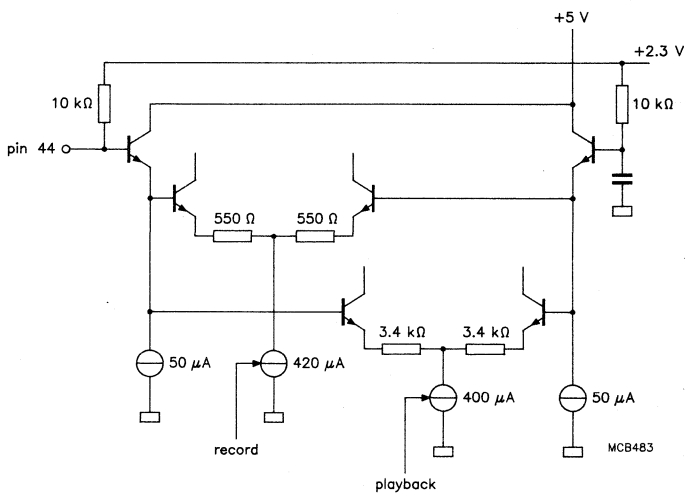

Fig.37 Chrominance AGC input.

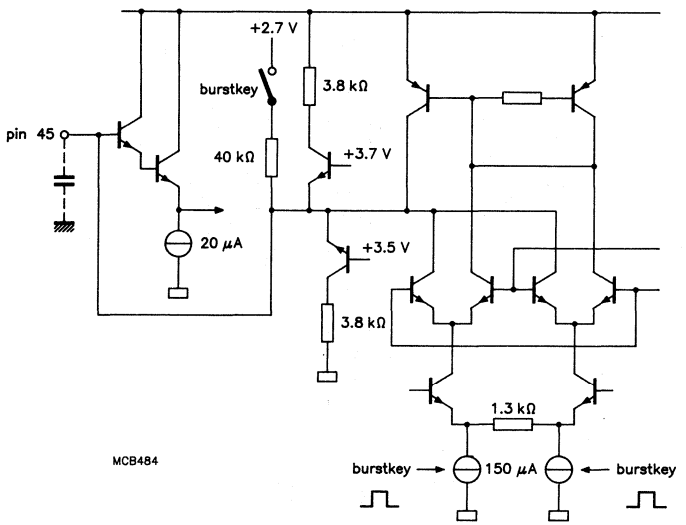

Fig.38 AGC control input.

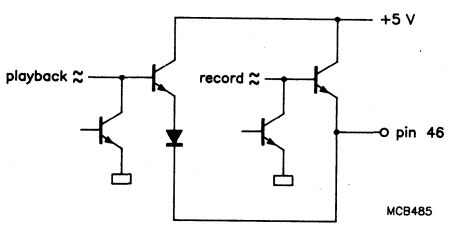

Fig.39 Chrominance output.

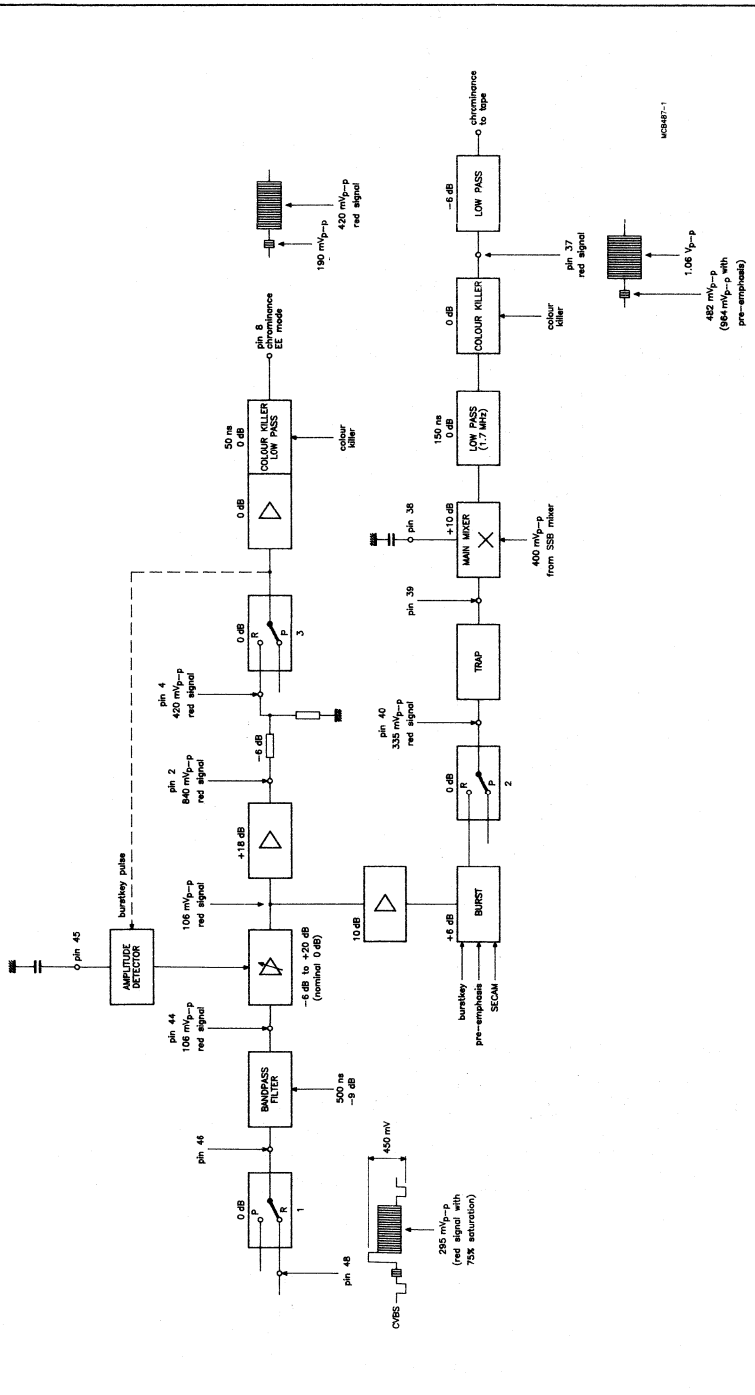

Fig.40 Signal path; record mode.

Where:

P = playback
R = record

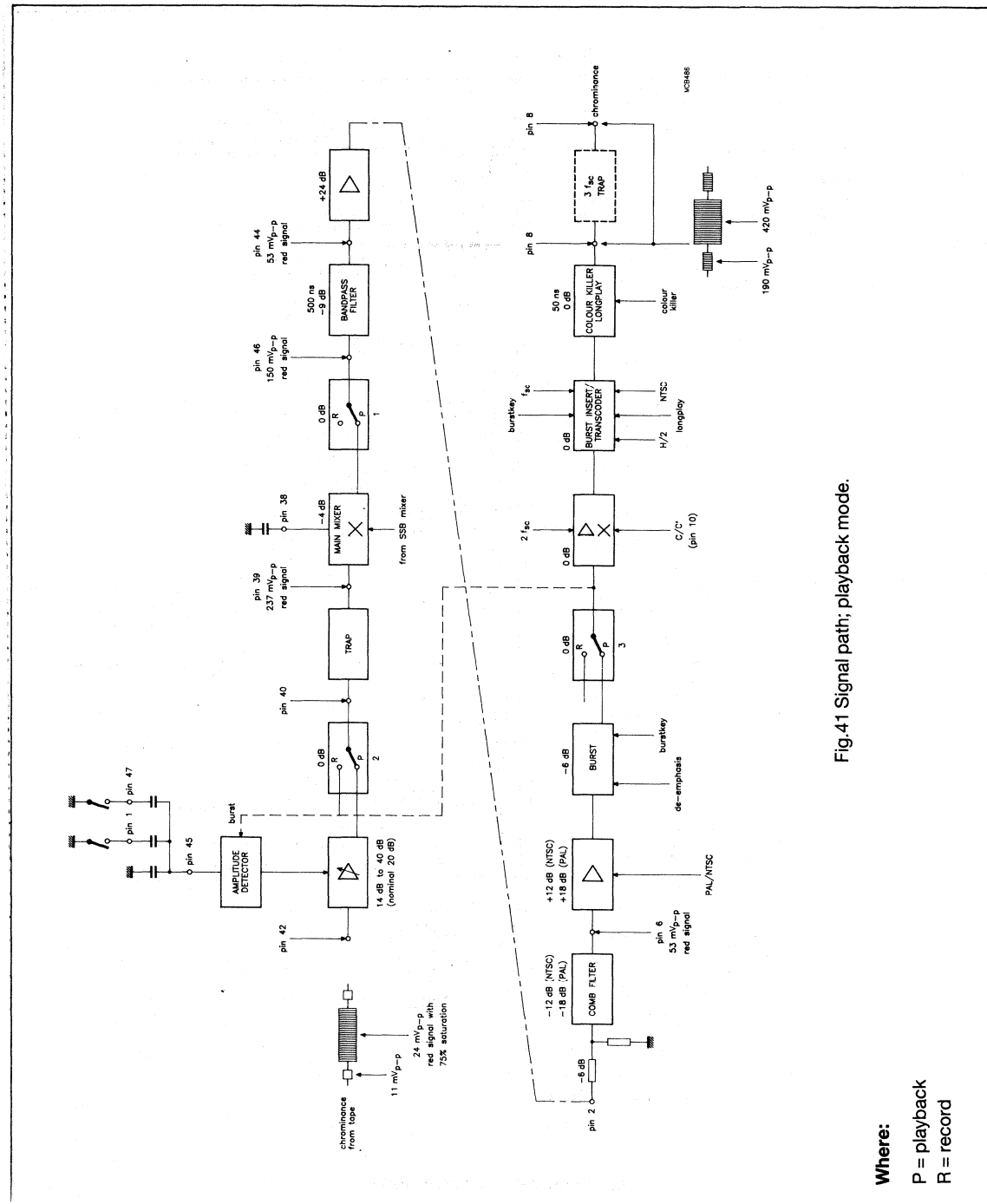

Fig.41 Signal path; playback mode.

Where:

P = playback
R = record

VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder

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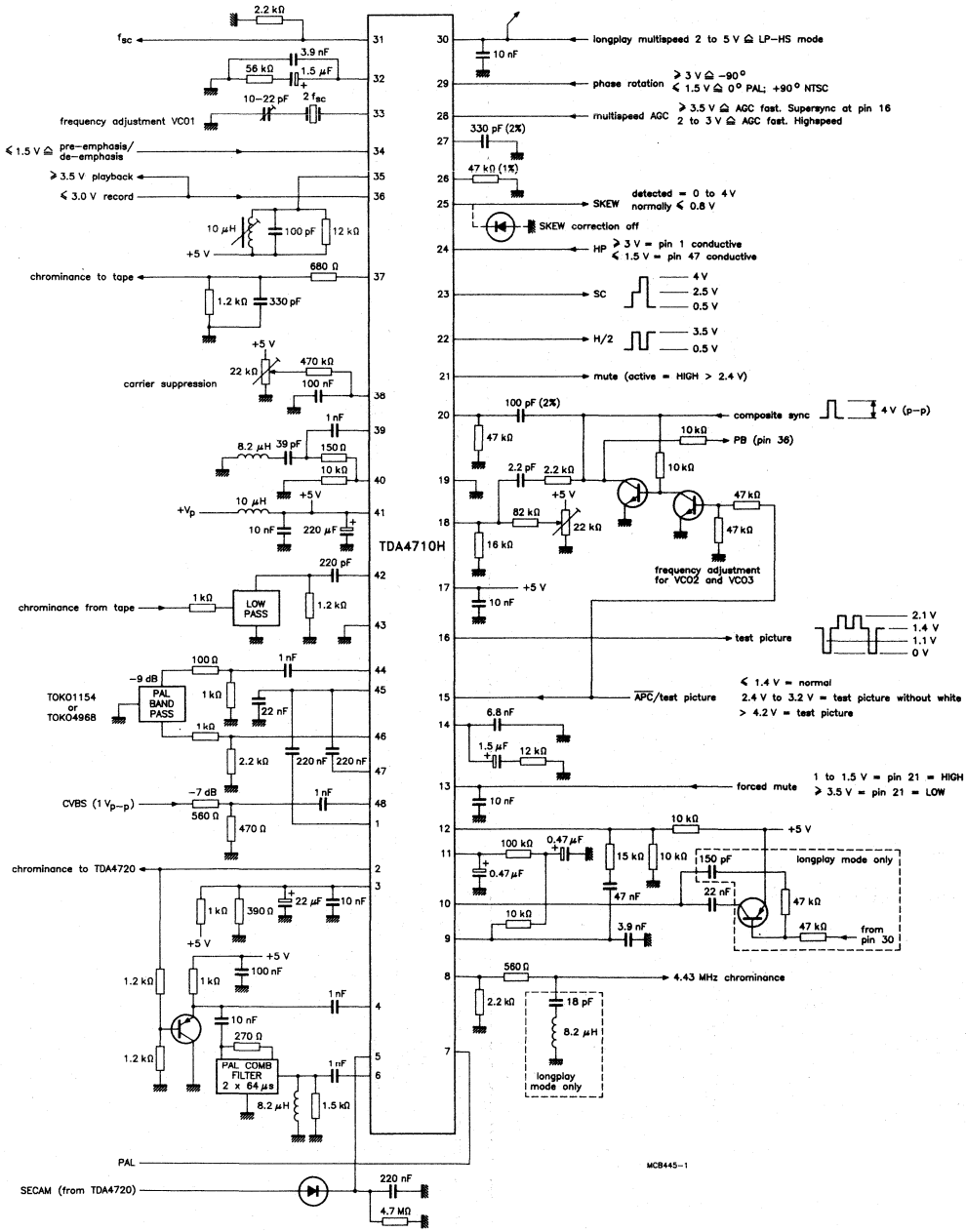

Fig.42 Application diagram (PAL).

Note to Fig.42

If not otherwise stated, the tolerance for external components is:
resistors ±5%
capacitors ±20%
inductors ±10%

SECAM IDENTIFICATION AND CHROMINANCE CORRECTION CIRCUIT

The TDA4720T is a monolithic integrated circuit for SECAM identification and chrominance signal correction in VHS video cassette recorders (VCR). It can be applied as a stand-alone SECAM identification circuit and, when used in conjunction with TDA4710, together they provide all the functions necessary for PAL/SECAM B, G chrominance processing in VHS VCRs.

Features

- Very reliable SECAM identification by means of chrominance burst amplitude, presence of both SECAM colour carriers and line alternation of both carriers
- Two identification outputs: SECAM YES/NO
- Internal phase correction of the demodulated burst
- Internal detection and switching for SECAM long-play VCR (for 'trick' modes)
- Internal buffers and switches for correction of the line-alternating colour carriers

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_P	4,5	5,0	5,5	V
Supply current	I_P	–	16	17	mA
Chrominance input signal to phase detector (peak-to-peak value)	$V_{14,15-4(p-p)}$	60	–	300	mV
Chrominance input signal to line correction circuit (peak-to-peak value)	$V_{5,12-4(p-p)}$	–	–	1	V
Chrominance output signal from line correction circuit (peak-to-peak value)	$V_{7-4(p-p)}$	–	–	1	V

PACKAGE OUTLINES

TDA4720: 16-lead DIL; plastic (SOT38).
TDA4720T: 16-lead mini-pack; plastic (SO16; SOT109A).

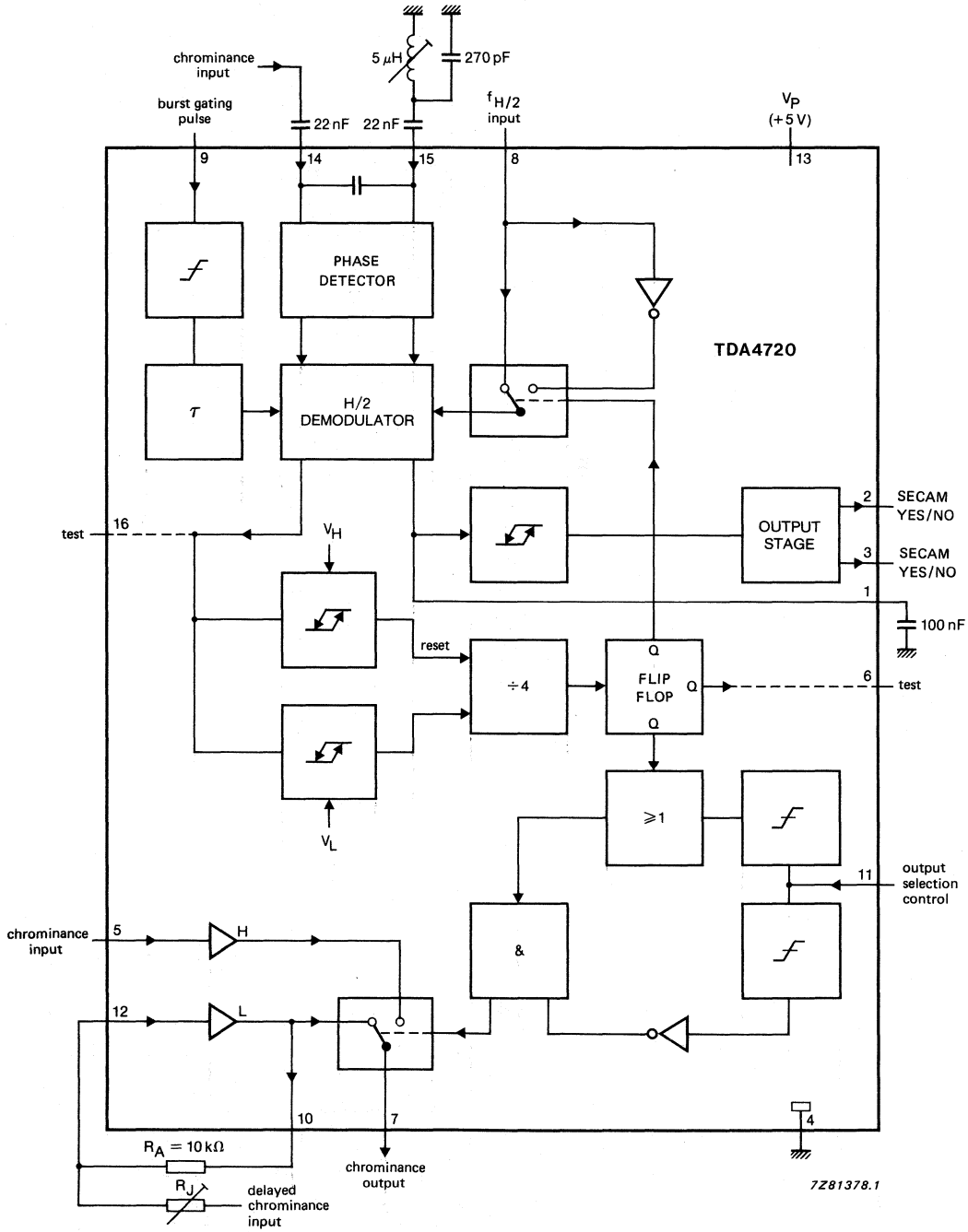

Fig. 1 Block diagram and test circuit.

PINNING

pin. no.	function
1	Integration of demodulated bursts.
2	Buffered output; SECAM YES/NO.
3	Buffered output; SECAM YES/NO.
4	Ground.
5	Chrominance input (only if line correction of SECAM carrier is used).
6	Test pin (internal connection).
7	Chrominance output (of line-corrected SECAM; only if line correction of SECAM carrier is used).
8	$f_{H/2}$ frequency input for chrominance burst demodulation.
9	Burst gating pulse input.
10	Feedback resistor for pin 12 signal path (only if line correction of SECAM carrier is used).
11	Output selection control (selects signal path to pin 7).
12	Delayed chrominance input (delayed by 1H; only if line correction of SECAM carrier is used).
13	Positive supply voltage (V_P = + 5 V).
14,15	The LC circuit at pin 15 has to be tuned to the centre frequency between the two chrominance carriers (at pin 14). The phase detector then provides a positive or negative output voltage depending on the first or second chrominance carrier.
16	Test pin (internal connection).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 13)	$V_P = V_{13-4}$	–	6,0	V
Voltage range on pins 6, 8, 9, 11, 12, 14 and 15	V_{n-4}	0	V_P	V
Maximum current at pins 1, 2, 3, 7, 15, 16 and 18	I_n	–	2	mA
Total power dissipation	P_{tot}	–	120	mW
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

CHARACTERISTICS

$V_P = V_{13-4} = 5$ V; $T_{amb} = 25\ ^oC$; test circuit as per Fig. 1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 13)		V_P	4,5	5,0	5,5	V
Supply current		I_{13}	–	16	17	mA
Identification						
AC input voltage (peak-to-peak value)		$V_{14,15-4}$	60	125	300	mV
Input resistance		$R_{14,15-4}$	14	18	22	kΩ
Charge capacitor		C_{1-4}	–	100	–	nF
Forced SECAM-ON voltage		V_{1-4}	3,8	–	–	V
Forced SECAM-OFF voltage		V_{1-4}	–	–	2	V
Sensitivity of phase detector	$V_{14,15-4(p-p)}$ = 125 mV	α	–	1,6	–	V/rad.
Output voltage						
in SECAM mode		$V_{2,3-4}$	4,3	–	–	V
in non-SECAM mode		$V_{2,3-4}$	–	–	0,8	V
Output current						
in SECAM mode		$I_{2,3}$	1	–	–	mA
in non-SECAM mode		$I_{2,3}$	–	–	0,3	μA
Burst gating						
Input resistance		R_{9-4}	20	25	–	kΩ
Threshold voltage HIGH (phase detector active)		V_{9-4}	3,0	3,25	3,5	V
H/2 demodulator						
Input resistance		R_{8-4}	20	25	–	kΩ
Threshold voltage for changing conditions of H/2 demodulator		V_{8-4}	3,0	3,25	3,5	V
Chrominance correction						
Chrominance input signal (peak-to-peak value)		$V_{5-4(p-p)}$	–	–	1	V
Input resistance		R_{5-4}	10	13	16	kΩ
Input capacitance		C_{5-4}	–	–	10	pF

parameter	conditions	symbol	min.	typ.	max.	unit
Delayed chrominance input signal (peak-to-peak value)		$V_{12\text{-}4(p\text{-}p)}$	–	–	1	V
Input resistance		$R_{12\text{-}4}$	–	50	–	kΩ
Input capacitance		$C_{12\text{-}4}$	–	–	10	pF
Voltage gain		$\frac{V_{7\text{-}4}}{V_{12\text{-}4}}$	–	$\frac{R_A}{R_J}$	–	
Gain adjustment range		ΔG	19	–	–	dB
Gain bandwidth product		f_G	30	–	–	MHz
Output signal (peak-to-peak value)		$V_{7\text{-}4(p\text{-}p)}$	–	–	1	V
Output resistance		$R_{7\text{-}4}$	$\frac{V_T}{I_C}$	–	–	Ω
DC output voltage		$V_{7\text{-}4}$	–	–	2,5	V
Difference in DC output levels at pin 7 with pin 5/pin 12 switching		$\Delta V_{7\text{-}4}$	–	–	20	mV
Output selection control						
Input resistance		$R_{11\text{-}4}$	20	25	30	kΩ
Input voltage to select pin 5 signal for output		$V_{11\text{-}4}$	0	–	1,5	V
Input voltage to select pin 12 signal for output		$V_{11\text{-}4}$	2,75	–	5,0	V
Input voltage for automatic output switching*		$V_{11\text{-}4}$	2,0	–	2,6	V

* This voltage is generated internally if pin 11 is not connected.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA4725T

SECAM-L chrominance processor for VHS video recorders

FEATURES

- Forced recording or playback mode input
- SECAM identification circuit
- One circuit for Bell and anti-Bell filter (1.07 MHz)
- Fully ESD protected
- Low power consumption (170 mW)
- 5 V supply.

GENERAL DESCRIPTION

The TDA4725 is a bipolar integrated circuit for chrominance processing of SECAM-L signals in SECAM-L or Multistandard VHS video recorders.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{18\text{-}24,26}$	supply voltage		4.5	5.0	5.5	V
I_{18}	supply current		-	34	-	mA
$V_{25\text{-}24(p\text{-}p)}$ $V_{21\text{-}24(p\text{-}p)}$	chrominance input (peak-to-peak value)	record mode playback mode	- -	- 300	645 600	mV mV
$V_{15\text{-}24(p\text{-}p)}$ $V_{1\text{-}24(p\text{-}p)}$	chrominance output (peak-to-peak value)	record mode playback mode	560 -	630 -	700 1000	mV mV
T_{amb}	operating ambient temperature range		0	-	70	°C
T_{stg}	storage temperature range		–25	-	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4725	28	DIL28	plastic	SOT117
TDA4725T	28	SO28	plastic	SOT136A

SECAM-L chrominance processor for VHS video recorders

TDA4725T

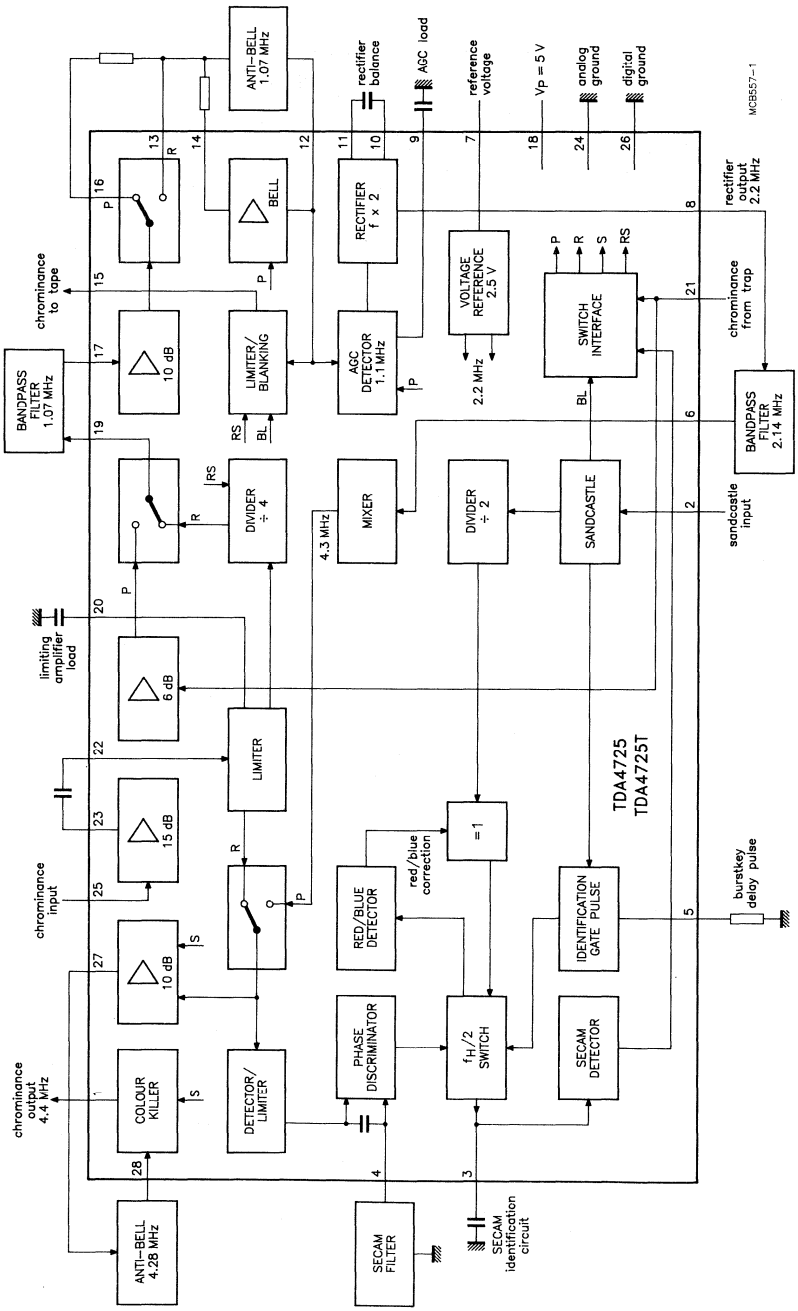

Fig.1 Block diagram.

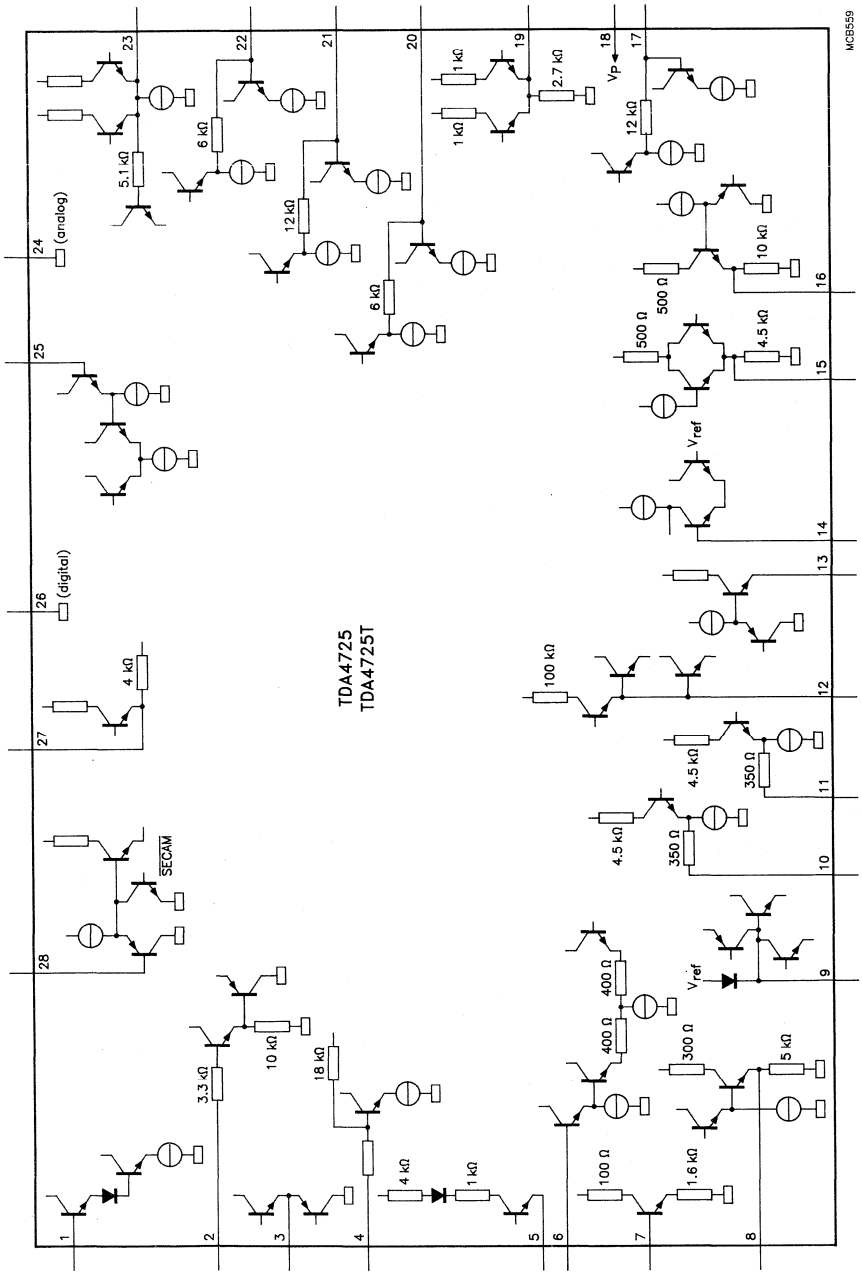

Fig.2 Internal pin configuration diagram.

PINNING

PIN	DESCRIPTION
1	chrominance output (4.4 MHz)
2	sandcastle pulse or composite synchronization pulse input
3	connection for external load capacitor for the SECAM identification circuit
4	connection for external resonance circuit for the phase discriminator circuit
5	connection for resistor required for internal delay of burstkey pulse
6	mixer input
7	reference voltage
8	rectifier circuit output (2.2 MHz)
9	connection for external load capacitor for the AGC
10	connection for external balancing capacitor for the rectifier circuit
11	connection for external balancing capacitor for the rectifier circuit
12	output to passive anti-Bell circuit and limiter circuit (record mode) or output to Bell circuit and AGC circuit (playback mode)
13	10 dB amplifier output to anti-Bell circuit (record mode only)
14	virtual ground
15	chrominance signal output to tape (1.1 MHz)
16	output 10 dB amplifier and input active Bell filter (playback mode only)
17	input to 10 dB amplifier
18	power supply
19	divider output (record mode) or 6 dB amplifier output (playback mode)
20	external capacitor for limiting amplifier
21	chrominance signal input from tape
22	limiting amplifier input
23	15 dB amplifier output
24	analog ground
25	15 dB amplifier input
26	digital ground
27	10 dB amplifier output
28	input for colour killer circuit

SECAM-L chrominance processor for VHS video recorders

TDA4725T

FUNCTIONAL DESCRIPTION (see Fig.1)

Recording mode

The chrominance signal is separated from the CVBS signal using an external bandpass filter and an external Bell circuit. The signal is applied to a divider (÷ 4) via a 15 dB amplifier (pin 25) and limiter (pin 22). Once divided the 1.1 MHz signal is fed via an external bandpass filter (pins 17 and 19), an internal 10 dB amplifier (via pin 17), an external anti-Bell filter (pins 12 and 13) and a limiter/blanking stage. The blanking stage is active during the sandcastle pulses.

E to E mode

The 4.4 MHz signal is obtained from a tap in the limiter circuit and is applied to the chrominance output (pin 1) via the 10 dB amplifier, the external anti-Bell circuit and the colour-killer stage

Playback mode

The 1.1 MHz signal from the tape is applied, via a trap, to an internal 6 dB amplifier (via pin 21). Once amplified the signal is applied via an external bandpass filter and 10 dB amplifier to an operational amplifier (pins 12 and 14). The operational amplifier has an external anti-Bell circuit connected in its feedback path and, consequently, performs as a Bell circuit. From the operational amplifier the signal is applied to the AGC stage. The output signal from the AGC stage is applied to a rectifier where the frequency is doubled. Unwanted harmonics are removed by an external bandpass filter (pins 6 and 8) and the frequency is again doubled by the mixer at pin 6. The resultant 4.4 MHz signal is applied to the output stage at pin 1 via the 10 dB amplifier, the external anti-Bell circuit and the colour killer stage.

NOTE: The 1.07 MHz bandpass filter (pins 17 and 19) and the anti-Bell circuit (pins 12 and 13) are used in both the record and playback mode.

SECAM identification

For SECAM identification the input signal is phase shifted by an external resonent circuit [$f_O = (f_b + f_r)/2$] and fed to the phase discriminator at pin 4. If the signal is a SECAM signal the positive- and negative-going pulses (with reference to the clamping voltage) are generated and rectified via the H/2 demodulator. The signal now consists of positive-going pulses only which are integrated via an external capacitor and applied to the SECAM detector at pin 3.

A non-SECAM signal (i.e. PAL) is removed from the phase discriminator having only positive-going pulses. After the H/2 demodulator, the signal has line-alternate positive- and negative-going pulses which compensate after integration.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Ratings System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	-	6	V
P_{tot}	total power dissipation	-	250	mW
T_{stg}	storage temperature range	−25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 1						
$V_{1-24(p-p)}$	chrominance output signal (peak-to-peak value)	4.4 MHz sinusoidal signal	-	-	1	V
V_{1-24}	DC level	SECAM signal non-SECAM signal	- -	V_{28-24} -	- 0.1	V V
R_{1-24}	output resistance		-	V_t/I_e	-	Ω
α_1	non-SECAM signal suppression		40	-	-	dB
Pin 2						
V_{2-24}	phase discriminator active voltage level		3.6	-	V_P	V
V_{2-24}	blanking active voltage level		2.0	2.5	3.0	V
V_{2-24}	blanking and phase discriminator inactive voltage level		-	-	1.5	V
R_{2-24}	input resistance		20	-	-	kΩ
Pin 4						
R_{4-24}	input resistance		14	18	22	kΩ
Pin 5						
R_{5-24}	required resistance to ground	for 1 μs	-	26	-	kΩ
Pin 6						
V_{6-24}	input signal	2.2 MHz sinusoidal signal	-	300	-	mV
V_{6-24}	DC level		-	V_{7-24}	-	V
R_{6-7}	input resistance		-	560	1200	Ω
C_{6-24}	input capacitance		-	-	5	pF
Pin 7						
V_{7-24}	DC level		2.4	2.5	2.6	V
$-I_7$	output current		-	-	5	mA
I_7	input current		1	-	-	mA
R_{7-24}	output resistance		-	-	1	Ω
Pin 8						
$V_{8-24(p-p)}$	output signal voltage (peak-to-peak)	2.2 MHz	-	600	-	mV
V_{8-24}	DC level		-	2.45	-	V
R_{8-24}	output resistance		-	V_t/I_e	-	Ω
α_8	1.1 MHz suppression		30	-	-	dB
α_8	3.3 MHz suppression		30	-	-	dB
α_8	4.4 MHz suppression		10	-	-	dB
Pin 12						
$V_{12-24(p-p)}$	input signal (peak-to-peak value)	playback mode	24	-	320	mV
V_{12-24}	DC level	record mode playback mode (closed loop)	- -	V_{13-24} V_{7-24}	- -	V V
B	gain bandwidth (operational amplifier)	playback mode	40	-	-	MHz
R_{12-24}	input resistance	record mode	100	-	-	kΩ
R_{12}	open-loop output resistance		-	V_t/I_e	-	Ω

SECAM-L chrominance processor for VHS video recorders

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SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 13 V_{13-24}	DC level	record mode	-	V_{7-24}– 85 mV	-	V
G_{13-24}	signal gain	record mode	-	10	-	dB
R_{13-24}	output resistance	record mode	-	V_t/I_e	-	Ω
Pin 14 V_{14-24}	DC level	playback mode	-	V_{7-24}	-	V
Pin 15 $V_{15-24(p-p)}$	chrominance output (peak-to-peak value)		560	630	700	mV
V_{15-24}	DC level		-	V_{7-24}– 80 mV	-	V
R_{15-24}	output resistance		-	-	10	Ω
α_{15}	playback suppression		30	-	-	dB
α_{15}	non-SECAM suppression		40	-	-	dB
α_{15}	blanking suppression		30	-	-	dB
Pin 16 V_{16-24}	DC level	playback mode	-	V_{7-24}– 54 mV	-	V
G_{16-17}	signal gain	playback mode	-	10	-	dB
R_{16-24}	input resistance	record mode	-	10	-	kΩ
R_{16-24}	output resistance	playback mode	-	V_t/I_e	-	Ω
Pin 17 $V_{17-24(p-p)}$	input signal (peak-to-peak value)		-	400	-	mV
V_{17-24}	DC level		-	V_{7-24}– 30 mV	-	V
R_{17-24}	input resistance		8	12	16	kΩ
C_{17-24}	input capacitance		-	-	5	pF
Pin 19 V_{19-24}	DC level	record mode playback mode	- -	1.82 1.7	- -	V V
$V_{19-24(p-p)}$	AC level (peak-to-peak value)	sinusoidal	-	800	-	mV
		block	-	621	-	mV
G_{19-24}	signal gain	playback mode	-	6	-	dB
R_{19-24}	output resistance		-	V_t/I_e	-	Ω
Pin 21 $V_{21-24(p-p)}$	input signal (peak-to-peak)	playback mode	-	300	600	mV
V_{21-24}	DC level		-	3.25	-	V
V_{21-24}	record mode active voltage level		-	-	1.5	V
V_{21-24}	playback mode active voltage level		2.2	-	-	V
R_{21-24}	input resistance		8	12	16	kΩ
C_{21-24}	input capacitance		-	-	5	pF
Pin 25 $V_{25-24(p-p)}$	input signal (peak-to-peak value)		-	-	645	mV
V_{25-24}	DC level		-	V_{7-24}	-	V
R_{25-24}	input resistance		100	-	-	kΩ
C_{25-24}	input capacitance		-	-	5	pF

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 27 R_{27-24}	output resistance		-	-	10	Ω
RECORD MODE $V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V_{22} = 600 mV (p-p)	-	1175	-	mV
$V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V_{22} = 300 mV (p-p)	-	1110	-	mV
$V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V_{22} = 30 mV(p-p)	-	272	-	mV
V_{27-24}	DC level		-	1.65	-	V
PLAYBACK MODE $V_{27-24(p-p)}$	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal	-	1175	-	mV
V_{27-24}	DC level		-	3	-	V
G_{27-6}	signal gain		-	12	-	dB
α_{27}	2.2 MHz suppression		23	-	-	dB
α_{27}	6.6 MHz suppression		30	-	-	dB
α_{27}	8.8 MHz suppression		10	-	-	dB
Pin 28 $V_{28-24(p-p)}$	input signal (peak-to-peak)		-	-	1000	mV
V_{28-24}	DC level		-	V_{27-24}	-	V
R_{28-24}	input resistance		100	-	-	kΩ
C_{28-24}	input capacitance		-	-	5	pF

SECAM-L chrominance processor for VHS video recorders

TDA4725T

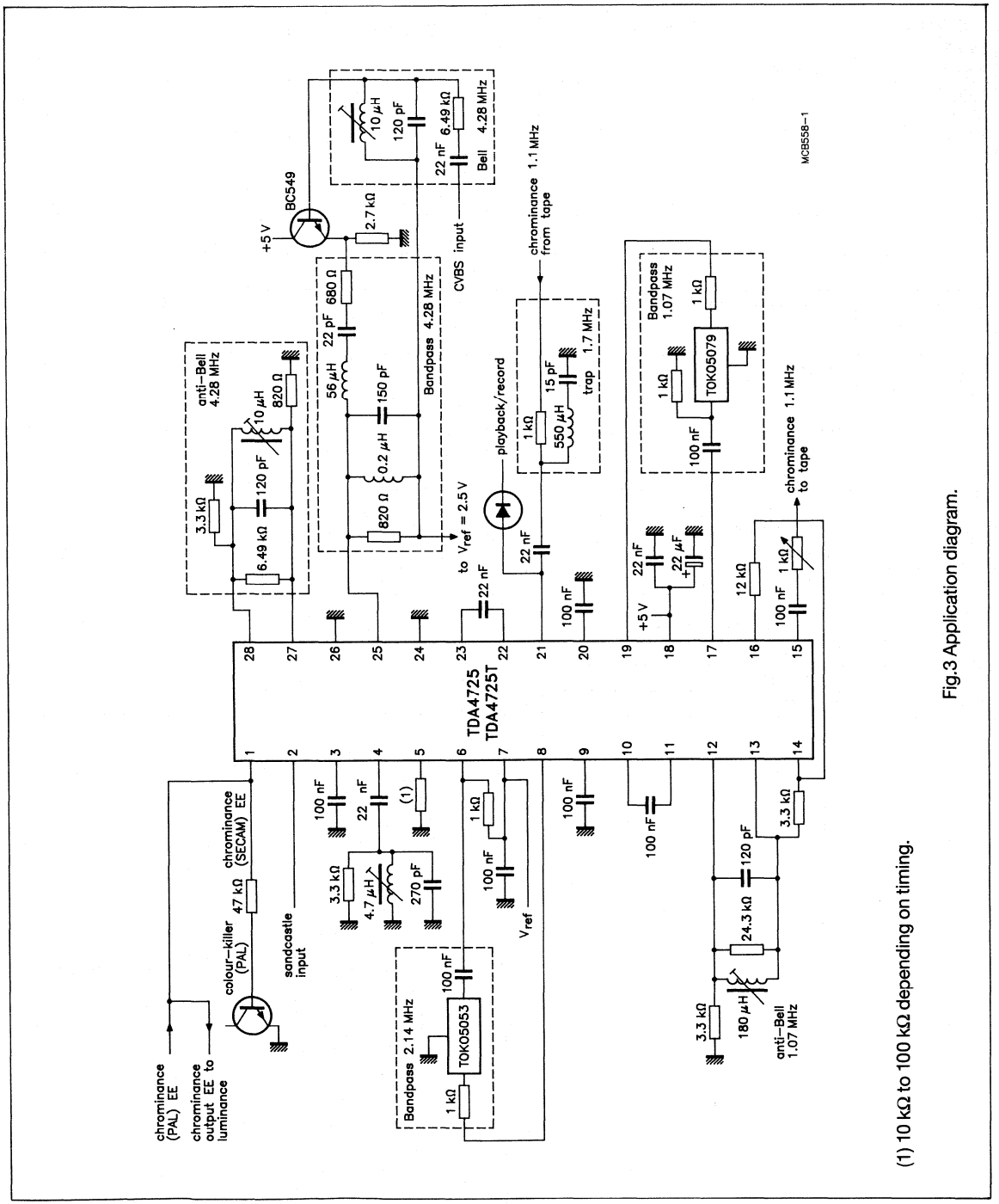


Fig.3 Application diagram.

(1) 10 kΩ to 100 kΩ depending on timing.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	February 1992

TDA4800

Vertical deflection circuit for monitor applications

FEATURES

- Fully integrated, few external components
- RC oscillator with wide sync range of 1:3 (e.g. 50 Hz to 150 Hz)
- Synchronization by positive or negative going sync pulse
- Blanking pulse duration is determined externally
- Dual frequency criterion for automatic amplitude switch-over (e.g. 50 Hz to 60 Hz)
- Guard circuit for screen protection
- Sawtooth generator with buffer stage supplied by external voltage
- Preamplifier
- Power output stage with thermal and SOAR protection
- Flyback generator
- Internal voltage stabilizer

GENERAL DESCRIPTION

The TDA4800 is a monolithic integrated circuit for vertical deflection primarily in monitors (and TV receivers). The complete circuit consists of 11 main functional blocks as shown in Fig.1.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 10)		10	–	45	V
V_P	supply voltage range (pin 6)		10	–	30	V
I_P	supply current (pins 6 and 10)	note 1	–	215	–	mA
I_7	output current (peak-to-peak value)		–	–	2.6	A
f_{sync}	picture frequency	note 1, 3	–	–	135	Hz
V_3	positive sync input pulse		1.0	–	6.0	V
V_3	negative sync input pulse		–0.5	–	–0.7	V
T_{amb}	operating ambient temperature range	note 2	–20	–	+ 70	°C

Notes to the quick reference data

1. Measured in circuit Fig.4
2. P_{tot} = 3.6 W for $R_{th\ j\text{-}a}$ = 20 K/W
3. f_o = 45 Hz ($f_{sync\ max} = 3f_o$)

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4800	13	DBS	plastic	SOT141

Vertical deflection circuit for monitor applications

TDA4800

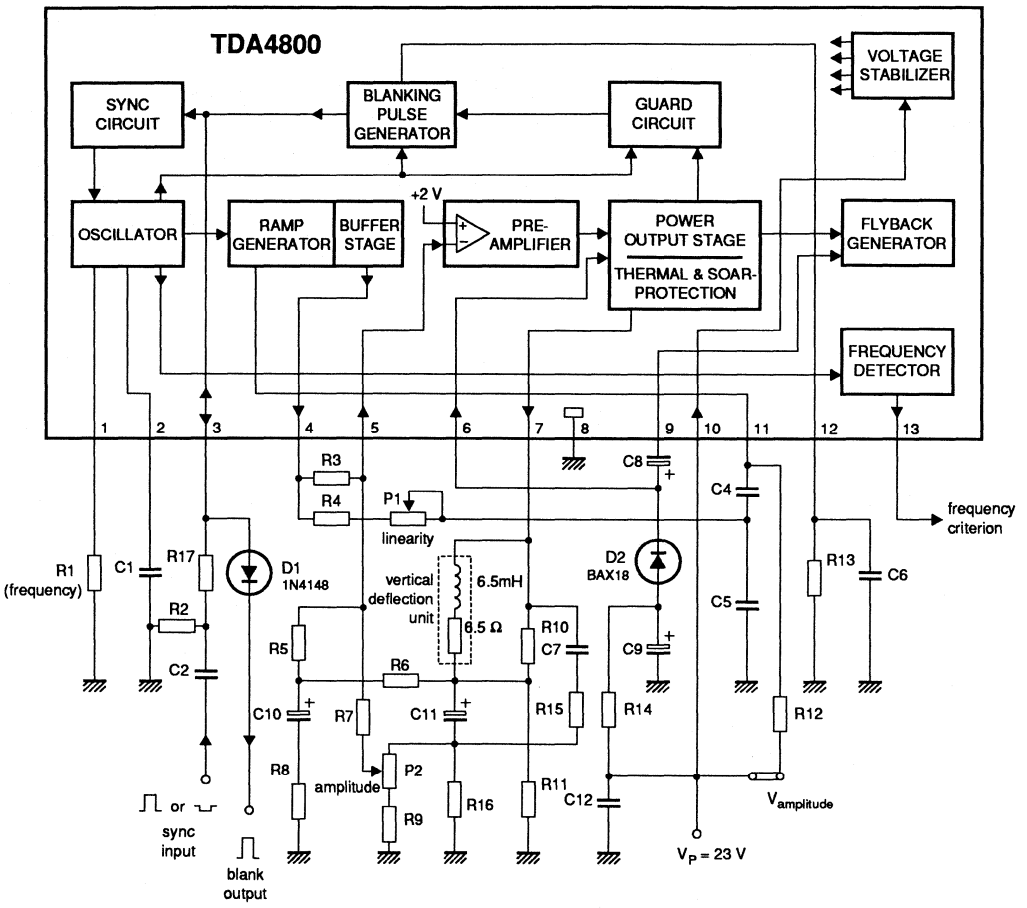


Fig.1 Block diagram.

Vertical deflection circuit for monitor applications

TDA4800

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

1. Oscillator
2. Synchronization circuit
3. Blanking pulse generator
4. Frequency detector and storage
5. Ramp generator
6. Buffer stage
7. Preamplifier
8. Power output stage
9. Flyback generator
10. Guard circuit
11. Voltage stabilizer

1. Oscillator (pins 1, 2)

The oscillator is an RC-oscillator with a threshold value switch, which ensures very good frequency stability.

The upper and lower threshold voltages are defined by an internal voltage divider.

An external capacitor C1 at pin 2 is charged by a constant current source. When the scan voltage of C1 reaches the upper threshold voltage, oscillator flyback starts. Capacitor C1 discharges via an internal resistor and transistor until the lower threshold is reached.

The constant charge current and free-running frequency f_o are adjusted by an external resistor R1 at pin 1:

$$f_o = \frac{1}{K \times R1 \times C1} \quad \text{with } K = 0.68$$

2. Synchronization circuit (pin 3)

A positive- or negative-going pulse fed to pin 3 synchronizes the oscillator by lowering the upper threshold voltage. The synchronizing range is f_o to 3 f_o. For example:

$f_o = 50$ Hz $\longrightarrow$ $f_{sync\ max} = 150$ Hz.

3. Blanking pulse generator (pin 3)

Also at pin 3 a blanking pulse is available. Diode D1 separates the synchronization pulse from the blanking pulse. During scanning, the external capacitor C6 at pin 12 is charged to an internal stabilized voltage V. The blanking pulse starts with the beginning of oscillator flyback; then capacitor C6 discharges via the external resistor R13 at pin 12. The blanking pulse stops when the capacitor voltage is V/2.

The blanking pulse duration is determined by the values of external components R13 and C6 at pin 12:

$$t_{bl} = R13 \times C6 \times Ln2$$

4. Frequency detector with storage (pin 13)

At the end of the scanning period a frequency detector detects the oscillator frequency (see *Note*). When this frequency is above the threshold a flip-flop is set to store this information. The output is an open collector output.

Note:

Frequency detector change-over at pin 13 from low (= low frequency) to high (= high frequency) is determined by f_o:

$$f_{threshold} = 1.23 \times f_o$$

5. Ramp generator (pin 11)

The ramp generator consists of two external series capacitors C4 and C5, external charge resistor R12 (connected to pin 11), and an internal differential amplifier which is synchronously-switched by the oscillator.

External capacitors C4 and C5 at pin 11 are charged by the charging current via the external charge resistor R12 until oscillator flyback starts. C4 and C5 are then discharged via pin 11 by an internal resistor and transistor. This generates a positive-going ramp voltage.

6. Buffer stage (pin 4)

The buffer stage consists of two emitter followers. The ramp voltage is fed via the buffer stage and is available at pin 4 with a low ohmic output impedance. With R4 and P1 it generates a ramp function, which, together with the feedback network of the deflection yoke, gives a high degree of linearity at the picture tube. The linearity can be adjusted by P1.

7. Preamplifier (pin 5)

The preamplifier is a differential amplifier. The non-inverting input is fixed at about 2 V by an internal voltage divider. The inverting input at pin 5 is connected to the ramp voltage via R3 and feedback network P2, R5 - R11, R15, R16, C7, C10 and C11.

8. Power output stage (pin 7)

The power output stage is an amplifier with a quasi-complementary class-B output. The output is connected to pin 7.

The power stage includes SOAR and thermal protection.

9. Flyback generator (pin 9)

The flyback generator has an external capacitor C8 at pin 9. During scanning, the internal circuit switches pin 9 almost to ground; thereby C8 is charged by the supply voltage via external components R14 and D2.

During the flyback time pin 9 is switched almost to the supply voltage, so that the supply voltage for the power output stage (pin 6) is nearly doubled. This high flyback voltage ensures a very short flyback time.

10. Guard circuit (pin 3)

When the vertical deflection current is absent (e.g. short-circuit, or open-circuit of the yoke) the guard circuit changes the blanking pulse at pin 3 into a DC signal which blanks the beam current to protect the screen.

Also an oscillator defect (C1 short-circuited or R1 disconnected from pin 1) switches on the guard circuit.

11. Voltage stabilizer

The voltage stabilizer circuit provides a stable operating voltage of about 7.5 V for several circuits of the TDA4800.

Vertical deflection circuit for monitor applications

TDA4800

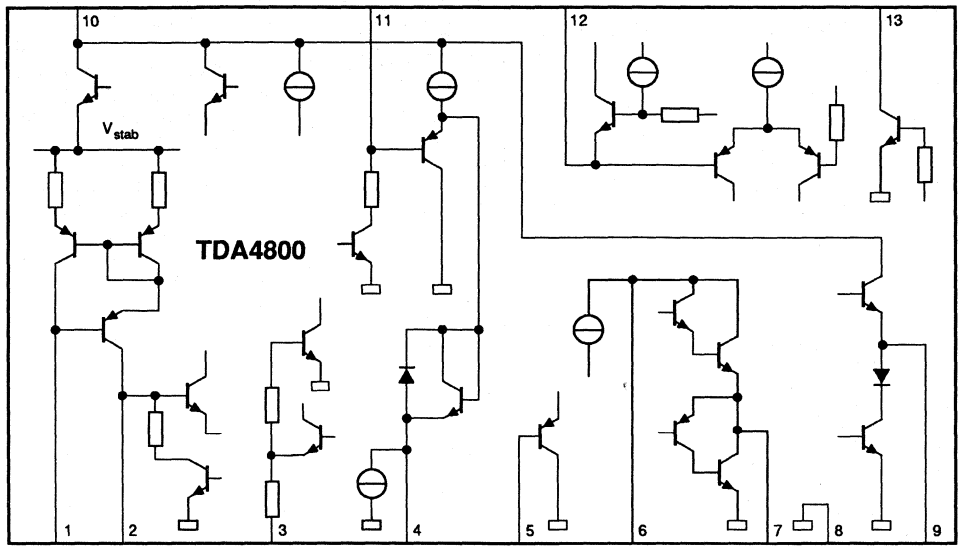


Fig.2 Internal circuits.

PINNING

SYMBOL	PIN	DESCRIPTION
OSC_R	1	oscillator resistor
OSC_C	2	oscillator capacitor
SYB_O	3	sync. input, blanking pulse output
S_{OUT}	4	sawtooth output
PRE_I	5	preamplifier input
P_{SUP}	6	power supply
OUTP	7	deflection output
GND	8	ground
C_{FLY}	9	pin for the flyback generator capacitor
V_P	10	supply voltage
S_{GEN}	11	sawtooth generator
BP_{DU}	12	blanking pulse duration
FRQ_C	13	frequency criterion

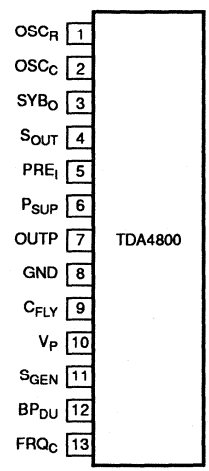


Fig.3 Pin configuration.

Vertical deflection circuit for monitor applications

TDA4800

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_2	voltages		0	6	V
V_{11}			0	24	V
V_{12}			0	6	V
V_{13}			0	50	V
V_{10}	supply voltages (V_P)		0	50	V
V_9			0	50	V
V_7			0	60	V
V_6			0	60	V
V_5			0	6	V
V_4			0	24	V
V_3			−0.7	6	V
I_1	currents	see note 1	0	−1	mA
I_3			+ 3	−10	mA
I_4			0	−5	mA
I_6, I_7, I_8					
I_9			−1.5	+ 1.5	A
I_{11}			−0.1	+ 30	mA
T_{stg}	storage temperature range		−25	+ 150	°C
T_{amb}	operating ambient temperature range	see note 2	−20	+ 70	°C
$T_{j\ max}$	maximum junction temperature	see note 3	–	150	°C
P_{tot}	total power dissipation	see note 2	–	–	W
V_{ESD}	ESD sensitivity	see note 4	−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient	20 K/W
$R_{th\ j\text{-}mb}$	from junction to mounting base	5 K/W

Notes to the limiting values

1. I_6, I_7 and I_8 are limited by SOAR protection circuit that ensures that a short-circuit between the output pin 7 and supply voltage or ground does not destroy the output stage. A short-circuit may be soldered into the printed-circuit board or may sometimes (non-periodically) occur in the applied circuit.
2. The maximum value for the operating ambient temperature range and the power dissipation depends on the heatsink.
3. Internally limited by thermal protection: switching temperature point at $T_j = 150\ °C \pm 8\ °C$.
4. Human body model: 1.5 kΩ, 100 pF, 5 pulses.

CHARACTERISTICS

All voltages are measured to V_{GND} (pin 8); T_{amb} = 25 °C; V_P = 23 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 10)		10	–	45	V
V_P	supply voltage range (pin 6)		10	–	30	V
I_{10}	supply current	V_{10} = 25 V; V_5 = 3 V without load	–	12	–	mA
I_6	supply current	V_6 = 25 V; V_5 = 1 V without load	–	20	–	mA
I_6	supply current	V_6 = 25 V; V_5 = 3 V without load	–	5	–	mA
V_7	minimum output voltage	I_7 = 1 A	–	1.4	1.65	V
V_7	maximum output voltage	I_7 = –1 A	V_6 –2.3	V_6 –2.0	–	V
V_9	output voltage during flyback	I_9 = –1 A	–	V_{10} –2.2	–	V
I_7	output current		–	–	± 1.3	A
I_9	output current		–	–	± 1.3	A
I_5	preamplifier input current		–	–0.1	–	µA
V_1	stabilized voltage		6.1	6.8	7.3	V
V_3	blanking pulse output voltage		–	5.7	–	V
R_3	blanking pulse output resistance		–	300	–	Ω
I_3	blanking pulse output current		0	–	–3	mA
t_{bl}	blanking pulse duration	R = 100 kΩ; C = 10 nF (pin 12)	640	680	730	µs
V_{11}	output voltage ramp generator		0.3	–	20	V
I_{11}	output current ramp generator		–2	–	15 x 10^3	µA
V_{13}	output voltage frequency detector	lower frequency I_{13} = 1mA	–	–	1.0	V
I_{13}	leakage current frequency detector	higher frequency V_{13} = 50 V	–	–	1.0	µA
V_4	output voltage buffer stage		0	–	20	V
I_4	output current buffer stage		–	–	–4.0	mA
V_3	synchronizing input voltage	positive sync	1.0	–	6.0	V
V_3	synchronizing input voltage	negative sync	–0.5	–	–0.7	V
	tolerance of free running oscillator	without sync	–3.0	–	+ 3.0	%
$\Delta f/f / \Delta T_C$	oscillator temperature dependency	T_{case} = 20 °C to 100 °C	–	10^{-4}	–	K^{-1}
$\Delta f/f / \Delta V_P$	oscillator voltage dependency	V_P = 10 V to 30 V	–	4 x 10^{-4}	–	K^{-1}
f_0 / f_{sync}	synchronizing ratio		1:2.9	1:3	–	–

Vertical deflection circuit for monitor applications

TDA4800

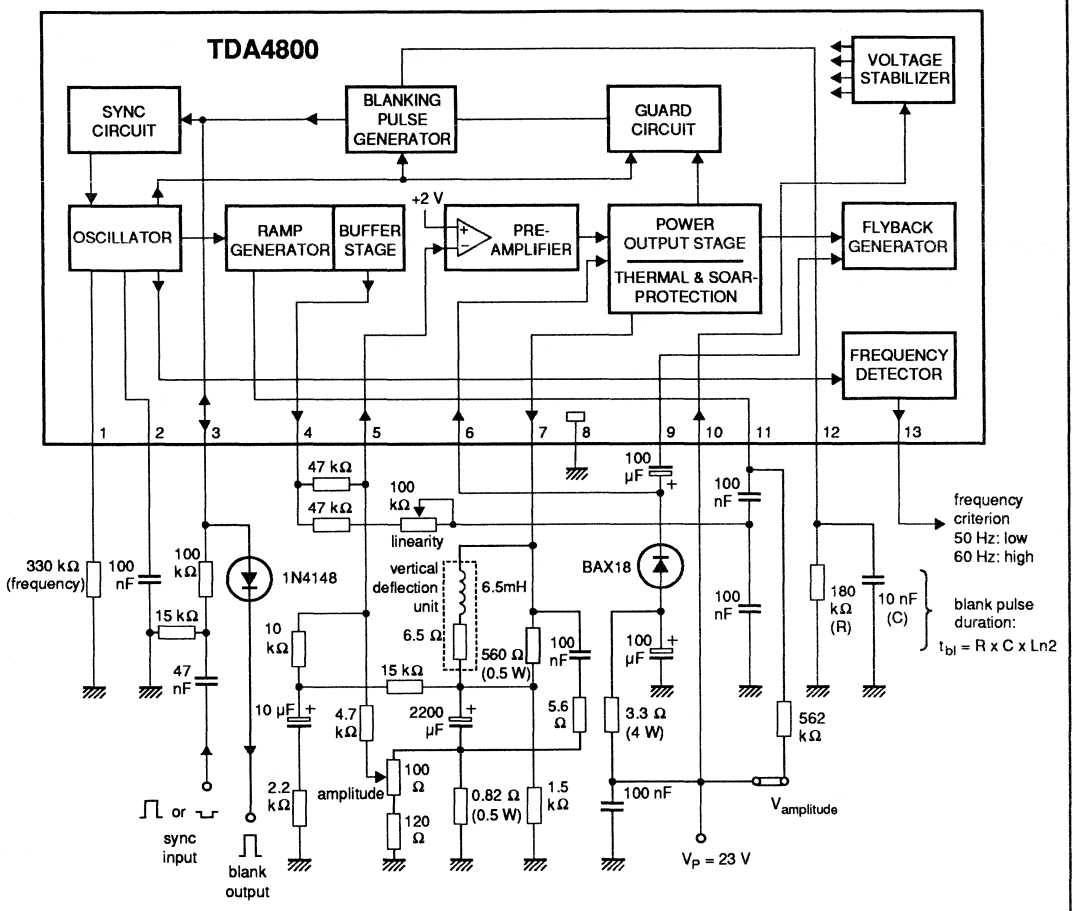


Fig.4 Test and application circuit.

TDA4800 IN THE TEST AND APPLICATION CIRCUIT (see Fig.4)

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
V_P	supply voltage		23	V
I_P	supply current		215	mA
V_7	DC output voltage		11.8	V
V_{7M}	peak output voltage		45	V
I_7	output current		0.8	A
$I_{Y(p-p)}$	vertical deflection current (peak to peak)		1.5	A
t_{fb}	flyback time		0.3	ms
t_{bl}	blanking pulse duration		1.25	ms
P_{tot}	total power dissipation		3.3	W
f_o	free running oscillator frequency	without sync	45	Hz

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1991

TDA4810

Sync processor and horizontal driver for monitors

FEATURES

- Sync separator with AC-coupled and DC-coupled inputs for signals of nearly all existing sync sources (e.g. TTL / video)
- Amplitude dependent sync slicing
- Automatic sync polarity correction
- Wide horizontal frequency range
- Artificial sync generator for sync pulse-width-independent operation
- Short vertical integration time
- Vertical/composite sync output signal selectable
- Super sandcastle pulse generator
- Two phase loops (PLL1, PLL2) to achieve excellent sync-locking and horizontal picture shift
- Horizontal output stage optimized for bipolar and Darlington deflection transistors
- Protection circuits against too low supply voltage and excessive EHT (X-ray protection)
- Voltage stabilizer with excellent ripple rejection
- Number of external components depend on the requirements and realized features

GENERAL DESCRIPTION

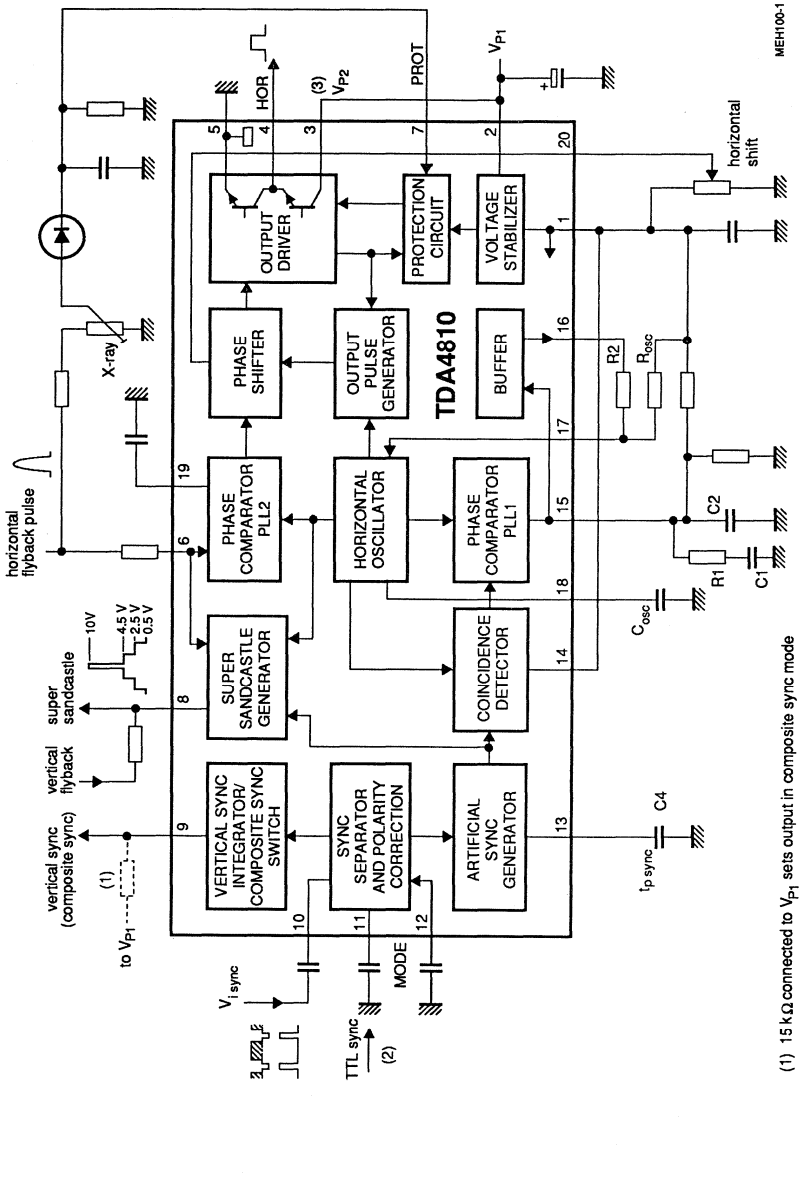
Monolithic integrated circuit for sync processing in monochrome and colour monitors, applicable for all commonly used graphic cards (e.g. EGA, Super VGA and IBM8514/A). The flexible sync separator handles different sync signals of either polarity over a wide amplitude range.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (pin 2)	8.5	12	16	V
V_{P2}	supply voltage (pin 3)	8.5	12	16	V
V_{stab}	stabilized output voltage (pin 1)	6.18	6.3	6.5	V
I_{P1}	supply current (pin 2)	-	35	-	mA
$V_{i\ sync}$	mode 1: AC-coupled negative-going input signal on pin 10 (peak-to-peak value)	-	1	1.5	V
	mode 2: AC-coupled positive- or negative-going sync pulse on pin 10 (peak-to-peak value)	2	-	5.5	V
	mode 3: DC-coupled positive- or negative-going sync pulse on pin 11 (peak value)	3.2	-	5.5	V
V_9	vertical/composite sync output voltage HIGH ($I_9 = -1$ mA)	-	10	-	V
I_4	maximum horizontal output current for Darlington deflection transistor ($-I_4 = I_3$)	-	-	–900	mA
	maximum horizontal output sink current for bipolar deflection transistor	-	-	100	mA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4810	20	DIL	plastic	SOT146



(1) 15 kΩ connected to V_{P1} sets output in composite sync mode
(2) connection for other modes as described in Fig.3
(3) connection for Darlington deflection transistor as described in Fig.4

Fig.1 Block diagram for full facility (mode 2); horizontal output signal suitable for bipolar deflection transistor .

Sync processor and horizontal driver for monitors

TDA4810

PINNING

SYMBOL	PIN	DESCRIPTION
V_{stab}	1	stabilizer voltage output (6.3 V)
V_{P1}	2	supply voltage
V_{P2}	3	supply voltage for horizontal output
HOR	4	horizontal pulse output
GND	5	ground (0 V)
FLB	6	horizontal flyback pulse input
PROT	7	protection input (for over-current /EHT protection)
SSC	8	super sandcastle generator output
VS	9	vertical sync / composite sync output
$V_{i\ sync}$	10	sync input signal , AC-coupled
TTL	11	alternative sync input DC-coupled, e.g. TTL
APC	12	automatic sync polarity correction
C_{SY}	13	capacitor of artificial sync generator
COIN	14	coincidence detector
PLL1	15	time constant of PLL1
BUF	16	buffered PLL1 output
R_{osc}	17	reference current of horizontal oscillator
C_{osc}	18	capacitor of horizontal oscillator
PLL2	19	time constant of PLL2
SHIFT	20	horizontal phase shift

PIN CONFIGURATION

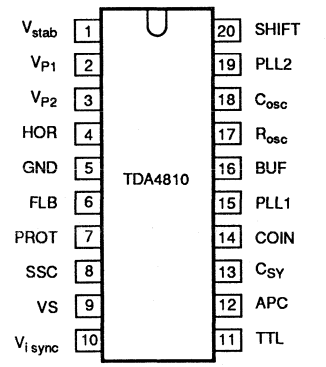


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Sync separator and polarity correction (Fig.1)

The circuit handles sync signals of nearly all existing standards . Features of the sync separator:

- inputs for DC-coupled signal or AC-coupled signal
- automatic sync polarity correction
- amplitude dependent sync slicer

The type of coupling and the necessary external components are shown in Figure 3.

Mode 1: A negative going sync signal (V_i sync < 1.5 V (p-p)) is fed via a coupling capacitor to pin 10. The sync separator clamps the bottom of the input signal on 1.28 V. Sync is sliced 120 mV above. Since the automatic polarity correction does not work below 2 V (p-p), pins 11 and 12 are connected to ground.

Mode 2: Positive or negative going sync pulses >2 V(p-p) (e.g. TTL) are AC-coupled to pin 10. The upper level is peak-rectified referred to the external capacitor on pin 11 at $V_{11} = 1.28V + 0.5 \times V_{i\ sync}$. This means, the slicing level tracks with typical 50% of $V_{i\ sync}$. The polarity switch corrects the polarity automatically by means of the external capacitor on pin 12. If only sync pulses of one polarity are applied to the input, the capacitor on pin 12 is not necessary. Then pin 12 can be connected to ground or V_{stab} (pin 1) to force the polarity.

Mode 3: Positive or negative going sync signals >3.2 V(p) (e.g. TTL) are DC-coupled to pin 11. They are sliced at 1.4 V according to TTL standard. If only sync pulses of one polarity are applied to the input, the capacitor on pin 12 is not necessary. Pin 12 can be connected to ground or V_{stab} (pin 1) to select the polarity from external.

Vertical/composite sync output

If a video signal or composite sync signal is applied to pin 10 the vertical sync separator generates a vertical sync trigger pulse. The separated vertical and composite sync pulses are fed to the vertical or composite sync switch and to the output stage (pin 9).

The external load current at pin 9 determines which of the two signals is fed out of pin 9. If there is an additional current from V_{P1} via the 15 kΩ resistor, composite sync signal is achieved (without additional current the vertical sync pulse is output.

Artificial sync generator

The sync signal from the sync separator is directly fed to the phase comparator (with unchanged leading and trailing edges), if the internal monoflop at pin 13 is connected to ground. This operation is possible.

Sync signals with leading edge as only sync reference (because the trailing edge could occur at an undefined time) is achieved by connecting a time-determining capacitor from pin 13 to ground. The internal monoflop generates an artificial sync signal triggered by the leading edge of the incoming sync signal.

Furthermore, the artificial sync generator reduces disturbances of the PLL1 during vertical sync.

Coincidence detector

Coincidence is detected between the input sync pulse and the gating pulse of the oscillator. The centring current for PLL1 is switched off at coincidence (V_{14} > 3 V).

Phase comparator PLL1

This stage compares the PLL1 (timing reference of the oscillator) with the centre of the horizontal input sync pulse (respectively with the artificial sync pulse, Fig.6). The time difference is converted into a proportional current on pin 15 to tune the oscillator via the buffer amplifier. This ensures that the phase relationship in the TDA4810 is stable independent of changes in frequency.

Horizontal oscillator (Fig.6)

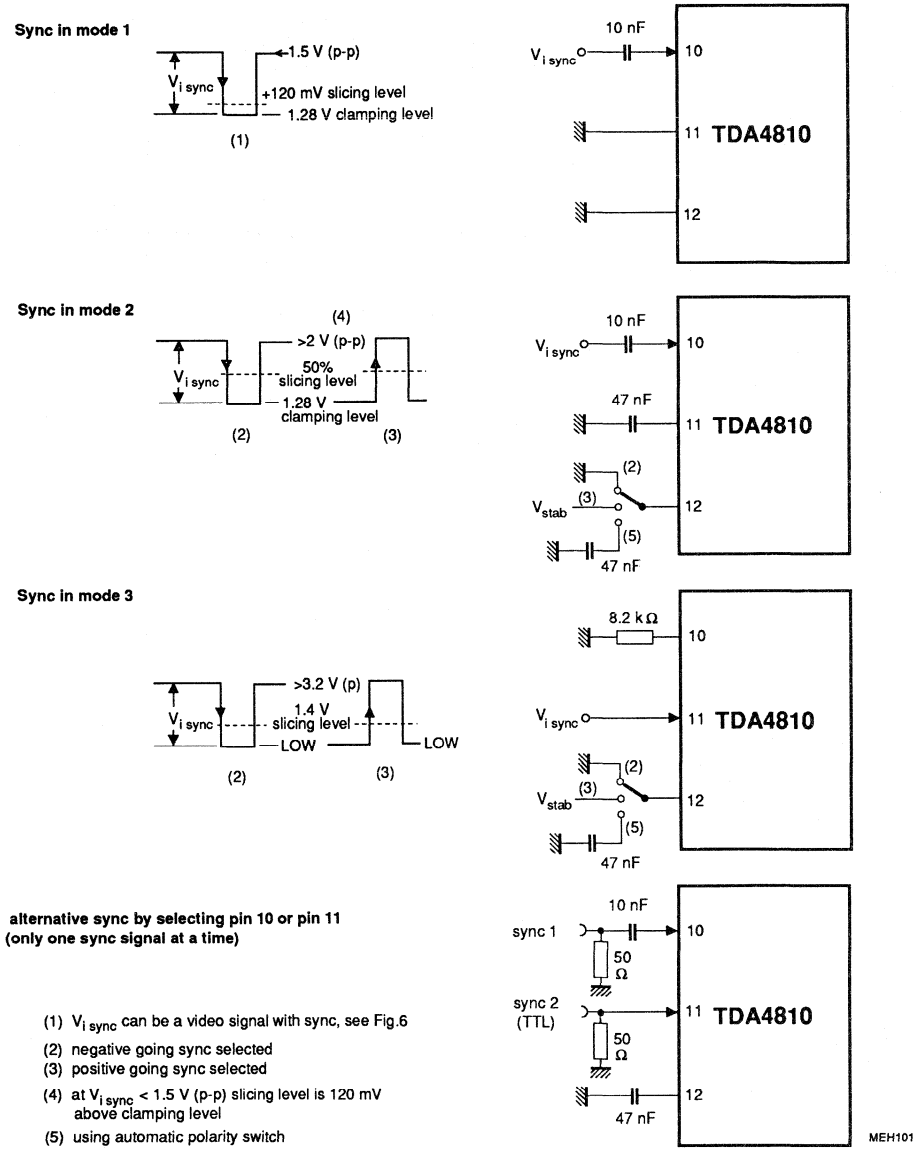
The frequency of the free-running oscillator is determined by the capacitor on pin 18 and the reference current via pin 17. The reference current is fed from the voltage stabilizer via R_{osc}, and also from the PLL1 buffer amplifier via R2 to define the catching range. In order to cover a wide frequency range (one octave) R_{osc} can be modified as described in notes to the characteristics.

Phase comparator PLL 2 (Fig.6)

This stage compares the centre of the positive-going flyback pulse (on pin 6, internal threshold voltage 3 V) with the PLL2 timing reference generated by the horizontal oscillator. A time difference is converted into a proportional current on pin 19. The line flyback pulse and the oscillator pulse are compared to eliminate the delay time in the horizontal deflection stage.

Horizontal phase shifter

An external stabilized voltage on pin 20 sets the phase relationship between sync pulse and horizontal flyback pulse. The horizontal output pulse can be adjusted over a wide range (±20% referred to the horizontal period time) by means of the external potentiometer (Fig.1).



(1) $V_{i\,sync}$ can be a video signal with sync, see Fig.6
(2) negative going sync selected
(3) positive going sync selected
(4) at $V_{i\,sync}$ < 1.5 V (p-p) slicing level is 120 mV above clamping level
(5) using automatic polarity switch

Fig.3 Sync modes of TDA4810.

Output pulse generator and horizontal output (Fig.4)

The output pulse generator generates a pulse of constant width within the control range of the PLL 2. The horizontal output driver generates two different pulse widths (Fig.6) depending on the voltage between pins 2 and 3

- 45% relative pulse width for standard bipolar deflection transistor ($V_3 = V_2$)
- 30% relative pulse width for Darlington deflection transistor. ($V_3 < V_2$)

NON-INVERTED POLARITY.

The push-pull output stage of the horizontal driver is connected between the supply voltage (pin 3) and ground (pin 5). The output signal (pin 4) is usually fed to a transformer-coupled driver. The upper transistor (collector on pin 3) is designed for a maximum current of 900 mA, the lower one for 100 mA.

INVERTED POLARITY

The horizontal output signal is now available on pin 3 by means of the 220 Ω pull-up resistor. Pin 4 is connected to ground. The open-collector output can directly drive a Darlington deflection transistor.

Voltage stabilizer

A stabilized voltage of 6.3 V, based on a bandgap reference, is provided on pin 1. This avoids phase jitter in deflection, caused by an insufficient filtered supply voltage. The excellent performance of the voltage stabilizer allows the TDA4810 to be driven directly by a switch mode power supply.

Super sandcastle pulse generator

Three levels are generated (Fig.6):

a) The 2.5 V level is generated by a external vertical blanking current which is fed into pin 8.

b) The 4.5 V level is derived from the line flyback pulse referred to a threshold of 0.3 V for horizontal blanking. When horizontal flyback pulses are absent, the 4.5 V level is inserted by the protection circuit to blank the screen continuously .

c) The 10 V level starts with the trailing edge of the sync pulse (respectively with artificial sync) and ends with a pulse, derived from the horizontal oscillator saw-tooth signal.

Protection circuit

The protection circuit is activated and the horizontal output is switched off when the voltage on pin 7 exceeds V_{stab} = 6.3 V or decreases below –0.2 V . One of these both thresholds can be used for X-ray protection or for over-current protection (Fig.1).

There is an additional protection against too low supply voltage (V_{P1}< 5.8 V).

Operations:

- output pin 4 goes to ground when $V_2 = V_3$ (e.g. in a bipolar deflection transistor application)
- output pin 3 goes to ground when $V_3 < V_2$ (e.g. in a Darlington deflection transistor application)
- the error indication is latched; therefore all the supply voltages must be switched off and on again, to enable the circuit.

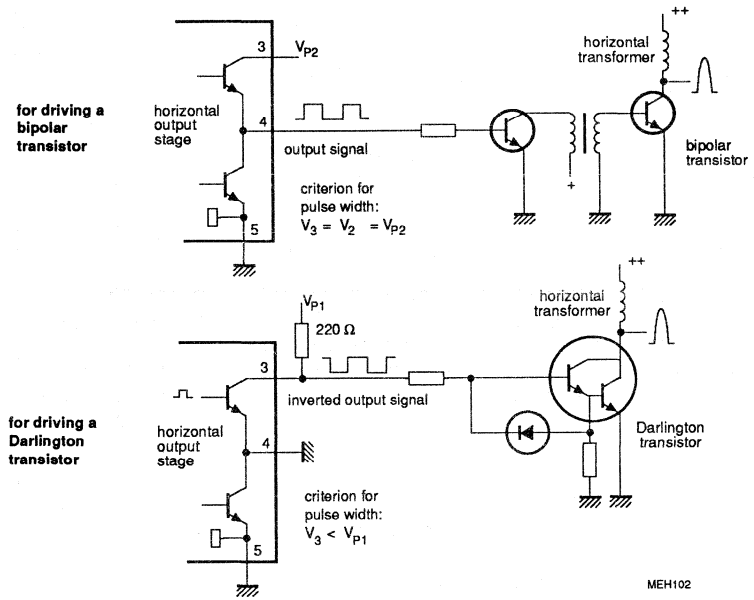


Fig.4 Horizontal output stage.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 2)	0	16	V
V_{P2}	supply voltage (pin 3)	0	16	V
$V_{10, 11}$	input voltage	–0.5	8	V
I_3	supply current for horizontal output	-	1.0	A
I_4	horizontal output current	-	+200	mA
		-	–1.0	A
I_6	flyback input current	-	±10	mA
I_9	vertical sync output current	-	–10	mA
I_{16}	buffer output current	-	±10	mA
P_{tot}	total power dissipation	-	1.2	W
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±300	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C and measurements taken in Fig.5 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage range (pin 2)		8.5	12	16	V
V_{P2}	supply voltage range (pin 3)		8.5	12	16	V
I_{P1}	supply current		-	35	-	mA
V_{stab}	stabilized voltage (pin 1)		6.18	6.3	6.5	V
RR	ripple rejection for V_{stab}	f_R = 1 kHz (sinewave) on supply voltage	60	70	-	dB
Sync input signal modes 1 and 2, AC-coupled to pin 10						
$V_{i\ sync}$	negative-going sync input signal (peak-to-peak value, pin 10)	mode 1; Fig.3; R_S = 50 to 500 Ω	-	1	1.5	V
	sync amplitude in video signal		180	300	400	mV
	clamping voltage		-	1.28	-	V
	slicing level above clamping level	$t_{p\ sync}/t_H$ = 0.1	-	120	-	mV
	voltage for automatic polarity correction inactive	mode 1	-	-	1.5	V
	positive or negative-going sync input signal (peak-to-peak value, pin 10)	mode 2; Fig.3; R_S = 50 to 500 Ω	2	-	5.5	V
	voltage for automatic polarity correction active	mode 2	2	-	-	V
	slicing level	mode 2	25	50	75	%
I_{10p}	input current	during video signal	1	2	3.5	μA
R_{10}	input resistance	V_{10} < 1.28 V	-	50	-	Ω
		V_{10} > 1.28 V	-	high-ohmic	-	Ω
V_{11}	charging current (peak value)	mode 2	-	–6	-	mA
	discharging current	V_{11} > 1.4 V	-	10	-	μA
V_{12}	threshold voltage for automatic polarity correction	mode 2	2.6	3.0	3.4	V
	voltage to select positive-going sync		3.5	V_{stab}	-	V
	voltage to select negative-going sync		0	-	2.5	V
I_{12}	charging current at positive-going sync	mode 2	-	–50	-	μA
	discharging current at negative-going sync		-	50	-	μA
Sync input signal mode 3 DC-coupled to pin 11 (8.2 kΩ from pin 10 to ground)						
V_{11}	positive or negative-going sync input signal (peak value, pin 11)	mode 3; Fig.3	3.2	-	5.5	V
	slicing level of sync pulses		1.25	1.4	1.55	V
	voltage for automatic polarity switch active		3.2	-	-	V
V_{12}	input voltage to select polarity correction	positive-going sync	3.5	V_{stab}	-	V
		negative-going sync	0	-	2.5	V
$t_{p\ sync}/t_H$	duty cycle for automatic correction in polarity		-	-	25	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical/composite sync output						
$V_{9\,H}$	sync output voltage HIGH	$I_9 = -1$ mA	9.3	10	11	V
$V_{9\,L}$	sync output voltage LOW	$I_9 = 0.3$ mA	-	0.7	1.1	V
R_9	resistor from V_{P1} to pin 9 to achieve composite sync mode	Fig.1	-	15	-	kΩ
t_d	delay time between leading edge of vertical sync and vertical trigger pulse	pin 9	7.5	15	20	µs
Artificial sync generator						
V_{13}	threshold voltage	lower threshold; Fig.6	-	1.6	-	V
		upper threshold	-	4.8	-	V
	input voltage for generator off	direct sync	ground-connected			V
I_{13}	output current	generator active	-	$\pm I_{17}$	-	µA
$t_{p\,sync}$	internal sync pulse width	C4 = 120 pF; note 5 f_{osc} = 64 kHz	-	1.5	-	µs
Coincidence detector		with 47 nF from pin 14 to ground				
V_{14}	capacitor voltage	during coincidence	-	5	-	V
		during catching	-	-	1.5	V
I_{14}	charging current	during sync pulse	-	−150	-	µA
	discharging current	during gating pulse	-	25	-	µA
Phase comparator PLL1						
V_{15}	control voltage	lower limit	-	1.6	-	V
		upper limit	-	4.6	-	V
I_{15}	control current	during sync pulse	-	$\pm 0.8 I_{17}$	-	µA
I_{16}	buffer output current		-	±2	-	mA
R_{16}	buffer output resistance		-	10	-	Ω
Horizontal oscillator						
f_{osc}	free-running frequency	R_{osc} = 12 kΩ; C_{osc} = 1.1 nF; note 1	-	65	-	kHz
$\Delta f / f_o$	frequency deviation with fixed external components		-	-	±3	%
TC	temperature coefficient	$(\Delta f/f_o)/\Delta T$	-	-	±15	10^{-5}/K
$\Delta f/\Delta V_{P1}$	frequency dependent on supply voltage	8.5 V < V_{P1} < 16 V	-	±5	±20	Hz/V
φ_H / t_H	relative holding/catching range	R2 = 100 kΩ; note 2	±4.5	±5	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Phase comparator PLL2 and phase shifter						
V_{19}	control voltage	upper limit	-	4.6	-	V
		lower limit	-	1.6	-	V
I_{19}	control current during flyback	$V_6 > 3.4$ V	-	$\pm 0.8 I_{17}$	-	µA
V_{20}	input voltage range		-	1.6 to 4.6	-	V
$\Delta t_s/t_H$	phase shifting range, Fig.6	leading edge of sync to middle of flyback	-	±20	-	%
$t_{d\ FLB}$	relative delay time between middle of sync pulse and middle of flyback pulse	Fig.6	3.6	4.4	5.3	%
Horizontal flyback input						
V_6	maximum input voltage		internal limited			V
	slicing level for PLL2	Fig.6	-	3	3.4	V
	slicing level for horizontal blanking		-	0.3	0.45	V
Horizontal pulse generator and output for bipolar deflection transistor						
V_4	output voltage LOW	$I_4 = 100$ mA	-	0.8	1.2	V
I_4	output current (sink)	Fig.4	-	-	100	mA
t_p/t_H	relative pulse width	$V_3 = V_2 = V_{P1}$	-	45	-	%
Horizontal pulse generator and output for Darlington deflection transistor						
V_{3-4}	saturation voltage	$I_3 = -I_4 = 900$ mA	-	1.4	2	V
		$I_4 = -100$ mA	-	0.25	0.4	V
I_3	output current (sink)		-	-	900	mA
t_p/t_H	relative pulse width	$V_3 < V_{P1}$	-	30	-	%
Super sandcastle pulse generator (SSC)						
V_8	output voltage during horizontal scan	$I_8 = 0$	-	-	0.5	V
	output voltage during vertical blanking	$I_8 = 2.8$ mA	2.15	2.5	3.0	V
	output voltage during horizontal blanking		4.2	4.5	4.9	V
	output voltage during clamping pulse	note 3	-	11	-	V
I_8	sink current during trailing edge	$V_8 = 1.5$ V	-	2	-	mA
	vertical blanking current	$V_8 > 2.15$ V	2.3	-	-	mA
		$V_8 < 3$ V	-	-	3.3	mA
$t_{p\ SC}$	gating pulse width	Figures 5 and 6; note 6	-	0.8	-	µs

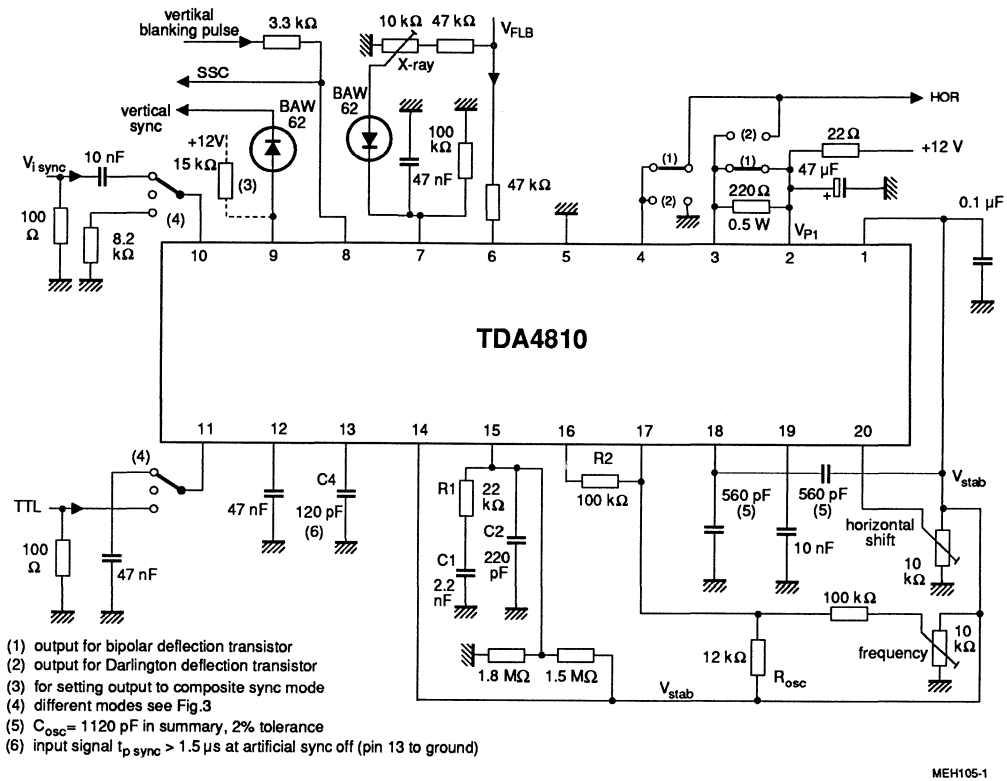
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Protection circuit input						
V_7	threshold input voltage for horizontal output off	note 4 V_7 positive-going V_7 negative-going	 6.18 -	 6.3 –0.2	 6.5 -	 V V
t_d	switching off delay time		-	17	-	µs
V_{P1}	too low supply voltage threshold	horizontal output off horizontal output on	5.4 6.0	5.8 6.4	6.2 6.8	V V

Notes to the characteristics

1. $T_{osc} = 1.16 \times R_{osc} \times C_{osc}$ (approximate value); R_{osc}: 9 kΩ to 18 kΩ
2. $R2 = 48 / p \times R_{osc}$ (approximate value); p ≤10% (catching range)
3. The leading edge of the clamping pulse starts after the trailing edge of the sync pulse respectively with artificial sync.
4. The effect of the protection circuit is to switch off the horizontal output and to latch the error indication. Therefore, the supply voltage must be switched off and on to enable the circuit again
5. Approximate sync pulse width $t_{p\ sync} = C4 \times R_{osc}$
6. Gating pulse width $t_{p\ SC} = 0.1t_H - t_{p\ sync} / 2$ (approximate value at $V_8 = 7$ V)

Sync processor and horizontal driver for monitors

TDA4810



(1) output for bipolar deflection transistor
(2) output for Darlington deflection transistor
(3) for setting output to composite sync mode
(4) different modes see Fig.3
(5) C_{osc}= 1120 pF in summary, 2% tolerance
(6) input signal $t_{p\,sync}$ > 1.5 µs at artificial sync off (pin 13 to ground)

MEH105-1

Fig.5 Test and application circuit for 64 kHz deflection.

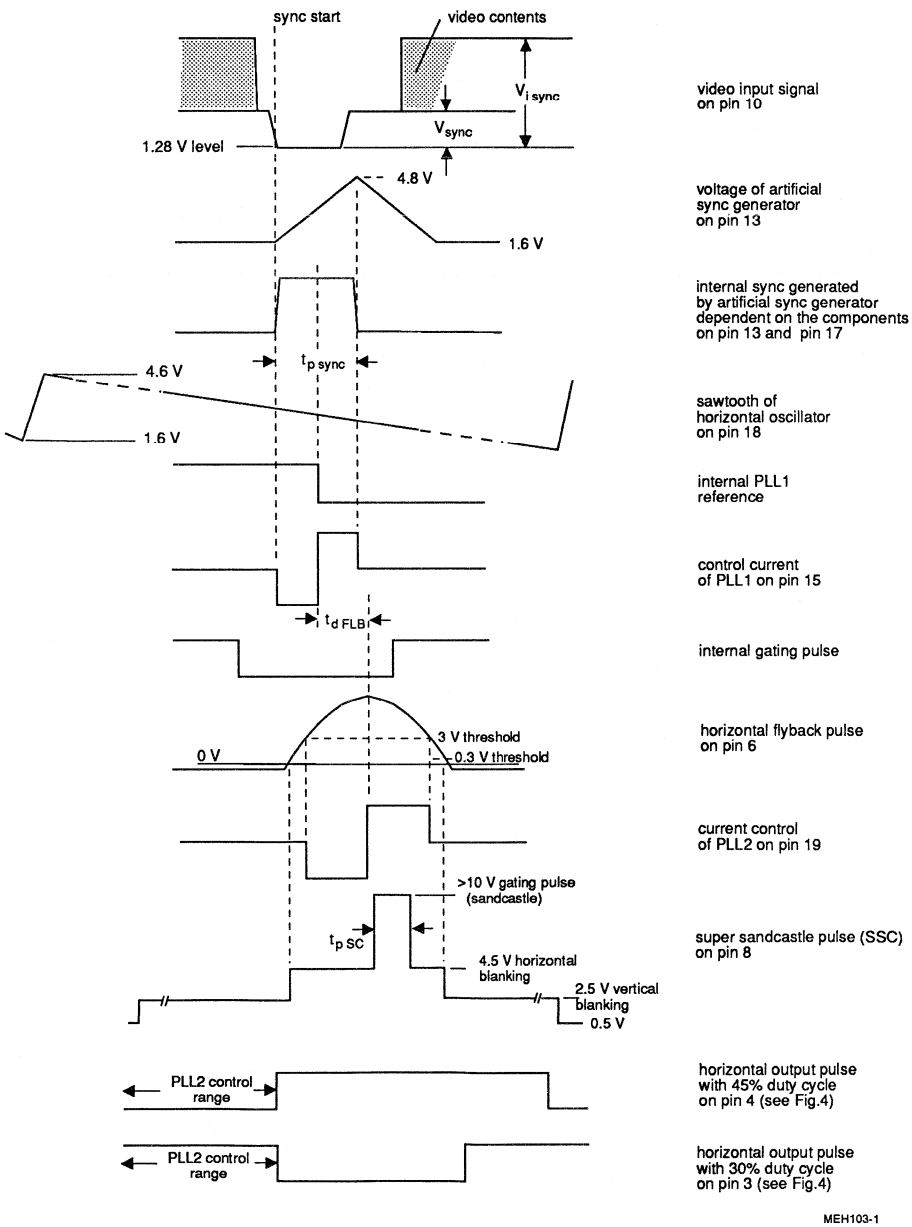


Fig.6 Timing diagram using the artificial sync generator.

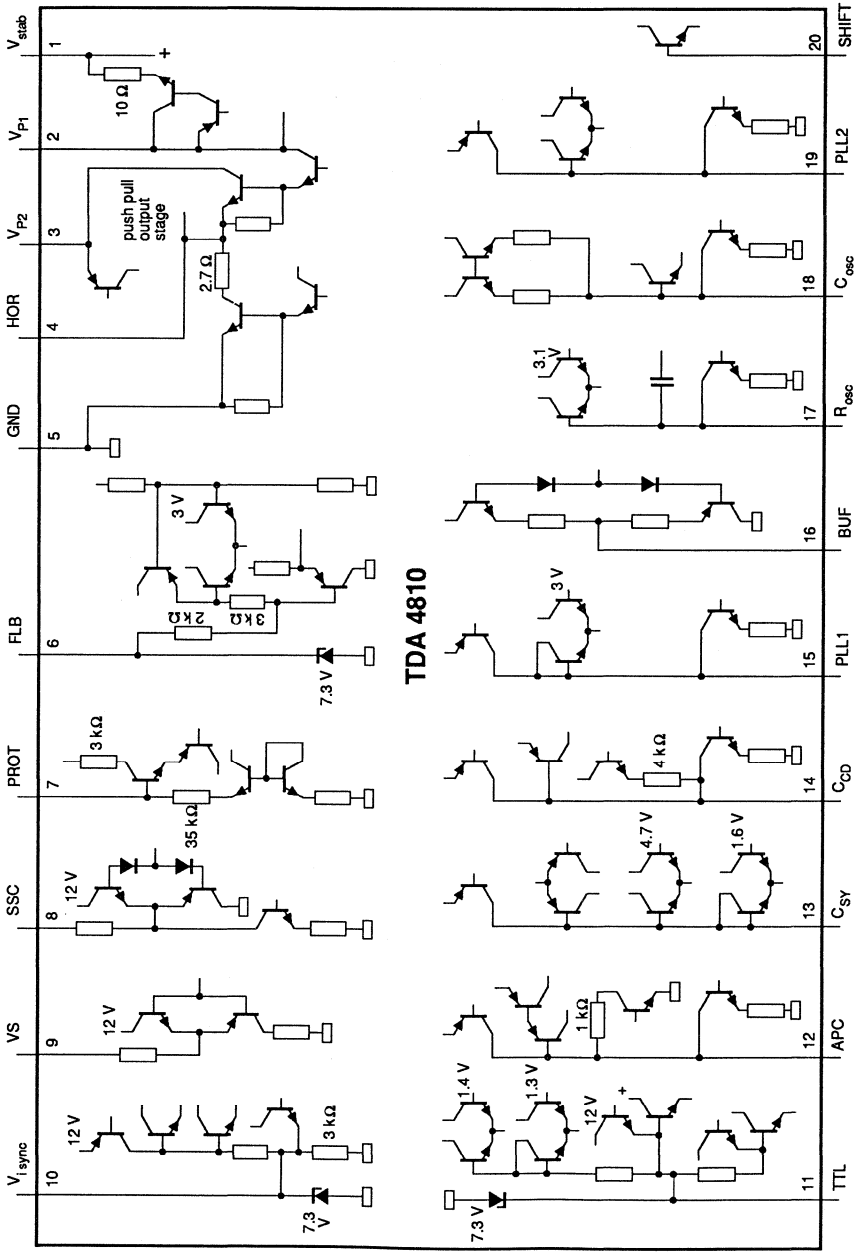


Fig.7 Internal circuit.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	June 1990

TDA4820T
Sync separation circuit for video applications

FEATURES

- Fully integrated, few external components
- Positive video input signal, capacitively coupled
- Operates with non-standard video input signals
- Black level clamping
- Generation of composite sync slicing level at 50% of peak sync voltage
- Vertical sync separator with double slope integrator
- Delay time of the vertical output pulse is determined by an external resistor
- Vertical sync generation with a slicing level at 40% of peak sync voltage
- Output stage for composite sync
- Output stage for vertical sync

GENERAL DESCRIPTION

The TDA4820T is a monolithic integrated circuit including a horizontal and a vertical sync separator, offering composite sync and vertical sync extracted from the video signal.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		10.8	12	13.2	V
I_P	supply current (pin 1)		–	8	12	mA
$V_{2(p-p)}$	input voltage amplitude (peak-to-peak value)		0.2	1	3	V
$V_{sync(p-p)}$	sync pulse input voltage amplitude (pin 2) (peak-to-peak value)		50	300	500	mV
V_o	maximum vertical sync output voltage (pin 6)	$I_6 = -1$ mA	10.0	–	–	V
V_o	maximum composite sync output voltage (pin 7)	$I_7 = -3$ mA	10.0	–	–	V
V_o	minimum output voltage (pins 6 and 7)	$I_{6,7} = 1$ mA	–	–	0.6	V
T_{amb}	operating ambient temperature range		0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4820T	8	mini-pack	plastic	SO8; SOT96A

Sync separation circuit for video applications

TDA4820T

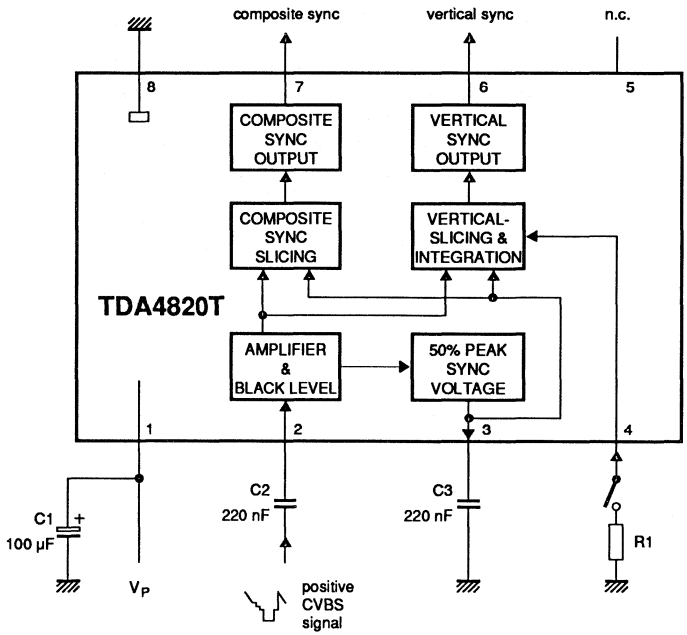


Fig. 1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
V_{CVBS}	2	video input signal
SLEV	3	slicing level
VDEL	4	vertical integration delay time
n.c.	5	not connected
VSYN	6	vertical sync output signal
CSYN	7	composite sync output signal
GND	8	ground

PIN CONFIGURATION

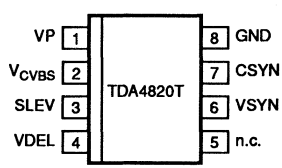


Fig. 2 Pin configuration.

Sync separation circuit for video applications

TDA4820T

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

- Video amplifier and black level clamping
- 50% peak sync voltage
- Composite sync slicing
- Vertical slicing and double slope integrator
- Vertical sync output
- Composite sync output

Video amplifier and black level clamping (pin 2)

The sync separation circuit TDA4820T is designed for positive video input signals.

The video signal (supplied via capacitor C2 at pin 2) is amplified by approximately 15 in the input amplifier. The black level clamping voltage (approximately 2 V) is stored by capacitor C2.

50% peak sync voltage (pin 3)

From the black level and the peak sync voltage, the 50% value of the peak sync voltage is generated and stored by capacitor C3 at pin 3.

A slicing level control circuit ensures a constant 50% value, as long as the sync pulse amplitude at pin 2 is between 50 mV and 500 mV, independent of the amplitude of the picture content.

Composite sync slicing

A comparator in the composite sync slicing stage compares the amplified video signal with the DC voltage derived from 50% peak sync voltage. This generates the composite sync output signal.

Vertical slicing and double slope integrator

Vertical slicing compares the composite sync signal with a DC level equal to 40 % of the peak sync voltage, similar to the composite sync slicing.

With signal interference (reflections or noise) the reduced vertical slicing level ensures more energy for the vertical pulse integration. The slope is double-integrated to eliminate the influence of signal interference.

The vertical integration delay time t_{dV} can be set from typically 45 µs (pin 4 open) to typically 18 µs (pin 4 grounded). Between these maximum and minimum values, t_{dV} can be set by a resistor R1 from pin 4 to ground. For optimum sync behaviour with input line sync pulses only, R1 has to be $\geq$ 3.3 kΩ. In this case t_{dV} is typically $\geq$ 23 µs.

Vertical sync output
Composite sync output

Both output stages are emitter followers with bias currents of 2 mA.

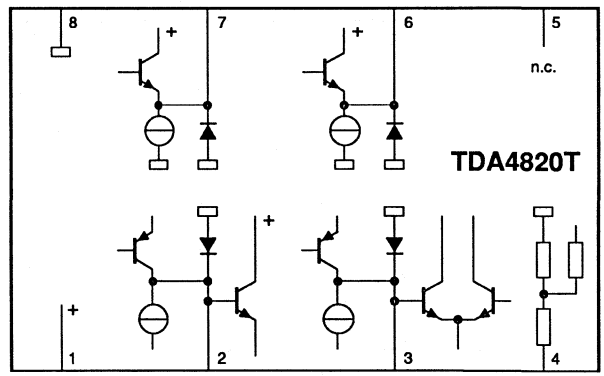


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	0	13.2	V
V_i	input voltage (pin 2)	–0.5	6	V
I_o	output current (pin 6 and pin 7)	3	–10	mA
T_{stg}	storage temperature range	–25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
T_j	maximum junction temperature	–	150	°C
P_{tot}	total power dissipation	–	500	mW

Sync separation circuit for video applications

TDA4820T

CHARACTERISTICS

All voltages measured to GND (pin 8); V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		10.8	12.0	13.2	V
I_P	supply current (pin 1)		4	8	12	mA
Video amplifier						
$V_{2(p-p)}$	input amplitude (peak-to-peak value)	positive video signal AC coupled	0.2	1	3	V
$V_{sync\ (p-p)}$	sync pulse amplitude (pin 2) (peak-to-peak value)	composite sync slicing level 50% for 0.2 V ≤ $V_{2(p-p)}$ ≤ 1.5 V	50	300	500	mV
Z_s	source impedance		–	–	200	Ω
Black level clamping						
I_2	discharge current of C2	during video content	–	5	–	µA
	charge currents of C2	sync below slicing level	–	–40	–	µA
		sync above slicing level	–	–25	–	µA
		during black level	–	–20	–	µA
50% peak sync voltage						
I_3	discharge current of C3	during video content	–	16	–	µA
	maximum charge current of C3		–	–345	–	µA
	reduced charge current of C3	during vertical sync	–	–255	–	µA
	charge current of C3	during sync pulse	–	–160	–	µA
Composite sync slicing (see Fig.4)						
	composite sync slicing level	0.2 V ≤ $V_{2(p-p)}$ ≤ 1.5 V	–	50	–	%
t_{dH}	horizontal delay time (pin 7)	maximum load at pin 7: C_L ≤ 5 pF; R_L ≥ 100 kΩ	–	250	500	ns
Vertical sync separation (see Fig.5)						
	slicing level for vertical sync	0.2 V ≤ $V_{2(p-p)}$ ≤ 1.5 V	–	40	–	%
t_{dV}	vertical leading edge delay times (pin 6)	pin 4 open	30	45	60	µs
		pin 4 grounded	11	18	25	µs
Vertical and composite sync outputs						
V_o	maximum vertical sync output voltage (pin 6)	I_6 = –1 mA	10.0	10.5	11.5	V
V_o	maximum composite sync output voltage (pin 7)	I_7 = –3 mA	10.0	10.5	11.5	V
V_o	minimum output voltages (pins 6 and 7)	$I_{6,7}$ = 1 mA	0.1	0.3	0.6	V
t_W	vertical sync pulse width	pin 4 open; standard signal of 625 lines	–	180	–	µs

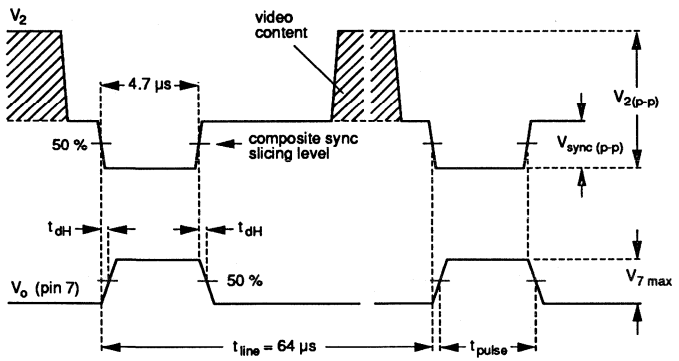
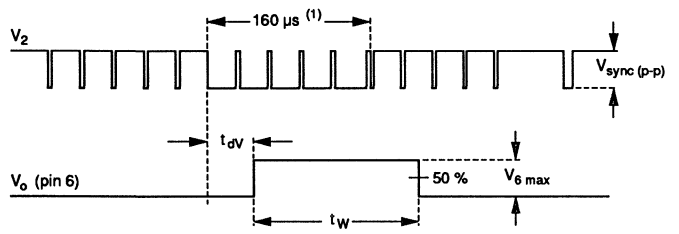


Fig.4 Typical horizontal sync signal.



(1) due to 625 line standard

Fig.5 Typical vertical sync signal.

Philips Semiconductors

Data sheet	
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date of issue	September 1991

TDA4860

Vertical deflection power amplifier for monitors

FEATURES

- Vertical pre-amplifier with differential inputs
- Powerless vertical shift
- Flyback voltage generation suitable for two operating modes (doubling the supply voltage or external supply for the short flyback time, this achieves a minimum of power dissipation)
- Vertical output stage with thermal and SOAR protection
- High deflection frequency up to 140 Hz
- High linear sawtooth signal amplification
- Possibility of guarding the deflection
- Voltage stabilizer

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{P1} = V_1$	positive supply voltage (pin 1)	9	-	30	V
$V_{P2} = V_4$	positive supply voltage (pin 4)	9	-	60	V
$V_{P3} = V_8$	flyback supply voltage (pin 8)	9	-	60	V
I_{P1}	supply current (pin 1)	-	-	10	mA
I_{P2}	supply quiescent current (pin 4)	-	9	-	mA
V_I	input voltage range (pins 2 and 3)	1.6		V_{P1}-0.5	V
$\pm I_{5\,M}$	deflection output current (maximum value, pin 5)	-	-	±1	A
T_{amb}	operating ambient temperature range	–20	-	+75	°C

Note to quick reference data
Measurements referenced to substrate (pin 6).

GENERAL DESCRIPTION

The TDA4860 is a vertical power amplifier for differential input signals suitable for colour monitor/TV systems with deflection frequency up to 140 Hz.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4860	9	SIL	plastic	SOT110

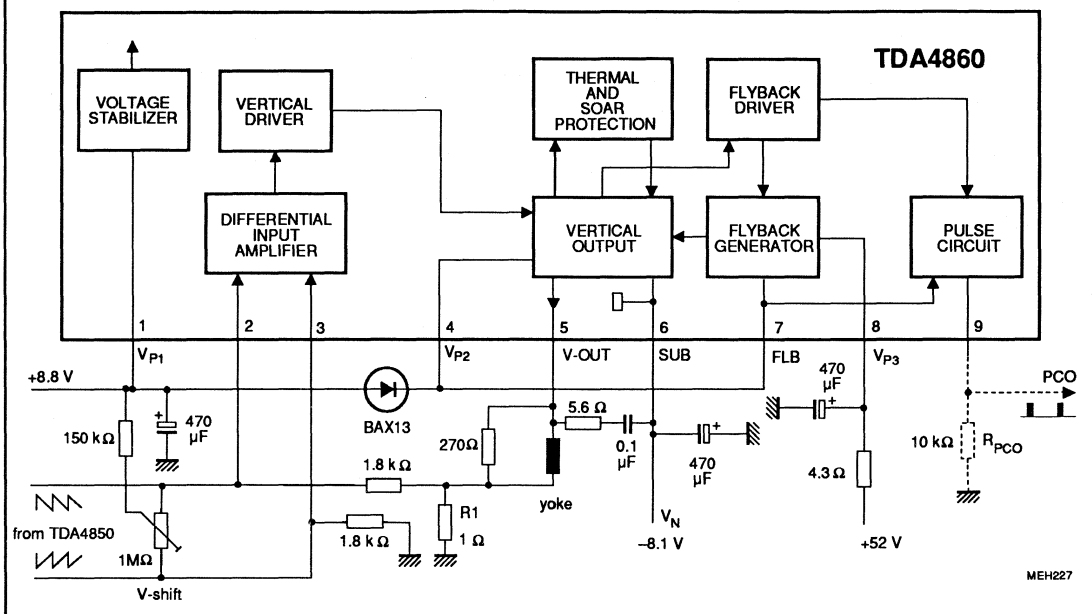


Fig.1 Block diagram and application circuit with flyback supply voltage V_{P3} from an external source. Deflection frequency range from 50 Hz up to 100 Hz.

Notes to Fig.1

Assumed values

I_{yoke}	=	1.42 A	P_{yoke}	=	1.2 W
R_{yoke}	=	4.17 Ω + 7% + ΔR(T) = 6.12 Ω	P_{IC}	=	1.8 W
L_{yoke}	=	5.25 mH	P_{tot}	=	3.0 W
R_1	=	1.0 Ω ±1%	$t_{p\ FLB}$	=	typically 250 µs
T_{amb}	=	65 °C			
$T_{j\ max}$	=	105 °C			
T_{yoke}	=	75 °C			

Attention: the heatsink of the IC must be isolated against ground; the cooling fin is connected to pin 6.

Vertical deflection power amplifier for monitors

TDA4860

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P1}	1	positive supply voltage 1
INP1	2	input 1 of differential input amplifier
INP2	3	input 2 of differential input amplifier
V_{P2}	4	positive supply voltage 2 for vertical output stage
V-OUT	5	vertical output
SUB	6	substrate
FLB	7	flyback generator output
V_{P3}	8	positive flyback supply voltage 3
PCO	9	pulse circuit output

PIN CONFIGURATION

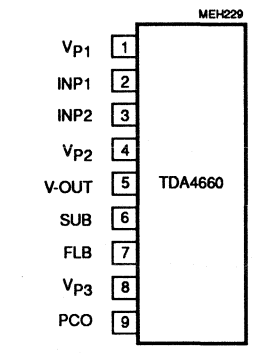


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Differential input amplifier

The differential sawtooth input signal (coming from ramp output of the TDA 4850 for example) is fed to the input pins 2 and 3. The non-inverted signal is attached to pin 3. The vertical feedback signal is superimposed to the inverted input signal on pin 2.

Vertical shift is applied at the inputs in a power-less way (Fig.1).

Flyback generator

Signals for the flyback generator and the pulse circuit are composed in the flyback driver stage.The flyback output consists of a Darlington transistor and a flyback diode. The flyback generator can operate in two modes:

- a supply voltage from external is applied for the short flyback time, thus the power dissipation is a minimum (Fig.1).
- the flyback voltage is generated by doubling the supply voltage (Fig.5). The 100 µF capacitor C2 between pins 4 and 7 is charged up to V_{P1} during scan, using the external diode and the resistor R2. The cathode of the capacitor C2 is connected to the positive rail during flyback. Thus, the flyback voltage is double the supply voltage.

Vertical output

The vertical output stage is a quasi-complementary class-B amplifier with a high linearity. The output contains SOAR (short-circuit protection) and thermal protection. The output current on pin 5 is reduced for a short time (to let the temperature decrease to T_j <150 °C), when the junction temperature T_j exceeds 160 °C.

Deflection guard

Pin 9 goes to HIGH in case of too high junction temperature (Fig.3).

A pulse signal with 50% duty cycle is output on pin 9, if the deflection coil is open-circuit . A flyback pulse signal is output at normal condition.

Further watching can be achieved by means of an external guard circuit as shown in Fig.4. The 22 µF capacitor is charged during flyback time ($V_5 > V_8$) at normal condition.

In case of failures, the capacitor is discharged – the guard output becomes HIGH.

Guard output level (Fig.4):

- LOW for normal condition
- HIGH for deflection coil short-circuit respectively open-circuit
- HIGH when there are neither input nor output signals.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134);
voltages referenced to substrate (pin 6).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	positive supply voltage (pin 1)	-	40	V
V_{P2}	positive supply voltage (pin 4)	-	60	V
V_{P3}	positive supply voltage (pin 8)	-	60	V
$V_{2,3,9}$	voltage on pins 2, 3, and 9	-	V_{P1}	V
$V_{5,7}$	voltage on pins 5 and 7	-	60	V
I_4	current on pin 4	-	1	A
$I_{5\,(M)}$	output current* on pin 5 (peak value)	-	±1.3	A
$I_{7(M)}$	flyback current on pin 7 (peak value)	-	±1.3	A
I_9	current on pin 9	-	–8	mA
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	–20	+75	°C
T_j	junction temperature*	-	+168	°C
V_{ESD}	electrostatic handling** for all pins	-	±300	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}c}$	from junction-to-case	-	10	K/W

The heatsink can be estimated according to application circuit Fig.1.

$R_{th\ j\text{-}a} = R_{th\ j\text{-}c} + R_{th\ c\text{-}h} + R_{th\ h\text{-}a} = (T_{j\ max} - T_{amb}) / P_{IC\ max} = (105 - 65)\ °C / 1.8\ W = 22.2\ K/W.$

A heatsink is needed at $R_{th\ j\text{-}c} < 10$ K/W and $R_{th\ c\text{-}h} = 0.5$ K/W (using silicon grease) with

$R_{th\ h\text{-}a} = 22.2\ K/W - (10 + 0.5)\ K/W = \underline{11.7\ K/W}$

* Internally limited by thermal protection; switching temperature point at 160 ±8 °C.

** Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor

CHARACTERISTICS

$V_{P1} = V_{P2} = 25$ V; $V_N = V_6 = 0$ V; $T_{amb} = 25$ °C and voltages referenced to substrate (pin 6) unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	positive supply voltage 1 range (pin 1)		9	25	30	V
V_{P2}	positive supply voltage 2 range (pin 4)		9	25	60	V
V_{P3}	positive supply voltage 3 range (pin 8)		9	-	60	V
I_{P1}	supply current (pin 1)		-	-	10	mA
I_{P2}	supply quiescent current (pin 4)	without input signal	-	9	-	mA
Pre-amplifier						
$V_{2,3}$	input voltage range (pins 2 and 3)		1.6	-	V_{P1}-0.5	V
$I_{2,3}$	input quiescent current	without input signal	-	100	-	nA
Flyback generator						
V_7	output voltage	upper value; $I_7 = -1$ A	-	V_{P3}-2.2	-	V
$I_{7\,(M)}$	flyback output current (maximum value, pin 7)	-		-	±1	A
V_{1-5}	threshold voltage to switch flyback	on/off threshold	-	1.4	-	V
$t_{p\,FLB}$	flyback pulse time	Fig.1; Fig.3	-	250	-	µs
Vertical output		Fig.3				
V_5	output voltage	upper value; $I_5 = -1$ A	V_{P2}-2.3	V_{P2}-2	-	V
		lower value; $I_5 = 1$ A	-	1.5	1.7	V
$I_{5\,(M)}$	vertical output current (maximum value, pin 5)		-	±1	A	
LIN	non-linearity of output signal		-	-	1	%
Pulse circuit output		Fig.3				
V_9	output voltage range	$R_{PCO} = 10$ kΩ; Fig.1	0.4	-	V_{P1}-0.4	V
	output voltage for thermal protection active		V_{P1}-0.4	-	-	V
V_{1-5}	voltage to insert flyback pulse on pin 9	normal condition	-	-	1.4	V
$t_{p\,9}$	pulse width	deflection open-circuit	-	50	-	%
		normal condition	$t_{p\,FLB}$	-	-	µs

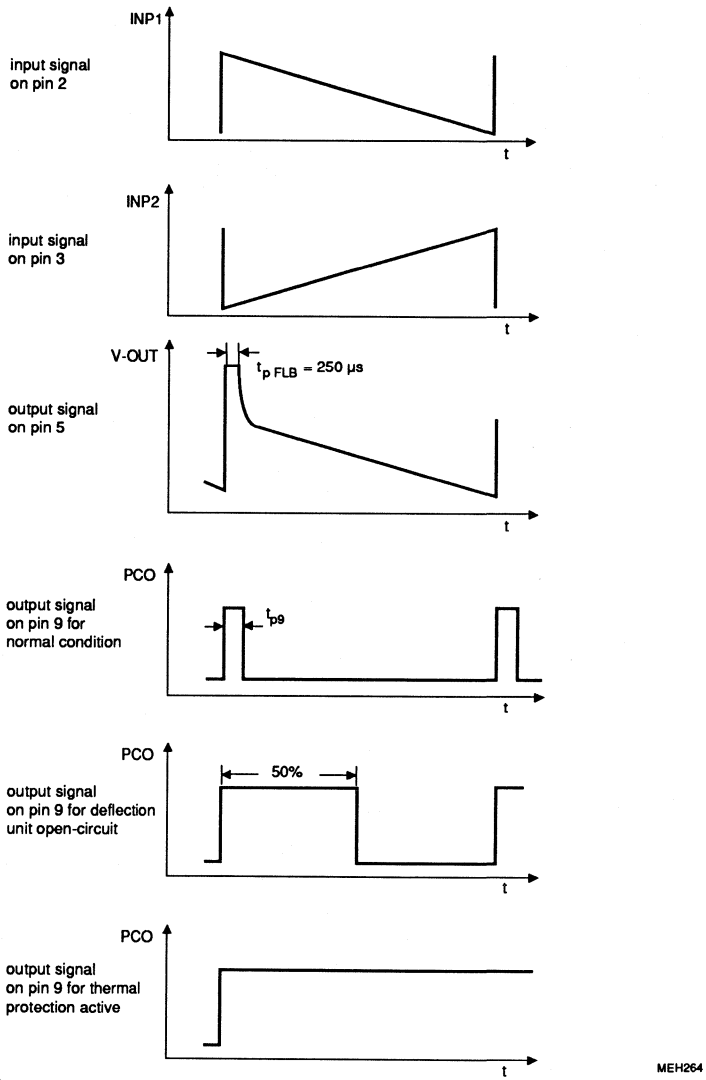


Fig.3 Vertical timing.

APPLICATION INFORMATION

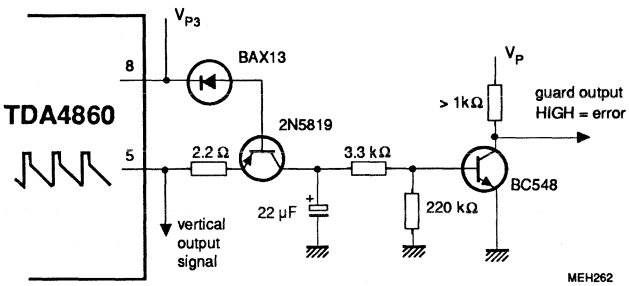


Fig.4 Guard circuit application on vertical output.

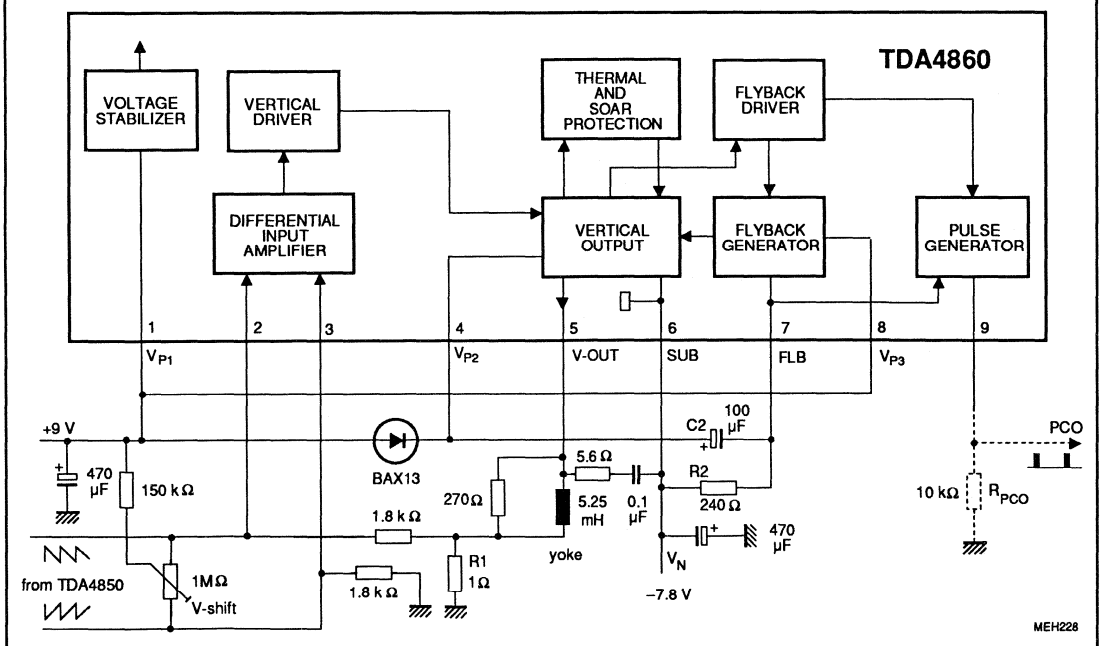


Fig.5 Application for flyback voltage generation by doubling the supply voltage.

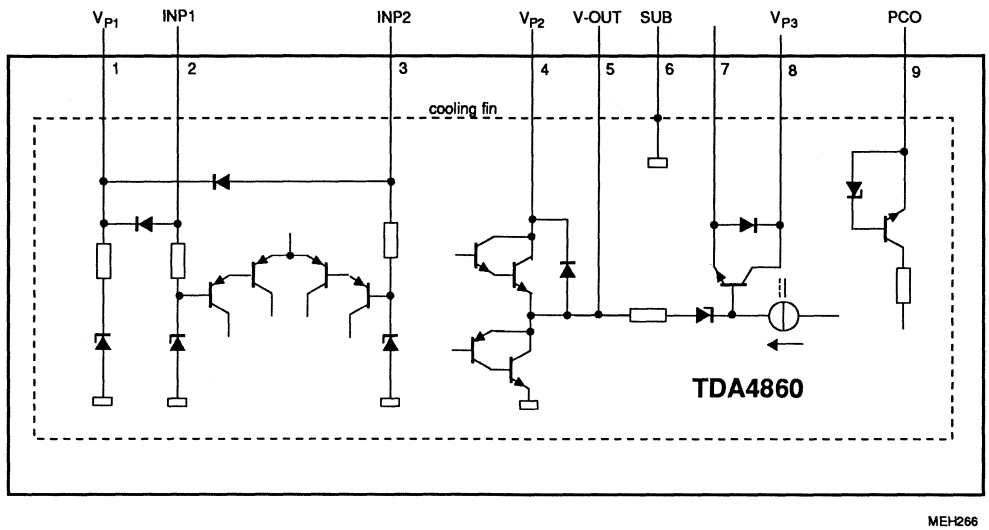


Fig.6 Internal circuit.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1992

TDA4861

Vertical deflection power amplifier for monitors

FEATURES

- Vertical pre-amplifier with differential inputs
- Powerless vertical shift
- Flyback voltage generation suitable for two operating modes (doubling the supply voltage or external supply for the short flyback time, this achieves a minimum of power dissipation)
- Vertical output stage with thermal and SOAR protection
- High deflection frequency up to 140 Hz
- High linear sawtooth signal amplification
- Possibility of guarding the deflection
- Voltage stabilizer

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	positive supply voltage (pin 1)	9	-	30	V
V_{P2}	positive supply voltage (pin 4)	9	-	60	V
V_{P3}	flyback supply voltage (pin 8)	9	-	60	V
I_{P1}	supply current (pin 1)	-	-	10	mA
I_{P2}	supply quiescent current (pin 4)	-	9	-	mA
V_I	input voltage range (pins 2 and 3)	1.6		V_{P1}-0.5	V
I_5	deflection output current (peak-to-peak value, pin 5)	-	-	2.8	A
T_{amb}	operating ambient temperature range	–20	-	75	°C

Note to quick reference data

Measurements referenced to substrate (pin 6).

GENERAL DESCRIPTION

The TDA4861 is a vertical power amplifier for differential input signals suitable for colour monitor/TV systems with deflection frequency up to 140 Hz.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4861	9	SIL	plastic	SOT131

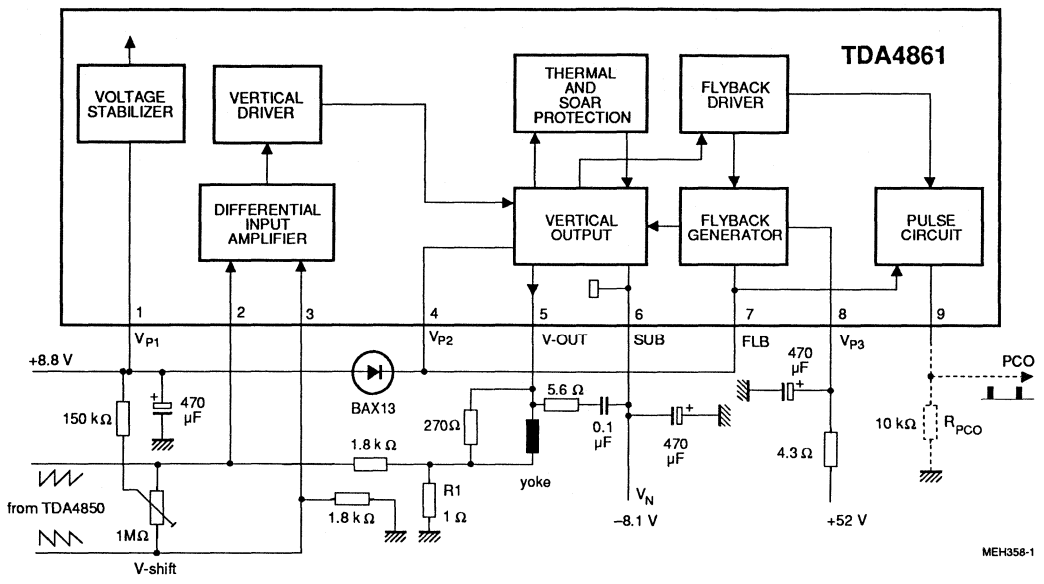


Fig.1 Block diagram and application circuit with flyback supply voltage V_{P3} from an external source. Deflection frequency range from 50 Hz up to 100 Hz.

Notes to Fig.1

Assumed values

I_{yoke}	=	1.42 A	P_{yoke}	=	1.2 W
R_{yoke}	=	4.17 Ω + 7% + ΔR(T) = 6.12 Ω	P_{IC}	=	1.8 W
L_{yoke}	=	5.25 mH	P_{tot}	=	3.0 W
R_1	=	1.0 Ω ±1%	$t_{p\ FLB}$	=	typically 250 µs
T_{amb}	=	65 °C			
$T_{j\ max}$	=	105 °C			
T_{yoke}	=	75 °C			

Attention: the heatsink of the IC must be isolated against ground (it is connected to pin 6).

Vertical deflection power amplifier for monitors

TDA4861

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P1}	1	positive supply voltage 1
INP1	2	input 1 of differential input amplifier
INP2	3	input 2 of differential input amplifier
V_{P2}	4	positive supply voltage 2 for vertical output stage
V-OUT	5	vertical output
SUB	6	substrate
FLB	7	flyback generator output
V_{P3}	8	positive flyback supply voltage 3
PCO	9	pulse circuit output

PIN CONFIGURATION

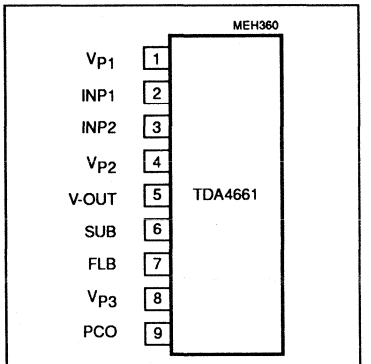


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Differential input amplifier

The differential sawtooth input signal (coming from ramp output of the TDA 4850 for example) is fed to the input pins 2 and 3. The non-inverted signal is attached to pin 3. The vertical feedback signal is superimposed to the inverted input signal on pin 2.

Vertical shift is applied at the inputs in a power-less way (Fig.1).

Flyback generator

Signals for the flyback generator and the pulse circuit are composed in the flyback driver stage.The flyback output consists of a Darlington transistor and a flyback diode. The flyback generator can operate in two modes:

- a supply voltage from external is applied for the short flyback time, thus the power dissipation is a minimum (Fig.1).
- the flyback voltage is generated by doubling the supply voltage (Fig.5). The 100 µF capacitor C2 between pins 4 and 7 is charged up to V_{P1} during scan, using the external diode and the resistor R2. The cathode of the capacitor C2 is connected to the positive rail during flyback. Thus, the flyback voltage is double the supply voltage.

Vertical output

The vertical output stage is a quasi-complementary class-B amplifier with a high linearity. The output contains SOAR (short-circuit protection) and thermal protection. The output current on pin 5 is reduced for a short time (to let the temperature decrease to T_j <150 °C), when the junction temperature T_j exceeds 160 °C.

Deflection guard

Pin 9 goes to HIGH in case of too high junction temperature (Fig.3).

A pulse signal with 50% duty cycle is output on pin 9, if the deflection coil is open-circuit . A flyback pulse signal is output at normal condition.

Further watching can be achieved by means of an external guard circuit as shown in Fig.4. The 22 µF capacitor is charged during flyback time ($V_5 > V_8$) at normal condition.

In case of failures, the capacitor is discharged – the guard output becomes HIGH.

Guard output level (Fig.4):

- LOW for normal condition
- HIGH for deflection coil short-circuit respectively open-circuit
- HIGH when there are neither input nor output signals.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134);
voltages refering to substrate pin 6.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	positive supply voltage (pin 1)	-	40	V
V_{P2}	positive supply voltage (pin 4)	-	60	V
V_{P3}	positive supply voltage (pin 8)	-	60	V
$V_{2,3,9}$	voltage on pins 2, 3, and 9	-	V_{P1}	V
$V_{5,7}$	voltage on pins 5 and 7	-	60	V
I_4	current on pin 4	-	1	A
$I_{5\,(M)}$	output current* on pin 5 (peak value)	-	±1.5	A
$I_{7(M)}$	flyback current on pin 7 (peak value)	-	±1.5	A
I_9	current on pin 9	-	–8	mA
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	–20	75	°C
T_j	junction temperature*	-	168	°C
V_{ESD}	electrostatic handling** for all pins	-	±300	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-case	-	5	K/W

The heatsink can be estimated according to application circuit Fig.1.

$R_{th\ j\text{-}a} = R_{th\ j\text{-}c} + R_{th\ c\text{-}h} + R_{th\ h\text{-}a} = (T_{j\ max} - T_{amb}) / P_{IC\ max} = (105 - 65)\ °C / 1.8\ W = 22.2\ K/W.$

A heatsink is needed at $R_{th\ j\text{-}c} < 5$ K/W and $R_{th\ c\text{-}h} = 0.5$ K/W (using silicon grease) with

$R_{th\ h\text{-}a} = 22.2\ K/W - (5 + 0.5)\ K/W = \underline{16.7\ K/W}$

* Internally limited by thermal protection; switching temperature point at 160 ±8 °C.

** Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor

CHARACTERISTICS

$V_{P1} = V_{P2} = 25$ V; $V_N = V_6 = 0$ V; $T_{amb} = 25$ °C and voltages referenced to substrate (pin 6) unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	positive supply voltage 1 range (pin 1)		9	25	30	V
V_{P2}	positive supply voltage 2 range (pin 4)		9	25	60	V
V_{P3}	positive supply voltage 3 range (pin 8)		9	-	60	V
I_{P1}	supply current (pin 1)		-	-	10	mA
I_{P2}	supply quiescent current (pin 4)	without input signal	-	9	-	mA
Pre-amplifier						
$V_{2,3}$	input voltage range (pins 2 and 3)		1.6	-	V_{P1}-0.5	V
$I_{2,3}$	input quiescent current	without input signal	-	100	-	nA
Flyback generator						
V_7	output voltage	upper value; $I_7 = -1$ A	-	V_{P3}-2.2	-	V
$I_{7\,(M)}$	flyback output current (maximum value, pin 7)	-		-	±1.3	A
V_{1-5}	threshold voltage to switch flyback	on/off threshold	-	1.4	-	V
$t_{p\,FLB}$	flyback pulse time	Fig.1; Fig.3	-	250	-	µs
Vertical output		Fig.3				
V_5	output voltage	upper value; $I_5 = -1$ A	V_{P2}-2.3	V_{P2}-2	-	V
		lower value; $I_5 = 1$A	-	1.5	1.7	V
		upper value; $I_5 = -1.4$ A	-	V_{P2}-2.3	-	V
		lower value; $I_5 = 1.4$ A	-	1.7	-	V
I_5	vertical output current (peak-to-peak value, pin 5)		-	-	2.8	A
LIN	non-linearity of output signal		-	-	1	%
Pulse circuit output		Fig.3				
V_9	output voltage range	$R_{PCO} = 10$ kΩ; Fig.1	0.4	-	V_{P1}-0.4	V
	output voltage for thermal protection active		V_{P1}-0.4	-	-	V
V_{1-5}	voltage to insert flyback pulse on pin 9	normal condition	-	-	1.4	V
$t_{p\,9}$	pulse width	deflection open-circuit	-	50	-	%
		normal condition	$t_{p\,FLB}$	-	-	µs

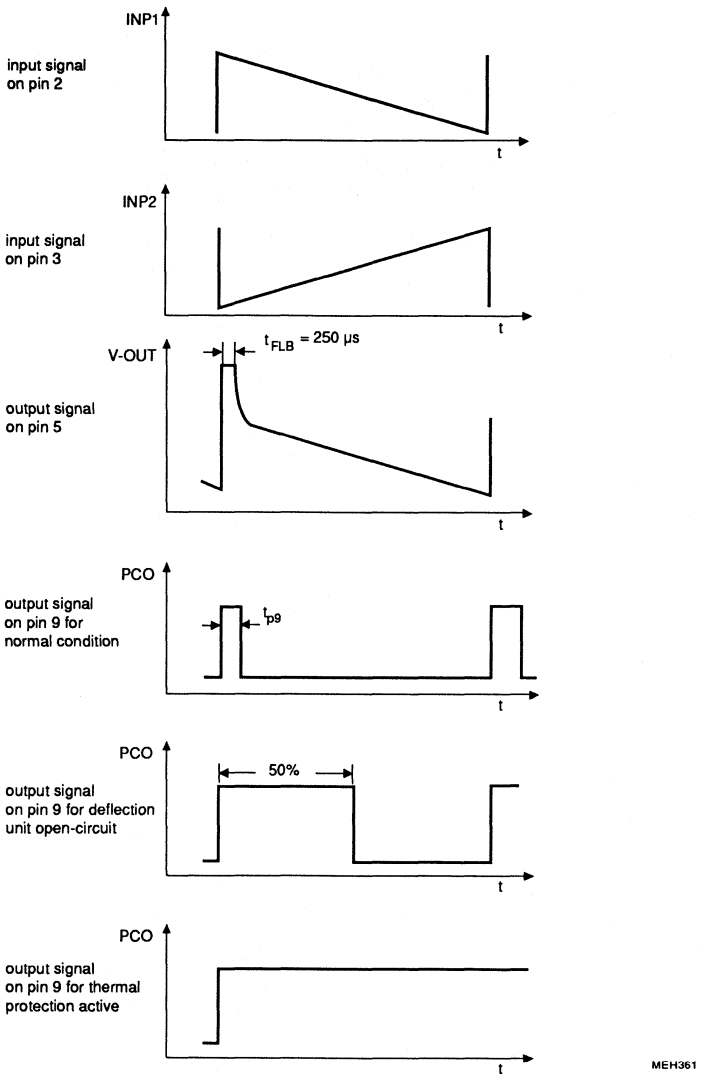


Fig.3 Vertical timing.

APPLICATION INFORMATION

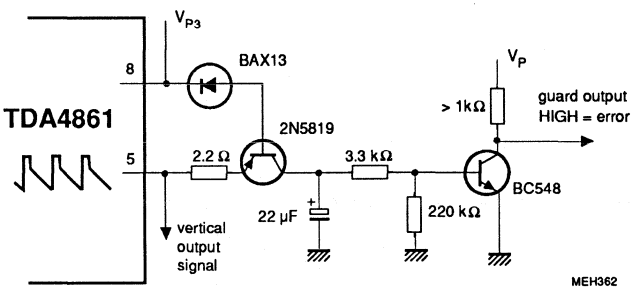


Fig.4 Guard circuit application on vertical output.

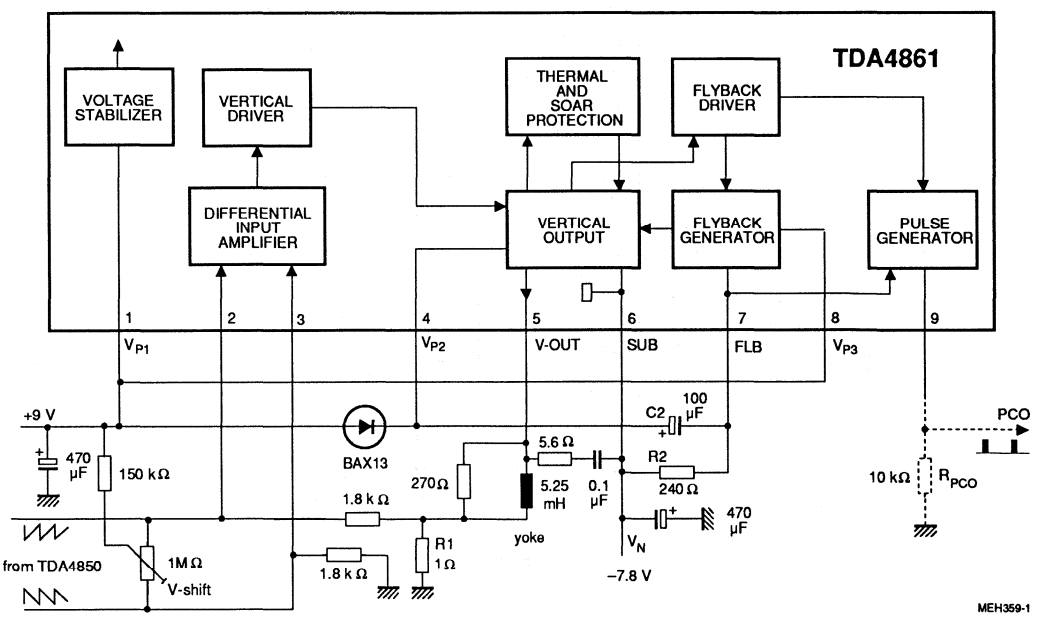


Fig.5 Application for flyback voltage generation by doubling the supply voltage.

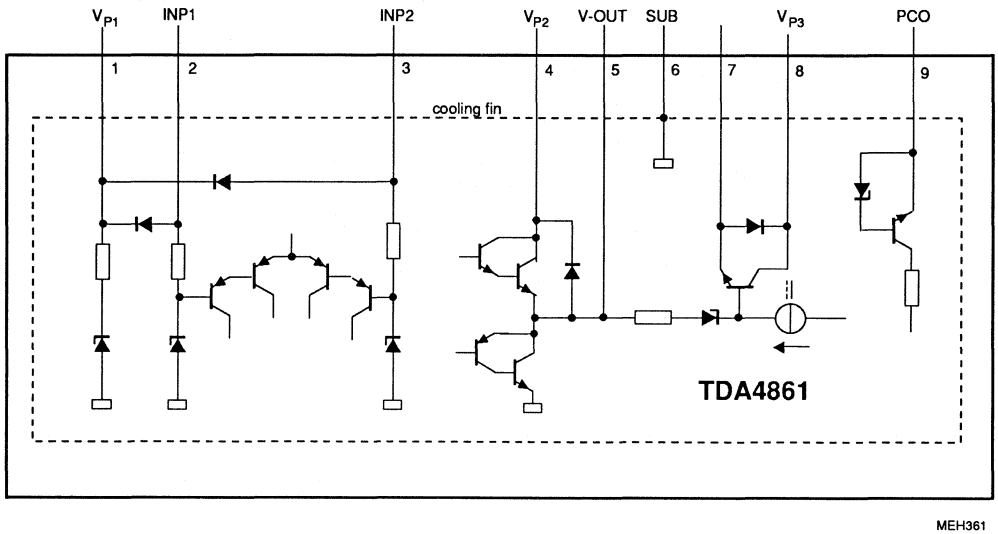


Fig.6 Internal circuit.

Philips Semiconductors

Data sheet	
status	Objective specification
date of issue	August 1991

TDA4880
Advanced monitor video controller

FEATURES

- Fully DC controllable
- 3 separate video channels
- Input black level clamping
- Individual gain control for white level adjustment
- Brightness control with correct grey scale tracking
- Contrast control for the 3 channels simultaneously
- Cathode feedback to internal reference for black level control
- Current outputs for RGB signal currents
- RGB voltage outputs to external peaking circuits
- Blanking and switch off input for screen protection

GENERAL DESCRIPTION

The TDA4880 is a monolithic integrated RGB amplifier for colour monitor systems with super VGA performance, intended for DC or AC coupling of the colour signals to the cathodes of the CRT. With special advantages the circuit can be used in conjunction with the TDA4850.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 7)		7.2	8.0	8.8	V
I_P	supply current (pin 7)		–	40	–	mA
$V_{I(b-w)}$	input voltage (pins 2, 5 and 8) (black-to-white)		–	0.7	–	V
$V_{O(b-w)}$	output voltage (pins 19, 16 and 13) (black-to-white)		–	1.0	–	V
$I_{O(b-w)}$	output current (pins 20, 17 and 14) (black-to-white)		–	50	–	mA
I_M	peak output current (pins 20, 17 and 14)		–	100	–	mA
B	bandwidth	–3 dB	70	–	–	MHz
G_{nom}	nominal gain		–	3		dB
G_v	gain control range (relative to G_{nom})		–6	–	0	dB
C_v	contrast control range (relative to G_{nom})		–20	–	3	dB
ΔV_{bl}	brightnesss control range		–0.1	–	0.3	V
T_{amb}	operating ambient temperature range		0	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4880	20	DIL	plastic	SOT146

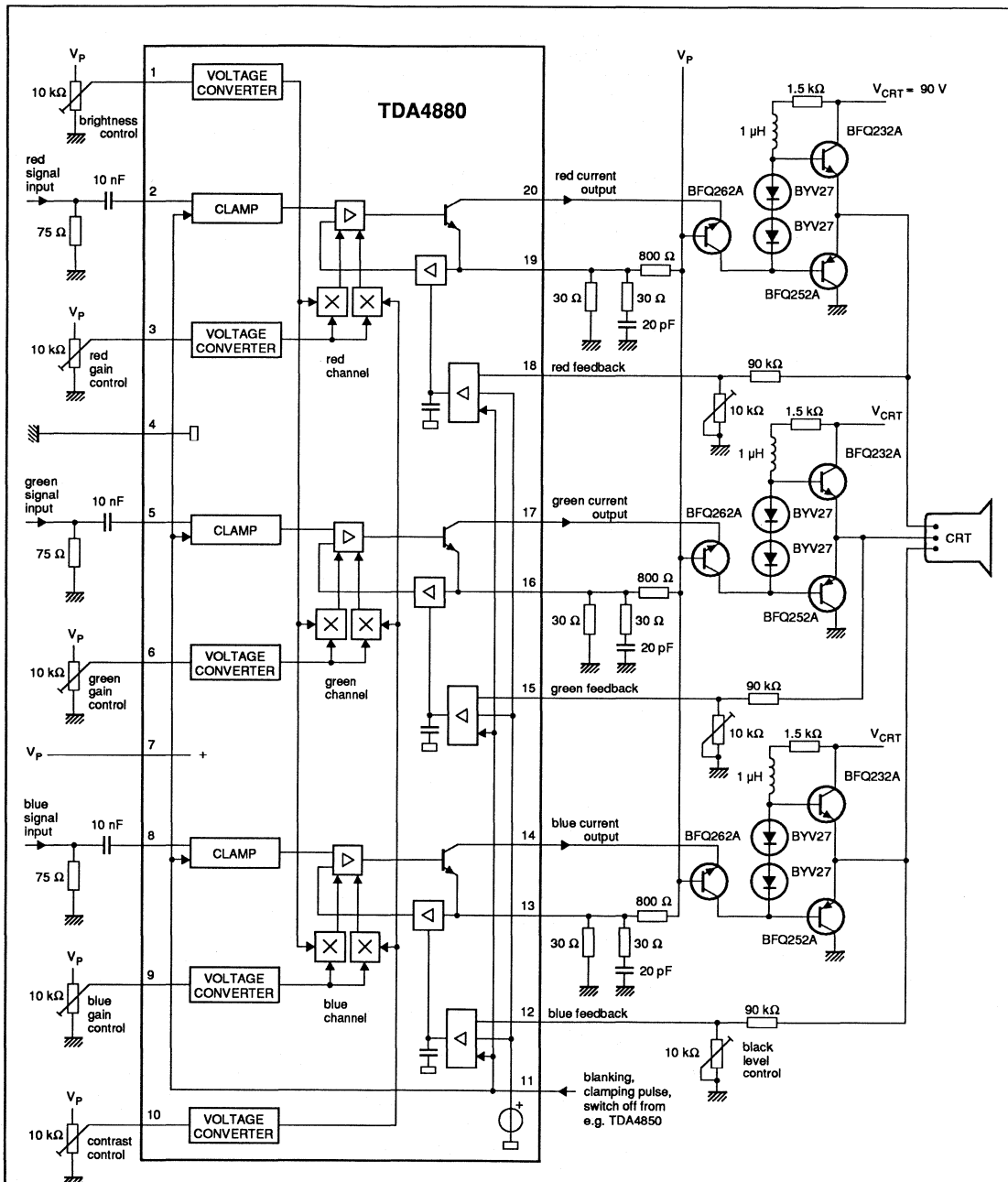


Fig. 1 Block diagram and basic application circuit for DC coupling.

Advanced monitor video controller TDA4880

PIN CONFIGURATION

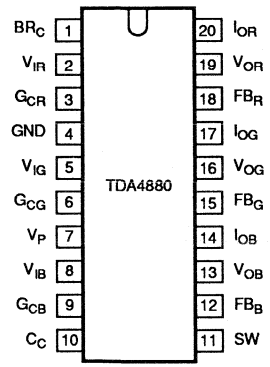


Fig. 2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
BR_C	1	brightness control
V_{IR}	2	red signal input
G_{CR}	3	red gain control
GND	4	ground
V_{IG}	5	green signal input
G_{CG}	6	green gain control
V_P	7	supply voltage
V_{IB}	8	blue signal input
G_{CB}	9	blue gain control
C_C	10	contrast control
SW	11	blanking / clamping pulse, switch off
FB_B	12	blue feedback
V_{OB}	13	blue voltage output
I_{OB}	14	blue current output
FB_G	15	green feedback
V_{OG}	16	green voltage output
I_{OG}	17	green current output
FB_R	18	red feedback
V_{OR}	19	red voltage output
I_{OR}	20	red current output

FUNCTIONAL DESCRIPTION

RGB input signals are capacitively coupled into the TDA4880 from a low ohmic source and are clamped to an internal DC voltage. Sync-on-green will not disturb normal operation. Each channel has a maximum voltage gain of 6 dB. With the nominal gain of 3 dB the nominal black-to-white output voltage is 1 V(p-p).

DC voltages are used for brightness, contrast and gain control.

For **brightness control** (pin 1) the signal black levels are shifted relative to a reference black level voltage. The brightness is set internally to the nominal brightness level during blanking and clamping pulses.

Contrast control is adjusted simultaneously for the three colour signals by a voltage at pin 10.

The **RGB gain controls** (pins 3, 6 and 9) adjust the RGB signal levels of each channel separately to provide the correct white point. Variable RGB gain affects contrast as well as brightness to achieve correct grey scale tracking.

Each **RGB output stage** provides a current output (pins 20, 17 and 14) and a voltage output (pins 19, 16 and 13).

External cascode transistors reduce power consumption and prevent breakdown of the output transistors.

RGB signal output currents and peaking characteristics are determined by resistors and capacitors (pins 19, 16 and 13) and inductors connected to the 90 V supply.

The RGB colour channels have separate internal feedback loops. This ensures high signal linearity and marginal signal distortion in spite of output transistor thermal V_{BE} variation.

The **sandcastle pulse** (e.g. from the TDA4850) is used for input clamping, black level clamping and blanking during flyback. During the clamping pulse the input signals are clamped to an internal black level. During blanking and clamping the brightness is set internally to a nominal value.

For **black level stabilization** the signals at the colour feedback inputs (pins 18, 15 and 12) are compared with an internal reference voltage. Input voltages higher than the reference voltage will increase (lower voltages will decrease) the black level voltage during the clamping pulse. The actual CRT cathode voltage is used for feedback. Therefore, variations of the 90 V supply voltage only marginally affect the black level stabilization. A voltage proportional to the black level is stored on internal capacitors. An integrated colour switch-off facility allows the RGB outputs to be switched to ultra-black for screen protection.

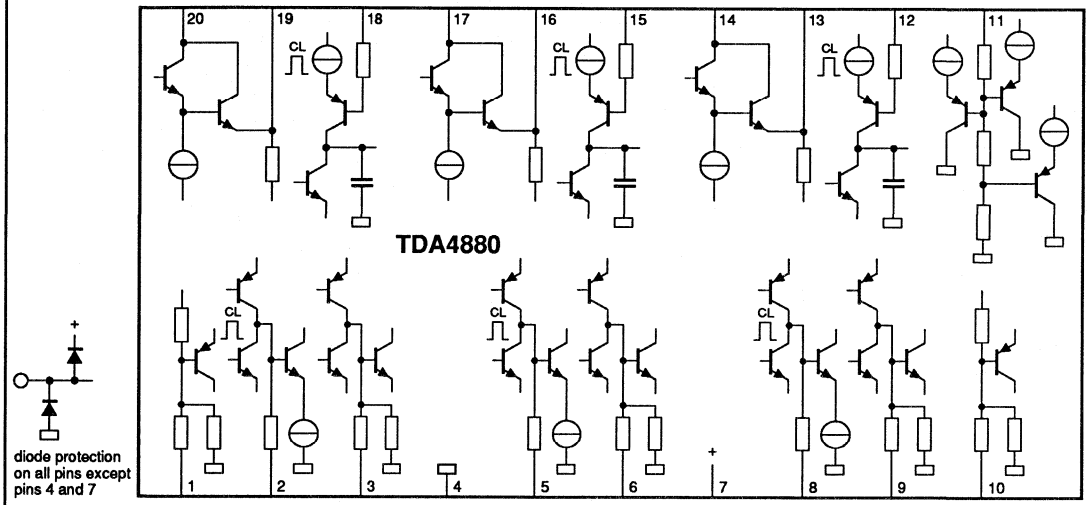


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 7)	0	8.8	V
V_i	input voltage range (pins 2, 5 and 8)	−0.1	V_P	V
V_{ext}	external DC voltage ranges pins 20, 17 and 14	−0.1	V_P	V
	pins 19,16 and 13	–	–	V
	pins 1, 3, 6, 9 and 10	−0.1	V_P	V
	pin 11	−0.7	$V_P + 0.7$	V
I_M	peak output current (pins 20, 17 and 14)	–	150	mA
T_{stg}	storage temperature range	−25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
T_j	maximum junction temperature	–	150	°C
P_{tot}	total power dissipation	–	1200	mW

CHARACTERISTICS

V_P = 8.0 V; T_{amb} = 25 °C; all voltages measured to GND (pin 4); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 7)		7.2	8.0	8.8	V
I_P	supply current (pin 7)		–	40	–	mA
Video signal inputs						
$V_{I(b-w)}$	input amplitude (pins 2, 5 and 8) (black-to-white)		–	0.7	1.0	V
$I_{2,5,8}$	DC current	no clamping	–0.1	–	0.1	μA
		during clamping	± 50	–	–	μA
Brightness control						
V_1	input voltage range		1.0	–	6.0	V
I_1	current		–	–	± 100	μA
ΔV_{bl1}	black level voltage change at nominal gain (pins 19, 16 and 13)	V_1 = 1.0 V; $V_{3,6,9}$ = 6 V	–	–0.1	–	V
		V_1 = 2.25 V; $V_{3,6,9}$ = 6 V	–	0	–	V
		V_1 = 6.0 V; $V_{3,6,9}$ = 6 V	–	0.3	–	V
Contrast control						
V_{10}	input voltage range		1.0	–	6.0	V
I_{10}	current		–	–	± 100	μA
C_v	contrast relative to nominal contrast	V_{10} = 6.0 V; $V_{3,6,9}$ = 6 V	–	3	–	dB
		V_{10} = 4.5 V; $V_{3,6,9}$ = 6 V	–	0	–	dB
		V_{10} = 1.0 V; $V_{3,6,9}$ = 6 V	–	–20	–	dB
Tr	tracking of RGB signals		–	0	0.5	dB
Gain control						
$V_{3,6,9}$	input voltage range		1.0	–	6.0	V
$I_{3,6,9}$	current		–	–	± 100	μA
G_v	gain relative to nominal gain	V_{10} = 4.5 V; $V_{3,6,9}$ = 6 V	–	0	–	dB
		V_{10} = 4.5 V; $V_{3,6,9}$ = 1 V	–	–6	–	dB
Frequency response						
G_{vf}	gain decrease by frequency response at pins 20, 17 and 14	70 MHz	–	–	–3	dB
t_{rO}	rise time at voltage output (pins 19,16 and 13)	10% to 90% amplitude; input rise time = 1 ns	–	5	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage outputs (pins 19, 16, 13)						
$V_{O(b-w)}$	signal output voltage (black-to-white value)	at nominal contrast, gain and nominal input signals	–	1.0	–	V
V_{bl}	black level voltage	during clamping	0.5	–	0.7	V
		during switch-off	–	–	0.3	V
S/N	signal to noise ratio	note 1	–	–	44	dB
Current outputs (pins 20, 17 and 14)						
$I_{O(b-w)}$	signal current (black-to-white)		–	50	–	mA
		with peaking (note 2)	–	100	–	mA
THD	total harmonic distortion	output swing = 1 V	–	–	1	%
Feedback input						
V_{int}	internal reference voltage		–	5.8	–	V
$I_{18,15,12}$	output current		–	–	–1	µA
Threshold voltages (note 3)						
V_{11}	threshold voltage for blanking		1.0	1.4	1.7	V
	threshold voltage for clamping		2.6	3.0	3.3	V
	threshold voltage for switch off		4.5	5.0	5.2	V
I_{11}	current		–	–	± 100	µA
t_{w11}	width of clamping pulse		1	–	–	µs

Notes to the characteristics

1. The signal-to-noise ratio is calculated by the formula (frequency range 1 to 70 MHz):

$$\frac{\text{peak-to peak value of the nominal signal output voltage}}{\text{RMS value of the noise output voltage}}$$

2. The external RC combinations at pins 19, 16 and 13 enables peak currents during transients.
3. The internal threshold voltages are derived from an internally stabilized voltage.

TV VHF MIXER/OSCILLATOR/UHF PREAMPLIFIER

GENERAL DESCRIPTION

The TDA5030A provides VHF local oscillator, VHF mixer and UHF IF preamplifier functions for VHF/UHF television receivers. It includes a buffered output from the VHF local oscillator, a VHF/UHF switching circuit and an IF amplifier stage for an external SAW filter.

Features

- Balanced VHF mixer
- Voltage-controlled VHF local oscillator
- IF amplifier for SAW filter
- UHF IF preamplifier
- Local oscillator buffer output for external prescaler
- Voltage stabilizer
- UHF/VHF switching circuit
- Electrostatic discharge protection diodes at pins 10, 11, 12 and 13

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 15	V_P	10	–	13,2	V
Supply current		I_P	–	42	–	mA
VHF mixer frequency range		f	50	–	470	MHz
Conversion gain			–	24,5	–	dB
Conversion noise	300 MHz		–	10	–	dB
Input signal for 1% cross modulation			–	99	–	dBμV
Storage temperature range		T_{stg}	−55	–	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	–	+ 85	°C

PACKAGE OUTLINE

18-lead DIL, plastic (SOT102).

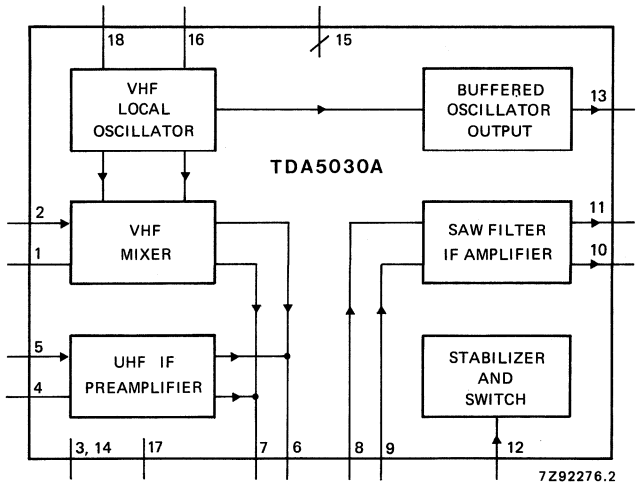


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 15	$V_P = V_{15-3}$	–	14	V
Input voltage	pins 1, 2, 4 and 5	V_i	0	5	V
VHF switching voltage	pin 12	V_{12}	0	$V_{15}+0,3$	V
Output current	pins 10, 11 or 13	$-I_{10, 11, 13}$	–	10	mA
Short-circuit time on outputs	pins 10 and 11	t_{ss}	–	10	s
Storage temperature range		T_{stg}	–55	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	+ 85	°C
Junction temperature range		T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 55 K/W

CHARACTERISTICS

Measured in circuit of Fig. 2, $V_P = V_{15-3} = 12$ V, $T_{amb} = 25$ °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	pin 15	V_{15-3}	10	–	13,2	V
Supply current		I_{15}	–	42	55	mA
Switch voltage level for VHF	pin 12	V_{12}	0	–	2,5	V
Switch voltage level for UHF	pin 12	V_{12}	9,5	–	$V_{15}+0,3$	V
Switch current	UHF selected	I_{12}	–	–	0,7	mA
VHF mixer (including IF amplifier)						
Frequency range		f	50	–	470	MHz
Noise factor	pin 2					
	f = 50 MHz	F	–	7,5	9	dB
	f = 225 MHz	F	–	9	10	dB
	f = 300 MHz	F	–	10	12	dB
	f = 470 MHz	F	–	11	13	dB
Optimum source conductance	pin 2					
	f = 50 MHz	G	–	0,5	–	mS
	f = 225 MHz	G	–	1,1	–	mS
	f = 300 MHz	G	–	1,2	–	mS
Input conductance	pin 2					
	f = 50 MHz	G_i	–	0,23	–	mS
	f = 225 MHz	G_i	–	0,5	–	mS
	f = 300 MHz	G_i	–	0,67	–	mS
Input capacitance	pin 2					
	f = 50 MHz	C_i	–	2,5	–	pF
Input voltage for 1% cross-modulation (in channel)		V_{2-3}	97	99	–	dBμV
Input voltage for 10 kHz pulling (in channel)	f < 300 MHz	V_{2-14}	100	–	–	dBμV
Voltage gain		A_v	22,5	24,5	26,5	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
UHF preamplifier (including IF amplifier)						
Input conductance	pin 5	G_i	–	0,3	–	mS
Input capacitance	pin 5	C_i	–	3,0	–	pF
Noise factor	pin 5	F	–	5	6	dB
Optimum source conductance	pin 5	G	–	3,3	–	mS
Input voltage for 1% cross-modulation (in channel)		$V_{5\text{-}14}$	88	90	–	dBμV
Voltage gain		A_v	31,5	33,5	35,5	dB
VHF mixer						
Conversion transadmittance	pins 2 to 6,7	$Yc_{2\text{-}6,7}$	–	5,7	–	mS
Output impedance	pins 6 and 7	Z_o	–	1,6	–	kΩ
VHF oscillator						
Frequency range		f	70	–	520	MHz
Frequency shift	ΔV_P = 10%; f = 70–330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 15 K; f = 70–330 MHz	Δf	–	–	250	kHz
Frequency drift	between 5 s and 15 min after switch-on	Δf	–	–	200	kHz
SAW filter IF amplifier						
Input impedance	$Z_{10,11}$ = 2 kΩ; f = 36 MHz	$Z_{8,9}$	–	300+ j100	–	Ω
Transimpedance		$Z_{8,9\text{-}10,11}$	–	2,2	–	kΩ
Output reflection coefficient:	f = 36 MHz					
modulus			0,45	0,37	0,41	
phase			–63	–112	–134	deg

parameter	conditions	symbol	min.	typ.	max.	unit
VHF local oscillator output buffer						
Output voltage	pin 13 R_L = 75 Ω					
	f < 100 MHz	V_{13}	14	20	–	mV
	f > 100 MHz	V_{13}	10	20	–	mV
Output impedance	f = 100 MHz	Z_{13}	–	90	–	Ω
RF signal on local oscillator output	R_L = 75 Ω					
	V_i = 1 V; f ≤ 225 MHz	RF/(RF+LO)	–	–	10	dB
	V_i = 0,3 V; f = 225–300 MHz	RF/(RF+LO)	–	–	10	dB
IF signal on local oscillator output	UHF selected; R_L = 75 Ω; V_i = 350 mV	IF/(IF+LO)	–	–	3	mV
Local oscillator harmonics w.r.t. local oscillator output signal	R_L = 75 Ω		–	–	–14	dB

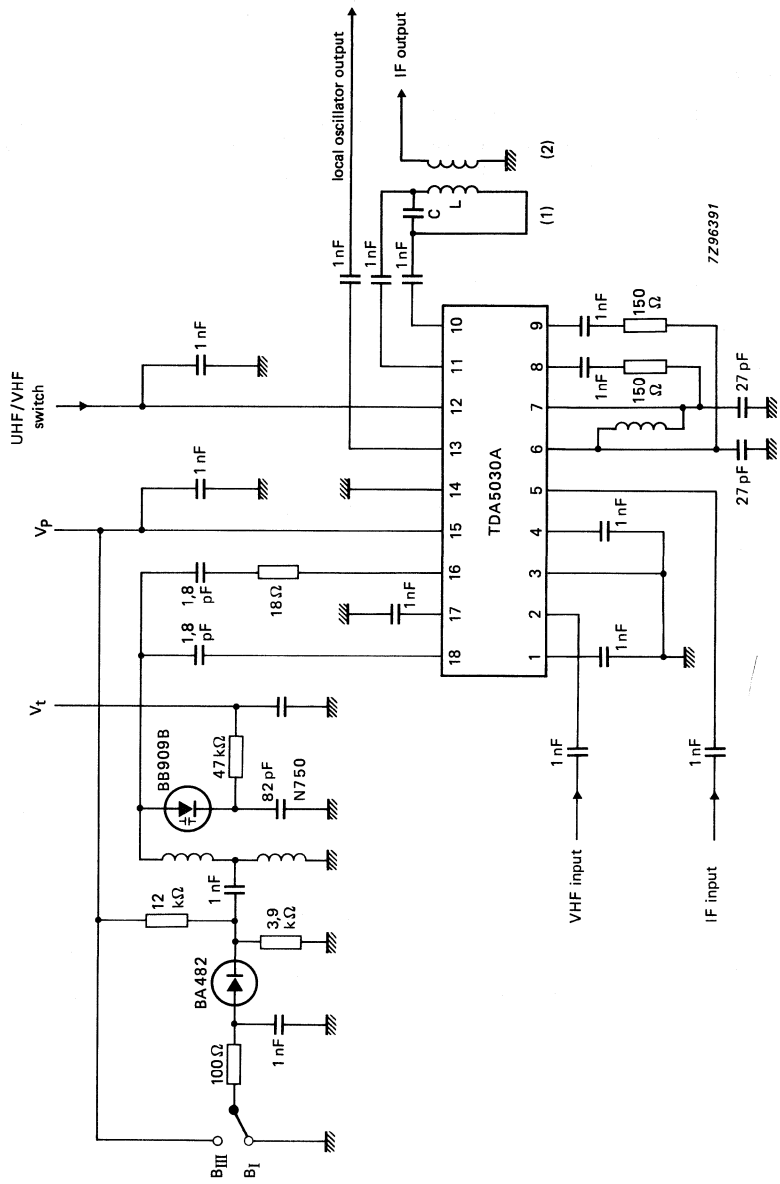


Fig. 2 Test circuit.

(1) C = 18 pF, L = 2,2 μH, f_{CL} = 36,5 MHz.
(2) Turns ratio = 7 : 1, load = 50 Ω.

TV VHF MIXER/OSCILLATOR/UHF PREAMPLIFIER

GENERAL DESCRIPTION

The TDA5030AT provides VHF local oscillator, VHF mixer and UHF IF preamplifier functions for VHF/UHF television receivers. It includes a buffered output from the VHF local oscillator, a VHF/UHF switching circuit and an IF amplifier stage for an external SAW filter.

Features

- Balanced VHF mixer
- Voltage-controlled VHF local oscillator
- IF amplifier for SAW filter
- UHF IF preamplifier
- Local oscillator buffer output for external prescaler
- Voltage stabilizer
- UHF/VHF switching circuit
- Electrostatic discharge protection diodes at pins 11, 12, 13 and 14

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 17)		V_P	10	–	13,2	V
Supply current		I_P	–	42	–	mA
VHF mixer frequency range		f	50	–	470	MHz
Conversion gain			–	25	–	dB
Conversion noise	300 MHz		–	10	–	dB
Input signal for 1% cross modulation			–	99	–	dBμV
Storage temperature range		T_{stg}	−55	–	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	–	+ 80	°C

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).

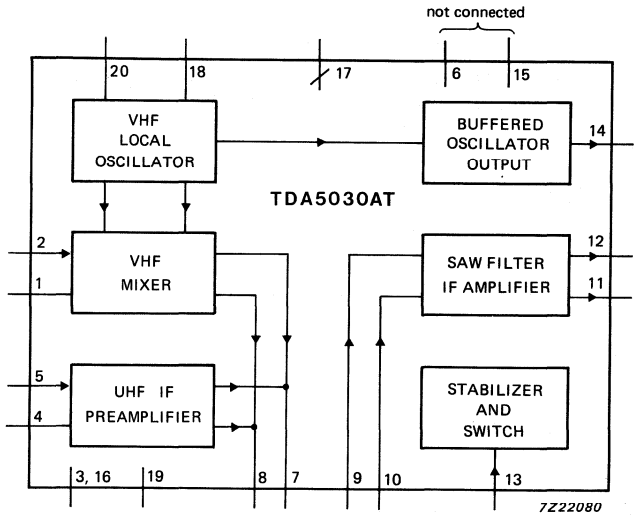


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	$V_P = V_{17-3}$	–	14	V
Input voltage (pins 1, 2, 4 and 5)	V_i	0	5	V
VHF switching voltage (pin 13)	V_{13}	0	V_P+0,3	V
Output current (pins 11, 12 or 14)	$-I_{11,12,14}$	–	10	mA
Short-circuit time on outputs (pins 11, 12 and 14)	t_{sc}	–	10	s
Storage temperature range	T_{stg}	–55	+125	°C
Operating ambient temperature range	T_{amb}	–25	+ 80	°C
Junction temperature range	T_j	–	+150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W

CHARACTERISTICS

$V_P = V_{17-3} = 12$ V; $T_{amb} = 25$ °C; measured in circuit of Fig. 2; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 17)		V_{17-3}	10	–	13,2	V
Supply current		I_{17}	–	42	55	mA
Switch voltage level for VHF (pin 13)		V_{13}	0	–	2,5	V
Switch voltage level for UHF (pin 13)		V_{13}	9,5	–	V_P+0,3	V
Switch current	UHF selected	I_{13}	−0,05	–	0,7	mA
VHF mixer (including IF amplifier)						
Frequency range		f	50	–	470	MHz
Noise factor (pin 2)	f = 50 MHz	NF	–	7,5	9	dB
	f = 225 MHz	NF	–	9	10	dB
	f = 300 MHz	NF	–	10	12	dB
	f = 470 MHz	NF	–	11	13	dB
Optimum source conductance (pin 2)	f = 50 MHz	G	–	0,5	–	mS
	f = 225 MHz	G	–	1,1	–	mS
	f = 300 MHz	G	–	1,2	–	mS
	f = 470 MHz	G	–	1,9	–	mS
Input conductance (pin 2)	f = 50 MHz	G_i	–	0,23	–	mS
	f = 225 MHz	G_i	–	0,5	–	mS
	f = 300 MHz	G_i	–	0,67	–	mS
	f = 470 MHz	G_i	–	1,45	–	mS
Input capacitance (pin 2)	f = 50 MHz	C_i	–	2,5	–	pF
Input voltage for 1% cross-modulation (in channel)		V_{2-3}	96	99	–	dBμV
Input voltage for 10 kHz pulling (in channel)	f < 300 MHz	V_{2-16}	100	–	–	dBμV
Input voltage for 100 kHz pulling	f = 470 MHz	V_{2-3}	73	–	–	dBμV
Voltage gain		A_v	23	25	27	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
UHF preamplifier (including IF amplifier)						
Input conductance (pin 5)		G_i	–	0,3	–	mS
Input capacitance (pin 5)		C_i	–	3,0	–	pF
Noise factor (pin 5)		NF	–	5	6	dB
Optimum source conductance (pin 5)		G	–	3,3	–	mS
Input voltage for 1% cross-modulation (in channel)		V_{5-16}	88	90	–	dBμV
Voltage gain		A_v	32	34	36	dB
VHF mixer						
Conversion transadmittance (pins 2 to 7, 8)		$Yc_{2-7,8}$	–	5,7	–	mS
Output impedance (pins 7 and 8)		Z_o	–	1,6	–	kΩ
VHF oscillator						
Frequency range		f	70	–	520	MHz
Frequency shift	ΔV_P = 10%; f = 70 to 330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 15 K; f = 70 to 330 MHz	Δf	–	–	250	kHz
Frequency drift	between 5 s and 15 min after switch-on	Δf	–	–	200	kHz
SAW filter IF amplifier						
Input impedance	$Z_{11,12}$ = 2 kΩ; f = 36 MHz	$Z_{9,10}$	–	300+ j100	–	Ω
Transimpedance		$Z_{9,10-11,12}$	–	2,2	–	kΩ
Output reflection coefficient:	f = 36 MHz					
modulus			0,45	0,37	0,41	
phase			–63	–112	–134	deg

parameter	conditions	symbol	min.	typ.	max.	unit
VHF local oscillator output buffer						
Output voltage (pin 14)	R_L = 75 Ω					
	f < 100 MHz	V_{14}	14	20	–	mV
	f > 100 MHz	V_{14}	10	20	–	mV
Output impedance	f = 100 MHz	Z_{14}	–	90	–	Ω
RF signal on local oscillator output	R_L = 75 Ω					
	V_i = 1 V; f ≤ 225 MHz	RF/(RF+LO)	–	–	10	dB
	V_i = 0,3 V; f = 225–300 MHz	RF/(RF+LO)	–	–	10	dB
IF signal on local oscillator output	UHF selected; R_L = 75 Ω; V_i = 350 mV	IF/(IF+LO)	–	–	3	mV
Local oscillator harmonics w.r.t. local oscillator output signal	R_L = 75 Ω		–	–	–14	dB

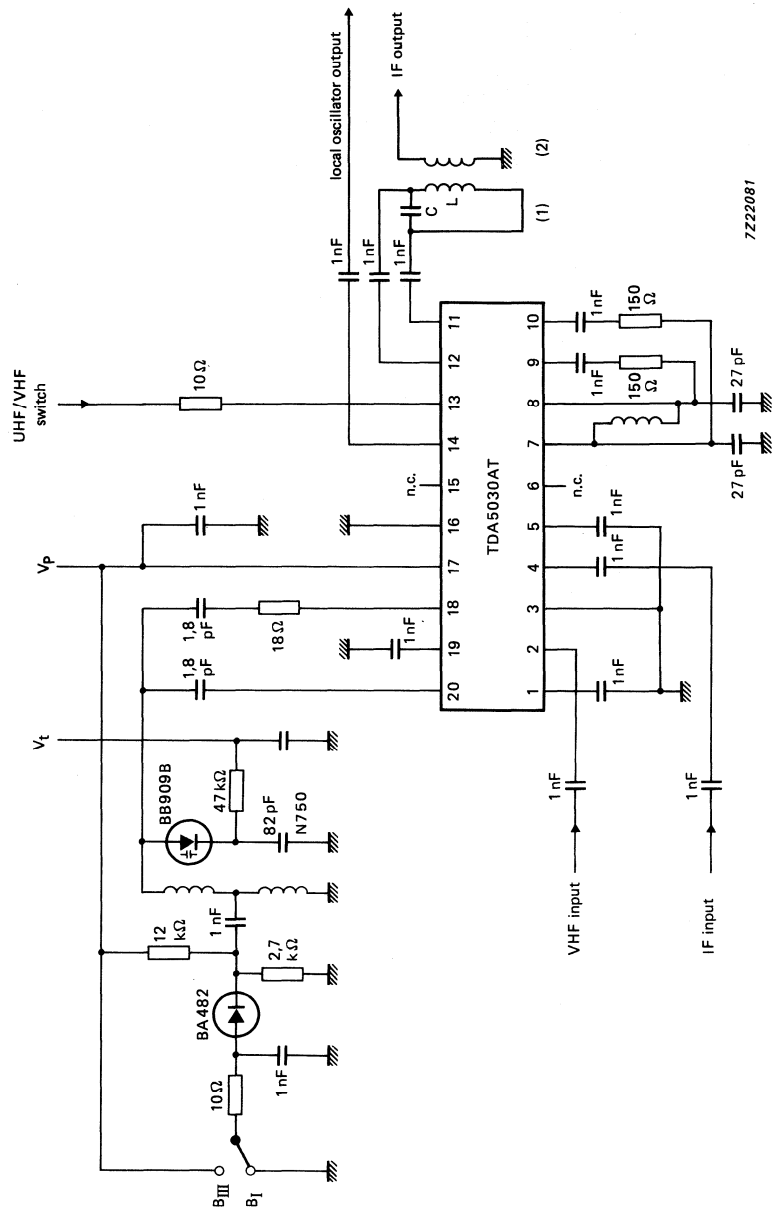


Fig. 2 Test circuit.

(1) C = 18 pF, L = 2,2 μH, f_{CL} = 36,5 MHz.
(2) Turns ratio = 7 : 1, load = 50 Ω.

Brushless DC motor drive circuit TDA5140A/AT

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 0.85 A output current
  - low saturation voltage
  - built-in current limiter
  - soft-switching outputs
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Position pulse stage for phase-locked-loop control
- Transconductance amplifier for an external control transistor

APPLICATIONS

- General purpose spindle driver (e.g. HDD, drum motor)

DESCRIPTION

The TDA5140A is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a hard disk drive motor.

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	3.7	5	mA
V_{VMOT}	input voltage to the output driver stages	1.7	–	16	V
V_O	driver output voltage range; I_O = 0 mA	0.2	–	V_{VMOT} – 0.9	V
I_{LIM}	current limiting	0.6	0.85	1	A

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN and –AMP IN at 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5140A	18	DIL	plastic	SOT102
TDA5140AT	20	SOL	plastic	SOT163A

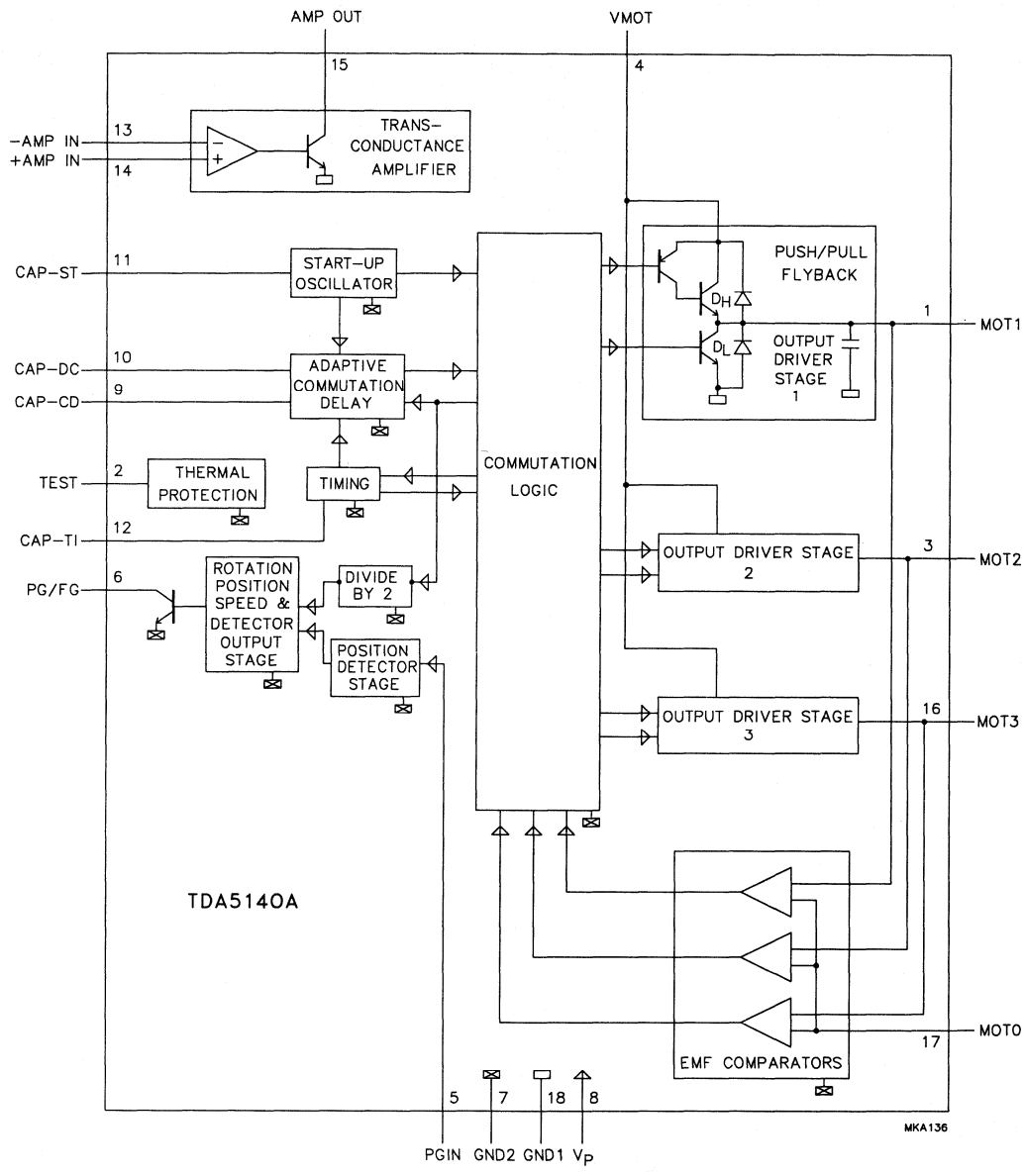


Fig.1 Block diagram (SOT102; DIL18).

PINNING

SYMBOL	PIN DIL18	PIN SO20	DESCRIPTION
MOT1	1	1	driver output 1
TEST	2	2	test input/output
n.c.		3	not connected
MOT2	3	4	driver output 2
VMOT	4	5	input voltage for the output driver stages
PG IN	5	6	position generator: input from the position detector sensor to the position detector stage (optional); only if an external position coil is used
PG/FG	6	7	position generator/frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
GND2	7	8	ground supply return for control circuits
V_P	8	9	positive supply voltage
CAP-CD	9	10	external capacitor connection for adaptive communication delay timing
CAP-DC	10	11	external capacitor connection for adaptive communication delay timing copy
CAP-ST	11	12	external capacitor connection for start-up oscillator
CAP-TI	12	13	external capacitor connection for timing
+AMP IN	13	14	non-inverting input of the transconductance amplifier
–AMP IN	14	15	inverting input of the transconductance amplifier
AMP OUT	15	16	transconductance amplifier output (open collector)
MOT3	16	17	driver output 3
n.c.		18	not connected
MOT0	17	19	input from the star point of the motor coils
GND1	18	20	ground (0 V) motor supply return for output stages

FUNCTIONAL DESCRIPTION

The TDA5140A offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5140A offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5140A offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Built-in flyback diodes
- Three phase full-wave drive
- High output current (0.85 A)
- Outputs protected by current limiting and thermal protection of each output transistor
- Low current consumption by adaptive base-drive
- Soft-switching pulse output for low radiation
- Accurate frequency generator (FG) by using the motor EMF
- Amplifier for external position generator (PG) signal
- Suitable for use with a wide tolerance, external PG sensor
- Built-in multiplexer that combines the internal FG and external PG signals on one pin for easy use with a controlling microprocessor
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive

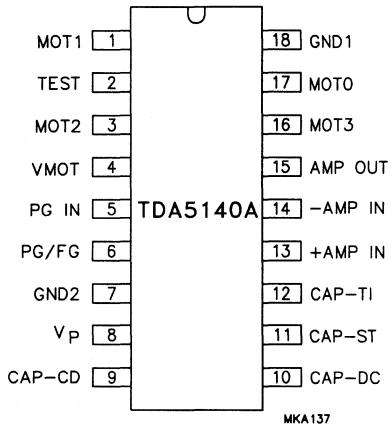


Fig.2 Pin configuration (SOT102; DIL18).

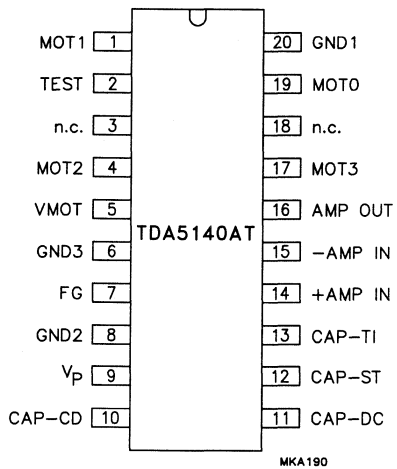


Fig.3 Pin configuration (SOT163A; SO20L).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	–	18	V
V_I	input voltage; all pins except VMOT: $V_I < 18$ V	–0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage	–0.5	17	V
V_O	output voltage AMP OUT and PG/FG	GND	V_P	V
V_O	output voltage MOT0, MOT1, MOT2 and MOT3	–1	$V_{VMOT} + V_D$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC	–	2.5	V
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
P_{tot}	total power dissipation	–	see Figs 4 and 5	
V_{es}	electrostatic voltage; see also handling	–	500	V

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 2. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin referenced to ground.

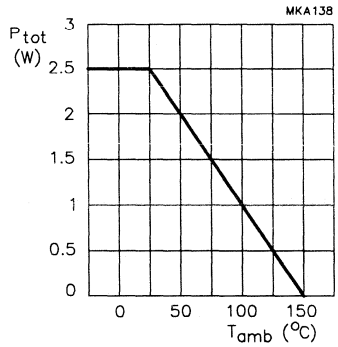


Fig.4 Power derating curve (SOT102; DIL18).

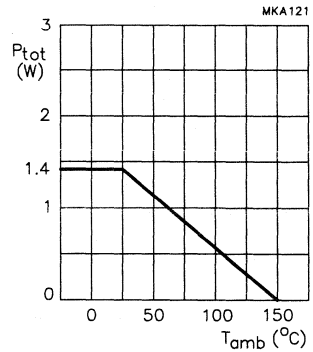


Fig.5 Power derating curve (SOT163A; SO20L).

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range	note 1	4	–	18	V
I_P	supply current range	note 2	–	3.7	5	mA
V_{VMOT}	input voltage to the driver output stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
MOT0 - centre tape						
V_I	input voltage range		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	0	µA
V_{CSW}	comparator switching level	note 3	±20	±30	±40	mV
ΔV_{CSW}	variation in comparator switching levels		–3	0	+3	mV
V_H	comparator input hysteresis		–	75	–	µV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MOT1, MOT2 and MOT3						
V_O	driver output voltage range	I_O = 100 mA	0.4	–	V_{VMOT} – 1.2	V
V_{DO}	drop-out voltage	I_O = 500 mA	–	2.1	–	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	lower transistor; V_{CE} = 6 V	0.6	0.85	1	A
t_{tr}	transition time switching output	V_{VMOT} = 14.5 V; see Fig.6	5	9	15	µs
V_{DHF}	diode forward voltage (diode D_H)	I_O = –500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	–1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	1	A
+AMP IN and -AMP IN						
V_{IAMP}	input voltage range		–0.3	–	V_P – 1.7	V
V_{IAMP}	differential mode voltage without 'latch-up'		–	–	$\pm V_P$	V
I_B	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{OFFSET}	input offset voltage		–	–	10	mV
I_I	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_{Omax}	maximum output voltage		18	–	–	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/µs
G_{tr}	transfer gain		0.3	–	–	S
PG IN						
V_I	input voltage		–0.3	–	5	V
I_B	input bias current		–	–	650	nA
R_I	input resistance		5	–	30	kΩ
V_{CWS}	comparator switching level		86	–	107	mV
V_H	comparator input hysteresis		–	±8	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PG/FG						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
V_{OHmax}	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	µs
	ratio of PG/FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%
t_{PL}	pulse width LOW	after a PG IN pulse	5	7	18	µs
CAP-ST						
I_I	output sink current		1.5	2.0	2.5	µA
I_O	output source current		–2.5	–2.0	–1.5	µA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_I	output sink current		–	28	–	µA
I_{OH}	HIGH level output source current		–	–57	–	µA
I_{OL}	LOW level output source current		–	–5	–	µA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-CD						
I_I	ouput sink current		10.6	16.2	22	µA
I_O	output source current		–5.3	–8.1	–11	µA
I_I/I_O	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V
CAP-DC						
I_I	output sink current		10.1	15.5	20.9	µA
I_O	output source current		–20.9	–15.5	–10.1	µA
I_I/I_O	ratio of sink to source current		0.9	1.025	1.15	

Notes to the characteristics

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P and I_O = 0 mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

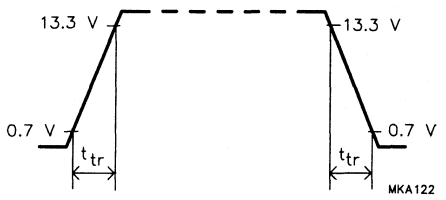
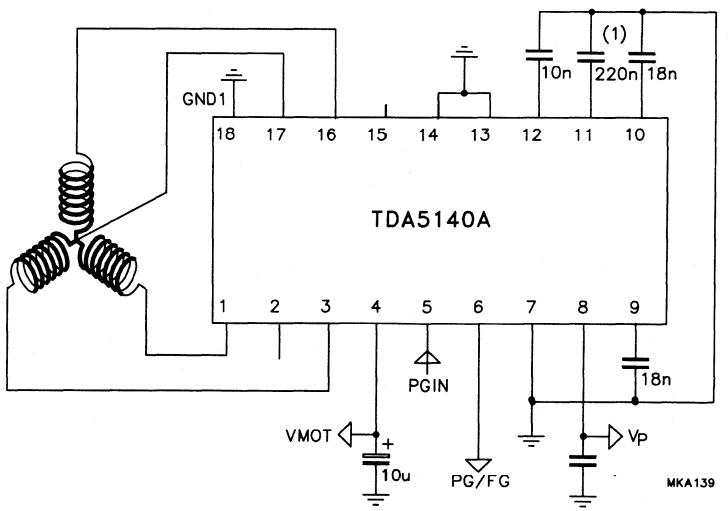


Fig.6 Output transition time measurement.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency

Fig.7 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.8)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The zero-crossings can be used to provide speed information such as the tacho signal FG. A VCR scanner also requires a PG phase sensor. This circuit has an interface for a simple pick-up coil. A multiplexer circuit is also provided to combine the FG and PG signals in time. This digital signal, FGPG, is available at an open-collector output.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5140A also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5140A is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented), possibility of using a pick-up coil without bias current.

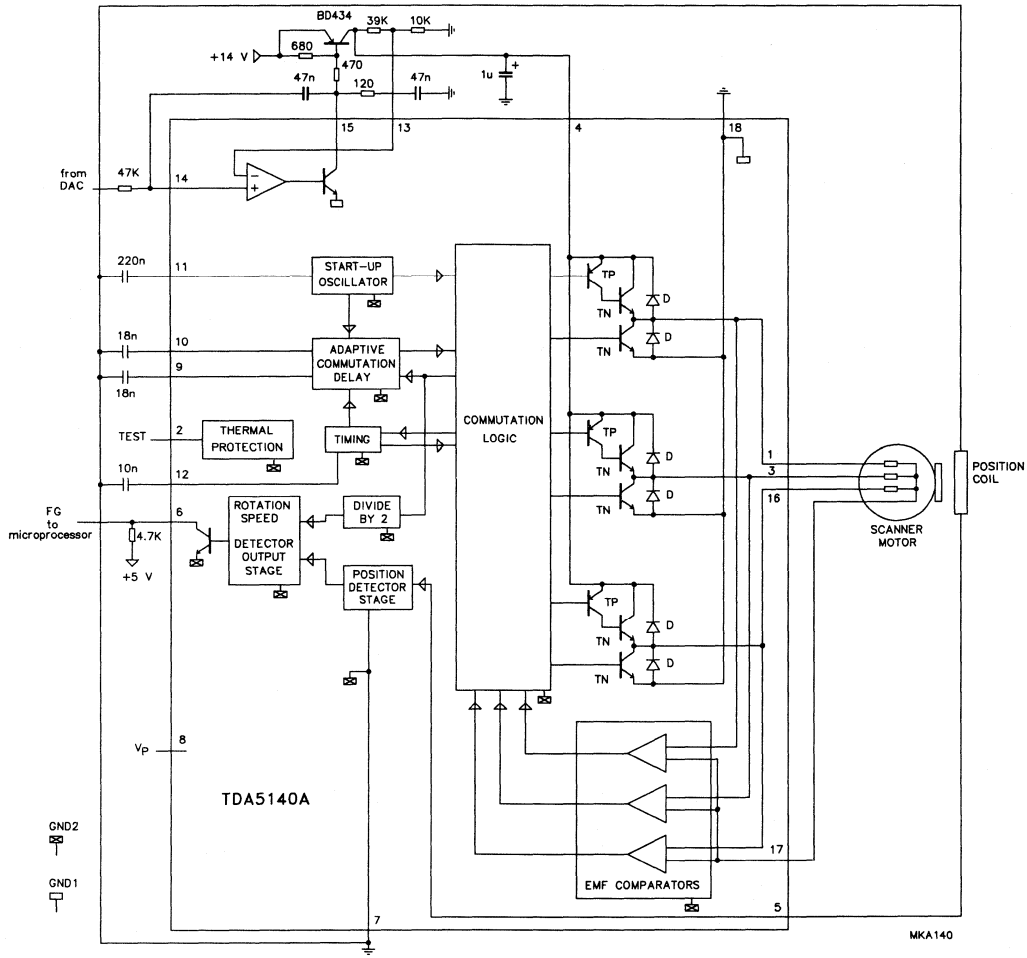


Fig.8 Typical application of the TDA5140A as a scanner driver, with use of OTA.

ADJUSTMENTS

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

t_{start} = (2.15 x C) s (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5140A will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$

where:
K_t = torque constant (N.m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J ($kg.m^2$)

Example: J = 72 x 10^{-6} $kg.m^2$, K = 25 x 10^{-3} N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF, (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

C = 8.1 x 10^{-6}/ f x 1.3 = $6231/f_{C1}$ (C in nF)

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA.

maximum delay = (0.076 x C) ms (witch C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

CAP-CD = 6231/400 = 15.6 (choose 18 nF)

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 μA. The same value can be chosen as for CAP-CD. Figure 9 illustrates typical voltage waveforms.

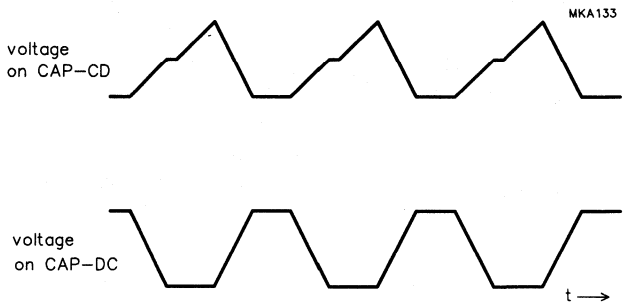


Fig.9 CAP-CD and CAP-DC voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 µA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 µA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 µA. The watchdog time is the time taken to charge the capacitor, with a current of 5 µA, from 0.3 to 2.2 V. The value of CAP-TI is given by:

$C = 5 \times 10^{-6} \times t_m/1.9 = 2.63\ t_m$(Cin nF; t in ms)

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$C = 2.63 \times 3.5 = 9.2$ (choose 10 nF)

Typical voltage waveforms are illustrated by Fig.10.

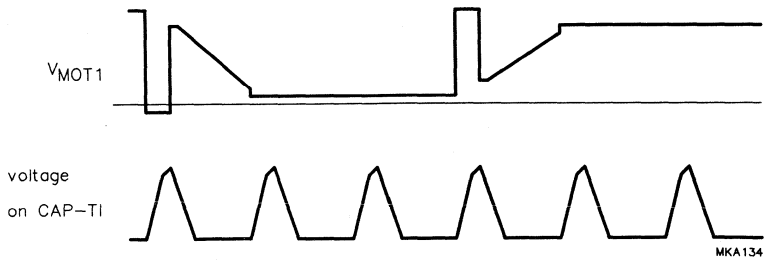


Fig.10 Typical CAP-TI and VMOT1 voltage waveforms in normal running mode.

Note to Fig.10

If the chosen value of CAP-TI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

THE EXTERNAL DAMPING COMPONENTS

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5140A. This distortion may influence the correct functioning of the TDA5140A, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 µs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 µs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp–8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 µF (use 1 µF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 µs. Eddy currents will also contribue to this phase shift. A shift of 20 µs corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or 0.1 mm on a VHS scanner drum.

OTHER DESIGN ASPECTS

There are other design aspects concerning the application of the TDA5140A besides the commutation function. They are:

- Generation of the tacho signal FG
- A built-in interface for a PG sensor
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability

FG SIGNAL

The FG signal is generated in the TDA5140A by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microprocessor.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 450 Hz.

PG SIGNAL

The accuracy of the PG signal in applications such as VCR must be high (phase information). This accuracy is obtained by combining the accurate FG signal with the PG signal by using a wide tolerance external PG sensor. The external PG signal (PG IN) is only used as an indicator to select a particular FG pulse. This pulse differs from the other FG pulses in that a short LOW-time of 15 µs after a HIGH-to-LOW transition. All other FG pulses have a 50% duty factor (see Fig.11).

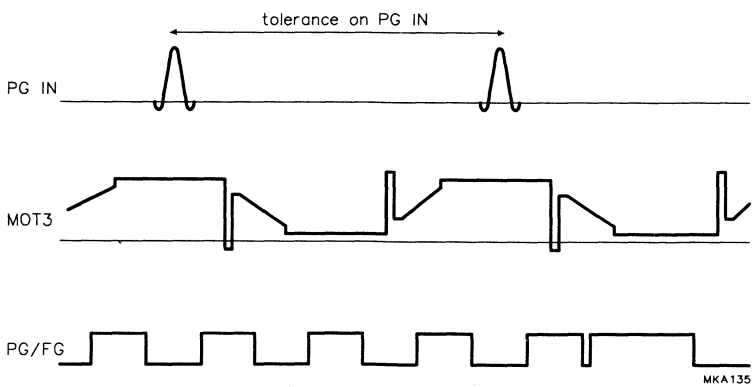


Fig.11 Timing and the FG and PGIN signals.

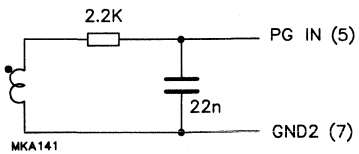


Fig.12 Pick-up coil as PG sensor.

The special PG pulse is derived from the negative-going zero-crossing from the MOT3 output (pin 16). The external PG signal (PG IN on pin 5) must sense a positive going (>80 mV) within 1.5 to 7.5 commutation periods before the negative-going zero-crossing in MOT3 (see Fig.11).

The voltage requirements of the PG IN input are shut that a cheap pick-up coil can be used as a sensor (see Fig.12).

Example: If p = 6, then one revolution contains 6 x 6 = 36 commutations. The tolerance is 6 periods, that is 60 degrees (mechanically) or 6.67 ms at 1500 rpm.

If a PG sensor is not used, the PG IN input must be grounded, this will result in a 50% duty factor FG signal.

The Operational Transconductance Amplifier (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier or as a level converter in a Switched Mode Power Supply (SMPS). The common mode input range includes ground (GND) and rises to $V_P - 1.7$ V. The high sinking current enables the OTA to drive a power transistor directly in an analog control amplifier or in a SMPS drive.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (pin 15) to the positive supply, a positive-going voltage is found when the non-inverting input (pin 13) is positive with respect to the inverting input (pin 14). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

Motor Control

DC motors can be controlled in an analog or digital (Pulse Width Modulation) manner, in either case the OTA may be used as follows:

- With analog control an external control transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.7).
- With digital or PWM control an external switching transistor is necessary. The OTA can make the level translation and drive the power transistor (see Fig.13).

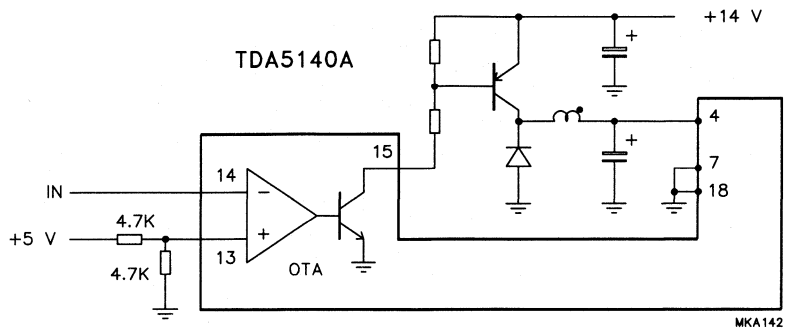


Fig.13 PWM drive of the output stages, OTA used as level converter.

A further aspect of motor control is current or voltage control; the TDA5140A is intended for voltage control applications. Both ground pins (7 and 18) must be connected externally. However the current from pin 7 can be considered as small and constant with respect to the current in the output stages. A resistor connected between pins 7, 18 and ground can be used for current control. Care must be taken that the voltage on pins 7, 18 does not disturb the (digital) FGPG signal too much (this signal is added to the digital signal).

An alternative method of voltage control is to increase the output impedance for a certain frequency, such as the commutation frequency; the circuit illustrated by Fig.7 uses this method. The low output impedance increases to approximately 10 Ω at 900 Hz. This circuit diagram is an example of the application of the TDA5140A with a VTR scanner for a PAL recorder running at 1500 rpm. The input signal is a PWM 5 V signal. The FGPG signal is read by a microprocessor that runs the servo control program.

A final aspect of motor control is braking; decreasing the speed to zero. No provisions have been made for this function. However, the generated voltage of the motor is rectified by the flyback diodes. If the voltage is loaded by a current drain on pin 5 then the motor will generate a braking torque that is proportional to the current.

Reliability

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

It is possible, that when braking (see previous section), the motor voltage (via the flyback diodes and the impedance on pin 5) may cause higher currents than allowed (>0.6 A). These currents must be limited externally.

Brushless DC motor drive circuit TDA5141/T/AT

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 1.8 A output current
  - low saturation voltage
  - built-in current limiter
  - soft-switching outputs
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Position pulse stage for phase-locked-loop control
- Transconductance amplifier for an external control transistor

APPLICATIONS

- General purpose spindle driver (e.g. HDD, drum motor)

DESCRIPTION

The TDA5141 is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a hard disk drive motor.

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	4.9	6.8	mA
V_{VMOT}	input voltage to the output driver stages	1.7	–	16	V
V_O	driver output voltage range; I_O = 0 mA	0.2	–	V_{VMOT} – 0.9	V
I_{LIM}	current limiting	1.3	1.8	2.3	A

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN and –AMP IN at 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5141	18	DIL	plastic	SOT102
TDA5141T	28	SOL	plastic	SOT136A
TDA5141AT	20	SOL	plastic	SOT163A

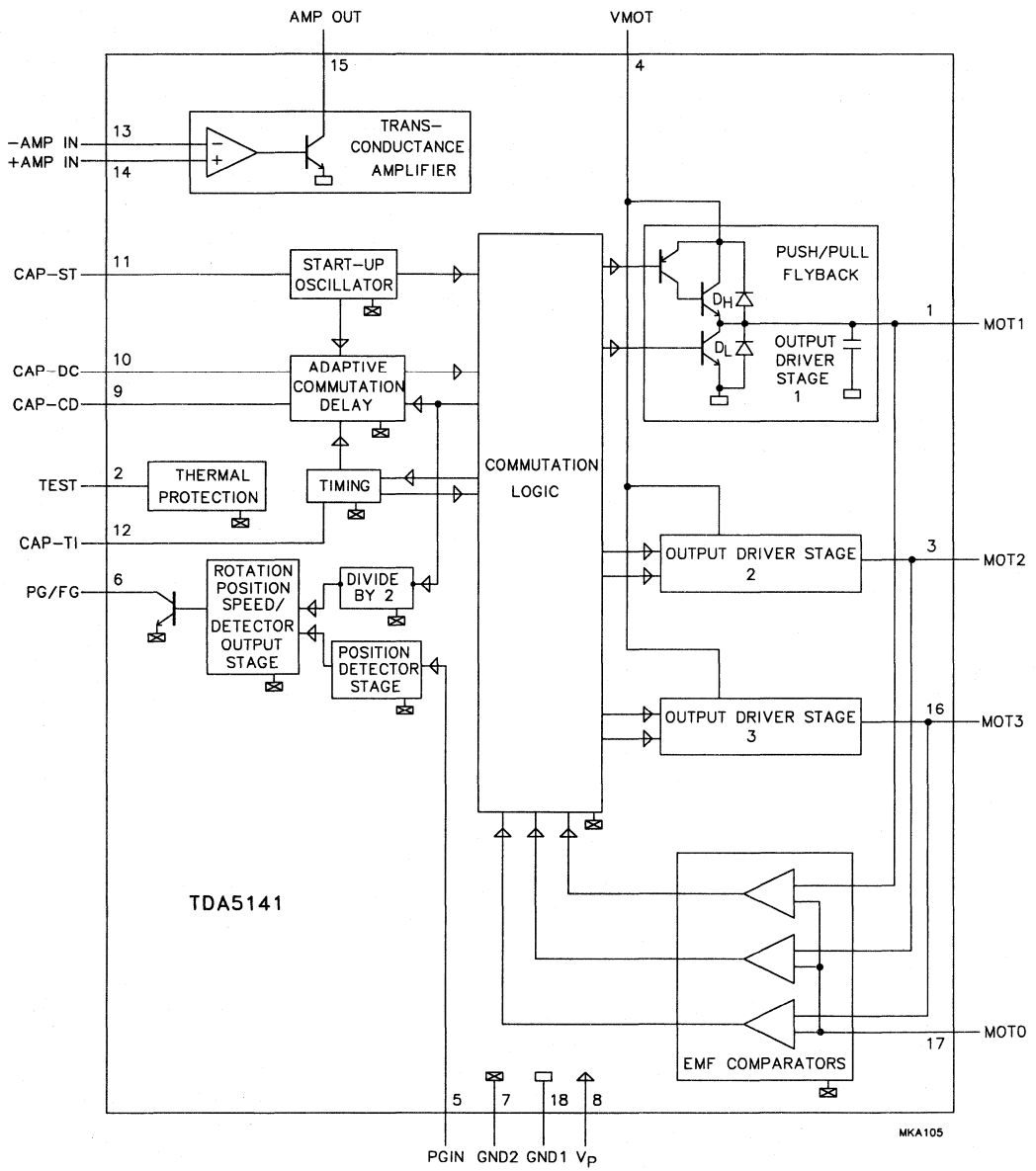


Fig.1 Block diagram (SOT102; DIL18).

PINNING

SYMBOL	PIN DIL18	PIN SO20	PIN SO28	DESCRIPTION
MOT1	1	1	1, 2	driver output 1
TEST	2	2	3	test input/output
n.c.		3	4	not connected
MOT2	3	4	5, 6	driver output 2
n.c.			7	not connected
VMOT	4	5	8, 9	input voltage for the output driver stages
PG IN	5	6	10	position generator: input from the position detector sensor to the position detector stage (optional); only if an external position coil is used
PG/FG	6	7	11	position generator/frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
GND2	7	8	12	ground supply return for control circuits
V_P	8	9	13	positive supply voltage
CAP-CD	9	10	14	external capacitor connection for adaptive communication delay timing
CAP-DC	10	11	15	external capacitor connection for adaptive communication delay timing copy
CAP-ST	11	12	16	external capacitor connection for start-up oscillator
CAP-TI	12	13	17	external capacitor connection for timing
+AMP IN	13	14	18	non-inverting input of the transconductance amplifier
–AMP IN	14	15	19	inverting input of the transconductance amplifier
AMP OUT	15	16	20	transconductance amplifier output (open collector)
n.c.			21, 22	not connected
MOT3	16	17	23, 24	driver output 3
n.c.		18	25	not connected
MOT0	17	19	26	input from the star point of the motor coils
GND1	18	20	27, 28	ground (0 V) motor supply return for output stages

FUNCTIONAL DESCRIPTION

The TDA5141 offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5141 offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5141 offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Built-in flyback diodes
- Three phase full-wave drive
- High output current (1.8 A)
- Outputs protected by current limiting and thermal protection of each output transistor
- Low current consumption by adaptive base-drive
- Soft-switching pulse output for low radiation
- Accurate frequency generator (FG) by using the motor EMF
- Amplifier for external position generator (PG) signal

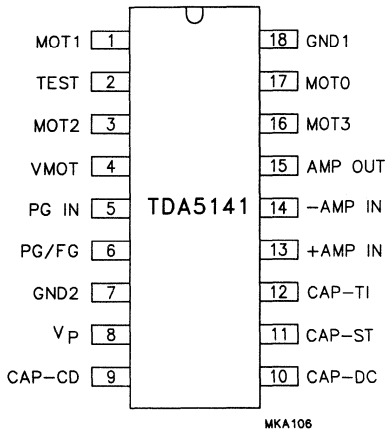


Fig.2 Pin configuration (SOT102; DIL18).

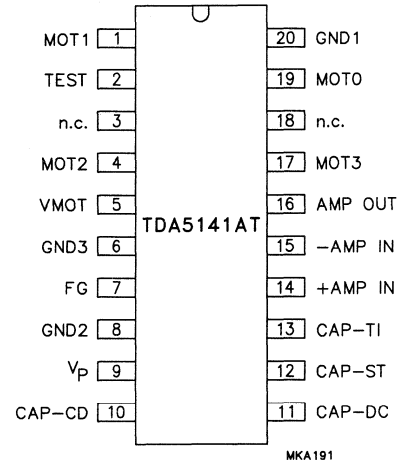


Fig.3 Pin configuration (SOT163A; SO20L).

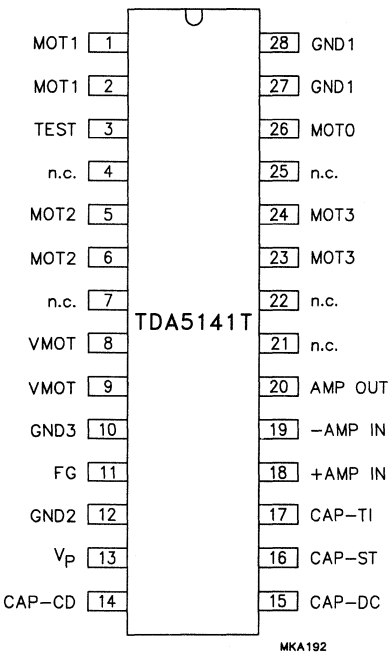


Fig.4 Pin configuration (SOT136A; SO28L).

- Suitable for use with a wide tolerance, external PG sensor
- Built-in multiplexer that combines the internal FG and external PG signals on one pin for easy use with a controlling microprocessor
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	–	18	V
V_I	input voltage; all pins except VMOT: $V_I < 18$ V	–0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage	–0.5	17	V
V_O	output voltage AMP OUT and PG/FG	GND	V_P	V
V_O	output voltage MOT0, MOT1, MOT2 and MOT3	–1	$V_{VMOT} + V_D$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC	–	2.5	V
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
P_{tot}	total power dissipation	–	see Figs 5, 6 and 7	
V_{es}	electrostatic voltage; see also handling	–	500	V

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 2. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin refernced to ground.

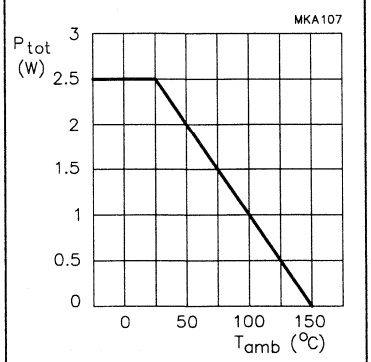


Fig.5 Power derating curve (SOT102; DIL18).

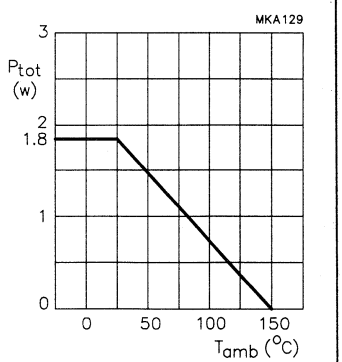


Fig.6 Power derating curve (SOT163A; SO20L).

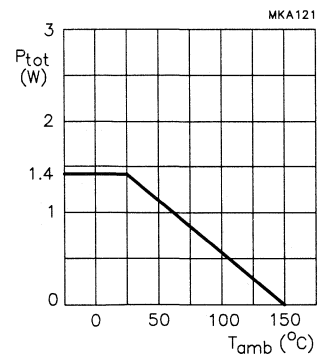


Fig.7 Power derating curve (SOT136A; SO28L).

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range	note 1	4	–	18	V
I_P	supply current range	note 2	–	4.9	6.8	mA
V_{VMOT}	input voltage to the driver output stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
MOT0 - centre tape						
V_I	input voltage range		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	0	µA
V_{CSW}	comparator switching level	note 3	±20	±30	±40	mV
ΔV_{CSW}	variation in comparator switching levels		–3	0	+3	mV
V_H	comparator input hysteresis		–	75	–	µV
MOT1, MOT2 and MOT3						
V_O	driver output voltage range	I_O = 100 mA	0.4	–	V_{VMOT} – 1.2	V
V_{DO}	drop-out voltage	I_O = 1000 mA	–	1.6	–	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	lower transistor; V_{CE} = 6 V	1.3	1.8	2.3	A
t_{tr}	transition time switching output	V_{VMOT} = 14.5 V;see Fig.8	5	9	15	µs
V_{DHF}	diode forward voltage (diode D_H)	I_O = –500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	–1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	1.8	A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
+AMP IN and -AMP IN						
V_{IAMP}	input voltage range		−0.3	–	$V_P - 1.7$	V
V_{IAMP}	differential mode voltage without 'latch-up'		–	–	$\pm V_P$	V
I_B	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{OFFSET}	input offset voltage		–	–	10	mV
I_I	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_{Omax}	maximum output voltage		–	–	18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/µs
G_{tr}	transfer gain		0.3	–	–	S
PG IN						
V_I	input voltage		−0.3	–	$V_P - 1.7$	V
I_B	input bias current		–	–	650	nA
R_I	input resistance		5	–	30	kΩ
V_{CWS}	comparator switching level		86	–	107	mV
V_H	comparator input hysteresis		–	±8	–	mV
PG/FG						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
V_{OHmax}	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	µs
	ratio of PG/FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%
t_{PL}	pulse width LOW	after a PG IN pulse	5	7	30	µs
CAP-ST						
I_I	output sink current		1.5	2.0	2.5	µA
I_O	output source current		−2.5	−2.0	−1.5	µA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_I	output sink current		–	28	–	µA
I_{OH}	HIGH level output source current		–	−57	–	µA
I_{OL}	LOW level output source current		–	−5	–	µA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CAP-CD						
I_I	ouput sink current		10.6	16.2	22	µA
I_O	output source current		–5.3	–8.1	–11	µA
I_I/I_O	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		–	875	–	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V
CAP-DC						
I_I	output sink current		10.1	15.5	20.9	µA
I_O	output source current		–20.9	–15.5	–10.1	µA
I_I/I_O	ratio of sink to source current		0.9	1.025	1.15	

Notes to the characteristics

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P and $I_O = 0$ mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

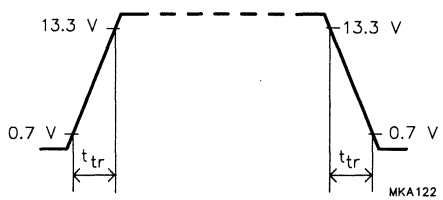
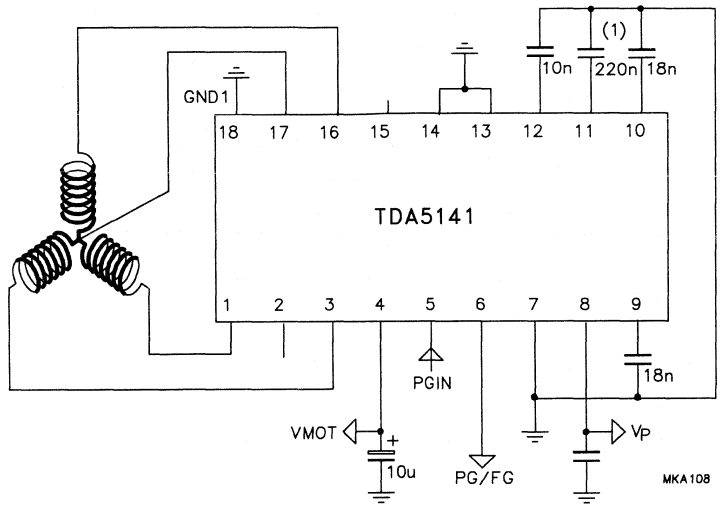


Fig.8 Output transition time measurement.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency

Fig.9 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.10)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The zero-crossings can be used to provide speed information such as the tacho signal FG. A VCR scanner also requires a PG phase sensor. This circuit has an interface for a simple pick-up coil. A multiplexer circuit is also provided to combine the FG and PG signals in time. This digital signal, FGPG, is available at an open-collector output.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5141 also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5141 is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented), possibility of using a pick-up coil without bias current.

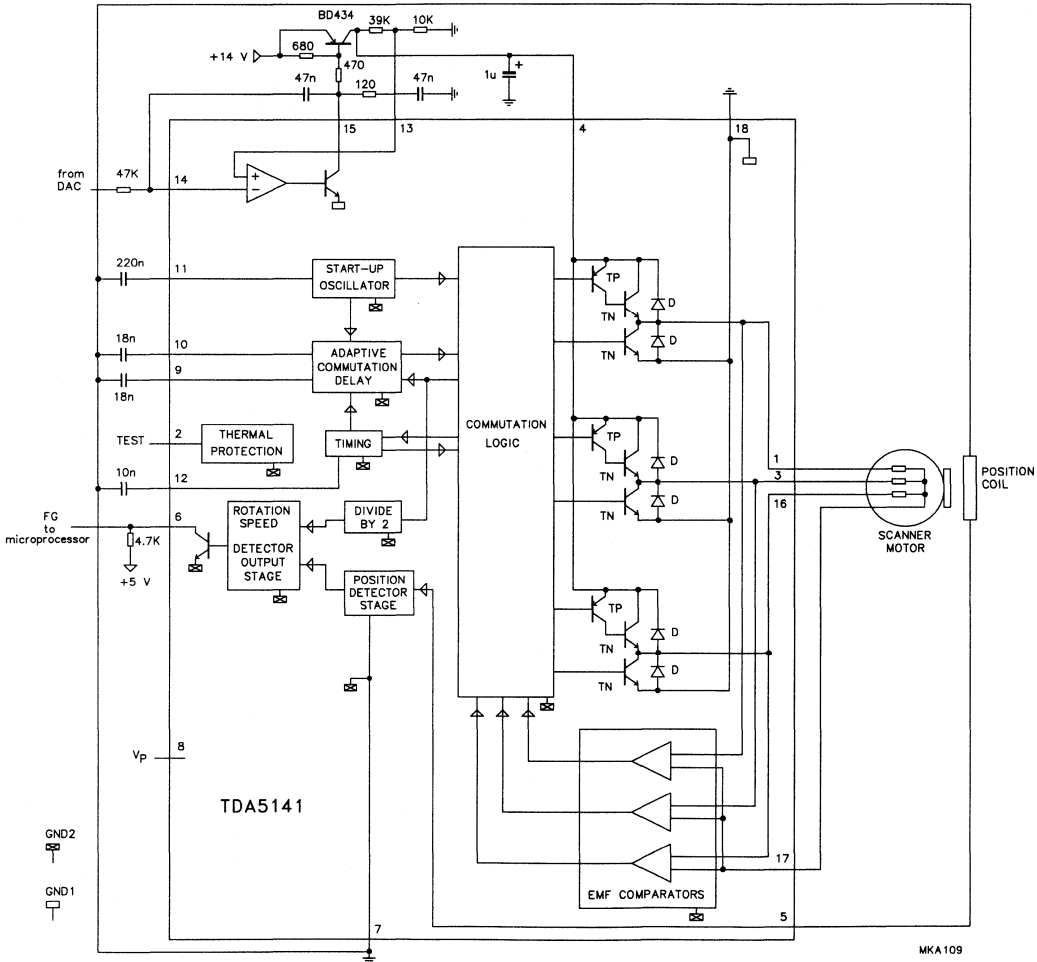


Fig.10 Typical application of the TDA5141 as a scanner driver, with use of OTA.

ADJUSTMENTS

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

$t_{start} = (2.15 \times C)$ s (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5141 will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$

where:
K_t = torque constant (N.m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J ($kg.m^2$)

Example: $J = 72 \times 10^{-6}$ $kg.m^2$, $K = 25 \times 10^{-3}$ N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF, (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

$C = 8.1 \times 10^{-6}/ f \times 1.3 = 6231/f_{C1}$ (C in nF)

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA.

maximum delay = (0.076 x C) ms (witch C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

CAP-CD = 6231/400 = 15.6 (choose 18 nF)

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 μA. The same value can be chosen as for CAP-CD. Figure 11 illustrates typical voltage waveforms.

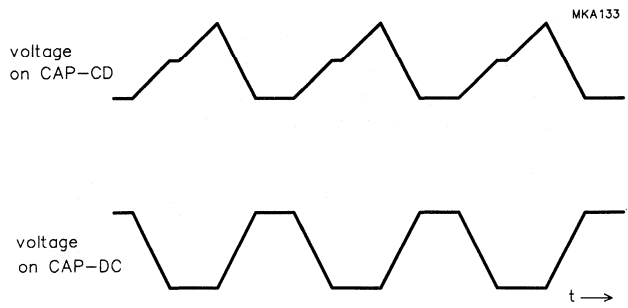


Fig.11 CAP-CD and CAP-DC voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 µA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 µA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 µA. The watchdog time is the time taken to charge the capacitor, with a current of 5 µA, from 0.3 to 2.2 V. The value of CAP-TI is given by:

$C = 5 \times 10^{-6} \times t_m/1.9 = 2.63\ t_m$ (C in nF; t in ms)

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$C = 2.63 \times 3.5 = 9.2$ (choose 10 nF)

Typical voltage waveforms are illustrated by Fig.12.

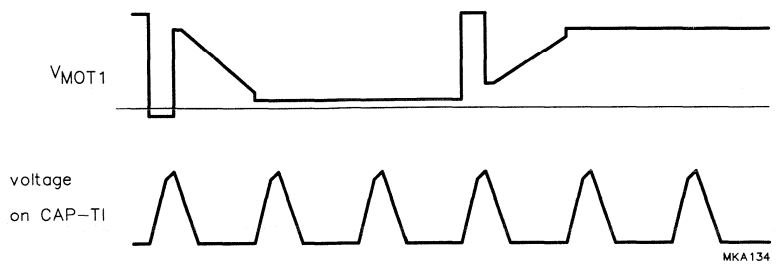


Fig.12 Typical CAP-TI and VMOT1 voltage waveforms in normal running mode.

Note to Fig.12

If the chosen value of CAP-TI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

THE EXTERNAL DAMPING COMPONENTS

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5141. This distortion may influence the correct functioning of the TDA5141, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 µs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 µs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp–8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 µF (use 1 µF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 µs. Eddy currents will also contribue to this phase shift. A shift of 20 µs corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or 0.1 mm on a VHS scanner drum.

OTHER DESIGN ASPECTS

There are other design aspects concerning the application of the TDA5141 besides the commutation function. They are:

- Generation of the tacho signal FG
- A built-in interface for a PG sensor
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability

FG SIGNAL

The FG signal is generated in the TDA5141 by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microprocessor.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 450 Hz.

PG SIGNAL

The accuracy of the PG signal in applications such as VCR must be high (phase information). This accuracy is obtained by combining the accurate FG signal with the PG signal by using a wide tolerance external PG sensor. The external PG signal (PG IN) is only used as an indicator to select a particular FG pulse. This pulse differs from the other FG pulses in that a short LOW-time of 15 µs after a HIGH-to-LOW transition. All other FG pulses have a 50% duty factor (see Fig.13).

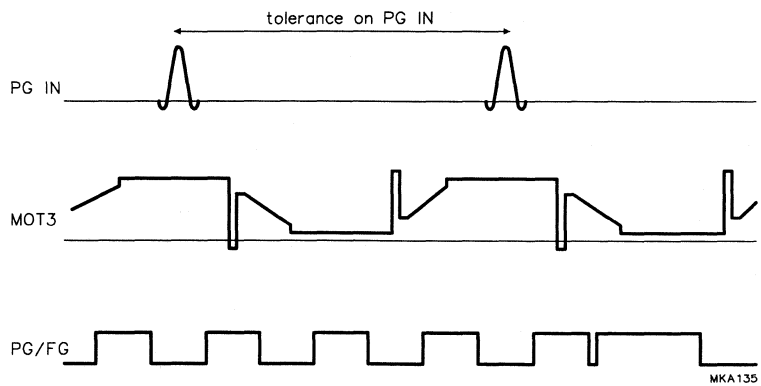


Fig.13 Timing and the FG and PGIN signals.

The special PG pulse is derived from the negative-going zero-crossing from the MOT3 output (pin 16). The external PG signal (PG IN on pin 5) must sense a positive going (>80 mV) within 1.5 to 7.5 commutation periods before the negative-going zero-crossing in MOT3 (see Fig.13).

The voltage requirements of the PG IN input are shut that a cheap pick-up coil can be used as a sensor (see Fig.14).

Example: If p = 6, then one revolution contains 6 x 6 = 36 commutations. The tolerance is 6 periods, that is 60 degrees (mechanically) or 6.67 ms at 1500 rpm.

If a PG sensor is not used, the PG IN input must be grounded, this will result in a 50% duty factor FG signal.

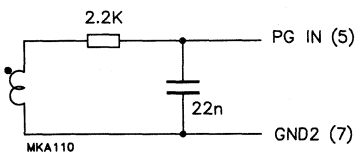


Fig.14 Pick-up coil as PG sensor.

The Operational Transconductance Amplifier (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier or as a level converter in a Switched Mode Power Supply (SMPS). The common mode input range includes ground (GND) and rises to $V_P - 1.7$ V. The high sinking current enables the OTA to drive a power transistor directly in an analog control amplifier or in a SMPS drive.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (pin 15) to the positive supply, a positive-going voltage is found when the non-inverting input (pin 13) is positive with respect to the inverting input (pin 14). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

Motor Control

DC motors can be controlled in an analog or digital (Pulse Width Modulation) manner, in either case the OTA may be used as follows:

- With analog control an external control transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.10).
- With digital or PWM control an external switching transistor is necessary. The OTA can make the level translation and drive the power transistor (see Fig.15).

A further aspect of motor control is current or voltage control; the TDA5141 is intended for voltage control applications. Both ground pins (7 and 18) must be connected externally. However the current from pin 7 can be considered as small and constant with respect to the current in the output stages. A resistor connected between pins 7, 18 and ground can be used for current control. Care must be taken that the voltage on pins 7, 18 does not disturb the (digital) FGPG signal too much (this signal is added to the digital signal).

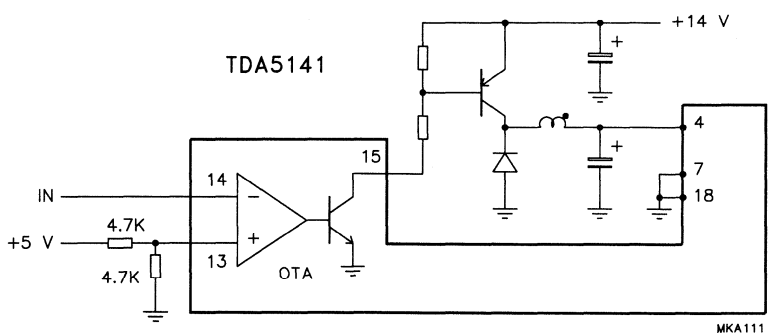


Fig.15 PWM drive of the output stages, OTA used as level converter.

An alternative method of voltage control is to increase the output impedance for a certain frequency, such as the commutation frequency; the circuit illustrated by Fig.10 uses this method. The low output impedance increases to approximately 10 Ω at 900 Hz. This circuit diagram is an example of the application of the TDA5141 with a VTR scanner for a PAL recorder running at 1500 rpm. The input signal is a PWM 5 V signal. The FGPG signal is read by a microprocessor that runs the servo control program.

A final aspect of motor control is braking; decreasing the speed to zero. No provisions have been made for this function. However, the generated voltage of the motor is rectified by the flyback diodes. If the voltage is loaded by a current drain on pin 5 then the motor will generate a braking torque that is proportional to the current.

Reliability

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

It is possible, that when braking (see previous section), the motor voltage (via the flyback diodes and the impedance on pin 5) may cause higher currents than allowed (>0.6 A). These currents must be limited externally.

Brushless DC motor drive circuit TDA5142T

FEATURES

- Full-wave commutation without position sensors
- Built-in start-up circuitry
- Six outputs that can drive three external transistor pairs:
  - 0.15 A output current
  - low saturation voltage
  - built-in current limiter
- Thermal protection
- Tacho output without extra sensor
- Transconductance amplifier for an external control transistor
- Motor brake facility

APPLICATIONS

- General purpose spindle driver (e.g. HDD, fan motor)

DESCRIPTION

The TDA5142T is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for power-drum motors (hard disk drives, tape drives, fan motors).

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	4.9	6.25	mA
V_{VMOT}	input voltage to the output driver stages	3	–	18	V
V_O	driver output voltage range;				
	I_O = 0 mA	0.2	–	–	V
	OUT-NA, NB, NC	–	–	V_{VMOT}	V
	OUT-PA, PB, PC	0.2	–	– 0.9	V
				–	

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; all other inputs at 0 V; all outputs at V_P and I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5142T	24	SOL	plastic	SOT137A

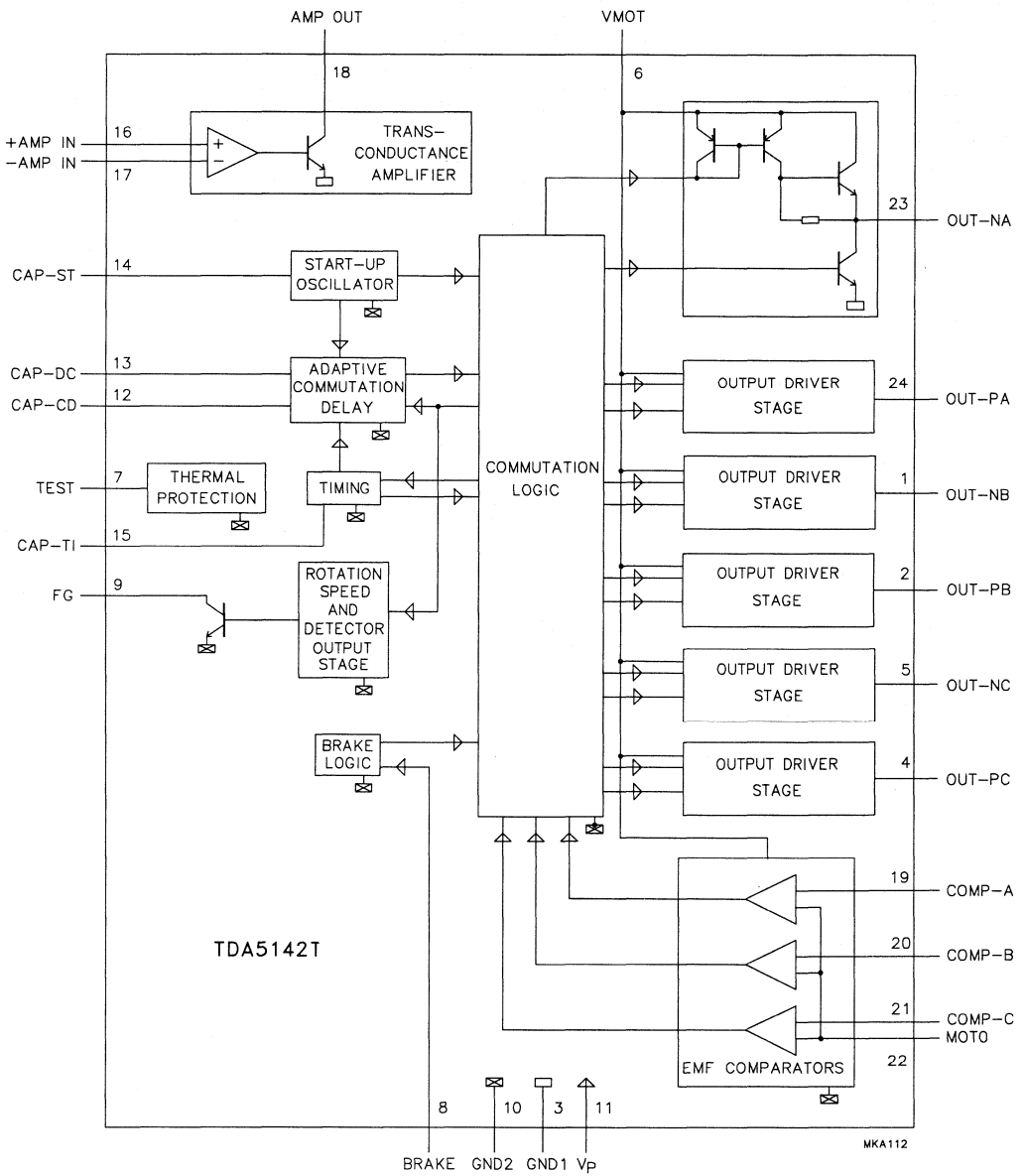


Fig.1 Block diagram.

Brushless DC motor drive circuit TDA5142T

PINNING

SYMBOL	PIN	DESCRIPTION
OUT-NB	1	driver output for driving the n-channel power FET or power NPN
OUT-PB	2	driver output for driving the p-channel power FET or power PNP
GND1	3	ground (0 V) motor supply return for output stages
OUT-PC	4	driver output for driving the p-channel power FET or power PNP
OUT-NC	5	driver output for driving the n-channel power FET or power NPN
VMOT	6	input voltage for the output driver stages
TEST	7	test input/output
BRAKE	8	brake input command
FG	9	output of the rotation speed position detector stage
GND2	10	ground supply return for control circuits
V_P	11	positive supply voltage
CAP-CD	12	external capacitor connection for adaptive communication delay timing
CAP-DC	13	external capacitor connection for adaptive communication delay timing copy
CAP-ST	14	external capacitor connection for start-up oscillator
CAP-TI	15	external capacitor connection for timing
+AMP IN	16	non-inverting input of the transconductance amplifier
–AMP IN	17	inverting input of the transconductance amplifier
AMP OUT	18	transconductance amplifier output (open collector)
COMP-A	19	input of comparator corresponding to output A
COMP-B	20	input of comparator corresponding to output B
COMP-C	21	input of comparator corresponding to output C
MOT0	22	input from the star point of the motor coils
OUT-NA	23	driver output for driving the n-channel power FET or power NPN
OUT-PA	24	driver output for driving the p-channel power FET or power PNP

FUNCTIONAL DESCRIPTION

The TDA5142T offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5142T offers protected outputs capable of driving external power FETs or bipolar power transistors. It can easily be adapted for different motors and applications. The TDA5142T offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Six output drivers
- Maximum output current (0.15 A)
- Outputs protected by current limiting and thermal protection
- Low current consumption
- Accurate frequency generator (FG) by using the motor EMF
- Brake function
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive

Brushless DC motor drive circuit TDA5142T

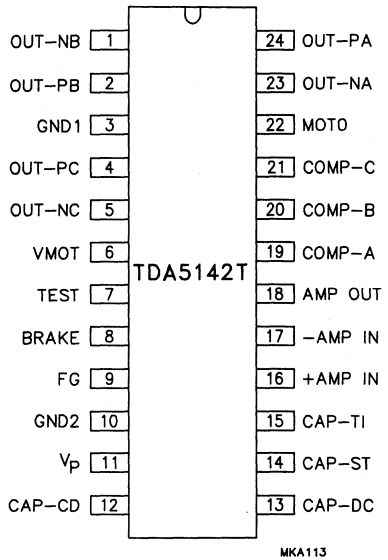


Fig.2 Pin configuration.

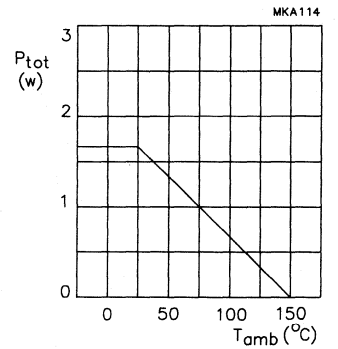


Fig.3 Power derating curve.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	4	18	V
V_I	input voltage; all pins except VMOT: V_I < 18 V	–0.3	V_P + 0.5	V
V_{VMOT}	VMOT input voltage	3	18	V
V_O	output voltage FG AMP OUT	 GND –	 V_P 18	 V V
V_O	output voltage OUT-NA, NB, NC OUT-PA, PB, PC	 – 0.2	 V_{VMOT} – 0.9 –	 V V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC	–	2.5	V
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
P_{tot}	total power dissipation	–	see Fig. 3	
V_{es}	electrostatic voltage; see also handling	–	500	V

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 2. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin referenced to ground.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range	note 1	4	–	18	V
I_P	supply current range	note 2	–	4.9	6.25	mA
V_{VMOT}	input voltage to the driver output stages	see Fig.1	3	–	18	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
COMP-A, COM-B, COMP-C and MOT0						
V_I	input voltage range		−0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	−10	–	0	µA
V_{CSW}	comparator switching level	note 3	±20	±25	±30	mV
ΔV_{CSW}	variation in comparator switching levels		−3	0	+3	mV
V_H	comparator input hysteresis		–	75	–	µV
OUT-N(A,B,C) and OUT-P(A,B,C)						
V_{OH-N}	driver output voltage range; n-channel, upper transistor	I_O = −100 mA	−1.2	–	–	V
V_{OL-N}	driver output voltage range; n-channel, lower transistor	I_O = 10 mA	–	–	0.45	V
V_{OH-P}	driver output voltage range; p-channel, upper transistor	I_O = −10 mA	−1.2	–	–	V
V_{OL-P}	driver output voltage range; p-channel, lower transistor	I_O = 100 mA	–	–	0.45	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = −100 mA	–	–	180	mV
I_{LIM}	current limiting	lower transistor; V_{CE} = 6 V	–	150	–	mA
VMOT						
V_{VMOT}	input voltage range		3	–	18	V

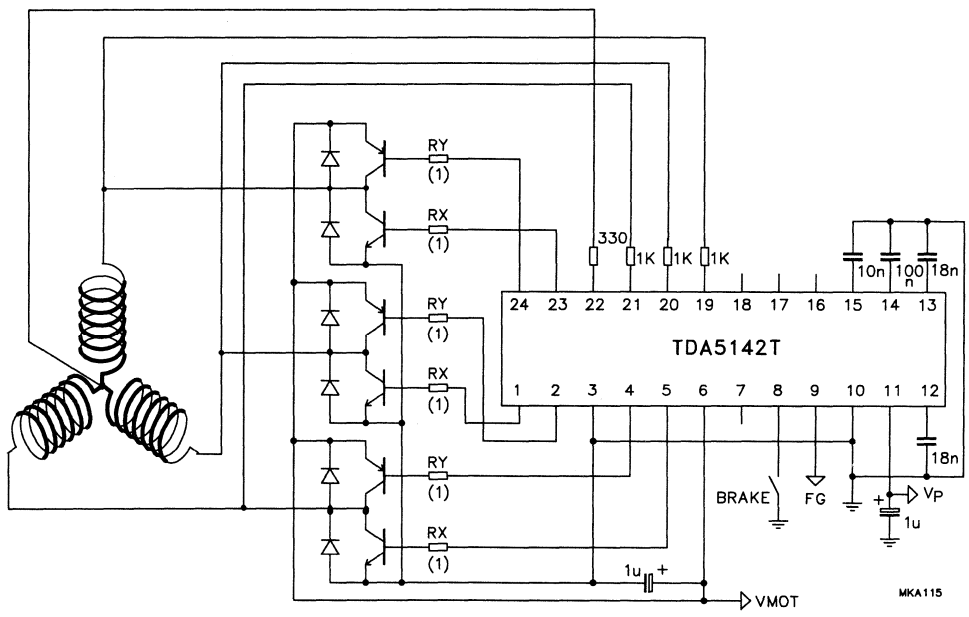
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
+AMP IN and -AMP IN						
V_{IAMP}	input voltage range		−0.3	–	$V_P - 1.7$	V
V_{IAMP}	differential mode voltage without 'latch-up'		–	–	$\pm V_P$	V
I_B	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{OFFSET}	input offset voltage		–	–	10	mV
AMP OUT						
I_I	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_{Omax}	maximum output voltage		–	–	18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	40	–	–	mA/µs
G_{tr}	transfer gain		0.3	–	–	S
BRAKE						
V_{BM}	break-mode voltage at pin 8	$4 < V_P < 18$ V	–	–	2.3	V
V_{DBM}	disable break-mode voltage	$4 < V_P < 18$ V	2.7	–	–	V
I_{BC}	brake current at pin 8		–	−20	30	µA
I_{NM}	normal-mode current at pin 8		–	0	–	µA
FG						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
V_{OHmax}	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	µs
	ratio of FG frequency and commutation frequency		–	1	–	
δ	duty factor		–	50	–	%
CAP-ST						
I_I	output sink current		1.5	2.0	2.5	µA
I_O	output source current		−2.5	−2.0	−1.5	µA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_I	output sink current		–	28	–	µA
I_{OH}	HIGH level output source current		–	−57	–	µA
I_{OL}	LOW level output source current		–	−5	–	µA
V_{SWL}	LOW level switching voltage		–	0.2	–	V
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CAP-CD						
I_I	ouput sink current		10.6	16.2	22	µA
I_O	output source current		–5.3	–8.1	–11	µA
I_I/I_O	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		–	875	–	mV
V_{IH}	HIGH level input voltage		2.3	–	2.5	V
CAP-DC						
I_I	output sink current		10.1	15.5	20.9	µA
I_O	output source current		–20.9	–15.5	–10.1	µA
I_I/I_O	ratio of sink to source current		0.9	1.025	1.15	

Notes to the characteristics

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P and $I_O = 0$ mA.
3. Switching levels with respect to driver outputs OUT-NA, NB, NC and OUT-PA, PB, PC.

APPLICATION INFORMATION



(1) RX = RY > 8 (VMOT – 1.5)

Fig.4 Application diagram without use of the operational transconductance amplifier (OTA) with bipolar power transistors.

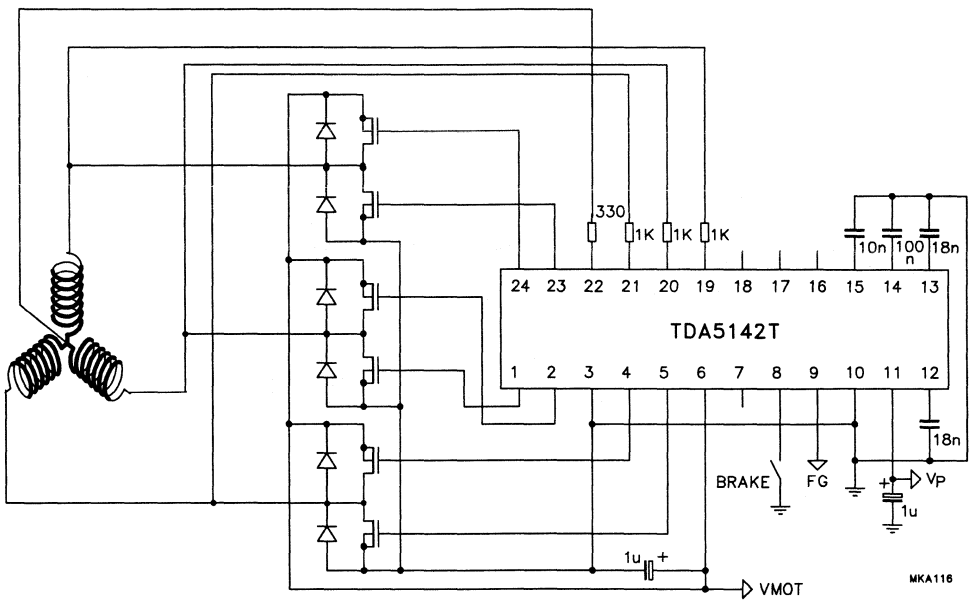


Fig.5 Application diagram without use of the operational transconductance amplifier (OTA) with MOS power transistors.

Introduction (see Fig.6)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

The driver output stages are also protected by a current limiting circuit and by thermal protection.

The zero-crossings can be used to provide speed information such as the tacho signal FG.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5142T also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5142T is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented).

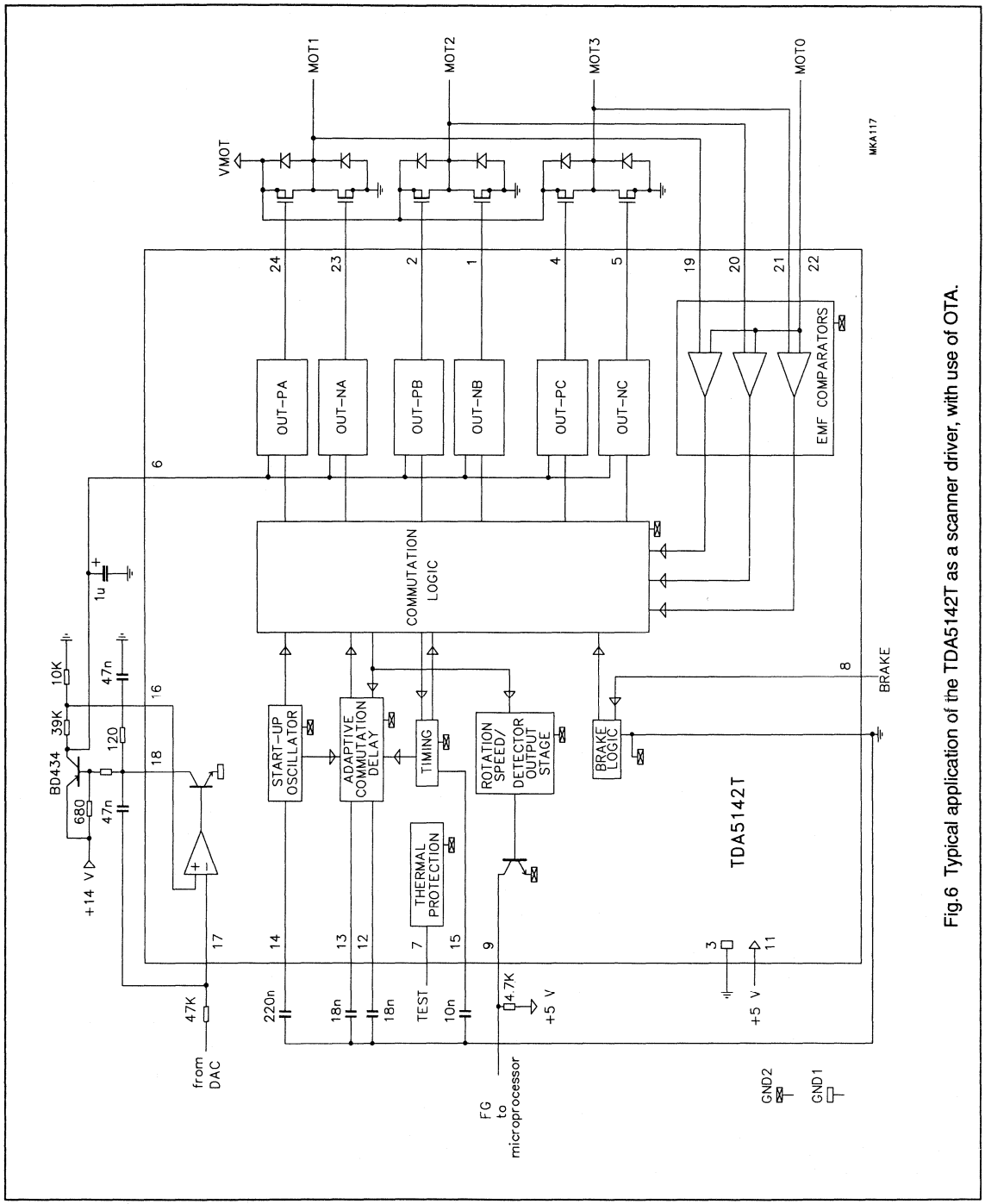


Fig.6 Typical application of the TDA5142T as a scanner driver, with use of OTA.

ADJUSTMENTS

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

t_{start} = (2.15 x C) s (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5142T will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$

where:
K_t = torque constant (N.m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J ($kg.m^2$)

Example: J = 72 x 10^{-6} $kg.m^2$, K = 25 x 10^{-3} N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF, (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

C = 8.1 x 10^{-6}/ f x 1.3 = 6231/f_{C1} (C in nF)

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 20 μA.

maximum delay = (0.076 x C) ms (witch C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

CAP-CD = 6231/400 = 15.6 (choose 15 nF)

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 μA. The same value can be chosen as for CAP-CD. Figure 7 illustrates typical voltage waveforms.

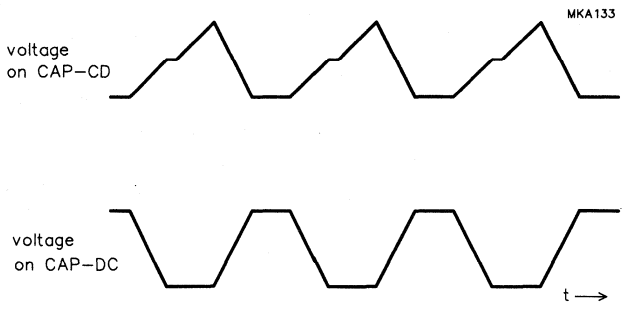


Fig.7 CAP-CD and CAP-DC voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 µA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 µA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 µA. The watchdog time is the time taken to charge the capacitor, with a current of 5 µA, from 0.3 to 2.2 V. The value of CAP-TI is given by:

$C = 5 \times 10^{-6} \times t_m/1.9 = 2.63\ t_m$ (C in nF; t in ms)

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$C = 2.63 \times 3.5 = 9.2$ (choose 10 nF)

Typical voltage waveforms are illustrated by Fig.8.

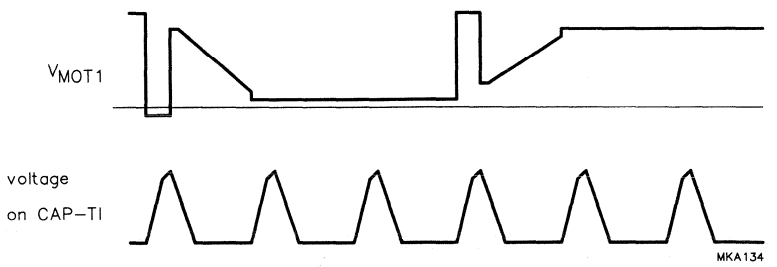


Fig.8 Typical CAP-TI and VMOT1 voltage waveforms in normal running mode.

Note to Fig.8

If the chosen value of CAP-TI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

THE EXTERNAL DAMPING COMPONENTS

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5142T. This distortion may influence the correct functioning of the TDA5142T, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 µs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 µs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp–8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 µF (use 1 µF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 µs. Eddy currents will also contribue to this phase shift. A shift of 20 µs corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or 0.1 mm on a VHS scanner drum.

OTHER DESIGN ASPECTS

There are other design aspects concerning the application of the TDA5142T besides the commutation function. They are:

- Generation of the tacho signal FG
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability

FG SIGNAL

The FG signal is generated in the TDA5142T by using the zero-crossing of the motor EMF from the three motor windings and the commutation signal.

Output FG switches from HIGH-to-LOW on all zero crossings and from LOW-to-HIGH on all commutations. Output FG can source typically 75 μA and sink more than 3 mA.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 900 Hz.

The Operational Transconductance Amplifier (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier or as a level converter in a Switched Mode Power Supply (SMPS). The common mode input range includes ground (GND) and rises to V_P – 1.7 V. The high sinking current enables the OTA to drive a power transistor directly in an analog control amplifier or in a SMPS drive.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (pin 18) to the positive supply, a positive-going voltage is found when the non-inverting input (pin 16) is positive with respect to the inverting input (pin 17). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

Motor Control

DC motors can be controlled in an analog or digital (Pulse Width Modulation) manner, in either case the OTA may be used as follows:

- With analog control an external control transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.6).
- With digital or PWM control an external switching transistor is necessary. The OTA can make the level translation and drive the power transistor (see Fig.9).

A further aspect of motor control is current or voltage control; the TDA5142T is intended for voltage control applications. Both ground pins (3 and 10) must be connected externally. However the current from pin 10 can be considered as small and constant with respect to the current in the output stages. A resistor connected between pins 3, 10 and ground can be used for current control. Care must be taken that the voltage on pins 3, 10 does not disturb the (digital) FG signal too much (this signal is added to the digital signal).

An alternative method of voltage control is to increase the output impedance for a certain frequency, such as the commutation frequency; the circuit illustrated by Fig.6 uses this method. The low output impedance increases to approximately 10 Ω at 900 Hz. This circuit diagram is an example of the application of the TDA5142T with a VTR scanner for a PAL recorder running at 1500 rpm. The input signal is a PWM 5 V signal. The FG signal is read by a microprocessor that runs the servo control program.

A final aspect of motor control is braking; decreasing the speed to zero. No provisions have been made for this function:

- If the voltage on pin 8 is less than 2.3 V the motor brakes.
- If pin 8 is floating or if the voltage on pin 8 is greater than 2.7 V the motor runs normally.

Reliability

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection is achived:
  the transistors are switched off when the local temperature becomes too high.

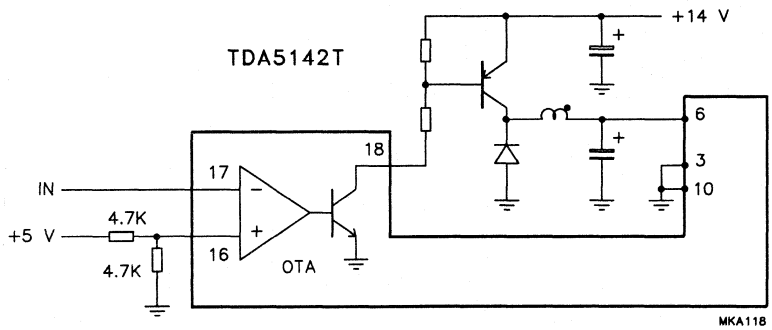


Fig.9 PWM drive of the output stages, OTA used as level converter.

Brushless DC motor drive circuit TDA5143T

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 0.85 A output current
  - low saturation voltage
  - built-in current limiter
  - soft-switching outputs
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Transconductance amplifier for an external control transistor

APPLICATIONS

- General purpose spindle driver (e.g. for HDD)

DESCRIPTION

The TDA5143 is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a hard disk drive motor.

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	3.7	5	mA
V_{VMOT}	input voltage to the output driver stages	1.7	–	16	V
V_O	driver output voltage range; I_O = 0 mA	0.2	–	V_{VMOT} – 0.9	V
I_{LIM}	current limiting	0.6	0.85	1	A

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN and –AMP IN at 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5143T	20	SOL	plastic	SOT163A

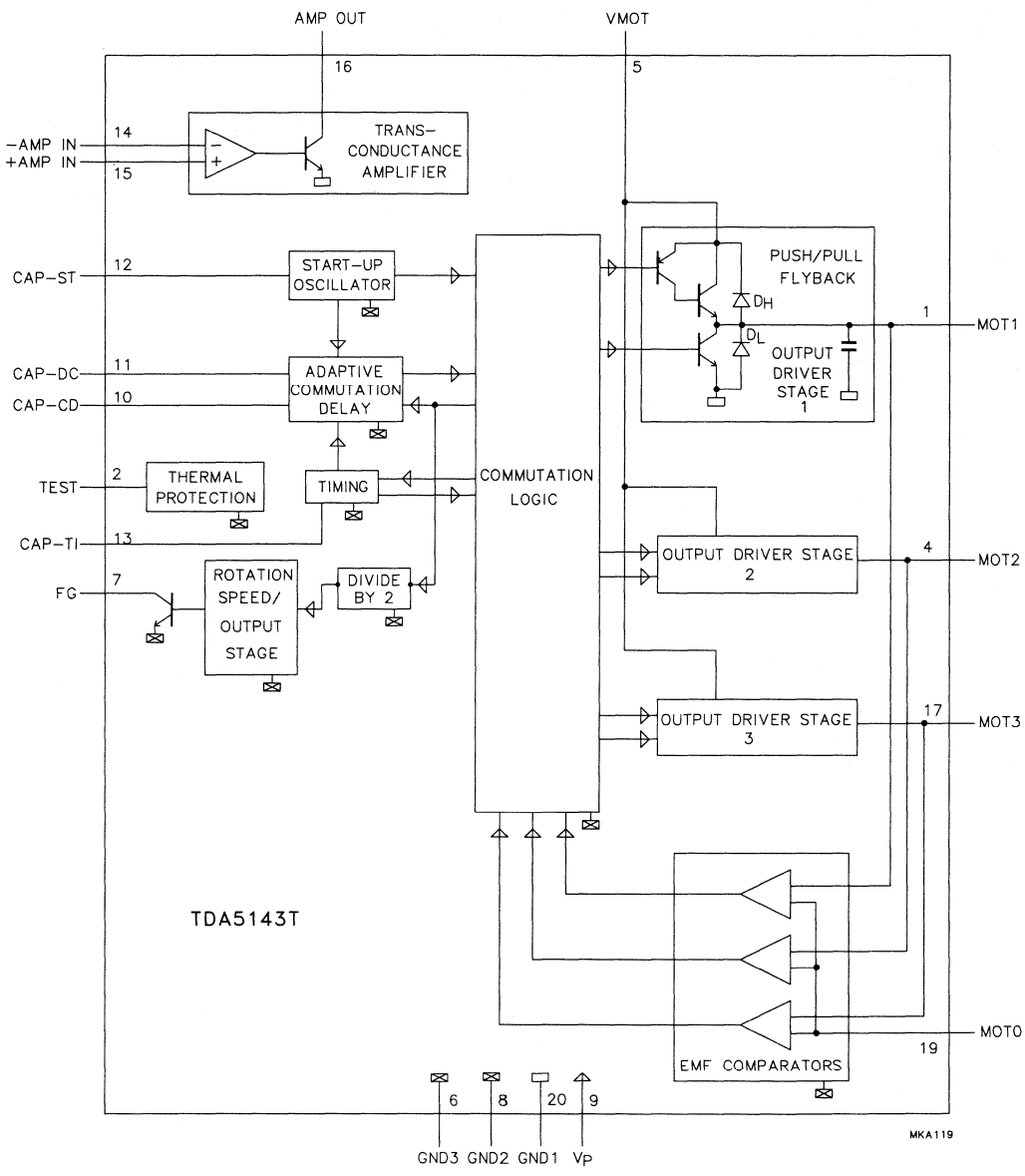


Fig.1 Block diagram.

Brushless DC motor drive circuit TDA5143T

PINNING

SYMBOL	PIN	DESCRIPTION
MOT1	1	driver output 1
TEST	2	test input/output
n.c.	3	not connected
MOT2	4	driver output 2
VMOT	5	input voltage for the output driver stages
GND3	6	ground supply
FG	7	frequency generator: output of the rotation speed (open collector digital output, negative-going edge is valid)
GND2	8	ground supply return for control circuits
V_P	9	positive supply voltage
CAP-CD	10	external capacitor connection for adaptive communication delay timing
CAP-DC	11	external capacitor connection for adaptive communication delay timing copy
CAP-ST	12	external capacitor connection for start-up oscillator
CAP-TI	13	external capacitor connection for timing
+AMP IN	14	non-inverting input of the transconductance amplifier
–AMP IN	15	inverting input of the transconductance amplifier
AMP OUT	16	transconductance amplifier output (open collector)
MOT3	17	driver output 3
n.c.	18	not connected
MOT0	19	input from the star point of the motor coils
GND1	20	ground (0 V) motor supply return for output stages

FUNCTIONAL DESCRIPTION

The TDA5143 offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5143 offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5143 offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Built-in flyback diodes
- Three phase full-wave drive
- High output current (0.85 A)
- Outputs protected by current limiting and thermal protection of each output transistor
- Low current consumption by adaptive base-drive
- Soft-switching pulse output for low radiation
- Accurate frequency generator (FG) by using the motor EMF
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive

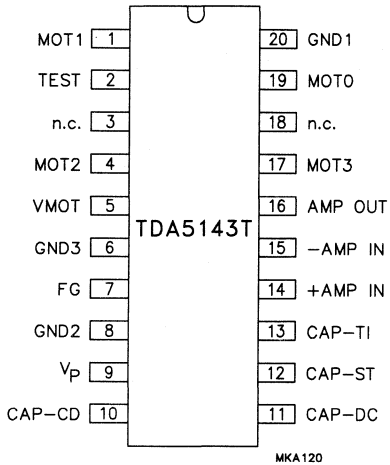


Fig.2 Pin configuration.

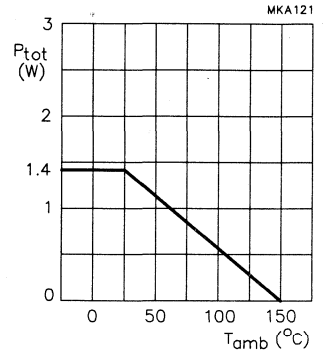


Fig.3 Power derating curve.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	–	18	V
V_I	input voltage; all pins except VMOT: $V_I < 18$ V	–0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage	–0.5	17	V
V_O	output voltage AMP OUT and FG	GND	V_P	V
V_O	output voltage MOT0, MOT1, MOT2 and MOT3	–1	$V_{VMOT} + V_D$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC	–	2.5	V
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
P_{tot}	total power dissipation	–	see Fig. 3	
V_{es}	electrostatic voltage; see also handling	–	500	V

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 2. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin referenced to ground.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range	note 1	4	–	18	V
I_P	supply current range	note 2	–	3.7	5	mA
V_{VMOT}	input voltage to the driver output stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
MOT0 - centre tape						
V_I	input voltage range		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	0	µA
V_{CSW}	comparator switching level	note 3	±20	±30	±40	mV
ΔV_{CSW}	variation in comparator switching levels		–3	0	+3	mV
V_H	comparator input hysteresis		–	75	–	µV
MOT1, MOT2 and MOT3						
V_O	driver output voltage range	I_O = 100 mA	0.4	–	V_{VMOT} – 1.2	V
V_{DO}	drop-out voltage	I_O = 500 mA	–	2.1	–	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	lower transistor; V_{CE} = 6 V	0.6	0.85	1	A
t_{tr}	transition time switching output	V_{VMOT} = 14.5 V; see Fig. 4	5	9	15	µs
V_{DHF}	diode forward voltage (diode D_H)	I_O = –500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	–1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	1	A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
+AMP IN and -AMP IN						
V_{IAMP}	input voltage range		−0.3	–	$V_P - 1.7$	V
V_{IAMP}	differential mode voltage without 'latch-up'		–	–	$\pm V_P$	V
I_B	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{OFFSET}	input offset voltage		–	–	10	mV
I_I	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_{Omax}	maximum output voltage		18	–	–	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/μs
G_{tr}	transfer gain		0.3	–	–	S
FG						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
V_{OHmax}	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	μs
	ratio of FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%
CAP-ST						
I_I	output sink current		1.5	2.0	2.5	μA
I_O	output source current		−2.5	−2.0	−1.5	μA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_I	output sink current		–	28	–	μA
I_{OH}	HIGH level output source current		–	−57	–	μA
I_{OL}	LOW level output source current		–	−5	–	μA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-CD						
I_I	ouput sink current		10.6	16.2	22	μA
I_O	output source current		−5.3	−8.1	−11	μA
I_I/I_O	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CAP-DC						
I_I	output sink current		10.1	15.5	20.9	µA
I_O	output source current		−20.9	−15.5	−10.1	µA
I_I/I_O	ratio of sink to source current		0.9	1.025	1.15	

Notes to the characteristics

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P and $I_O = 0$ mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

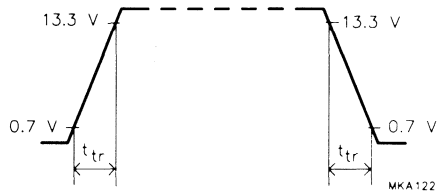
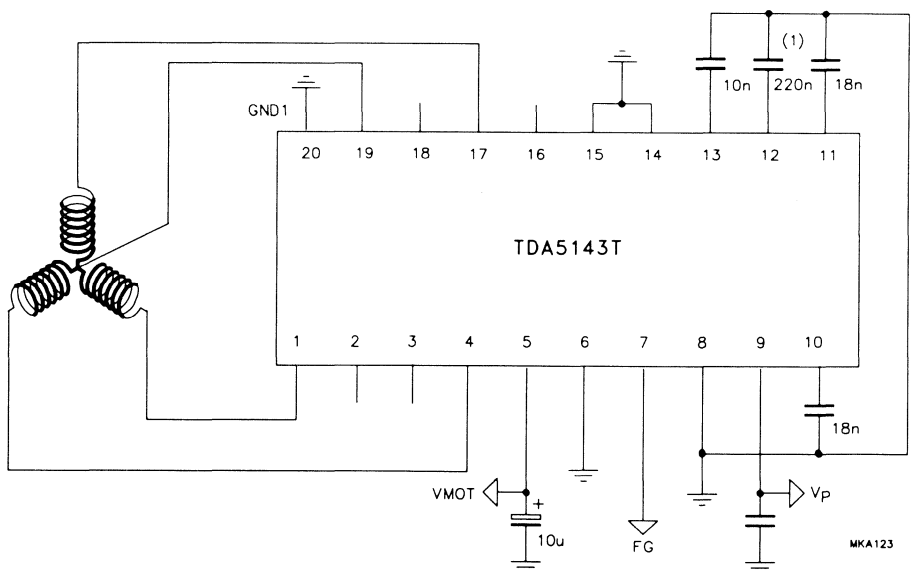


Fig.4 Output transition time measurement.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency

Fig.5 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.6)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5143 also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5143 is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented).

ADJUSTMENTS

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

$$t_{start} = (2.15 \times C)\ s \text{ (with C in } \mu F)$$

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5143 will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$$

where:

K_t = torque constant (N.m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J ($kg.m^2$)

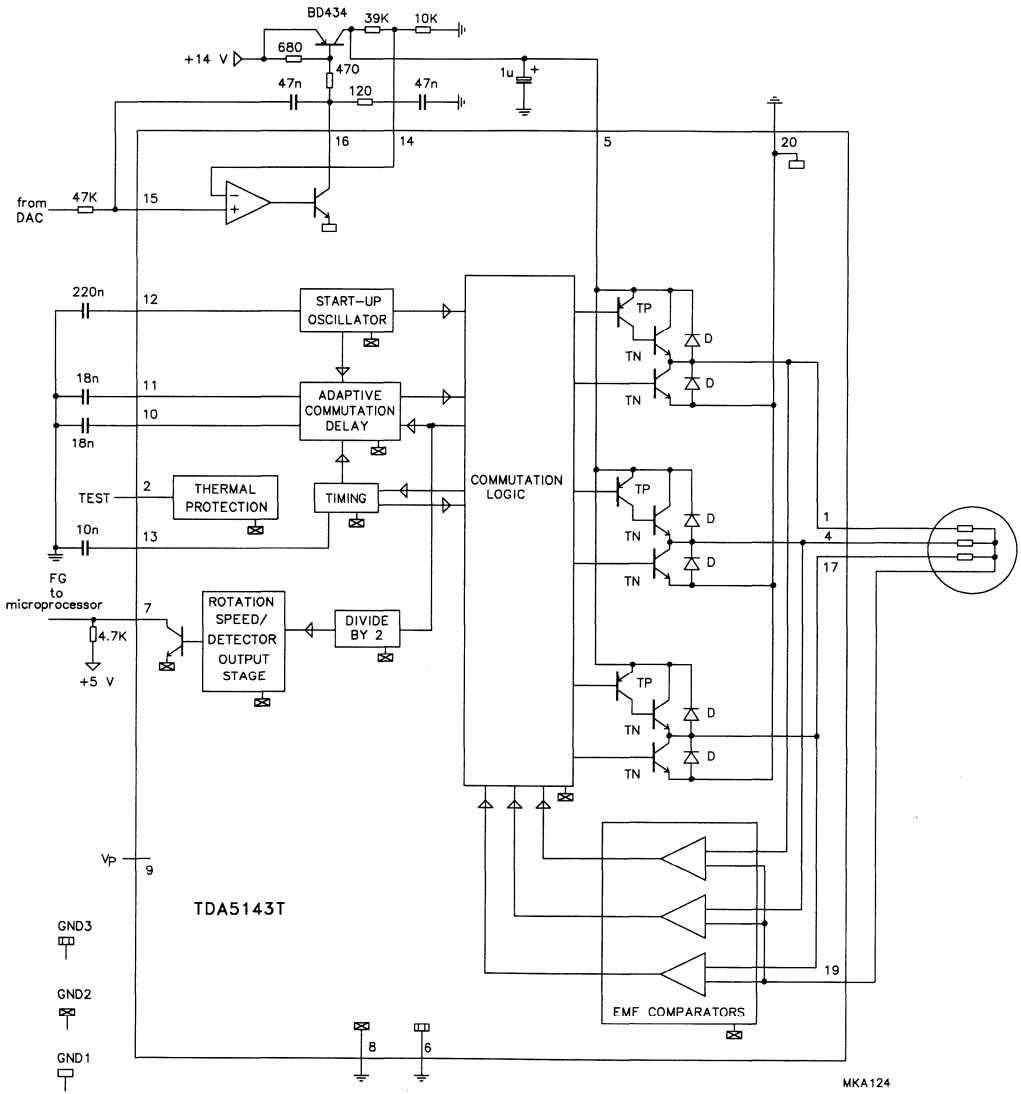


Fig.6 Typical application of the TDA5143T as a scanner driver, with use of OTA.

Example: J = 72 x 10^{-6} kg.m^2, K = 25 x 10^{-3} N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 µF, (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 µA and the discharging current 16.2 µA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

$C = 8.1 \times 10^{-6} / f \times 1.3 = 6231/f_{C1}$ (C in nF)

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 µA.

maximum delay = (0.076 x C) ms (witch C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

CAP-CD = 6231/400 = 15.6 (choose 18 nF)

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 µA. The same value can be chosen as for CAP-CD. Figure 7 illustrates typical voltage waveforms.

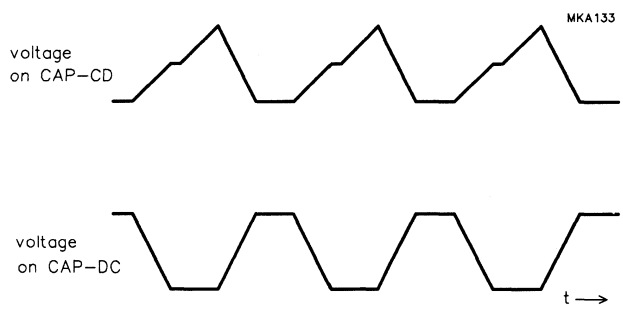


Fig.7 CAP-CD and CAP-DC voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 µA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 µA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 µA. The watchdog time is the time taken to charge the capacitor, with a current of 5 µA, from 0.3 to 2.2 V. The value of CAP-TI is given by:

$C = 5 \times 10^{-6} \times t_m/1.9 = 2.63\ t_m$ (C in nF; t in ms)

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$C = 2.63 \times 3.5 = 9.2$ (choose 10 nF)

Typical voltage waveforms are illustrated by Fig.8.

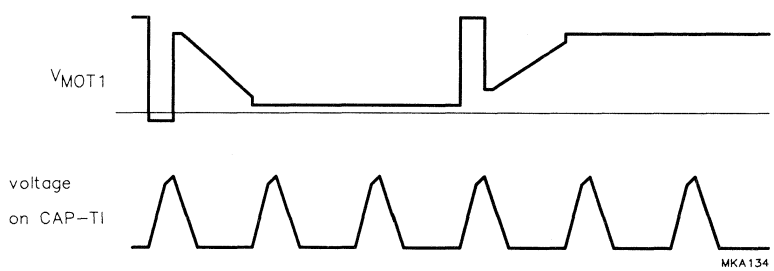


Fig.8 Typical CAP-TI and VMOT1 voltage waveforms in normal running mode.

Note to Fig.8

If the chosen value of CAP-TI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

THE EXTERNAL DAMPING COMPONENTS

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5143. This distortion may influence the correct functioning of the TDA5143, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 µs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 µs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp–8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 µF (use 1 µF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 µs. Eddy currents will also contribue to this phase shift. A shift of 20 ms corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or 0.1 mm on a VHS scanner drum.

OTHER DESIGN ASPECTS

There are other design aspects concerning the application of the TDA5143 besides the commutation function. They are:

- Generation of the tacho signal FG
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability

FG SIGNAL

The FG signal is generated in the TDA5143 by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microprocessor.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 450 Hz.

The Operational Transconductance Amplifier (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier or as a level converter in a Switched Mode Power Supply (SMPS). The common mode input range includes ground (GND) and rises to $V_P - 1.7$ V. The high sinking current enables the OTA to drive a power transistor directly in an analog control amplifier or in a SMPS drive.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (pin 16) to the positive supply, a positive-going voltage is found when the non-inverting input (pin 14) is positive with respect to the inverting input (pin 15). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

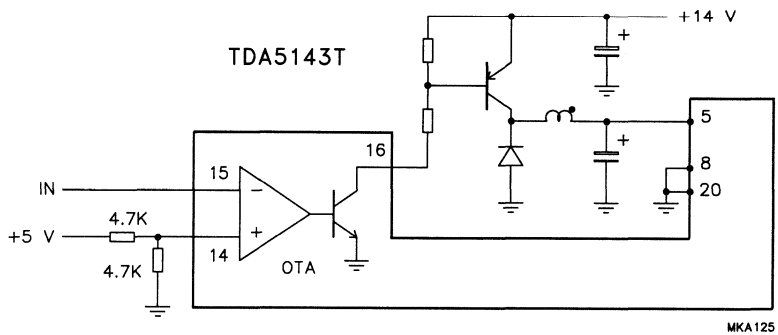


Fig.9 PWM drive of the output stages, OTA used as level converter.

Motor Control

DC motors can be controlled in an analog or digital (Pulse Width Modulation) manner, in either case the OTA may be used as follows:

- With analog control an external control transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.6).
- With digital or PWM control an external switching transistor is necessary. The OTA can make the level translation and drive the power transistor (see Fig.9).

A further aspect of motor control is current or voltage control; the TDA5143 is intended for voltage control applications. Both ground pins (6, 8 and 20) must be connected externally. However the current from pin 8 can be considered as small and constant with respect to the current in the output stages. A resistor connected between pins 6, 8, 20 and ground can be used for current control.

An alternative method of voltage control is to increase the output impedance for a certain frequency, such as the commutation frequency; the circuit illustrated by Fig.6 uses this method. The low output impedance increases to approximately 10 Ω at 900 Hz. This circuit diagram is an example of the application of the TDA5143 with a VTR scanner for a PAL recorder running at 1500 rpm. The input signal is a PWM 5 V signal. The FG signal is read by a microprocessor that runs the servo control program.

A final aspect of motor control is braking; decreasing the speed to zero. No provisions have been made for this function. However, the generated voltage of the motor is rectified by the flyback diodes. If the voltage is loaded by a current drain on pin 5 then the motor will generate a braking torque that is proportional to the current.

Reliability

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

It is possible, that when braking (see previous section), the motor voltage (via the flyback diodes and the impedance on pin 5) may cause higher currents than allowed (>0.6 A). These currents must be limited externally.

Brushless DC motor drive circuit TDA5144T/AT

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 1.8 A output current
  - low saturation voltage
  - built-in current limiter
  - soft-switching outputs
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Transconductance amplifier for an external control transistor

APPLICATIONS

- General purpose spindle driver (e.g. for HDD)

DESCRIPTION

The TDA5144 is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a hard disk drive motor.

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	4.9	6.8	mA
V_{VMOT}	input voltage to the output driver stages	1.7	–	16	V
V_O	driver output voltage range; I_O = 0 mA	0.2	–	V_{VMOT} – 0.9	V
I_{LIM}	current limiting	1.3	1.8	2.3	A

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN and –AMP IN at 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5144AT	20	SOL	plastic	SOT163A
TDA5144T	28	SOL	plastic	SOT136A

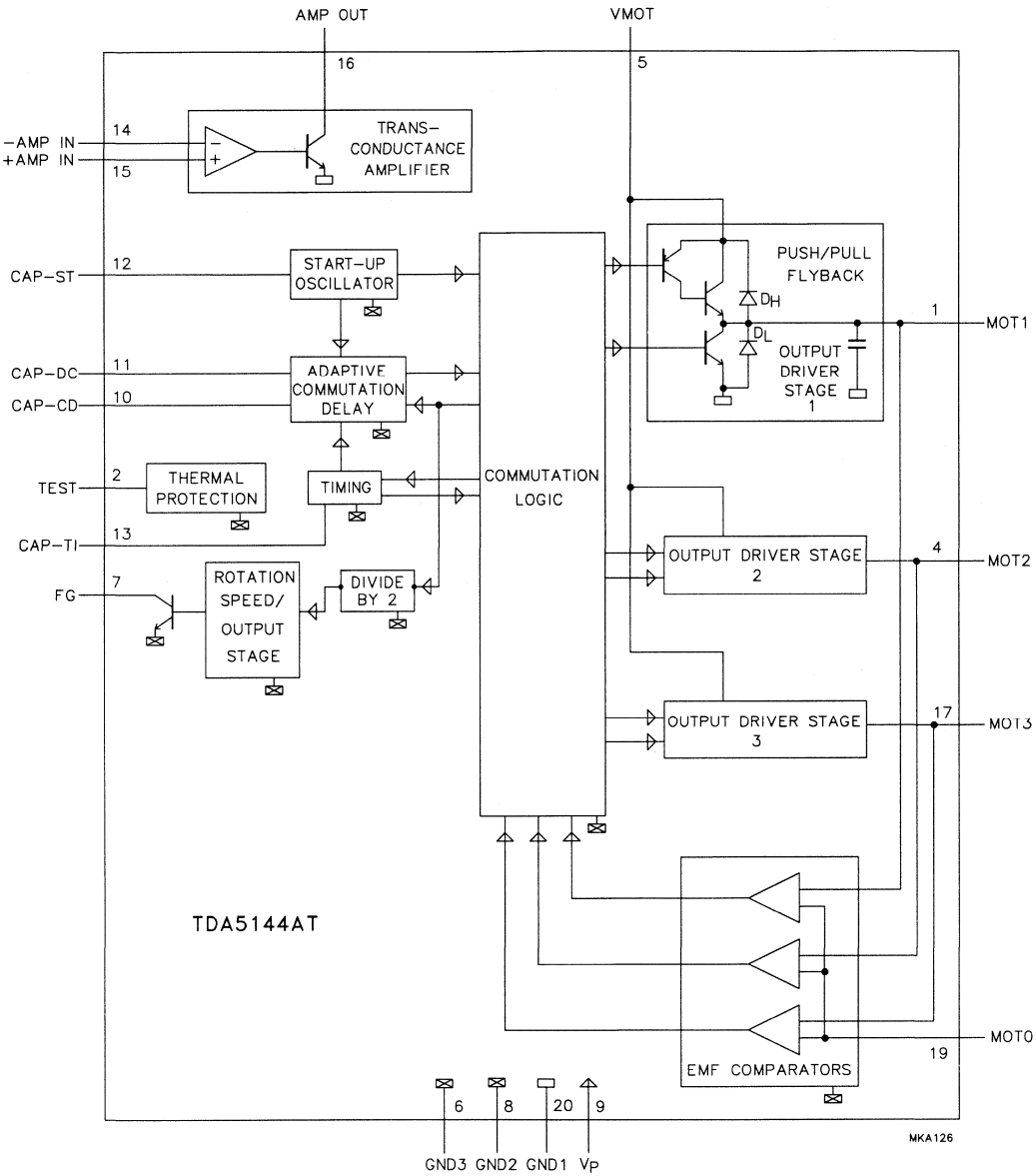


Fig.1 Block diagram (SOT163A; SO20L).

Brushless DC motor drive circuit TDA5144T/AT

PINNING

SYMBOL	PIN SO20	PIN SO28	DESCRIPTION
MOT1	1	1, 2	driver output 1
TEST	2	3	test input/output
n.c.	3	4	not connected
MOT2	4	5, 6	driver output 2
n.c.		7	not connected
VMOT	5	8, 9	input voltage for the output driver stages
GND3	6	10	ground supply
FG	7	11	frequency generator: output of the rotation speed (open collector digital output, negative-going edge is valid)
GND2	8	12	ground supply return for control circuits
V_P	9	13	positive supply voltage
CAP-CD	10	14	external capacitor connection for adaptive communication delay timing
CAP-DC	11	15	external capacitor connection for adaptive communication delay timing copy
CAP-ST	12	16	external capacitor connection for start-up oscillator
CAP-TI	13	17	external capacitor connection for timing
+AMP IN	14	18	non-inverting input of the transconductance amplifier
–AMP IN	15	19	inverting input of the transconductance amplifier
AMP OUT	16	20	transconductance amplifier output (open collector)
n.c.		21, 22	not connected
MOT3	17	23, 24	driver output 3
n.c.	18	25	not connected
MOT0	19	26	input from the star point of the motor coils
GND1	20	27, 28	ground (0 V) motor supply return for output stages

FUNCTIONAL DESCRIPTION

The TDA5144 offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5144 offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5144 offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Built-in flyback diodes
- Three phase full-wave drive
- High output current (1.8 A)
- Outputs protected by current limiting and thermal protection of each output transistor
- Low current consumption by adaptive base-drive
- Soft-switching pulse output for low radiation
- Accurate frequency generator (FG) by using the motor EMF
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive

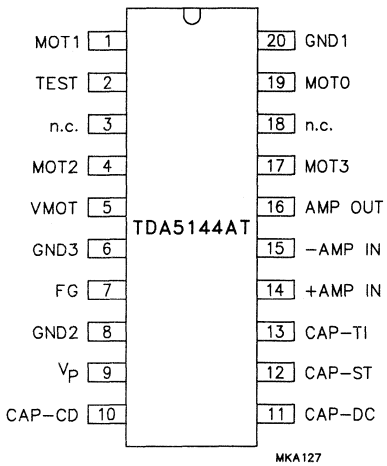


Fig.2 Pin configuration (SOT163A; SO20L).

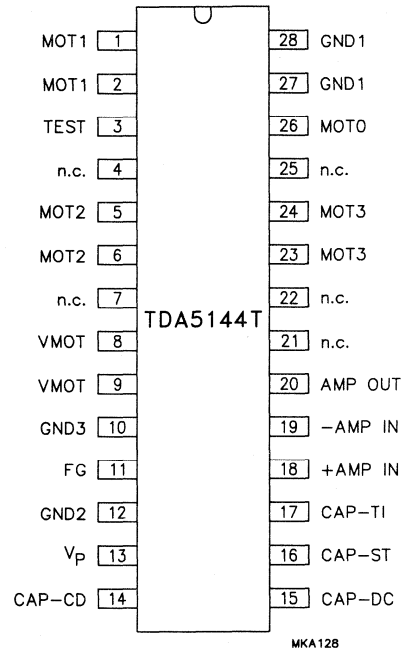


Fig.3 Pin configuration (SOT136A; SO28L).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	–	18	V
V_I	input voltage; all pins except VMOT: $V_I < 18$ V	–0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage	–0.5	17	V
V_O	output voltage AMP OUT and FG	GND	V_P	V
V_O	output voltage MOT0, MOT1, MOT2 and MOT3	–1	$V_{VMOT} + V_D$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC	–	2.5	V
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
P_{tot}	total power dissipation	–	see Figs 4 and 5	
V_{es}	electrostatic voltage; see also handling	–	500	V

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 2. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin referenced to ground.

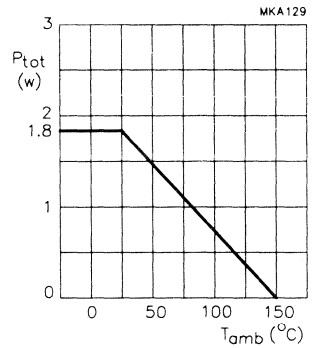


Fig.4 Power derating curve (SOT136A; SO28L).

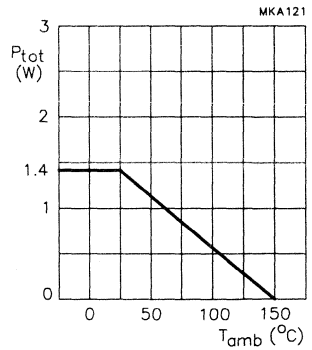


Fig.5 Power derating curve (SOT163A; SO20L).

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range	note 1	4	–	18	V
I_P	supply current range	note 2	–	4.9	6.8	mA
V_{VMOT}	input voltage to the driver output stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
MOT0 - centre tape						
V_I	input voltage range		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	0	µA
V_{CSW}	comparator switching level	note 3	±20	±25	±30	mV
ΔV_{CSW}	variation in comparator switching levels		–3	0	+3	mV
V_H	comparator input hysteresis		–	75	–	µV
MOT1, MOT2 and MOT3						
V_O	driver output voltage range	I_O = 100 mA	0.4	–	V_{VMOT} – 1.2	V
V_{DO}	drop-out voltage	I_O = 1000 mA	–	1.6	–	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	lower transistor; V_{CE} = 6 V	1.3	1.8	2.3	A
t_{tr}	transition time switching output	V_{VMOT} = 14.5 V; see Fig.6	5	9	15	µs
V_{DHF}	diode forward voltage (diode D_H)	I_O = –500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	–1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	1.8	A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
+AMP IN and -AMP IN						
V_{IAMP}	input voltage range		−0.3	–	$V_P - 1.7$	V
V_{IAMP}	differential mode voltage without 'latch-up'		–	–	$\pm V_P$	V
I_B	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{OFFSET}	input offset voltage		–	–	10	mV
I_I	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_{Omax}	maximum output voltage		–	–	18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/μs
G_{tr}	transfer gain		0.3	–	–	S
FG						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
V_{OHmax}	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	μs
	ratio of FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%
CAP-ST						
I_I	output sink current		1.5	2.0	2.5	μA
I_O	output source current		−2.5	−2.0	−1.5	μA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_I	output sink current		–	28	–	μA
I_{OH}	HIGH level output source current		–	−57	–	μA
I_{OL}	LOW level output source current		–	−5	–	μA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-CD						
I_I	ouput sink current		10.6	16.2	22	μA
I_O	output source current		−5.3	−8.1	−11	μA
I_I/I_O	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		–	875	–	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CAP-DC						
I_I	output sink current		10.1	15.5	20.9	µA
I_O	output source current		−20.9	−15.5	−10.1	µA
I_I/I_O	ratio of sink to source current		0.9	1.025	1.15	

Notes to the characteristics

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P and $I_O = 0$ mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

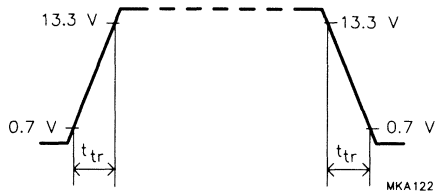
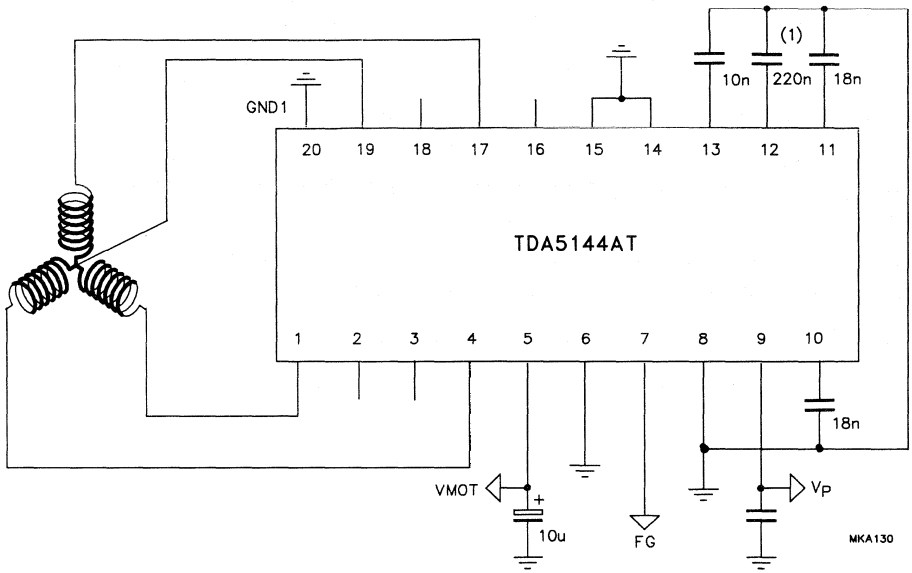


Fig.6 Output transition time measurement.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency

Fig.7 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.8)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The zero-crossings can be used to provide speed information such as the tacho signal FG.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5144 also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5144 is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented).

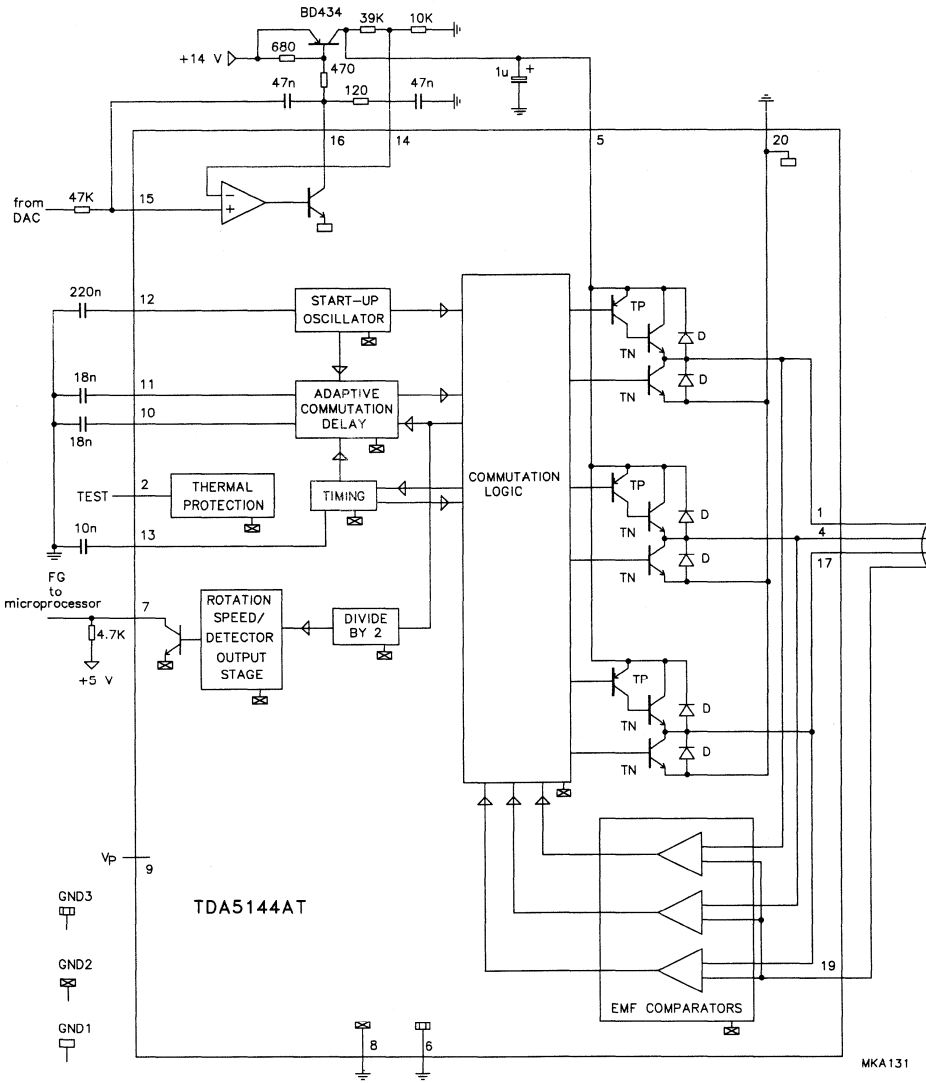


Fig.8 Typical application of the TDA5144AT as a scanner driver, with use of OTA.

ADJUSTMENTS

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

$$t_{start} = (2.15 \times C)\ s \text{ (with C in } \mu F)$$

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5144 will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$$

where:
K_t = torque constant (N.m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J ($kg.m^2$)

Example: $J = 72 \times 10^{-6}$ $kg.m^2$, $K = 25 \times 10^{-3}$ N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF, (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

$$C = 8.1 \times 10^{-6}/f \times 1.3 = 6231/f_{C1} \text{ (C in nF)}$$

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA.

$$\text{maximum delay} = (0.076 \times C)\ ms \text{ (witch C in nF)}$$

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

$$CAP\text{-}CD = 6231/400 = 15.6 \text{ (choose 18 nF)}$$

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 μA. The same value can be chosen as for CAP-CD. Figure 9 illustrates typical voltage waveforms.

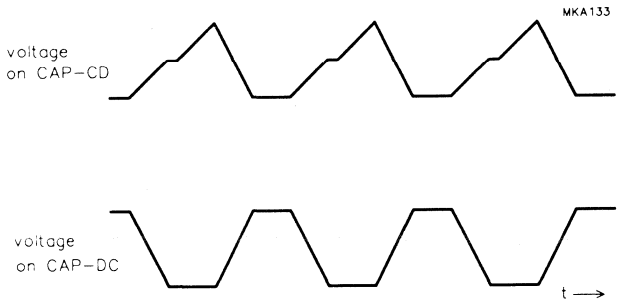


Fig.9 CAP-CD and CAP-DC voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 µA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 µA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 µA. The watchdog time is the time taken to charge the capacitor, with a current of 5 µA, from 0.3 to 2.2 V. The value of CAP-TI is given by:

$C = 5 \times 10^{-6} \times t_m/1.9 = 2.63\ t_m$ (C in nF; t in ms)

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$C = 2.63 \times 3.5 = 9.2$ (choose 10 nF)

Typical voltage waveforms are illustrated by Fig.10.

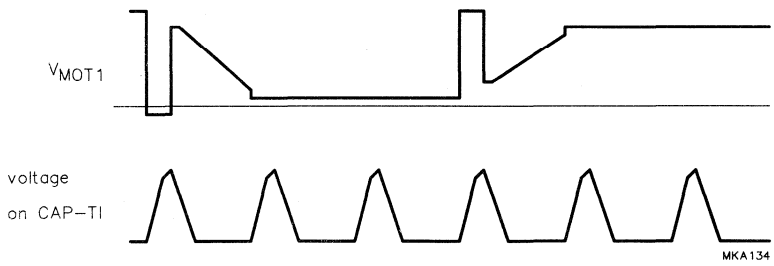


Fig.10 Typical CAP-TI and VMOT1 voltage waveforms in normal running mode.

Note to Fig.10

If the chosen value of CAP-TI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

THE EXTERNAL DAMPING COMPONENTS

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5144. This distortion may influence the correct functioning of the TDA5144, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 µs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 µs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp–8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 µF (use 1 µF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 µs. Eddy currents will also contribue to this phase shift. A shift of 20 ms corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or 0.1 mm on a VHS scanner drum.

OTHER DESIGN ASPECTS

There are other design aspects concerning the application of the TDA5140A besides the commutation function. They are:

- Generation of the tacho signal FG
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability

FG SIGNAL

The FG signal is generated in the TDA5144 by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microprocessor.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 450 Hz.

The Operational Transconductance Amplifier (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier or as a level converter in a Switched Mode Power Supply (SMPS). The common mode input range includes ground (GND) and rises to $V_P - 1.7$ V. The high sinking current enables the OTA to drive a power transistor directly in an analog control amplifier or in a SMPS drive.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (pin 16) to the positive supply, a positive-going voltage is found when the non-inverting input (pin 14) is positive with respect to the inverting input (pin 15). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

Motor Control

DC motors can be controlled in an analog or digital (Pulse Width Modulation) manner, in either case the OTA may be used as follows:

- With analog control an external control transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.8).
- With digital or PWM control an external switching transistor is necessary. The OTA can make the level translation and drive the power transistor (see Fig.11).

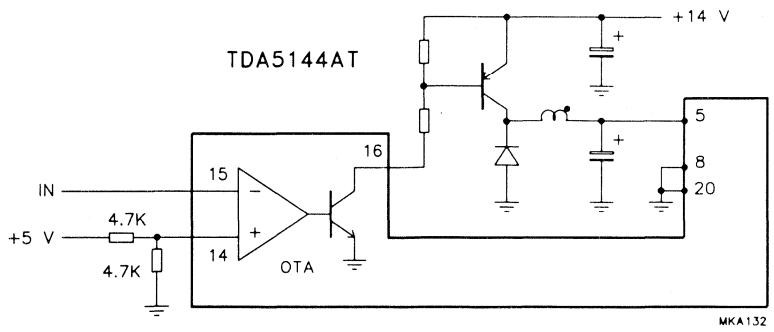


Fig.11 PWM drive of the output stages, OTA used as level converter.

A further aspect of motor control is current or voltage control; the TDA5144 is intended for voltage control applications. Both ground pins (6, 8 and 20) must be connected externally. However the current from pin 8 can be considered as small and constant with respect to the current in the output stages. A resistor connected between pins 6, 8, 20 and ground can be used for current control.

An alternative method of voltage control is to increase the output impedance for a certain frequency, such as the commutation frequency; the circuit illustrated by Fig.8 uses this method. The low output impedance increases to approximately 10 Ω at 900 Hz. This circuit diagram is an example of the application of the TDA5144 with a VTR scanner for a PAL recorder running at 1500 rpm. The input signal is a PWM 5 V signal. The FG signal is read by a microprocessor that runs the servo control program.

A final aspect of motor control is braking; decreasing the speed to zero. No provisions have been made for this function. However, the generated voltage of the motor is rectified by the flyback diodes. If the voltage is loaded by a current drain on pin 5 then the motor will generate a braking torque that is proportional to the current.

Reliability

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

It is possible, that when braking (see previous section), the motor voltage (via the flyback diodes and the impedance on pin 5) may cause higher currents than allowed (>0.6 A). These currents must be limited externally.

Brushless DC motor drive circuit TDA5145

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 1.8 A output current
  - built-in current limiter
- Thermal protection
- Soft-switching outputs
- Flyback diodes
- Tacho output without extra sensor
- Motor brake facility
- Direction control input
- Reset function
- Transconductance amplifier for an external control transistor

APPLICATIONS

- General purpose spindle driver (e.g.HDD, tape drives)

DESCRIPTION

The TDA5145 is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a hard disk drive motor or tape driver.

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	4.9	6.8	mA
V_{VMOT}	input voltage to the output driver stages	1.7	–	16	V
V_O	driver output voltage range; I_O = 0 mA	0.2	–	V_{VMOT} – 0.9	V
I_{LIM}	current limiting	1.45	1.75	2	A

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN and –AMP IN at 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5145	28	DIL	plastic	SOT117AG

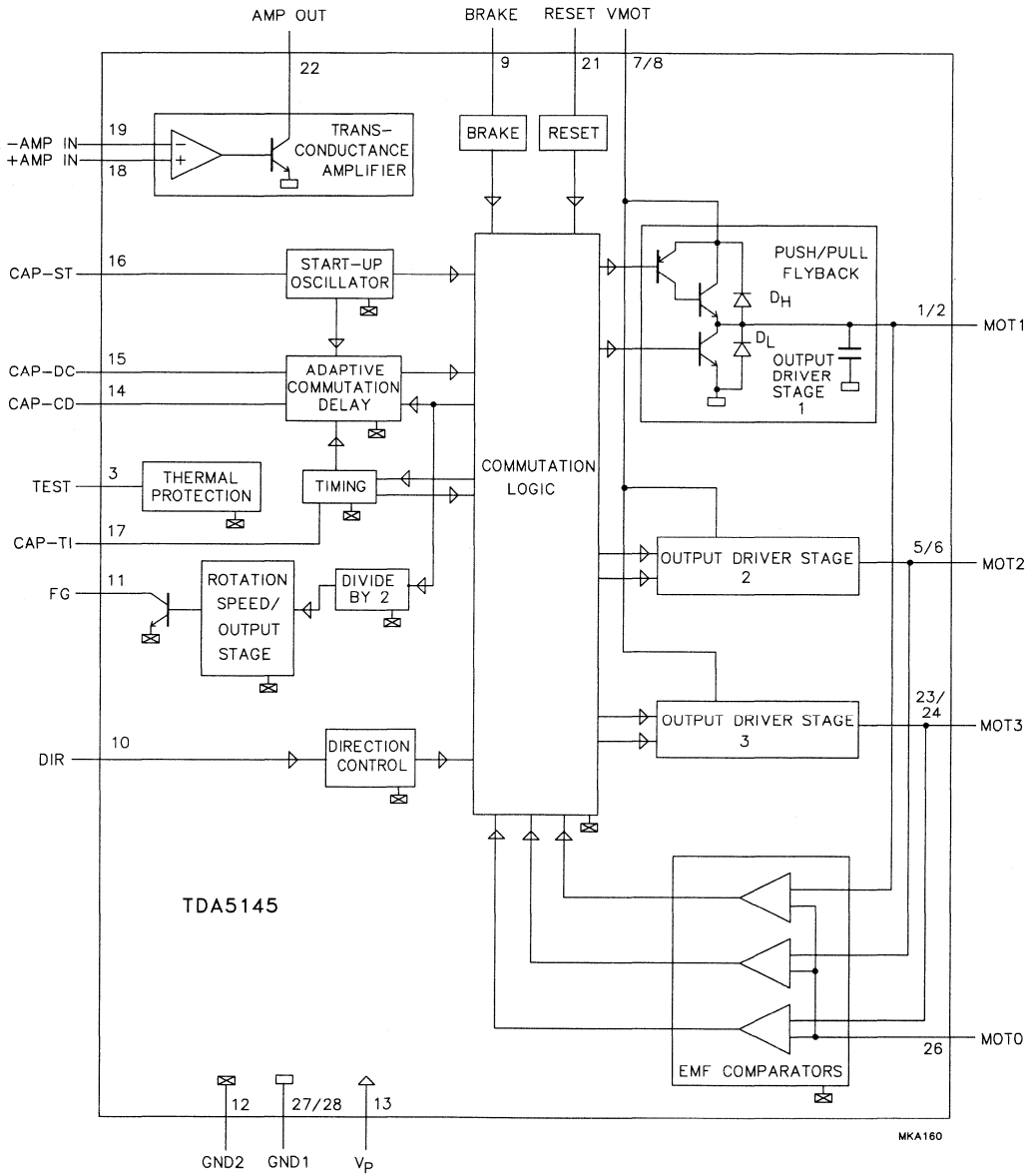


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
MOT1	1, 2	driver output 1
TEST	3	test input/output
n.c.	4	not connected
MOT2	5, 6	driver output 2
VMOT	7, 8	input voltage for the output driver stages
BRAKE	9	brake input
DIR	10	direction control input
FG	11	frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
GND2	12	ground supply return for control circuits
V_P	13	positive supply voltage
CAP-CD	14	external capacitor connection for adaptive communication delay timing
CAP-DC	15	external capacitor connection for adaptive communication delay timing copy
CAP-ST	16	external capacitor connection for start-up oscillator
CAP-TI	17	external capacitor connection for timing
+AMP IN	18	non-inverting input of the transconductance amplifier
–AMP IN	19	inverting input of the transconductance amplifier
n.c.	20	not connected
RESET	21	reset input
AMP OUT	22	transconductance amplifier output (open collector)
MOT3	23, 24	driver output 3
n.c.	25	not connected
MOT0	26	input from the star point of the motor coils
GND1	27, 28	ground (0 V) motor supply return for output stages

FUNCTIONAL DESCRIPTION

The TDA5145 offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5145 offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5145 offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Built-in flyback diodes
- Three phase full-wave drive
- High output current (1.8 A)
- Outputs protected by current limiting and thermal protection of each output transistor
- Low current consumption by adaptive base-drive
- Soft-switching pulse output for low radiation
- Accurate frequency generator (FG) by using the motor EMF
- Direction of rotation controlled by one pin
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive
- Brake function

Brushless DC motor drive circuit TDA5145

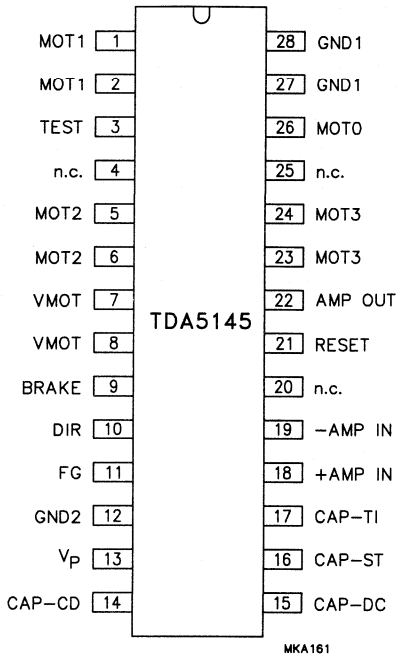


Fig.2 Pin configuration.

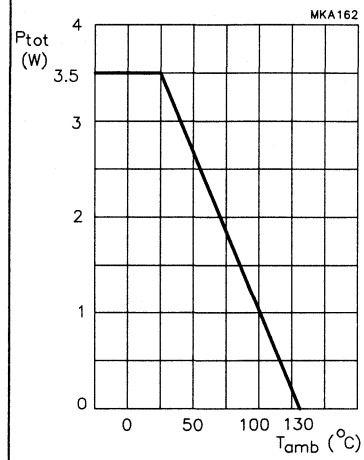


Fig.3 Power derating curve.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	–	18	V
V_I	input voltage; all pins except VMOT: $V_I < 18$ V	–0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage	–0.5	17	V
V_O	output voltage AMP OUT and FG	GND	V_P	V
V_O	output voltage MOT0, MOT1, MOT2 and MOT3	–1	$V_{VMOT} + V_D$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC	–	2.5	V
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
P_{tot}	total power dissipation	–	see Fig. 3	
V_{es}	electrostatic voltage; see also handling	–	2000	V

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 2. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin referenced to ground.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range	note 1	4	–	18	V
I_P	supply current range	note 2	–	4.9	6.8	mA
V_{VMOT}	input voltage to the driver output stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
MOT0 - centre tape						
V_I	input voltage range		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	–	µA
V_{CSW}	comparator switching level	note 3	±20	±25	±30	mV
ΔV_{CS}	variation in threshold voltage between comparators	note 3	–	–	3	mV
V_H	comparator input hysteresis		–	75	–	µV
MOT1, MOT2 and MOT3						
V_O	driver output voltage range	I_O = 100 mA	0.4	–	V_{VMOT} – 1.2	V
V_{DO}	drop-out voltage	I_O = 1000 mA	–	–	2	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	lower transistor; V_{CE} = 6 V	1.45	1.75	2	A
t_{tr}	transition time switching output	V_{VMOT} = 14.5 V; see Fig.5	5	9	15	µs
V_{DHF}	diode forward voltage (diode D_H)	I_O = –500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	–1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	1	A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
+AMP IN and -AMP IN						
V_{IAMP}	input voltage range		−0.3	–	$V_P - 1.7$	V
V_{IAMP}	differential mode voltage without 'latch-up'		–	–	$\pm V_P$	V
I_B	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{OFFSET}	input offset voltage		–	–	10	mV
I_I	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_{Omax}	maximum output voltage		–	–	18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/μs
G_{tr}	transfer gain		0.3	–	–	S
DIR						
V_{IH}	normal rotation voltage at pin 5; HIGH level	4 V < V_P < 18 V	2.0	–	–	V
V_{IL}	reverse rotation voltage at pin 5; LOW level	4 V < V_P < 18 V	–	–	0.8	V
I_{IL}	reverse rotation current; LOW level		–	−20	–	μA
I_{IH}	normal rotation current; HIGH level		–	−20	–	μA
RESET						
V_{IH}	HIGH level input voltage in reset mode	4 V < V_P < 18 V	2.0	–	–	V
V_{IL}	LOW level input voltage in normal mode	4 V < V_P < 18 V	–	–	0.8	V
I_{IL}	LOW level input current	V_I = 2.0 V	–	−20	–	μA
I_{IH}	HIGH level input current	V_I = 0.8 V	–	−20	–	μA
BRAKE						
V_{IH}	HIGH level input voltage in brake mode	4 V < V_P < 18 V	2.0	–	–	V
V_{IL}	LOW level input voltage in normal mode	4 V < V_P < 18 V	–	–	0.8	V
I_{IL}	LOW level input current	V_I = 2.0 V	–	−20	–	μA
I_{IH}	HIGH level input current	V_I = 0.8 V	–	−20	–	μA
FG						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
V_{OHmax}	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	μs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FG						
	ratio of FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%
CAP-ST						
I_I	output sink current		1.5	2.0	2.5	µA
I_O	output source current		–2.5	–2.0	–1.5	µA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_I	output sink current		–	28	–	µA
I_{OH}	HIGH level output source current		–	–57	–	µA
I_{OL}	LOW level output source current		–	–5	–	µA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-CD						
I_I	ouput sink current		10.6	16.2	22	µA
I_O	output source current		–5.3	–8.1	–11	µA
I_I/I_O	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		0.85	–	0.9	V
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V
CAP-DC						
I_I	output sink current		10.1	15.5	20.9	µA
I_O	output source current		–20.9	–15.5	–10.1	µA
I_I/I_O	ratio of sink to source current		0.9	1.025	1.15	

Notes to the characteristics

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P and $I_O = 0$ mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3; see also Fig.4.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

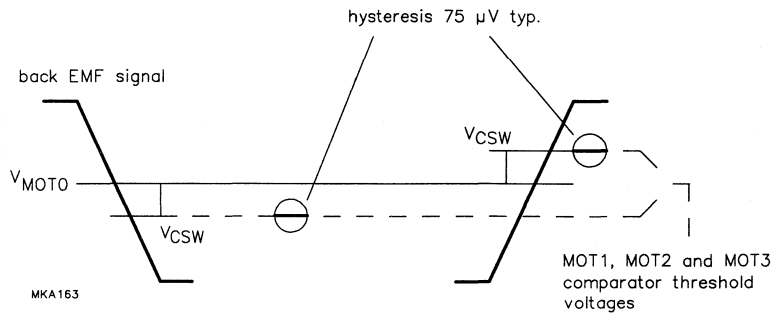


Fig.4 Switching levels with respect to MOT1, MOT2 and MOT3.

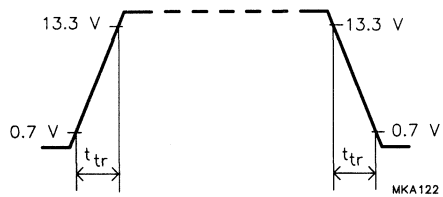
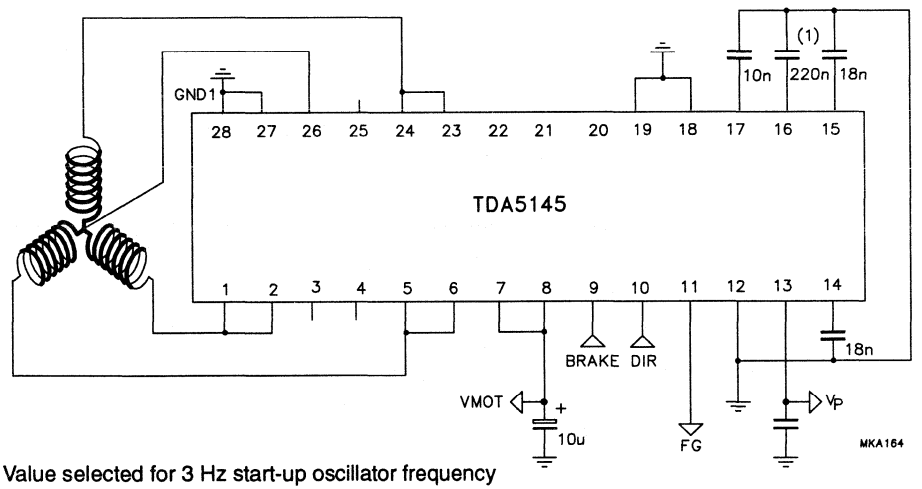


Fig.5 Output transition time measurement.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency

Fig.6 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.7)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The zero-crossings can be used to provide speed information such as the tacho signal FG.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5145 is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented).

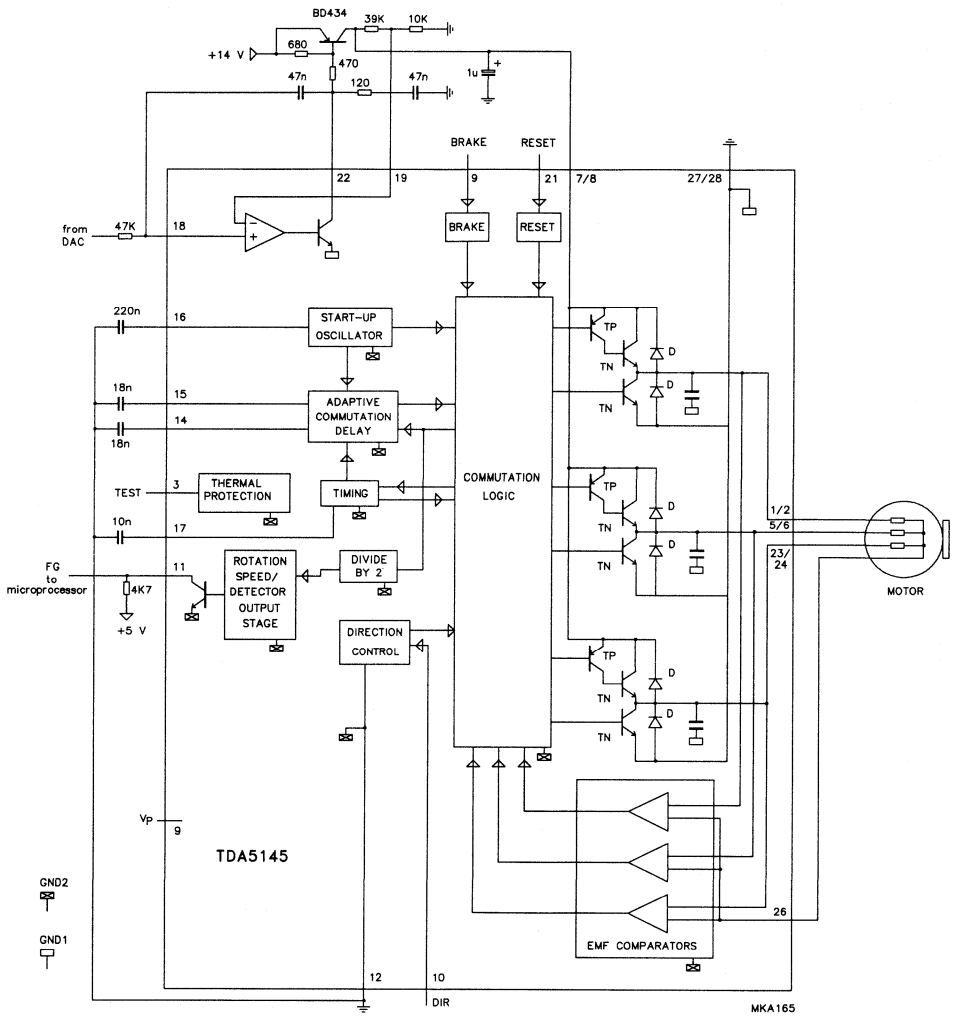


Fig.7 Typical application of the TDA5145 as a scanner driver, with use of OTA.

ADJUSTMENTS

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

$$t_{start} = (2.15 \times C)\ s \text{ (with C in } \mu F)$$

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5145 will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$$

where:
K_t = torque constant (N.m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J ($kg.m^2$)

Example: $J = 72 \times 10^{-6}$ $kg.m^2$, $K = 25 \times 10^{-3}$ N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF, (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

$$C = 8.1 \times 10^{-6}/\ f \times 1.3 = 6231/f_{C1} \text{ (C in nF)}$$

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA.

$$\text{maximum delay} = (0.076 \times C)\ ms \text{ (witch C in nF)}$$

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

$$CAP\text{-}CD = 6231/400 = 15.6 \text{ (choose 18 nF)}$$

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 μA. The same value can be chosen as for CAP-CD. Figure 8 illustrates typical voltage waveforms.

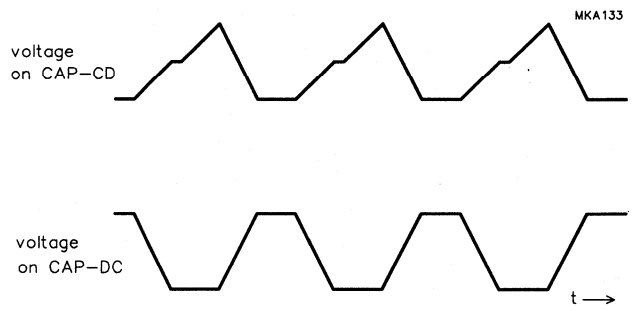


Fig.8 CAP-CD and CAP-DC voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 μA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 μA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V. The value of CAP-TI is given by:

$$C = 5 \times 10^{-6} \times t_m/1.9 = 2.63\ t_m \text{ (C in nF; t in ms)}$$

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$$C = 2.63 \times 3.5 = 9.2 \text{ (choose 10 nF)}$$

Typical voltage waveforms are illustrated by Fig.9.

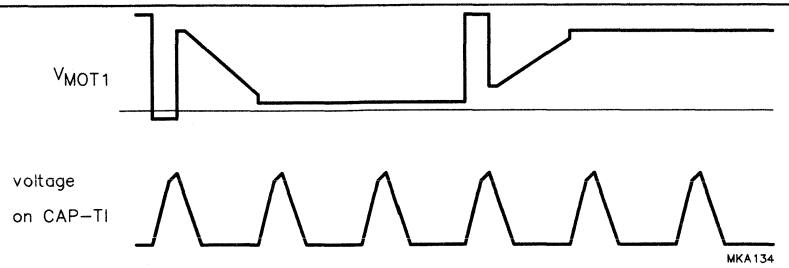


Fig.9 Typical CAP-TI and VMOT1 voltage waveforms in normal running mode.

Note to Fig. 9

If the chosen value of CAP-TI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

THE EXTERNAL DAMPING COMPONENTS

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5145. This distortion may influence the correct functioning of the TDA5145, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 µs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 µs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp–8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 µF (use 1 µF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 µs. Eddy currents will also contribue to this phase shift. A shift of 20 µs corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or 0.1 mm on a VHS scanner drum.

OTHER DESIGN ASPECTS

There are other design aspects concerning the application of the TDA5140A besides the commutation function. They are:

- Generation of the tacho signal FG
- Possibilities of motor control
- Preposition input
- Direction input
- Brake input
- Reliability

FG SIGNAL

The FG signal is generated in the TDA5145 by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microprocessor.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 450 Hz.

Direction input

If the voltage at pin 10 is less than 0.8 V, the motor is running in one direction (depending on the motor connections). If the voltage at pin 10 is higher than 2.0 V, the motor is running in the other direction.

Brake function

If the voltage at pin 9 is higher than 2.0 V, the motor brakes. In that condition, the 3 outputs MOT1, MOT2 and MOT3 are forced at a LOW voltage level and the current limitation is done internally by the sink drivers.

Test function

It is possible to turn off the three outputs by forcing a current of 600 μA into pin 3 (see Fig.10).

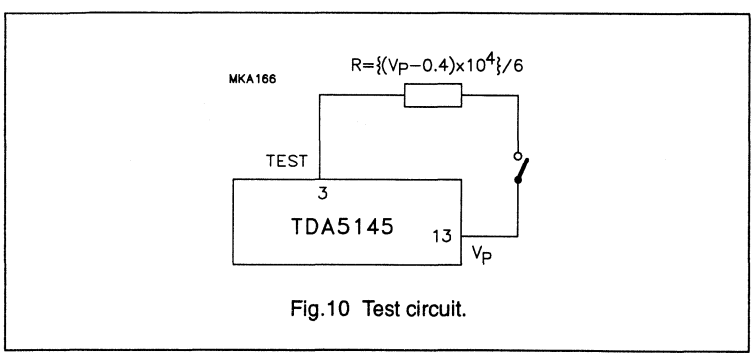


Fig.10 Test circuit.

Reset function

If the voltage at pin 21 is higher than 2.0 V, the output states are:

- MOT1 - FLOATING (F)
- MOT2 - LOW (L)
- MOT3 - HIGH (H)

Table 1 Switching sequence after a reset pulse

DIR	RESET	MOT1	MOT2	MOT3	FUNCTION
H	H	F	L	H	reset
H	L	F	L	H	normal direction mode sequence
H	L	H	L	F	
H	L	H	F	L	
H	L	F	H	L	
H	L	L	H	F	
H	L	L	F	H	
L	H	H	L	F	reset
L	L	H	L	F	reverse direction mode sequence
L	L	F	L	H	
L	L	L	F	H	
L	L	L	H	F	
L	L	F	H	L	
L	L	H	F	L	

Table 2 Priority of function

BRAKE	TEST	RESET	FUNCTION
L	L	L	normal
L	L	H	reset
L	H	L	test
L	H	H	test
H	L	L	brake
H	L	H	brake
H	H	L	brake
H	H	H	brake

VHF, UHF AND HYPERBAND MIXER/OSCILLATOR FOR TV AND VCR 3-BAND TUNERS

GENERAL DESCRIPTION

The TDA5330T is a monolithic integrated circuit that performs the band A, band B and band C mixer/oscillator functions in TV and VCR tuners. This device gives the designer the capability to design an economical and physically small 3-band tuner which will be capable of meeting the most stringent requirements e.g. FTZ or FCC. The tuner development time can be drastically reduced by using this device.

Features

- Balanced mixer with a common emitter input for band A
- Amplitude-controlled oscillator for band A
- Balanced mixer with common base input for band B and C
- Balanced oscillator for band B and C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with an output impedance of 100 Ω
- Bandgap voltage stabilizer for oscillator stability
- Electronic bandswitch

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_{19\text{-}2,\ 26}$	–	12	–	V
Band A frequency range		f_A	48	–	180	MHz
Band B frequency range		f_B	160	–	470	MHz
Band C frequency range		f_C	430	–	860	MHz
Conversion noise		F	7	–	11	dB
Band A input voltage	1% cross-modulation	$V_{24\text{-}26}$	–	100	–	dBμV
Band B and C input power	1% cross-modulation	P_I	–	–21	–	dBm
Band A voltage gain		G_v	–	24	–	dB
Band B voltage gain		G_v	–	37	–	dB
Band C voltage gain		G_v	–	36	–	dB

PACKAGE OUTLINE

28-lead mini-pack, plastic (SO20; SOT163A).

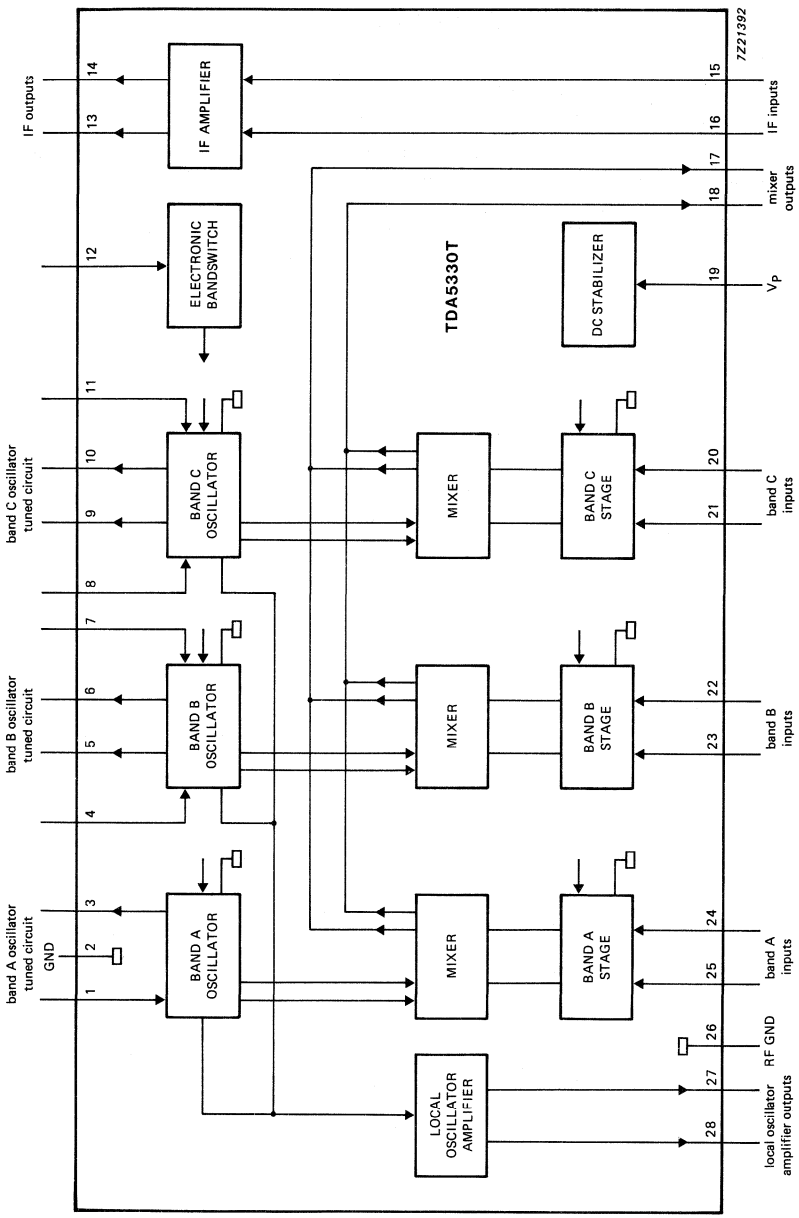


Fig. 1 Block diagram.

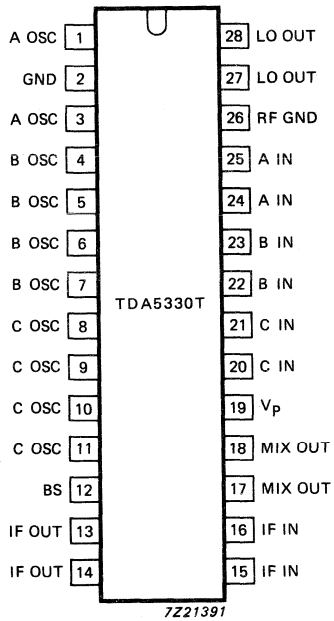


Fig. 2 Pinning diagram.

PINNING

1	A OSC	band A oscillator input
2	GND	ground (0 V)
3	A OSC	band A oscillator output
4	B OSC	band B oscillator input
5	B OSC	band B oscillator output
6	B OSC	band B oscillator output
7	B OSC	band B oscillator input
8	C OSC	band C oscillator input
9	C OSC	band C oscillator output
10	C OSC	band C oscillator output
11	C OSC	band C oscillator input
12	BS	electronic bandswitch
13	IF OUT	IF amplifier output
14	IF OUT	IF amplifier output
15	IF IN	IF amplifier input
16	IF IN	IF amplifier input
17	MIX OUT	mixer output
18	MIX OUT	mixer output
19	V_P	positive supply voltage
20	C IN	band C input
21	C IN	band C input
22	B IN	band B input
23	B IN	band B input
24	A IN	band A input
25	A IN	band A input
26	RF GND	ground for RF inputs
27	LO OUT	local oscillator amplifier output
28	LO OUT	local oscillator amplifier output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_{19-2, 26}$	−0.3	14	V
Switching voltage		V_{12}	0	14	V
Output current of each pin to ground		I_O	−	−10	mA
Maximum short-circuit time (all pins)		t_{sc}	−	10	s
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−25	+80	°C

THERMAL RESISTANCE

From junction to ambient in free air $R_{th\ j\text{-}a}$ typ. 75 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_{19\text{-}2,\ 26}$	10	–	13.2	V
Supply current		I_{19}	–	42	55	mA
Switching voltage;						
band A		V_{12}	0	–	1.1	V
band B		V_{12}	1.6	–	2.4	V
band C		V_{12}	3.0	–	5.0	V
Switching current;						
band C		I_{12}	–	–	50	μA
Band A Mixer (including IF amplifier)	measured using circuit shown in Fig. 9					
Frequency range		f_A	48	–	180	MHz
Noise figure	note 1;					
	50 MHz	NF	–	7.5	9	dB
	180 MHz	NF	–	9	10	dB
Optimum source conductance	50 MHz	$G_{24\text{-}26}$	–	0.5	–	mS
	180 MHz	$G_{24\text{-}26}$	–	1.1	–	mS
Input admittance	see Fig. 9					
Input capacitance	50 - 180 MHz	$C_{24\text{-}26}$	–	2	–	pF
Input voltage	1% cross-modulation;					
	in channel	$V_{24\text{-}26}$	97	100	–	dBμV
Input voltage	10 kHz pulling;					
	in channel	$V_{24\text{-}26}$	100	108	–	dBμV
Voltage gain	20 log $(V_{13\text{-}14}/V_{24})$	G_V	22.5	25.0	27.5	dB
Band A mixer						
Conversion transadmittance mixer	$Sc = I_{17}/V_{24}$ $= -I_{18}/V_{24}$	$Sc_{24\text{-}17,\ 18}$	–	3.5	–	mS
Mixer output admittance	pins 15 and 16		–	0.1	–	mS
Mixer output capacitance		$C_{17\text{-}18}$	–	2	–	pF

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Band A oscillator						
Frequency range		f_A	80	–	216	MHz
Frequency shift	ΔV_P = 10%	Δf	–	–	200	kHz
Frequency drift	ΔT = 25 °C	Δf	–	–	400	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–	200	kHz
Band B mixer (including IF)	measured using circuit shown in Fig. 9; measurements using hybrid; note 2					
Frequency range		f_B	160	–	470	MHz
Noise figure	pins 22 and 23;					
	200 MHz	NF	–	8	10	dB
	470 MHz	NF	–	8	10	dB
Input admittance	see Fig. 5					
Available input power	1% cross-modulation; in channel; pins 22 and 23;					
	200 MHz	P_{AI}	–24	–21	–	dBm
	470 MHz	P_{AI}	–24	–21	–	dBm
10 kHz pulling	pins 22 and 23; in channel;					
	470 MHz		–	–11	–	dBm
N+5 – 1 MHz pulling	note 3;					
	430 MHz		–	–11	–	dBm
Voltage gain	note 4;					
	200 MHz	G_V	33	36	39	dB
	470 MHz	G_V	33	36	39	dB
Band B oscillator						
Frequency range		f_B	200	–	500	MHz
Frequency shift	ΔV_P = 10%	Δf	–	–	400	kHz
Frequency drift	ΔT = 25 °C	Δf	–	–	500	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–	200	kHz

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.		max.	unit
Band C mixer (including IF)	measured using circuit shown in Fig. 9; measurements using hybrid; note 2						
Frequency range		f_C	430	–		860	MHz
Noise figure	pins 20 and 21;						
	430 MHz	NF	–	9		11	dB
	860 MHz	NF	–	9		11	dB
Input admittance	see Fig. 6						
Available input power	1% cross-modulation in channel; pins 20 and 21;						
	430 MHz	P_{AI}	–25	–21		–	dBm
	860 MHz	P_{AI}	–25	–21		–	dBm
10 kHz pulling	pins 20 and 21; in channel;						
	860 MHz		–	–20		–	dBm
N+5 – 1 MHz pulling	note 3;						
	820 MHz		–42	–35		–	dBm
Voltage gain	note 4;						
	430 MHz	G_v	33	36		39	dB
	860 MHz	G_v	33	36		39	dB
Band C oscillator							
Frequency range		f_C	470	–		900	MHz
Frequency shift	ΔV_b = 10%	Δf	–	–		400	kHz
Frequency drift	ΔT = 25 °C	Δf	–	–		800	kHz
Frequency drift	5 s to 15 min after switching on	Δf	–	–		200	kHz
				mod.	phase		
IF Amplifier	note 5, differentially measured at 36 MHz; see Fig. 7						
Input reflection coefficient		S_{11}	–	–0,5	–2.0	–	dB/deg
Reverse transmission coefficient		S_{12}	–	–41	–7	–	dB/deg
Forward transmission coefficient		S_{21}	–	12	160	–	dB/deg
Output reflection coefficient	see Fig. 8	S_{22}	–	–9	10	–	dB/deg

parameter	conditions	symbol	min.	typ.	max.	unit
LO output						
Output voltage into 50 Ω resistor		V_{27-28}	14	35	100	mV
Spurious signal on LO output with respect to LO output signal	note 6	SRF	–	–	−10	dB
LO signal harmonics with respect to LO signal	measured at 50 Ω	SHD	–	–	−10	dB

Notes to the characteristics

1. Measured with an input circuit for optimum noise. (See Fig. 3).

DEVELOPMENT DATA

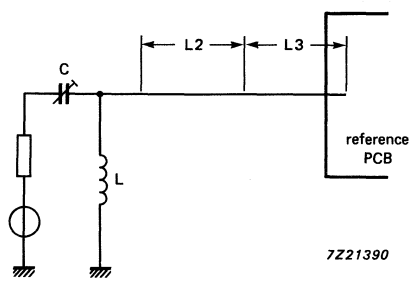


Fig. 3 Input circuit for optimum noise.

Table 1 Component values

component	f = 50 MHz	f = 180 MHz
L	13 t, ϕ 5.5 mm, wire 0.7 mm	*
L2	rigid cable, 2.9 cm	*
L3	rigid cable, 4 cm	*
C	9.6 pF	*

* Value to be fixed.

Notes to the characteristics (continued)

Table 2 Electrical parameters of the circuit (for appropriate impedance and selectivity)

parameter	f = 50 MHz	f = 180 MHz	unit
Insertion loss	0.3	*	dB
Bandwidth	8	*	MHz
Image suppression	15	*	dB
Output impedance (source for IC)	2	*	kΩ

2. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
3. The input level of a N+5 — 1 MHz signal (just visible).
4. The gain is defined as the transducer gain (measured in Fig. 9) plus the voltage transformation ratio of L6 to L7 (6:1, 16 dB).
5. All S parameters are referred to a 50 Ω system.
6. Measured with 50 Ω output impedance on pins 26 and 27 and a RF input signal level of:
   RF level = 1 V at $f < 180$ MHz
   RF power = 0.5 dBm at 100 MHz $< f <$ 225 MHz
   RF power = −10 dBm at 225 MHz $< f <$ 860 MHz

* Value to be fixed.

DEVELOPMENT DATA

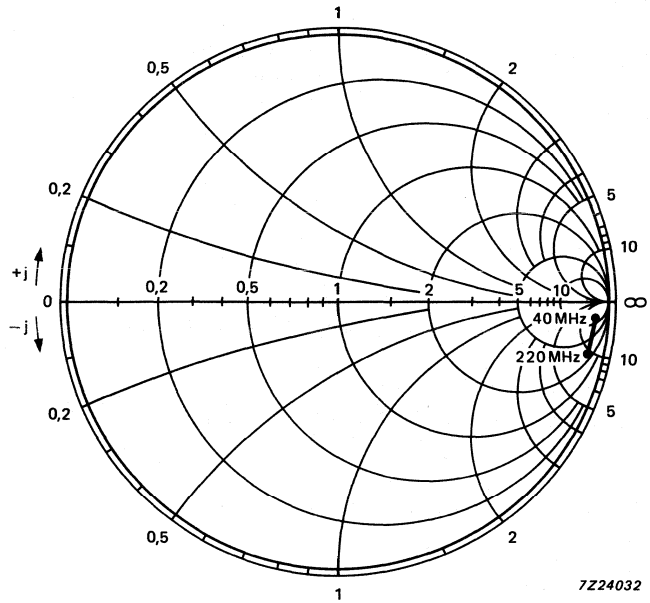


Fig. 4 S11 of the band A mixer input (40 to 220 MHz).

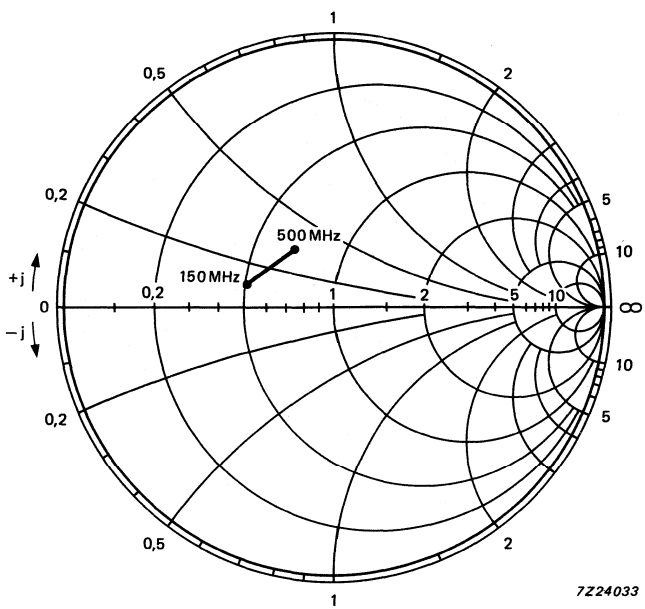


Fig. 5 S11 of the band B mixer input (150 to 500 MHz).

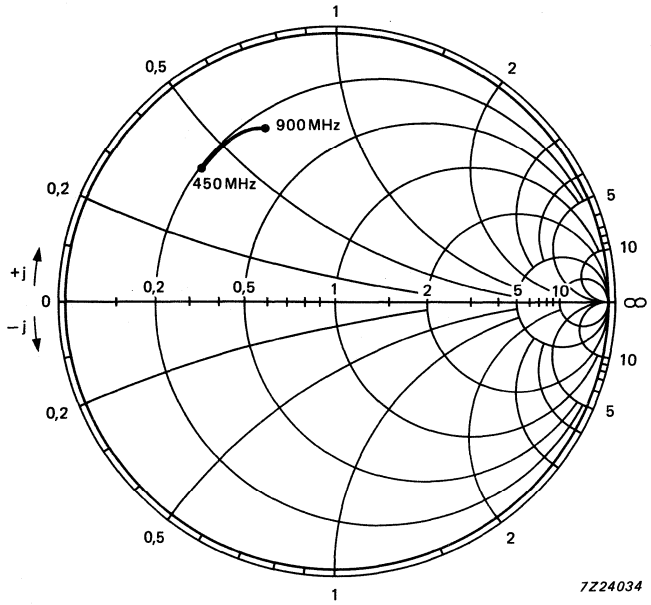


Fig. 6 S11 of the band C mixer input (450 to 900 MHz).

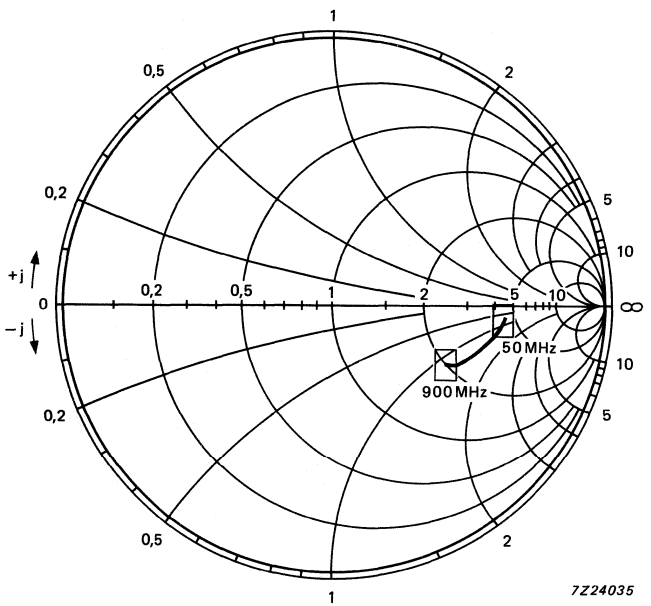


Fig. 7 S11 of the LO output (50 to 900 MHz).

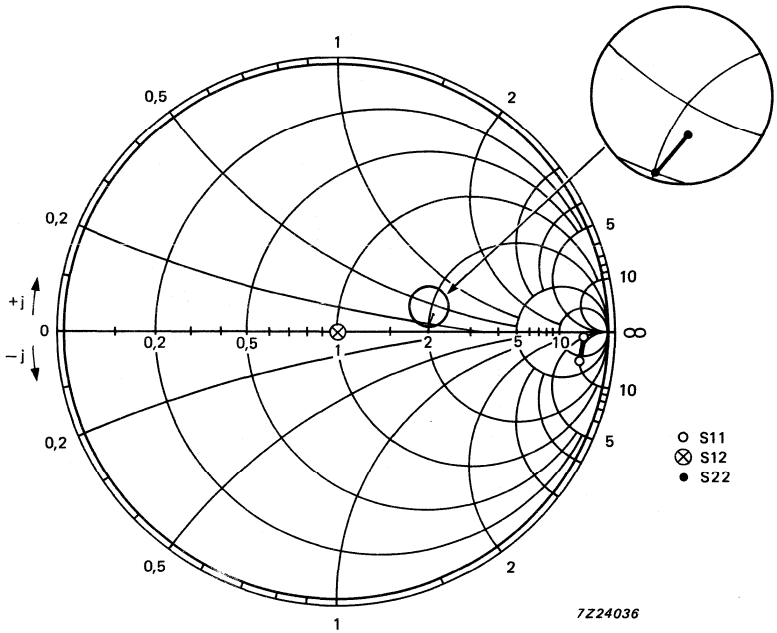


Fig. 8 S11, S12 and S22 of the IF amplifier (30 to 60 MHz).

DEVELOPMENT DATA

APPLICATION INFORMATION

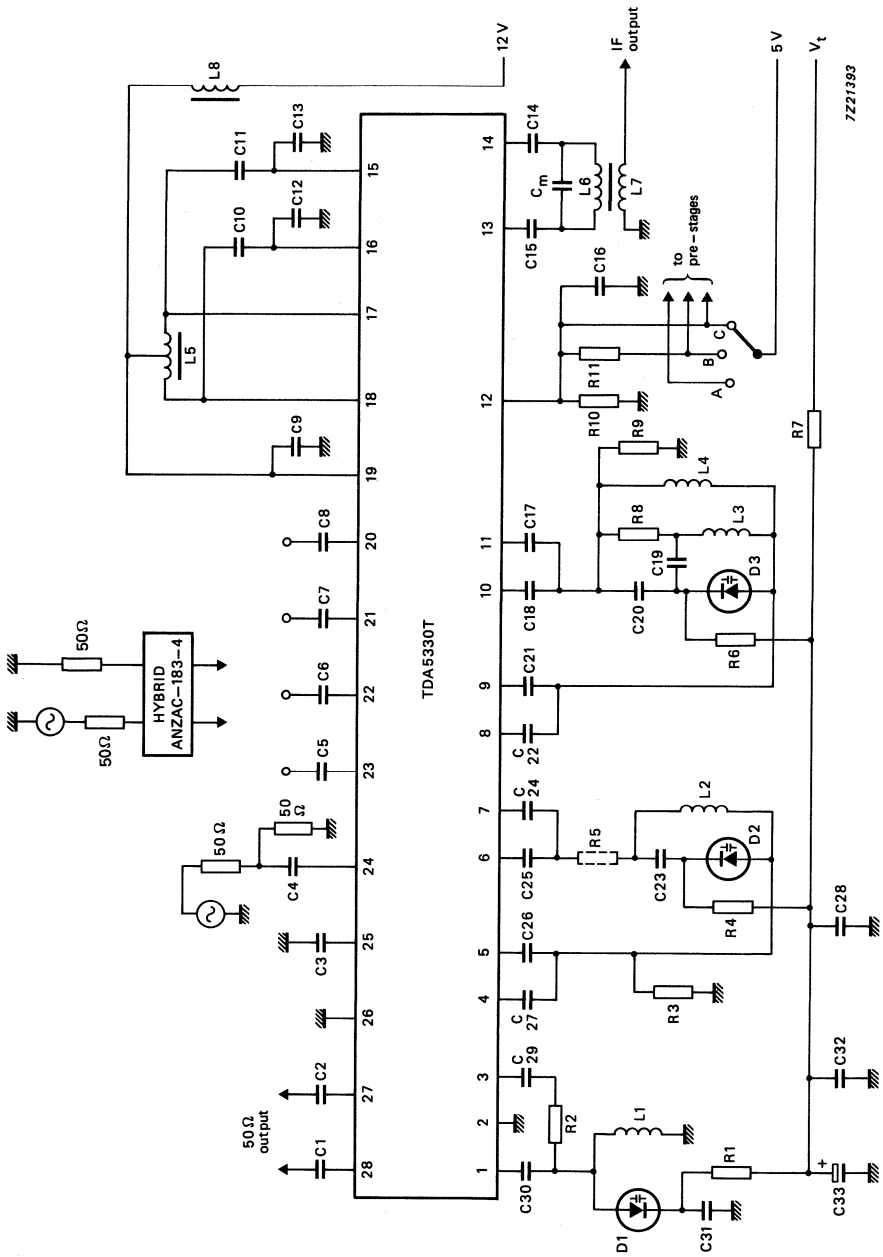


Fig. 9 Test circuit diagram.

DEVELOPMENT DATA

Component values of the test circuit

resistors

R1 = 47 kΩ	R2 = 18 Ω	R3 = 22 kΩ	R4 = 22 kΩ
R5 = 22 Ω (SMD)	R6 = 22 kΩ	R7 = 1 kΩ	R8 = 2.2 kΩ
R9 = 22 kΩ	R10 = 15 kΩ	R11 = 22 kΩ	

capacitors

C1 = 1 nF	C2 = 1 nF	C3 = 1 nF	C4 = 1 nF
C5 = 1 nF	C6 = 1 nF	C7 = 1 nF	C8 = 1 nF
C9 = 1 nF	C10 = 1 nF	C11 = 1 nF	C12 = 15 pF (N750)
C13 = 15 pF (N750)	C14 = 1 nF	C15 = 1 nF	C16 = 1 nF
C17 = 0.68 pF (SMD)	C18 = 1 pF (SMD)	C19 = 100 pF (SMD)	C20 = 5.6 pF (SMD)
C21 = 1 pF	C22 = 0.68 pF (SMD)	C23 = 150 pF (N750)	C24 = 1.8 pF (N750)
C25 = 3.3 pF (SMD)	C26 = 3.3 pF (SMD)	C27 = 1.8 pF (SMD)	C28 = 1 nF
C29 = 1 pF (NPO)	C30 = 1 pF (NPO)	C31 = 82 pF (N750)	C32 = 1 nF
C33 = 1 μF (40 V)	Cm = 18 pF (N750)		

diodes and IC

D1 = BB911	D2 = BB909B	D3 = BB405B
IC = TDA5330T		

coils

L1 = 6.5 t (ϕ3)	L2 = 1.5 t (ϕ3)	L3 = 1.5 t (ϕ3)	L4 = 1.5 t (ϕ3)
L5 = 2 x 6 t*	L6 = 12 t*	L7 = 2 t (mounted on L6)	L8 = 5 μH (choke coil)

wire size for L1 to L4 = 0.4 and for L5 to L7 = 0.1 mm.

* Coil type: TOKO 7 kN; material: 113 kN, screw core (03-0093), pot core (04-0026).

DOUBLE MIXER/OSCILLATOR FOR TV AND VCR TUNERS

GENERAL DESCRIPTION

The TDA5332T is an integrated circuit that performs the mixer/oscillator functions in TV and VCR tuners. This device gives the designer the capability to design an economical and physically small tuner which will be capable of meeting the most stringent requirements e.g. FTZ or FCC. The tuner development time can be drastically reduced by using this device.

Features

- Balanced mixer with a common emitter input for band A
- Amplitude-controlled oscillator for band A
- Balanced mixer with common base input for band B
- Balanced oscillator for band B
- SAW filter preamplifier with an output impedance of 75 Ω in application
- Bandgap voltage stabilizer for oscillator stability
- Electronic bandswitch

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	–	12	–	V
Band A frequency range	depending on application	f_A	45	–	470	MHz
Band B frequency range	depending on application	f_B	160	–	860	MHz
Band A noise factor	50 MHz	NF_A	–	7.5	–	dB
Band B noise factor	860 MHz	NF_B	–	9	–	dB
Band A input voltage	1% cross-modulation	V_{18-20}	–	100	–	dBμV
Band B input power	1% cross-modulation note 5	P_I	–	–21	–	dBm
Band A voltage gain		G_{VA}	–	25	–	dB
Band B voltage gain		G_{VB}	–	36	–	dB

PACKAGE OUTLINE

20-lead mini-pack, plastic (SO20L; SOT163A).

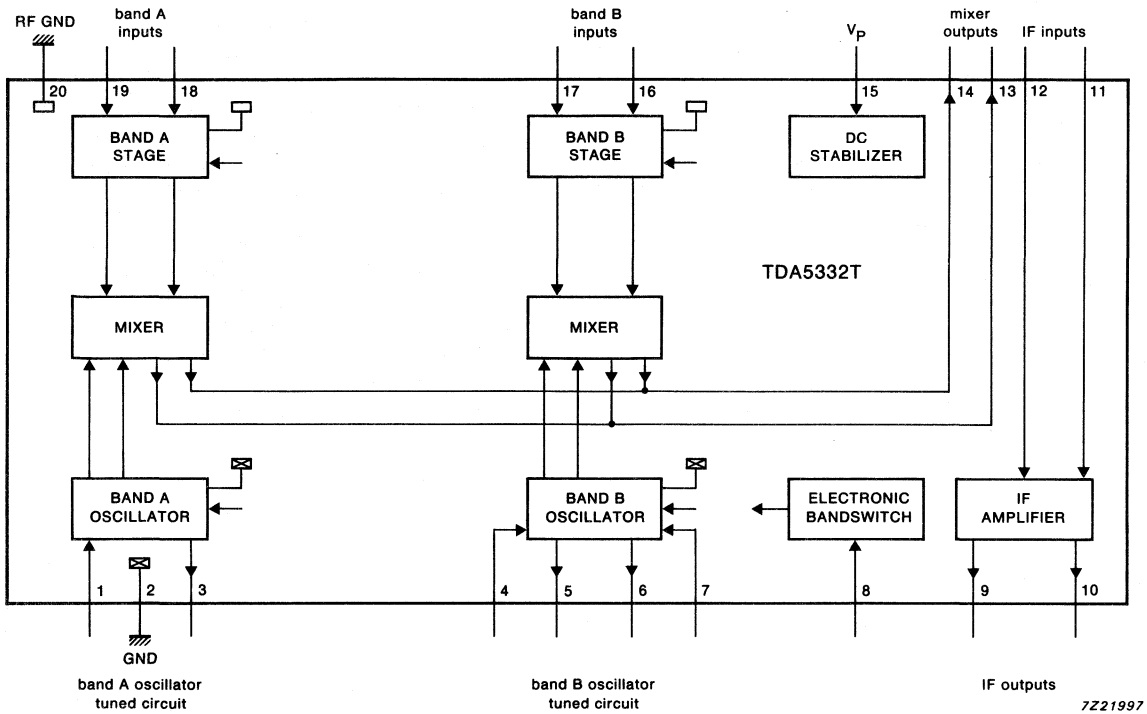


Fig.1 Block diagram.

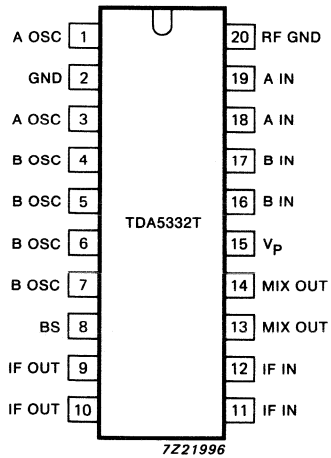


Fig.2 Pinning diagram.

PINNING

1	A OSC	band A oscillator input
2	GND	ground (0 V)
3	A OSC	band A oscillator output
4	B OSC	band B oscillator input
5	B OSC	band B oscillator output
6	B OSC	band B oscillator output
7	B OSC	band B oscillator input
8	BS	electronic bandswitch
9	IF OUT	IF amplifier output
10	IF OUT	IF amplifier output
11	IF IN	IF amplifier input
12	IF IN	IF amplifier input
13	MIX OUT	mixer output
14	MIX OUT	mixer output
15	V_P	positive supply voltage
16	B IN	band B input
17	B IN	band B input
18	A IN	band A input
19	A IN	band A input
20	RF GND	ground for RF inputs

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	−0.3	14	V
Switching voltage		V_8	0	14	V
Output current of each pin to ground		I_O	−	−10	mA
Maximum short-circuit time (all pins)		t_{sc}	−	10	s
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−25	+80	°C
Junction temperature		T_j	−	+150	°C

THERMAL RESISTANCE

From junction to ambient in free air $R_{th\ j\text{-}a}$ typ. 100 K/W

HANDLING

Pins 8, 9 and 10 withstand the ESD test in accordance with MIL-STD-883C category B (2000 V).

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; all voltages are referenced to ground (pins 2 and 20); measured in Fig.3; unless otherwise specified.

parameter	conditions	symbol	min.	typ.		max.	unit
Supply voltage		V_{15}	10	–		13.2	V
Supply current		I_{15}	–	42		55	mA
Switching voltage;							
band A		V_{SA}	0	–		1.1	V
band B		V_{SB}	3	–		5	V
Switching current							
band A		I_{SA}	–	–		10	μA
band B		I_{SB}	–	–		50	μA
IF Amplifier	differentially measured at 36 MHz			mod.	phase		
Input reflection coefficient	note 4	S_{11}	–	–0.5	–2	–	dB/°
Reverse transmission coefficient		S_{12}	–	–41	–7	–	dB/°
Forward transmission coefficient		S_{21}	–	12	160	–	dB/°
Output reflection coefficient		S_{22}	–	–9	10	–	dB/°
Input admittance in application		Y_I	–	–	1.4	–	mS
					0.9	–	pF
Output admittance in application		Z_O	–	–	55	–	Ω
					230	–	nH
Band A mixer (including IF amplifier)	measured using circuit shown in Fig.3						
Frequency range		f_A	45	–		470	MHz
Noise factor	50 MHz	NF	–	7.5		9	dB
	225 MHz	NF	–	9		11	dB
	300 MHz	NF	–	10		12	dB
	470 MHz	NF	–	11		13	dB
Optimum source conductance	50 MHz	$G_{18\text{-}20}$	–	0.5		–	mS
	225 MHz	$G_{18\text{-}20}$	–	1.1		–	mS
	300 MHz	$G_{18\text{-}20}$	–	1.2		–	mS
	470 MHz	$G_{18\text{-}20}$	–	1.9		–	mS

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance	50 - 470 MHz	$C_{18\text{-}20}$	–	2.5	–	pF
Input voltage	1% cross-modulation; in channel	$V_{18\text{-}20}$	97	100	–	dBμV
Input voltage	10 kHz pulling; in channel; f < 300 MHz	$V_{18\text{-}20}$	100	108	–	dBμV
Voltage gain	20 log ($V_{9\text{-}10}/V_{18}$)	G_V	22.5	25.0	27.5	dB
Band A mixer						
Conversion transadmittance mixer	$I_{13}/V_{18} = -I_{14}/V_{18}$	C_t	–	3.5	–	mS
Mixer output admittance	pins 13 and 14		–	0.1	–	mS
Mixer output capacitance		$C_{13\text{-}14}$	–	2	–	pF
Band A oscillator						
Frequency range		f_A	80	–	520	MHz
Frequency shift	ΔV_P = 10% note 6; f = 330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 25 °C note 7; f = 330 MHz	Δf	–	–	400	kHz
Frequency drift	5 s to 15 min after switching on; f = 330 MHz	Δf	–	–	200	kHz
Band B mixer (including IF)	measured using circuit shown in Fig.3; measurements using hybrid; note 1					
Frequency range		f_B	160	–	860	MHz
Noise factor not corrected for image	pins 16 and 17					
	160 MHz	NF_B	–	9	11	dB
	860 MHz	NF_B	–	9	11	dB
Available input power	note 5; 1% cross-modulation; in channel; pins 16 and 17;					
	160 MHz	P_{IB}	–25	–21	–	dBm
	860 MHz	P_{IB}	–25	–21	–	dBm
10 kHz pulling	note 5; pins 16 and 17; in channel;					
	860 MHz		–	–20	–	dBm

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
N + 5 – 1 MHz pulling	notes 2 and 5; 820 MHz		–42	–35	–	dBm
Voltage gain	note 3;					
	160 MHz	G_{VB}	33	36	39	dB
	860 MHz	G_{VB}	33	36	39	dB
Band B oscillator						
Frequency range		f_B	200	–	900	MHz
Frequency shift	note 6;					
	ΔV_P = 10%	Δf	–	–	400	kHz
Frequency drift	note 7;					
	ΔT = 25 °C	Δf	–	–	800	kHz
Frequency drift	5 s to 15 min					
	after switching on	Δf	–	–	400	kHz

Notes to the characteristics

1. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
2. The input level of a N + 5 – 1 MHz signal (just visible).
3. The gain is defined as the transducer gain (measured in Fig.3) plus the voltage transformation ratio of L6 to L7 (6:1, 16 dB).
4. All S parameters are referred to a 50 Ω system.
5. The input power is defined as the power delivered by the generator on a 50 Ω load.
6. The frequency shift is defined for a variation of power supply from;

   (a) V_P = 12 V to V_P = 10.8 V
   (b) V_P = 12 V to V_P = 13.2 V

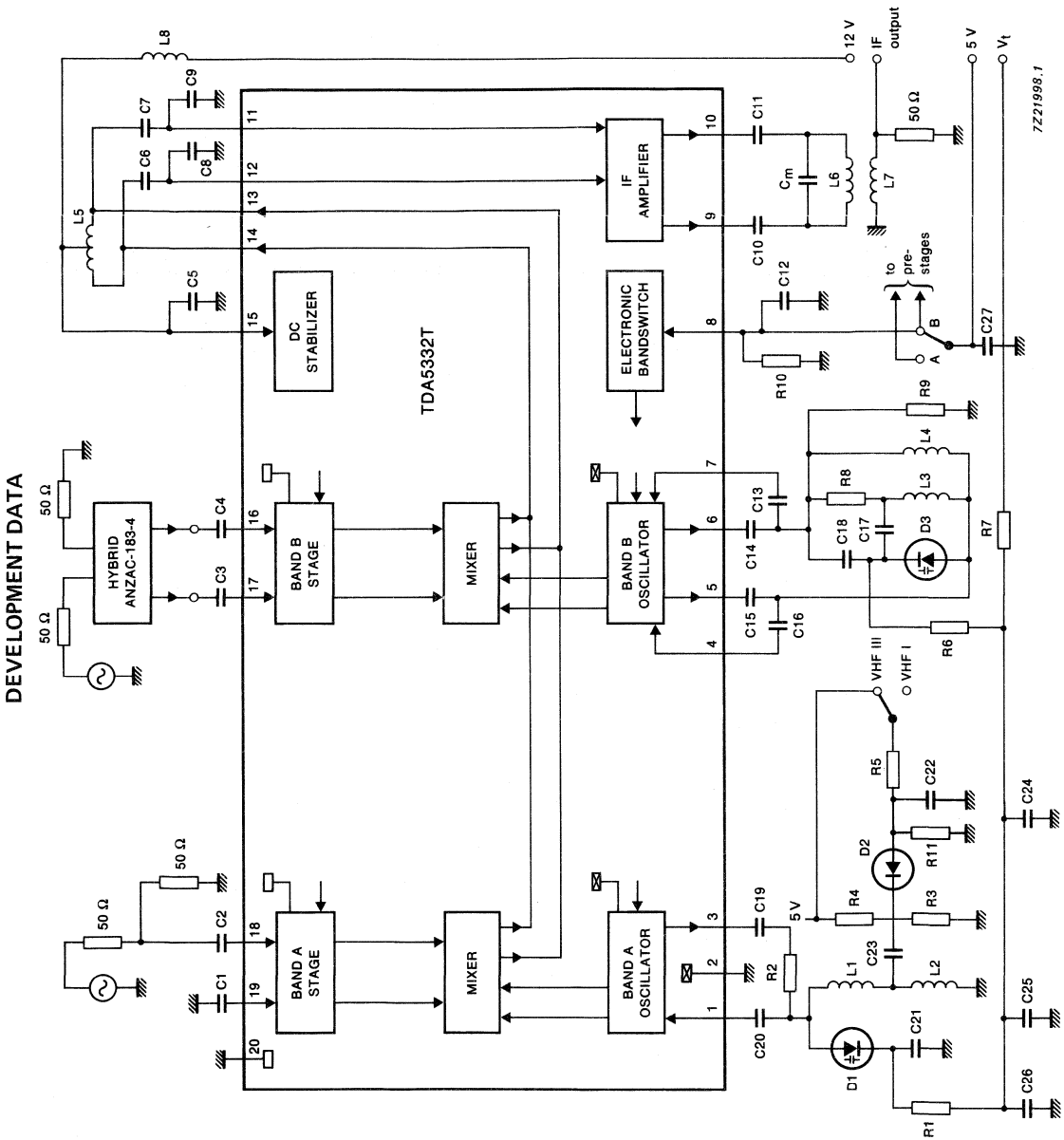
   In both cases the frequency shift is below the specified value.
7. The frequency drift is defined for a variation of ambient temperature from;

   (a) T_{amb} = 25 °C to T_{amb} = 0 °C
   (b) T_{amb} = 25 °C to T_{amb} = 50 °C

   In both cases the frequency shift is below the specified value.

APPLICATION INFORMATION

DEVELOPMENT DATA



Proposal of VHF/UHF tuner band A = VHF I + VHF III (45 to 300 MHz)
band B = UHF (470 to 900 MHz)

Fig.3 Application diagram.

Component values of the application diagram

resistors

R1 = 47 kΩ	R2 = 18 Ω	R3 = 1.2 kΩ	R4 = 4.7 kΩ
R5 = 100 Ω	R6 = 22 kΩ	R7 = 1 kΩ	R8 = 2.2 kΩ
R9 = 22 kΩ	R10 = 15 kΩ	R11 = 47 kΩ	

capacitors

C1 = 1 nF	C2 = 1 nF	C3 = 1 nF	C4 = 1 nF
C5 = 1 nF	C6 = 1 nF	C7 = 1 nF	C8 = 15 pF (N750)
C9 = 15 pF (N750)	C10 = 1 nF	C11 = 1 nF	C12 = 1 nF
C13 = 0.68 pF (SMD)	C14 = 1 pF (SMD)	C15 = 1 pF (SMD)	
C16 = 0.68 pF (SMD)	C17 = 100 pF (SMD)	C18 = 5.6 pF (SMD)	C19 = 1 pF (NPO)
C20 = 1 pF (NPO)	C21 = 82 pF (N750)	C22 = 1 nF	C23 = 1 nF
C24 = 1 nF	C25 = 1 nF	C26 = 1 μF (40V)	C27 = 1 nF

Cm = 18 pF (N750)

diodes and IC

D1 = BB911	D2 = BA482	D3 = BB405B	IC = TDA5332T

coils

L1 = 2.5 t (ϕ3)	L2 = 8.5 t (ϕ3)	L3 = 1.5 t (ϕ3)
L4 = 1.5 t (ϕ3)	L5 = 2 x 5 t*	L8 = 5 μH (choke coil)

transformer

L6 = 12 t*	L7 = 2 t

wire size for L1 to L4 = 0.4 and for L5 to L7 = 0.1 mm.

* Coil type: TOKO 7 kN; material: 113 kN, screw core (03-0093), pot core (04-0026).

Low-power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners

TDA5630T/TDA5630M

FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for bands A and B
- Balanced mixer with a common base input for bands B and C (balanced input)
- 3-pin oscillator for band C
- Local oscillator buffer output for external synthesizer
- SAW filter preamplifier with a low output impedance to drive the SAW filter directly
- Bandgap voltage stabilizer for oscillator stability
- Electronic bandswitch.

DESCRIPTION

The TDA5630 is a monolithic integrated circuit that performs the bands A, B and C mixer/oscillator functions in TV and VCR tuners. This low-power mixer/oscillator requires a power supply of 9 V and is available in a very small package.

The device gives the designer the capability to design an economical and physically small 3-band tuner.

The tuner development time can be drastically reduced by using this device. In addition, when hyperband is not necessary, the TDA5630 may be used in a VHF/UHF tuner with an appropriate tuned circuit for VHF I and VHF III in band A, and the tuned circuit of band C for UHF.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		–	9.0	–	V
I_P	positive supply current		–	35	–	mA
f_{RA}	frequency range, band A	RF input	45	–	180	MHz
f_{RB}	frequency range, band B	RF input	160	–	470	MHz
f_{RC}	frequency range, band C	RF input	430	–	860	MHz
NF_A	noise figure, band A		–	7.5	–	dB
NF_B	noise figure, band B		–	8	–	dB
NF_C	noise figure, band C		–	9	–	dB
V_{IA}	input voltage, band A	1% cross-modulation	–	93	–	dBμV
V_{IB}	input voltage, band B	1% cross-modulation	–	82	–	dBμV
V_{IC}	input voltage, band C	1% cross-modulation	–	82	–	dBμV
G_v	voltage gain					
	band A		–	25	–	dB
	band B		–	36	–	dB
	band C		–	36	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5630T	20	SO20-L	plastic	SOT163A
TDA5630M	20	SSOP	plastic	SOT266A

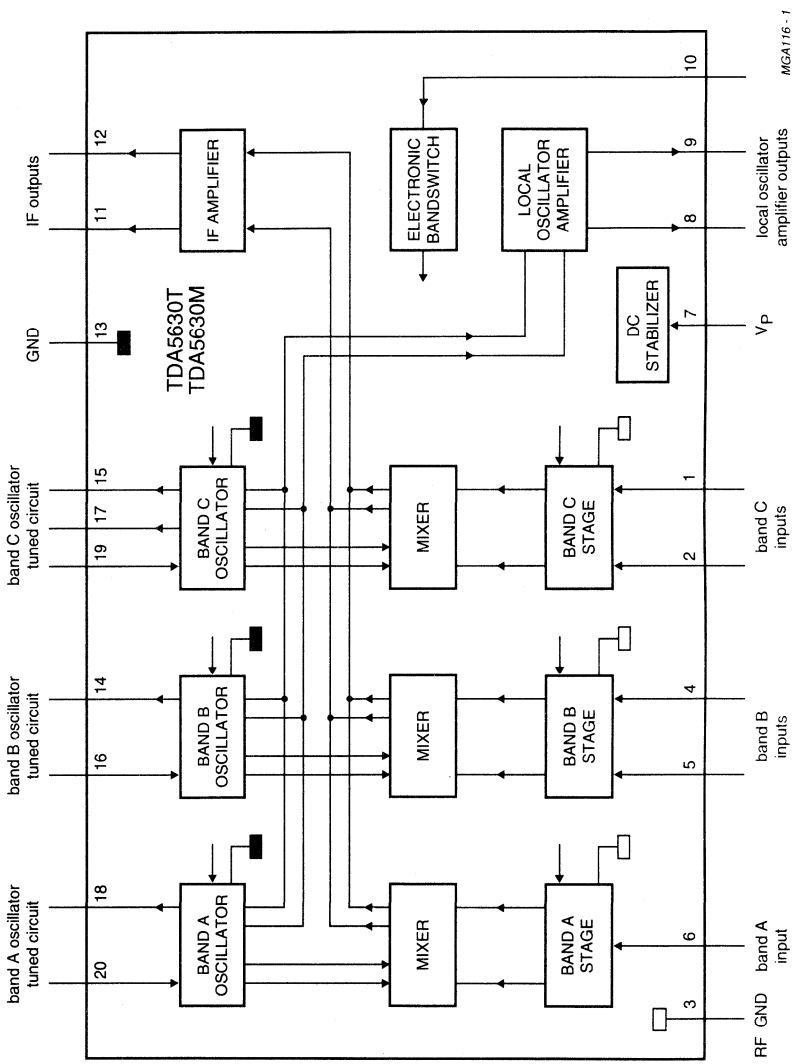


Fig. 1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
C IN	1	band C input
C IN	2	band C input
RF GND	3	ground for RF inputs
B IN	4	band B input
B IN	5	band B input
A IN	6	band A input
VP	7	positive supply voltage
LO OUT	8	local oscillator amplifier output
LO OUT	9	local oscillator amplifier output
BS	10	electronic bandswitch
IF OUT	11	IF amplifier output
IF OUT	12	IF amplifier output
GND	13	ground (0 V)
B OSC	14	band B oscillator output collector
C OSC	15	band C oscillator output collector
B OSC	16	band B oscillator input base
C OSC	17	band C oscillator output collector
A OSC	18	band A oscillator output collector
C OSC	19	band C oscillator input base
A OSC	20	band A oscillator input base

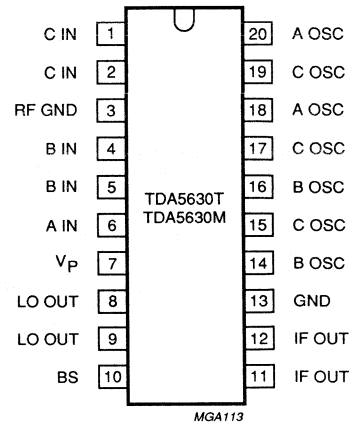


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

t.b.f.

LIMITING VALUES

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range	−0.3	+10.5	V
V_{SW}	switching voltage	0	10.5	V
I_O	output current of each pin to ground	–	−10	mA
t_{sc}	maximum short-circuit time (all pins)	–	10	s
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−10	+80	°C
T_j	junction temperature	–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT163A)	100 K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT266)	120 K/W

HANDLING

Human body model

The IC withstands 3000 V in accordance with UZW-BO-FQ-A302,(stress reference pins 3 and 13 shorted together).

Machine model

The IC withstands 200 V in accordance with UZW-BO-FQ-B302,(stress reference pins 3 and 13 shorted together).

CHARACTERISTICS

Measured in circuit of Fig.4, V_P = 9 V, T_{amb} = 25 °C, unless otherwise specified.

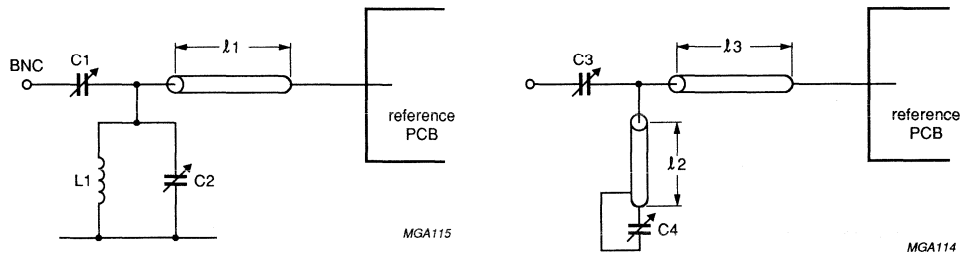
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.		MAX.	UNIT
Supply							
V_P	positive supply voltage		8.1	9		9.9	V
I_P	positive supply current		–	35		45	mA
V_{SW}	switching voltage						
	band A		0	–		1.1	V
	band B		1.6	–		2.4	V
	band C		3.0	–		5.0	V
I_{SW}	switching current						
	band A		–	–		2	µA
	band B		–	–		5	µA
	band C		–	–		10	µA
IF amplifier (differentially measured at 36 MHz)							
				MOD.	PHASE		
S_{22}	output reflection coefficient	see Fig.9	–	–10	9	–	dB/°C
Z_O	output impedance (RS + jLSΩ)						
	R_S		–	95		–	Ω
	L_S		–	45		–	nH
Band A mixer (pin 6); (including IF amplifier)							
f_R	frequency range		45	–		180	MHz
NF	noise figure	note 1					
		50 MHz	–	7.5		9	dB
		180 MHz	–	9		10	dB
g	source conductance for optimum noise figure						
		50 MHz	–	0.5		–	mS
		180 MHz	–	1.1		–	mS
g_i	input conductance	see Fig.5					
		50 MHz	–	0.26		–	mS
		180 MHz	–	0.35		–	mS
C_I	input capacitance	50 to 180 MHz	–	2		–	pF
V_I	input voltage	in channel f = 180 MHz					
		1% cross modulation	90	93		–	dBµV
		10 kHz pulling	–	100		–	dBµV
G_v	voltage gain	20 log (V12-11/V6)					
		50 MHz	22.5	25		27.5	dB
		180 MHz	22.5	25		27.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band A oscillator						
f_R	frequency range		80	–	216	MHz
f_S	frequency shift	note 2; ΔV_P = 10%	–	–	200	kHz
Δf	frequency drift	note 3				
		ΔT = 25 °C with no compensation; NPO capacitors	–	–	500	kHz
		5 s to 15 min after switch on	–	–	200	kHz
Band B mixer (pins 4 and 5); (including IF amplifier) measurements using hybrid; note 4						
f_R	frequency range		160	–	470	MHz
NF	noise figure (not corrected for image)					
		170 MHz	–	8	10	dB
		470 MHz	–	8	10	dB
Z_I	input impedance ($R_S + jL_S\Omega$)	(see Fig.6)				
	R_S		–	30	–	Ω
	L_S		–	8	–	nH
V_I	input voltage	1% cross-modulation; in channel				
		170 MHz	79	82	–	dBμV
		470 MHz	79	82	–	dBμV
		10 kHz pulling; in channel; 470 MHz				
	TDA5630T		–	91	–	dBμV
	TDA5630M		–	83	–	dBμV
		N + 5 – 1 MHz pulling; 430 MHz; note 5				
	TDA5630T		–	81	–	dBμV
	TDA5630M		–	66	–	dBμV
G_v	voltage gain	note 6				
		170 MHz	33	36	39	dB
		470 MHz	33	36	39	dB
Band B oscillator						
f_R	frequency range		200	–	500	MHz
f_S	frequency shift	note 2; ΔV_P = 10%	–	–	400	kHz
Δf	frequency drift	note 3				
		ΔT = 25 °C with no compensation: NPO capacitors	–	–	2	MHz
		5 s to 15 min after switch on	–	–	300	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band C mixer (pins 1 and 2) (including IF amplifier); measurements using hybrid; note 4						
f_R	frequency range		430	–	860	MHz
NF	noise figure (not corrected for image)	430 MHz	–	9	11	dB
		860 MHz	–	9	11	dB
Z_I	input impedance ($R_S + jL_S\Omega$)	see Fig.7				
	R_S	430 MHz	–	40	–	Ω
		860 MHz	–	53	–	Ω
	L_S	430 - 360 MHz	–	9	–	nH
V_I	input voltage	1% cross-modulation; in channel				
		430 MHz	79	82	–	dBμV
		860 MHz	79	82	–	dBμV
	TDA5630T	10 kHz pulling; in channel; 860 MHz	–	87	–	dBμV
	TDA5630M		–	93	–	dBμV
		N + 5 – 1 MHz pulling note 5; 820 MHz	–	61	–	dBμV
G_v	voltage gain	note 6				
		430 MHz	33	36	39	dB
		860 MHz	33	36	39	dB
Band C oscillator						
f_R	frequency range		470	–	900	MHz
f_S	frequency shift	note 2; ΔV_P = 10%	–	–	400	kHz
Δf	frequency drift	note 3				
		ΔT = 25 °C with no compensation: NPO capacitors	–	–	2.5	MHz
		5 s to 15 min after switching on	–	–	600	kHz
LO output (pins 8 and 9; R_L = 100 Ω)						
S_{22}	output reflection coefficient	see Fig.8				
V_{LO}	output voltage		14	35	100	mV
SRF	spurious signal on LO output w.r.t. LO output signal	note 8	–	–	–10	dB
SHD	LO signal harmonics w.r.t. LO signal		–	–	–10	dB

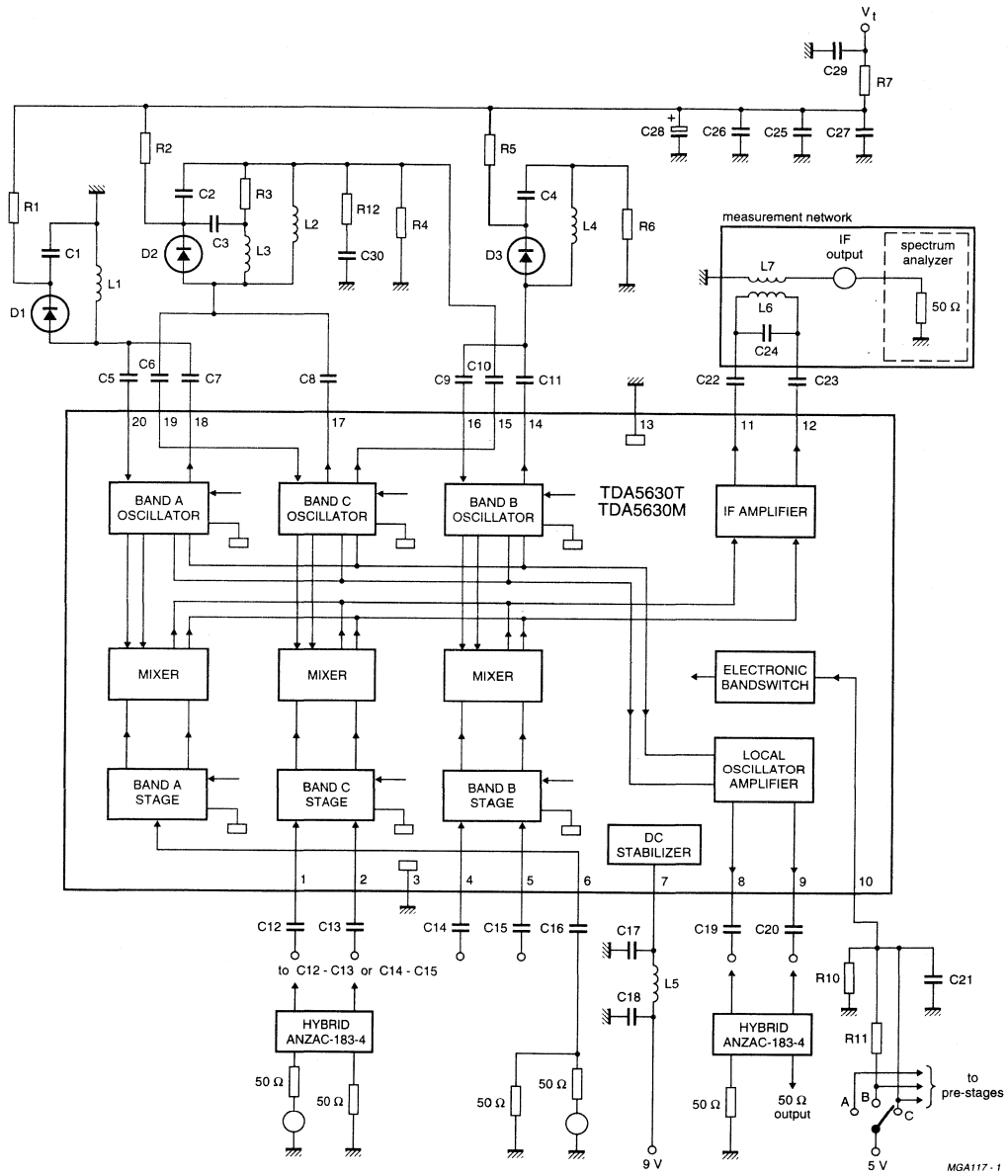
Notes to the characteristics

1. These measurements were made with an input circuit for optimum noise figure, as shown in Fig.3.
   for **f = 50** MHz:
   measured frequency = 57 MHz, loss = 0 dB
   image suppression = 16 dB
   C1 = 9 pF
   C2 = 15 pF
   L1 = 7 turns (dia. 5.5 mm, wire dia. 0.5 mm)
   l1 = rigid cable (RIM), length 5 cm, 33 dB/100 m, 50 Ω, 96 pF/m.
   for **f = 180** MHz:
   measured frequency = 150.3 MHz, loss = 1.3 dB
   image suppression = 13 dB
   C3 = 5 pF
   C4 = 25 pF
   l2 = rigid cable (RIM), length 30 cm, 33 dB/100 m, 50 Ω, 96 pF/m
   l3 = rigid cable (RIM), length 5 cm, 33 dB/100 m, 50 Ω, 96 pF/m.
2. The frequency shift is defined for a variation of power supply, first from V_P = 9 V to V_P = 8.1 V, then from V_P = 9 V to V_P = 9.9 V. In both cases, the frequency shift is below the specified value.
3. The frequency drift is defined for a variation of ambient temperature, first from T_{amb} = 25 °C to T_{amb} = 0 °C, then from T_{amb} = 25 °C to T_{amb} = 50 °C. In both cases, the frequency drift is below the specified value with NPO capacitors. Capacitor types C1 to C11, as specified in Fig.4 for non-PLL applications, must be changed to series with other temperature coefficients (e.g. N330, N750 etc.)
4. The values have been corrected for hybrid and cable losses. The symmetrical output impedance of the circuit is 100 Ω.
5. The input level of a N + 5 – 1 MHz signal which gives a signal 30 dB below the oscillator carrier at the LO output.
6. The gain is defined as the transducer gain (measured in Fig.4) plus the voltage transformation ratio of L6 to L7 (6:1, 15.4 dB).
7. Measured at 50 Ω, with RF input voltage:
   RF voltage = 120 dBμV at f < 180 MHz
   RF voltage = 107.5 dBμV at 180 MHz < f < 225 MHz
   RF voltage = 97 dBμV at 225 MHz < f < 860 MHz.
8. All S-parameters are referred to a 50 Ω system.



(1) f = 50 MHz.
(2) f = 180 MHz.

Fig.3 Input circuit for optimum noise figure.



L6, L7 and C24 are only required for measurement purposes; they are not used in a tuner.

Fig.4 Measurement circuit.

Component values for measurement circuit

COMPONENT	VALUE	REMARKS
Resistors (all SMD)		
R1	47 kΩ	
R2	22 kΩ	
R3	2.2 kΩ	
R4	22 kΩ	
R5	47 kΩ	
R6	22 Ω	
R7	1 kΩ	
R10	15 kΩ	
R11	36 kΩ	
R12	470 Ω	
Capacitors (all SMD and NPO except C28)		
C1	82 pF	
C2	5.6 pF	
C3	100 pF	
C4	150 pF	
C5	2.2 pF	
C6	1 pF	
C7	2.2 pF	
C8	1 pF	
C9	1.8 pF	
C10	2.2 pF	
C11	3.9 pF	
C12	1 nF	
C13	1 nF	
C14	1 nF	
C15	1 nF	
C16	1 nF	
C17	1.5 nF	
C18	1.5nF	
C19	1 nF	
C20	1 nF	
C21	1.5 nF	
C22	1 nF	
C23	1 nF	
C24	18 pF	
C25	1.5 nF	
C26	1.5 nF	

COMPONENT	VALUE	REMARKS
C27	1.5 nF	
C28	1 μF	40 V electrolytic
C29	1.5 nF	
C30	0.56 pF	
Diodes and IC		
D1	BB911	
D2	BB405/215	
D3	BB909/219	
IC	TDA5630T/ TDA5630M	
Coils		
L1	7.5 turns	dia. 3 mm, wire size 0.4 mm
L2	2.5 turns	dia. 3 mm, wire size 0.4 mm
L3	1.5 turns	dia. 2.5 mm, wire size 0.4 mm
L4	1.5 turns	dia. 4 mm, wire size 0.4 mm
L5	4.7 μH	choke coil
Transformer		
L6	2 x 5 turns	coil type: TOKO 7 kN; material: 113 kN; screw core 03-0093; pot core 04-0026
L7	2 turns	

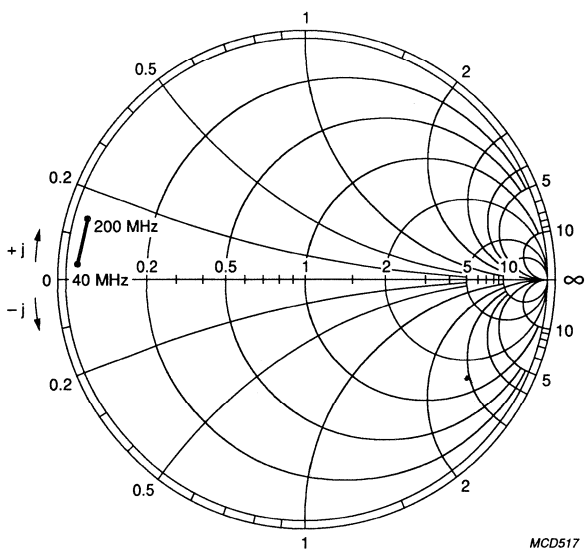


Fig.5 Input admittance (S_{11}) of the band A mixer input (40 to 200 MHz) (Y chart).

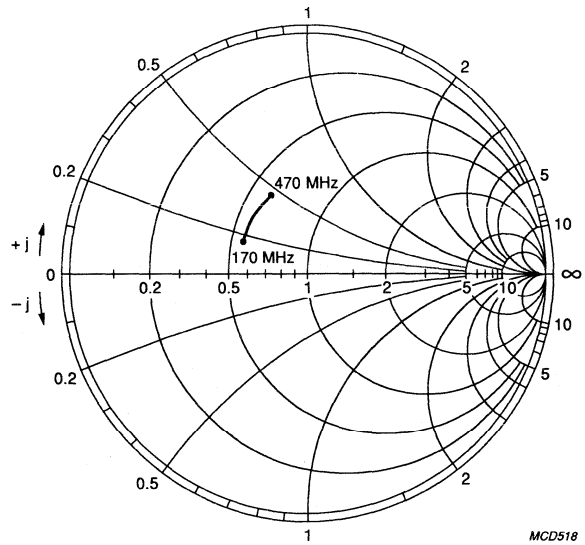


Fig.6 Input admittance (S_{11}) of the band B mixer input (170 to 470 MHz) (Z chart).

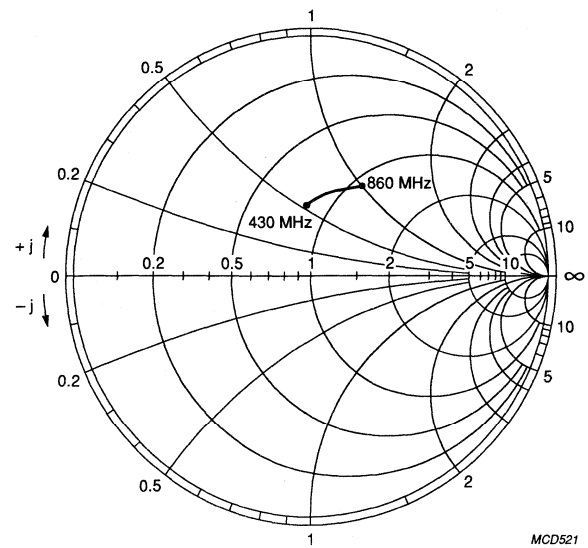


Fig.7 Input admittance (S_{11}) of the band C mixer input (430 to 860 MHz) (Z chart).

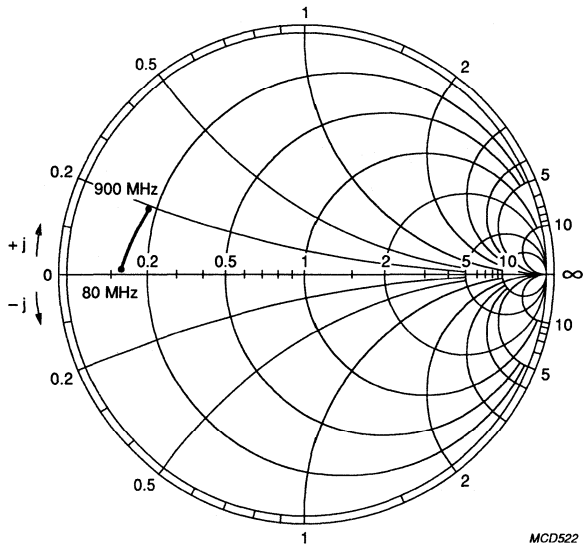


Fig.8 Output reflection coefficient (S_{22}) of the LO output (80 to 900 MHz) (Y chart).

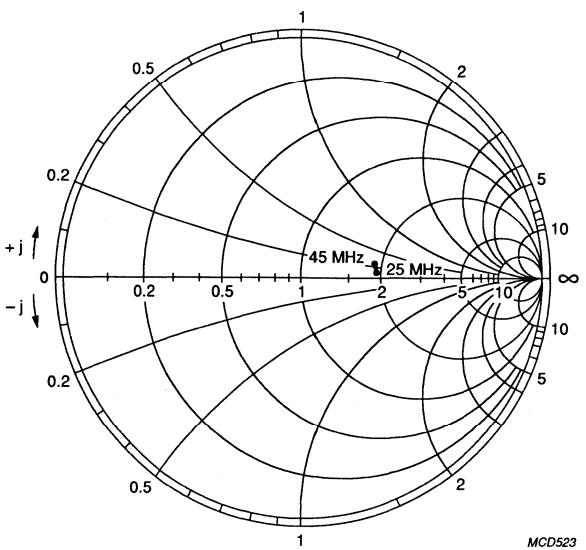


Fig.9 Output reflection coefficient (S_{22}) of the IF amplifier (25 to 45 MHz) (Z chart).

8 MHz VIDEO OUTPUT AMPLIFIER

GENERAL DESCRIPTION

The TDA6100Q is a video amplifier in a SIL 9 MP (Single In Line 9 pins Medium Power) package, using high-voltage DMOS technology and is intended to directly drive the cathode of a cathode ray tube (CRT).

Features

- High bandwidth and slew rate
- No external heatsink required
- Black-current measurement output for automatic black-current stabilization (ABS)
- A cathode output separated from the feedback output
- Internal protection against CRT flashover discharges
- Protection against electrostatic discharge (ESD)
- Simple application with a variety of colour decoders
- Differential input with designed-in maximum values of the following:
  - common mode input capacitance of 3 pF
  - differential mode input capacitance of 2 pF
  - differential input voltage temperature drift of 0.4 mV/K

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
High supply voltage	V_{P1}	180	–	210	V
Low supply voltage	V_{P2}	10.8	–	13.2	V
Total power dissipation	P_{tot}	0	–	1.9	W
Operating ambient temperature range	T_{amb}	0	–	+ 65	°C

PACKAGING OUTLINE

9-lead SIL; plastic (SOT111B).

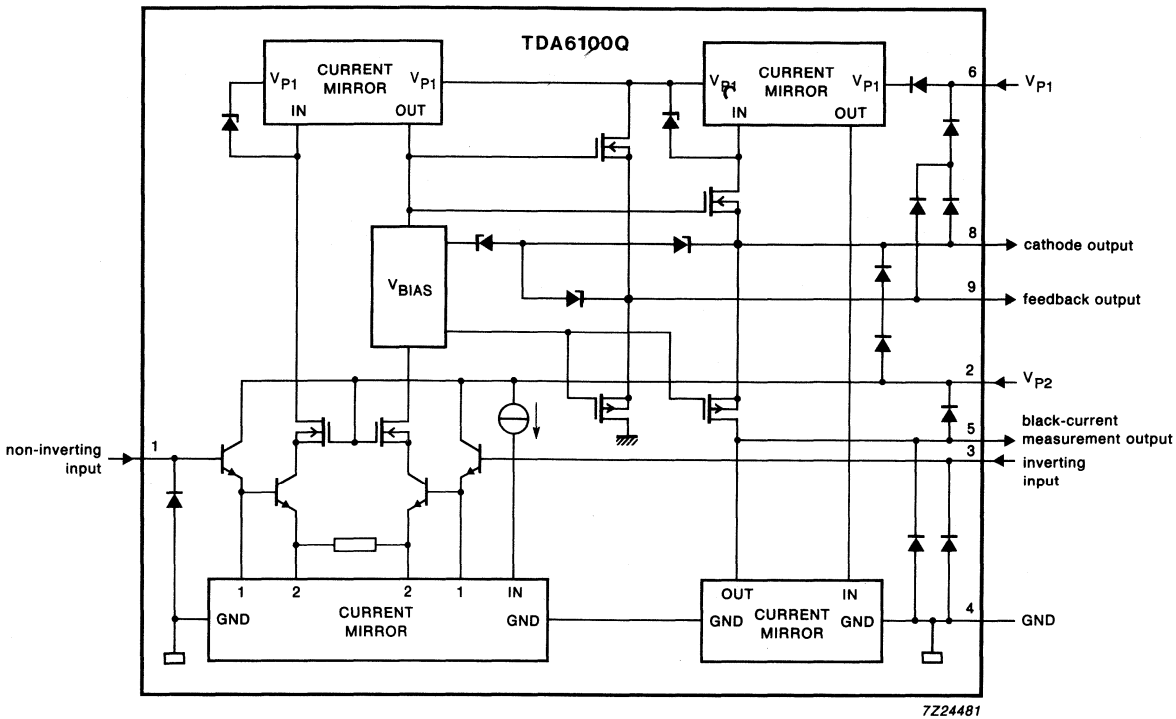


Fig.1 Block diagram.

PINNING

1 Non-inverting input
2 Low supply voltage
3 Inverting input
4 Ground, substrate, heat tab
5 Black-current measurement output
6 High supply voltage
7 Not connected
8 Cathode output
9 Feedback output

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	typ.	max.	unit
High supply voltage		V_{P1}	0	–	250	V
Low supply voltage		V_{P2}	0	–	14	V
Input voltage (pins 1 and 3)		V_1, V_3	0	–	V_{P2}	V
Differential mode input voltage (pin 1 to 3)		V_{1-3}	–6	–	6	V
Black-current measurement output voltage (pin 5)		V_5	0	–	V_{P2}	V
Cathode and feedback output voltage (pins 8 and 9)		V_8, V_9	V_{P2}	–	V_{P1}	V
Non-inverting and inverting input current (pins 1 and 3)		I_1, I_2	0	–	1	mA
Cathode and feedback repetitive peak output current (pins 8 and 9)		I_8, I_9	–25	–	+ 25	mA
Cathode non-repetitive peak output current						
LOW	Q = 50 μC	I_8	–2.5	–	+ 2.5	A
HIGH	Q = 100 nC	I_8	–10	–	+ 10	A
Total power dissipation		P_{tot}	0	–	1.9	W
Storage temperature range		T_{stg}	–65	–	+ 150	°C
Junction temperature range		T_j	0	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 45 K/W

From junction to case $R_{th\ j\text{-}c}$ = 10 K/W

CHARACTERISTICS

Operating range

V_{P1} = 180 to 210 V; V_{P2} = 10.8 to 13.2 V; V_1 = 2.6 to 5 V; V_5 = 1.4 V to the smallest of (V_8 − 8 V) or V_{P2}; T_{amb} = 0 to 65 °C.

Test conditions (unless otherwise specified)

V_{P1} = 200 V; V_{P2} = 12 V; V_5 = 6 V; T_{amb} = 25 °C; C_L = 10 pF; V_1 = 5 V (C_L consists of parasitic and cathode capacitance). For test circuit see Fig.2.

parameter	conditions	symbol	min.	typ.	max.	unit
Quiescent current						
high voltage supply	$V_8 = V_{P1}/2$	I_{P1}	4	4.9	6	mA
low voltage supply	$V_8 = V_{P1}/2$	I_{P2}	2.5	3.1	3.8	mA
Input bias current	$V_8 = V_{P1}/2$		0	–	20	μA
Input offset current	$V_8 = V_{P1}/2$		−3	–	+3	μA
Offset current of black-current measurement output	I_8 = 0 A; 50 V < V_8 < V_{P1} − 20 V; 1.4 V < V_5 < V_{P2}	$I_{5(off)}$	−10	0	+10	μA
Linearity of current transfer						
LOW I_8	I_8 = 0 to 10 μA; 50 V < V_8 < V_{P1} − 20 V; 1.4 V < V_5 < V_{P2}	$\Delta I_5/\Delta I_8$	0.9	1	1.1	
HIGH I_8	I_8 = 0 to 3 mA; 50 V < V_8 < V_{P1} − 20 V; 1.4 V < V_5 < V_{P2}	$\Delta I_5/\Delta I_8$	0.9	1	1.1	
Maximum peak output current (pins 8 and 9)	20 V < V_8 < V_{P1} − 20 V	$\lvert I_{O\,max}\rvert$	–	20	–	mA
Input offset voltage	$V_8 = V_{P1}/2$	$V_{I(off)}$	−50	–	+50	mV
Output voltage (pins 8 and 9)						
minimum	V_{1-3} = −1 V	$V_{O\,min}$	–	–	20	V
maximum	V_{1-3} = 1 V	$V_{O\,max}$	V_{P1} −20	–	–	V
Gain-bandwidth product of open loop gain V_9/V_{1-3}	f = 500 kHz; $V_{8(p-p)}$ = 60 V	BW_g	–	0.7	–	GHz
Small signal bandwidth	$V_{8(p-p)}$ = 60 V sine	BW_s	6.5	8	–	MHz
Large signal bandwidth	$V_{8(p-p)}$ = 100 V sine	BW_l	5	6.5	–	MHz
Cathode output propagation time 50% input – 50% output	V_8 = 50 to 150 V square wave; f < 1 MHz; t_f input < 20 ns	t_p	40	51	62	ns

parameter	conditions	symbol	min.	typ.	max.	unit
Cathode output rise time 10% output – 90% output	V_8 = 50 to 150 V square wave; f < 1 MHz; t_f input < 20 ns	t_r	40	53	65	ns
Cathode output fall time 90% output – 10% output	V_8 = 150 to 50 V square wave; f < 1 MHz; t_r input < 20 ns	t_f	40	53	65	ns
Settling time; 50% input – 99% < output < 101%	$V_{8(p-p)}$ = 100 V square wave; f < 1 MHz; t_r, t_f input < 20 ns	t_s	–	–	220	ns
Slew rate between 50 and 150 V	$V_{1-3(p-p)}$ = 2 V square wave; f < 1 MHz; t_r, t_f input < 20 ns	SR	–	1700	–	V/μs
Cathode output voltage overshoot	$V_{8(p-p)}$ = 100 V square wave; f < 1 MHz; t_r, t_f input < 20 ns; note 1	OV	–	–	5	%
Differential input resistance		R_I	–	100	–	kΩ
High voltage power supply rejection ratio	f < 50 kHz; note 2	HVPSRR	–	80	–	dB
Low voltage power supply rejection ratio	f < 50 kHz; note 2	LVPSRR	–	80	–	dB

DEVELOPMENT DATA

Notes to the characteristics

1. If $V_{P2} - V_1 < 7$ V, there can be more overshoot than specified.
2. PSRR: the ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.
3. The above electrical characteristics and stable operation are specified for a feedback range of 1/75 to 1/90.
4. The cathode output is protected against peak currents (caused by high-resistance flash) of 2.5 A maximum with a charge content of 50 μC.
5. The cathode output is also protected against peak currents (caused by low-resistance flash) of 10 A maximum with a charge content of 100 nC.

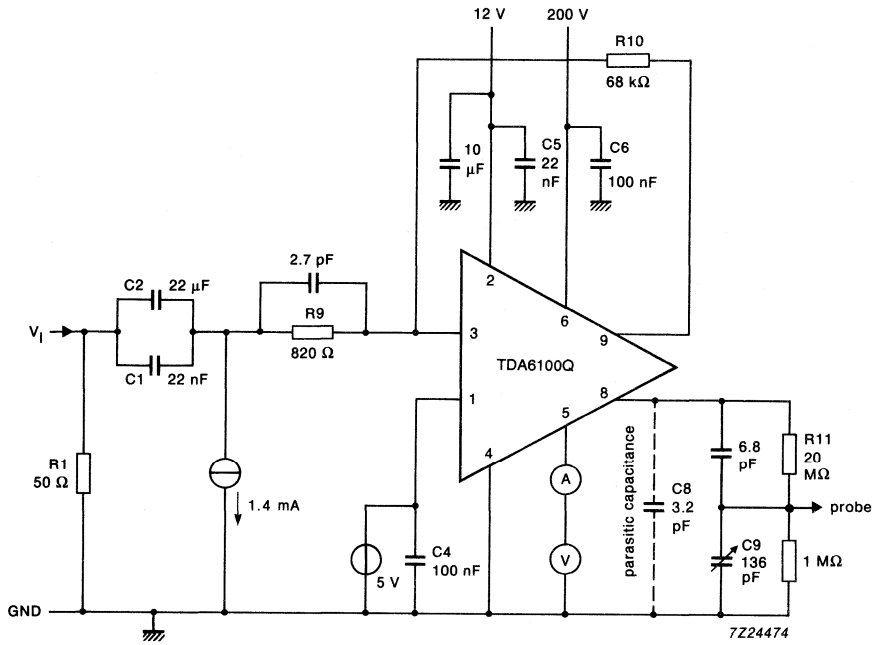


Fig.2 Test circuit with feedback factor of 1/83.

FLASHOVER PROTECTION

The device incorporates protection diodes to prevent CRT flashover discharges; these diodes clamp the cathode output voltage between $V_{P1} + V_{diode}$ and $V_{P2} - V_{diode}$. To limit the diode current the following is needed: an external 1.5 kΩ high-voltage carbon resistor in series with the cathode output and a 1 kV spark-gap (see Fig.9).

V_{P1} – GND has to be decoupled:

- With a capacitor > 20 nF with good HF characteristics (e.g. ceramic). This capacitor (between pins 6 and 4) must be placed as near as possible to the device and no more than 10 mm away from it.
- With a capacitor > 10 µF on the CRT's printed-circuit board (common for the three output stages).

V_{P2} – GND has to be decoupled with a capacitor > 20 nF on the CRT's printed-circuit board.

APPLICATION INFORMATION

Dissipation

There are two components of the dissipation — static dissipation (independent of the frequency) and dynamic dissipation (proportional to the frequency).

The static dissipation is due to both high- and low-voltage supply currents and load currents in the feedback network and CRT and is given by:

$P_{stat} = (V_{P1} \times I_{P1}) + (V_{P2} \times I_{P2}) + (V_8 \times I_8) - (V_9 \times V_9/R_{fb})$.

Where $V_9 = V_8 = 100$ V; feedback resistor $R_{fb} = 68$ kΩ; $I_8 = 0.3$ mA and other typical conditions as provided in the **CHARACTERISTICS**. The static dissipation, $P_{stat} = 0.9$ W.

The dynamic dissipation is given by:

$P_{dyn} = V_{P1} \times (C_L + C_{fb} + C_{int}) \times f \times V_{o(p\text{-}p)} \times b$.

Where load capacitance $C_L = 10$ pF; feedback capacitance $C_{fb} = 0$; internal load capacitance $C_{int} = 4$ pF; sine wave frequency $f = 4$ MHz; peak-to-peak output voltage $V_{o(p\text{-}p)} = 100$ V and the non-blanking duty factor $b = 80\%$. The dynamic dissipation, $P_{dyn} = 0.9$ W.

To minimize the load capacitance, C_L, TDA6100 must be mounted on the printed-circuit board at the base of the CRT.

The total dissipation, $P_{tot} = P_{stat} + P_{dyn} = 1.8$ W under the conditions given.
From $T_j = T_{amb} + (P_{tot} \times R_{th\ j\text{-}a}) < T_{j,\,max} = 150\ ^{o}C$, it follows that no additional heatsink is required for $T_{amb} < T_{amb\ max} = 65\ ^{o}C$.

Black-current stabilization

To use the black-current stabilization feature, a signal source including a black-current stabilization loop is needed (TDA3562A or TDA4580). The black-current needs to be converted to a voltage by, for example, an 82 kΩ resistor connected to ground and a 150 kΩ resistor connected to V_{P2}. A clamping diode connected to V_{P2} prevents capacitive load currents from causing the voltage to exceed $V_{P2} + V_{diode}$. Care must be taken to minimize the parasitic capacitance at the current-to-voltage conversion node. Both TDA4580 and TDA3562A feature sequential black-current stabilization, therefore the black-current measurement outputs of all three video output stages can be added. To obtain the correct ratio of cathode currents for colour balance at the stabilized black-level, the circuit illustrated by Fig.3 may be used.

The output voltage depends on the currents $I_{5,R}$, $I_{5,G}$ and $I_{5,B}$ as expressed in the following formula:

$$V_O = R4 \times \frac{[(R1 + R2 + R3)I_{5,B} + (R1 + R2)I_{5,G} + (R1)I_{5,R}]}{(R1 + R2 + R3 + R4)}.$$

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

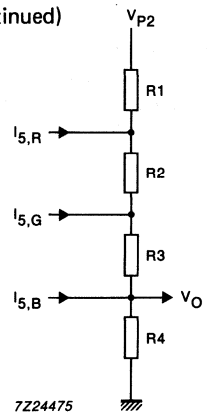


Fig.3 Colour balance diagram.

Figure 4 below illustrates a method for adjusting the ratios of the stabilized black-currents.

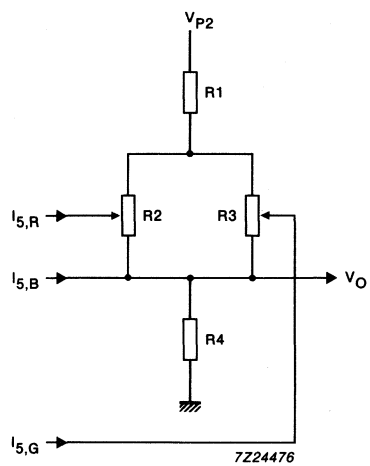


Fig.4 Stabilized black-current adjustment.

The black-current measurement output of the TDA6100Q deals with both positive and negative leakage currents at the cathode output.

DEVELOPMENT DATA

Gain and DC biasing

Figure 5 illustrates a circuit in which the gain and the black-level output can be adjusted independently. If the potentiometers have a relatively low value of resistance, the feedback factor remains approximately constant. The input black-level is given by $V_{I,BL}$. Figure 6 illustrates a circuit for this adjustment when ABS is used.

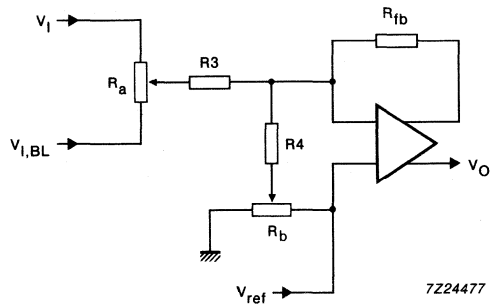


Fig.5 Gain and black-level adjustment.

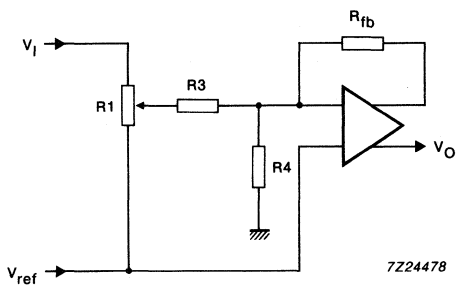


Fig.6 Gain and black-level adjustment with ABS.

APPLICATION INFORMATION (continued)

Referring to the circuit illustrated by Fig.6 the total gain is given by:

$$A = \frac{a \times R_{fb}}{R_a(a\text{-}a^2) + R3} \quad \text{with } 0 \leqslant R_a(a\text{-}a^2) \leqslant R_a/4$$

If the value of the gain is known, then the adjustment of the potentiometer can be found from:

$$a = 0.5 \left\{ \left[\left(\frac{R_{fb}}{A \times R_a} - 1 \right)^2 + \left(4 \times \frac{R3}{R_a} \right) \right]^{1/2} - \left(\frac{R_{fb}}{A \times R_a} - 1 \right) \right\}$$

The feedback factor (stipulating the bandwidth) of the circuit follows from:

$$1/k = 1 + \frac{R_{fb}}{R4//[R3 + R_a(a\text{-}a^2)]}$$

The output black-level is given by:

$$V_{O,BL} = V_{ref} \frac{R_{fb} + R4}{R4} - A(V_{I,BL} - V_{ref})$$

If the value of the black-level is known, then R4 can be calculated as a function of V_{ref} or, V_{ref} as a function of R4, as shown below:

$$R4 = R_{fb} \times \frac{V_{ref}}{V_{O,BL} + A(V_{I,BL} - V_{ref}) - V_{ref}}$$

$$V_{ref} = \frac{V_{O,BL} + A \times V_{I,BL}}{(A + 1 + R_{fb}/R4)}$$

To obtain the required feedback, R3 and R4 or V_{ref} must be chosen. The results can be read from the above formulae.

DC biasing at high gain

When the device is used as an 8 MHz and x 90 gain amplifier with AC coupling of the signal source, DC biasing can be accomplished by using the circuits illustrated by Figs 7 and 8.

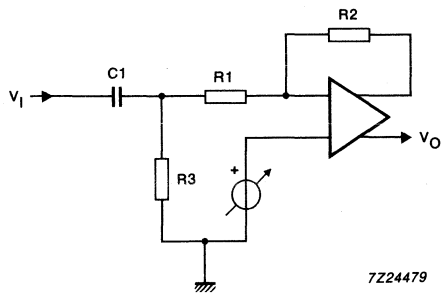


Fig.7 DC biasing using an adjustable voltage source.

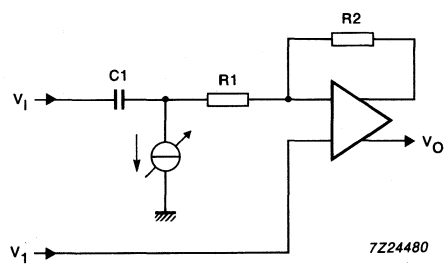
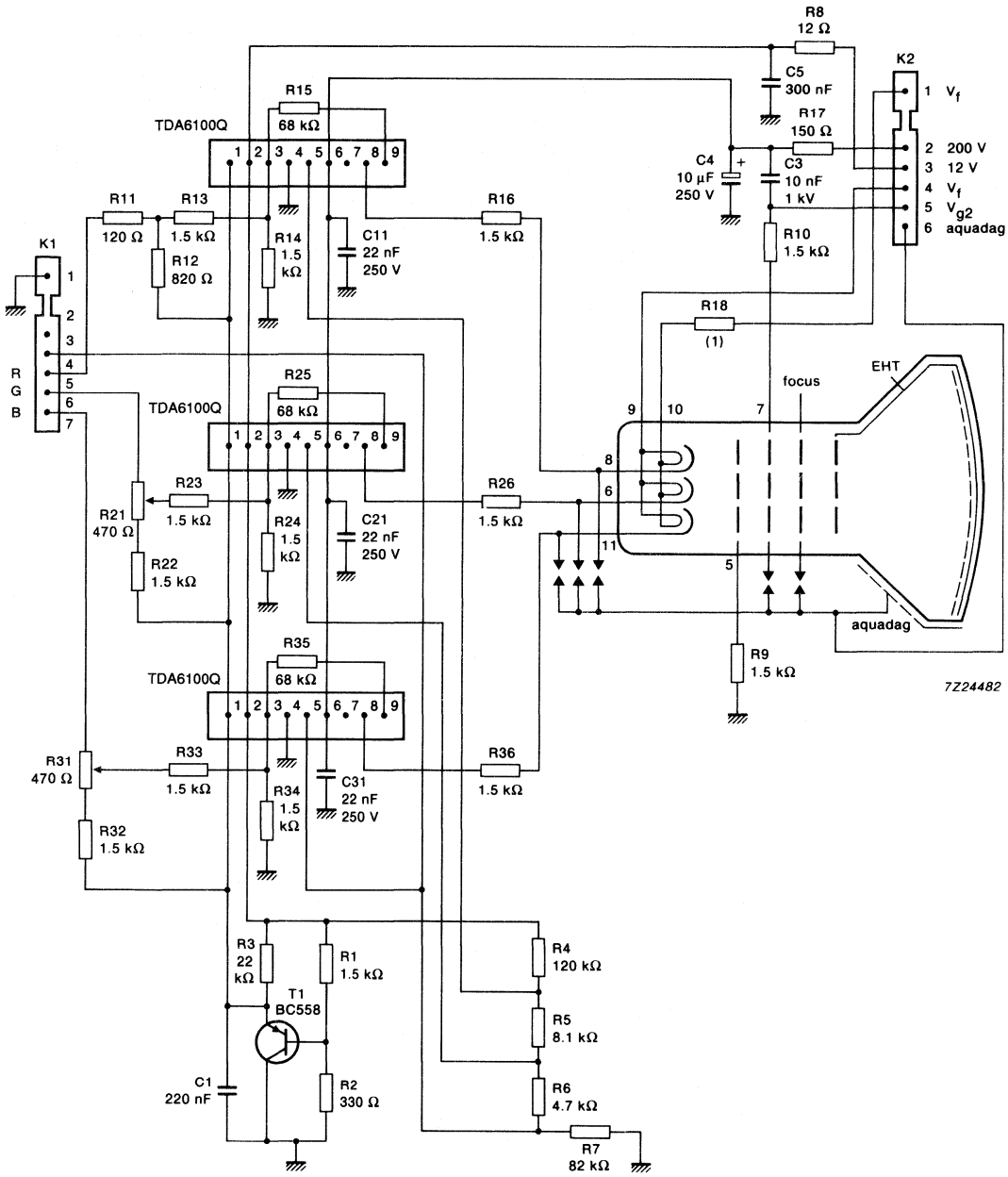


Fig.8 DC biasing using an adjustable current source.

Application circuit

Figure 9 illustrates an application circuit for use with ABS (eg TDA4580), in which a number of components are common for the three output stages.

APPLICATION INFORMATION (continued)



(1) Value to be fixed.

Fig.9 Application circuit for use with ABS (eg TDA4580) using CRT A66EAK00X (30AX).

Video output amplifier TDA6101Q

FEATURES

- High bandwidth and high slew rate
- No external heatsink needed
- Black-current measurement output for automatic black current stabilization (ABS)
- Two cathode outputs: one for DC currents and one for transient currents
- A feedback output separated from the cathode outputs
- Internal protection against positive appearing CRT flashover discharges
- ESD Protection
- Simple application with a variety of colour decoders
- Differential input, with a designed maximum common mode input capacitance of 3 pF; a differential mode input capacitance of 2 pF and a differential input voltage temperature drift of 0.4 mV/K.

GENERAL DESCRIPTION

The TDA6101Q is a monolithic video output amplifier with an 8 MHz bandwidth. The device is contained in a SIL 9 MP (single in line 9 pins Medium Power) package. The device employs high voltage DMOS technology, and is designed to drive the cathode of a CRT.

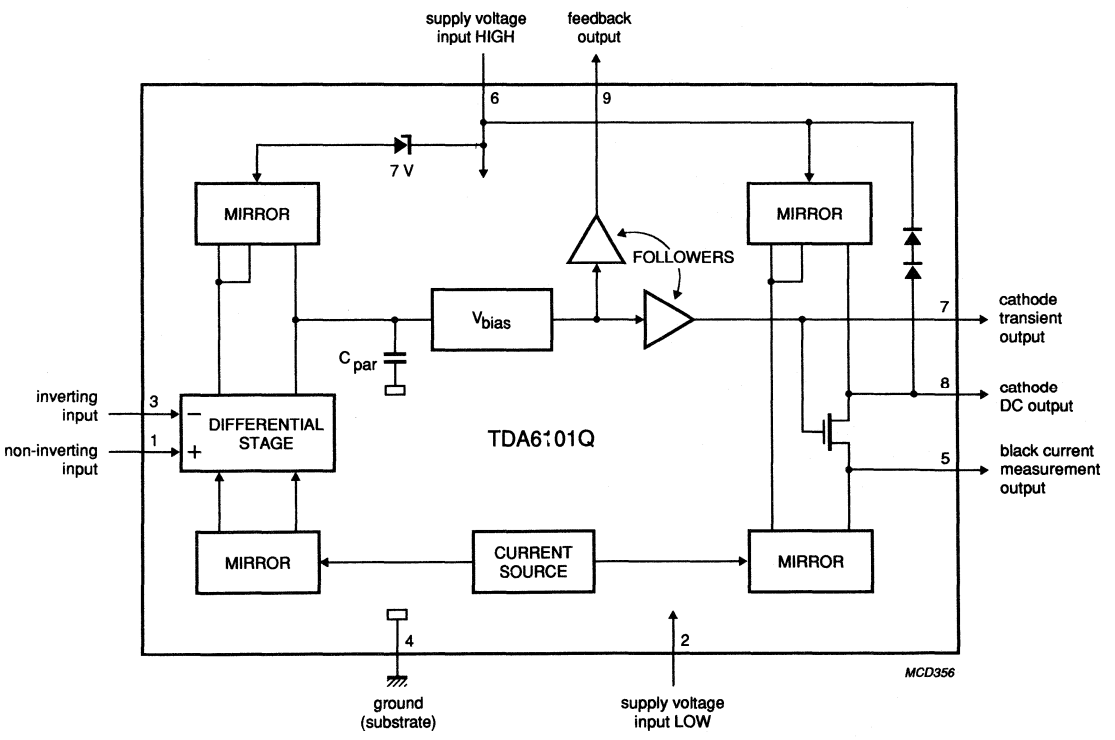


Fig.1 Block diagram.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA6101Q	9	DBS	plastic	SOT111

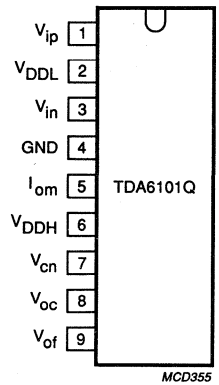


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{ip}	1	non inverting input
V_{DDL}	2	supply voltage LOW
V_{in}	3	inverting input
GND	4	ground, substrate
I_{om}	5	black current measurement output
V_{DDH}	6	supply voltage HIGH
V_{cn}	7	cathode transient output
V_{oc}	8	cathode DC-output
V_{of}	9	feedback output

FUNCTIONAL DESCRIPTION

Dissipation

A distinction must first be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6101Q is due to HIGH- and LOW-voltage supply currents and load currents in the feedback network and CRT.

$P_{stat} = V_{DDL} \times I_{DDL} + V_{DDH} \times I_{DDH} + V_{oc} \times I_{oc} - V_{of} \times V_{of}/Rt$

Where R_t = value of feedback resistor and I_{oc} = DC value of cathode current.

The dynamic dissipation equals:

$P_{dyn} = V_{DDH} \times (C_L + C_t + C_{int}) \times f \times V_{O(p-p)} \times b$

Where:

C_L = load capacitance

C_t = feedback capacitance

C_{int} = internal load capacitance (4 pF)

f = frequency

$V_{O(p-p)}$ = output voltage (peak-to-peak value)

b = non-blanking duty-cycle

The IC must be mounted on the picture tube base print to minimize the load capacitance C_L.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134). Voltages with respect to pin 4 (ground) unless otherwise specified, currents specified as in Fig.1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDH}	HIGH level supply voltage	0	250	V
V_{DDL}	LOW level supply voltage	0	14	V
V_I	input voltage	0	V_{DDL}	V
$V_{I,dm}$	differential mode input voltage	−6	6	V
V_{om}	measurement output voltage	0	V_{DDL}	V
V_{oc}, V_{of}	output voltage	V_{DDL}	V_{DDH}	V
I_{in}, I_{ip}	input current	0	1	mA
I_{cn}	repetitive peak output current	−25	25	mA
I_{OCL}	LOW non-repetitive peak cathode output current (50 μC)	0	5	A
I_{OCH}	HIGH non-repetitive peak cathode output current (100 nC)	0	10	A
P_{max}	total power dissipation	0	1.9	W
T_{stg}	storage temperature range	−55	+150	°C
T_j	junction temperature range	−20	+150	°C
V_{ESD}	voltage peak (ESD-HBM)	−	> 2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	59 K/W
$R_{th\ j\text{-}c}$	from junction to mounting case	13 K/W

Quality specification

Quality specification URV 4-259.602. is applicable.

CHARACTERISTICS

Operating range: T_{amb} = −20 to 65 °C; V_{DDH} = 180 to 210 V; V_{DDL} = 10.8 to 13.2 V; V_{ip} = 2.6 to 5 V; V_{om} = 1.4 V to V_{DDL}.
Test conditions: (unless otherwise specified) T_{amb} = 25 °C; V_{DDH} = 200 V; V_{DDL} = 12 V; V_{ip} = 5 V; V_{om} = 6 V; C_L = 10 pF (C_L consists of parasitic and cathode capacitance). (Test circuit: see Fig.3).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DDH}	quiescent HIGH voltage supply current	$V_{oc} = V_{DDH}/2$	3.5	4.4	5.5	mA
I_{DDL}	quiescent LOW voltage supply current	$V_{oc} = V_{DDH}/2$	2.3	2.9	3.6	mA
I_{bias}	input bias current	$V_{oc} = V_{DDH}/2$	0	–	20	µA
$I_{i,OFF}$	input offset current	$V_{oc} = V_{DDH}/2$	−3	–	3	µA
$I_{om,OFF}$	offset current of measurement output	I_{oc} = 0 µA; −1.0 V < V_{1-3} < 1.0 V; 1.4 < V_{om} < V_{DDL}	−5	0	5	µA
$\Delta I_{om} / \Delta I_{oc}$	linearity of current transfer	−10 µA < I_{oc} < 3 mA; −1.0 V < V_{1-3} < 1.0 V; 1.4 < V_{om} < V_{DDL}	0.9	1	1.1	
$V_{i,OFF}$	input offset voltage	$V_{oc} = V_{DDH}/2$	−50	–	50	mV
$V_{oc\ min}$	minimum output voltage	V_{1-3} = −1 V	–	–	20	V
$V_{oc\ max}$	maximum output voltage	V_{1-3} = 1 V	V_{DDH}−12 V	–	–	V
GB	gain-bandwidth product of Open Loop Gain: $V_{of}/V_{i,dm}$	f = 500 kHz; V_{oc-DC} = 100 V	–	0.85	–	GHz
B_S	small signal bandwidth	V_{oc-AC} = 60 V(p-p); V_{oc-DC} = 100 V	6.5	8	–	MHz
B_L	large signal bandwidth	V_{oc-AC} = 100 V(p-p); V_{oc-DC} = 100 V	5	6.5	–	MHz
t_p	cathode output propagation time 50% input – 50% output (see Figs 4 and 5)	V_{oc-AC} = 100 V(p-p); V_{oc-DC} = 100 V; square wave: f < 1 MHz; $t_{r,i}$, $t_{f,i}$ = 40 ns	32	43	54	ns
t_r	cathode output rise time 10% output – 90% output (see Fig.4)	V_{oc} = 50 to 150 V; square wave: f < 1 MHz; t_f, input = 40 ns;	43	55	68	ns
t_f	cathode output fall time 90% output – 10% output (see Fig.5)	V_{oc} = 150 to 50 V; square wave: f < 1 MHz; t_r, input = 40 ns;	43	55	68	ns
t_s	settling time 50% input – (99% < output < 101%) (see Figs 4 and 5)	V_{oc-AC} = 100 V(p-p); V_{oc-DC} = 100 V;; square wave: < 1 MHz; $t_{r,i}$; $t_{f,i}$ = 40 ns	–	–	350	ns
SR	slew rate between 50 V – 150 V	V_{1-3} = 2 V(p-p) square wave: f < 1 MHz; $t_{r,i}$; $t_{f,i}$ = 40 ns	–	1700	–	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
O_V	cathode output voltage overshoot (see Figs 4 and 5)	V_{oc-AC} = 100 V(p-p); V_{oc-DC} = 100 V;; square wave: f < 1 MHz; $t_{r,i}$; $t_{f,i}$ = 40 ns; note 1	–	5	–	%
R_i	differential input resistance		–	100	–	kΩ
SVRRH	HIGH voltage power supply rejection ratio	f < 50 kHz; note 2	–	80	–	dB
SVRRL	LOW voltage power supply rejection ratio	f < 50 kHz; note 2	–	80	–	dB

Notes to the characteristics

The cathode output is protected against peak currents (caused by positive voltage peaks during high-resistance flash) of 5 A maximum with a charge content of 50 μC.

The cathode output is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 10 A maximum with a charge content of 100 nC.

1. If the difference between V_{DDL} and V_{ip} is less then 7 V, overshoot cannot be specified.
2. SVRR: The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

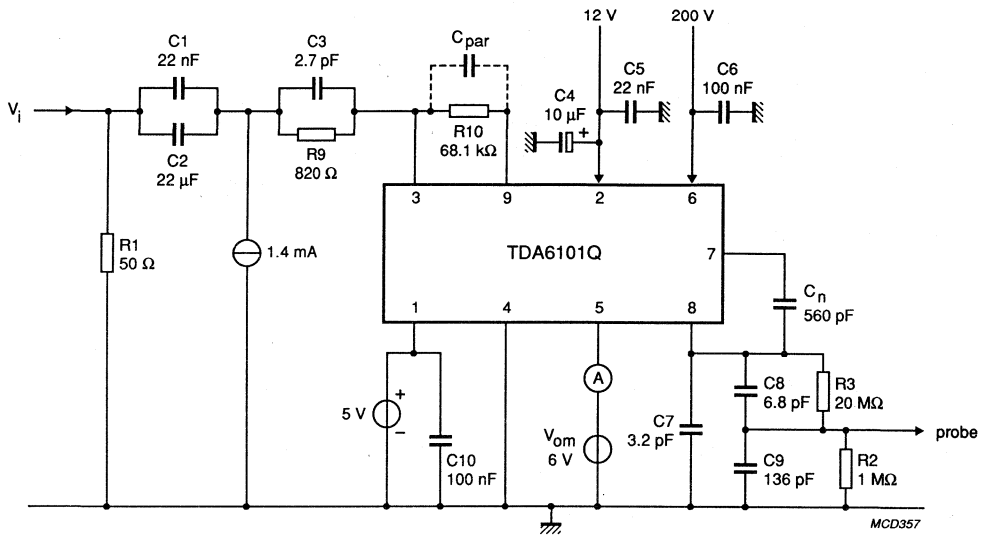


Fig.3 Test circuit with feedback factor 1/83. C_{par} is approximately 150 fF.

Note to Fig.3

FLASHOVER PROTECTION

The TDA6101Q incorporates protection diodes against CRT flashover discharges that clamp the cathode output voltage until maximum $V_{DDH} + V_{diode}$. To limit the diode current, an external 820 Ω carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are needed. For this resistor value the ground connection for the CRT must be connected to the main printed-circuit board. This addition produces an increase in the 'rise' and 'fall' times of approximately 5 ns and a decrease in the overshoot of approximately 3%.

V_{DDH} – GND must be decoupled:

a) With a capacitor > 20 nF with good HF behaviour (e.g. foil). This capacitance must be placed as close as possible to pin 6 and pin 4, definitely within 5 mm.

b) With a capacitor > 10 µF on the picture tube base print (common for three output stages).

V_{DDL} – GND must be decoupled with a capacitor > 20 nF with good HF behaviour (e.g. ceramic). This capacitance must be placed as close as possible to pin 2 and pin 4, definitely within 10 mm.

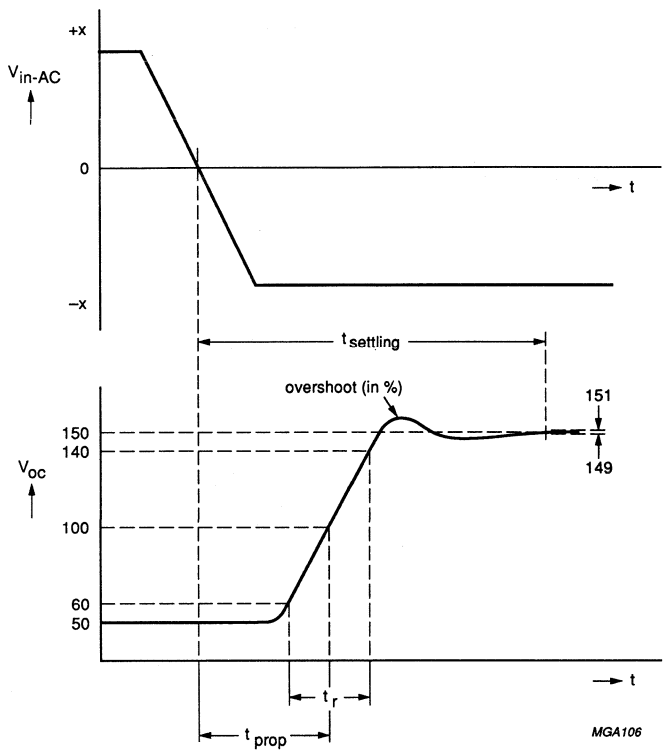


Fig.4 Output rising edge as a function of input signal.

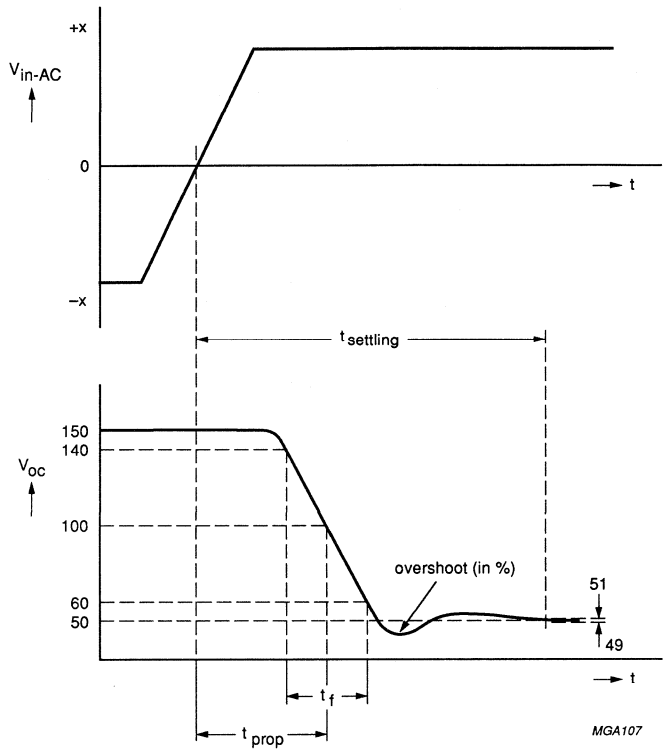


Fig.5 Output falling edge as a function of input signal.

Video output amplifier TDA6111Q

FEATURES

- High bandwidth and high slew rate
- Black-current measurement output for automatic black-current stabilization (ABS)
- Two cathode outputs: one for DC currents and one for transient currents
- A feedback output separated from the cathode outputs
- Internal protection against positive appearing CRT flashover discharges
- ESD protection
- Simple application for a variety of colour decoders
- Differential input, with a designed maximum common mode input capacitance of 3 pF; a differential mode input capacitance of 2 pF and a differential input voltage temperature drift of 0.4 mV/K.

GENERAL DESCRIPTION

The TDA6111Q is a monolithic video output amplifier with a 16 MHz bandwidth. The device is contained in a SIL 9 MP (single in-line 9 pins medium power) package. The device employs high voltage DMOS technology, and is designed to drive the cathode of a CRT.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA6111Q	9	DBS	plastic	SOT111

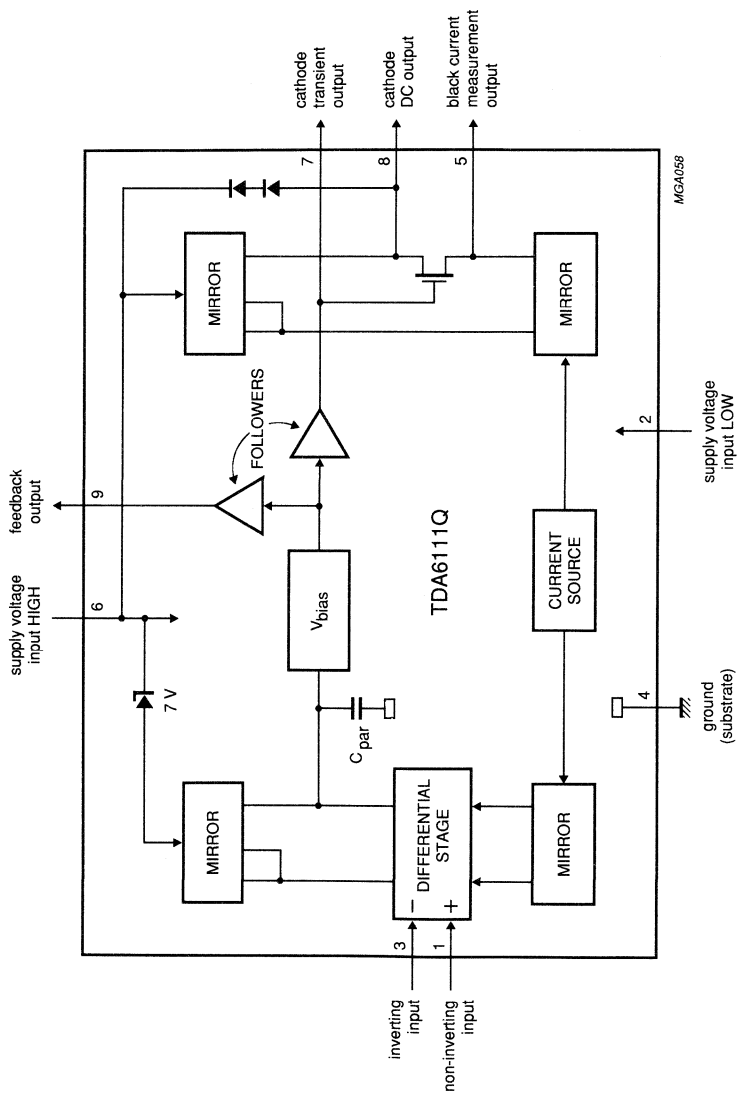


Fig.1 Block diagram.

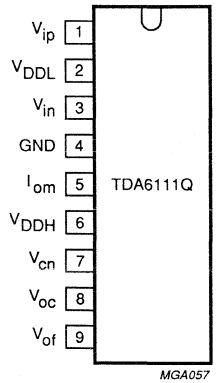


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{ip}	1	non inverting input
V_{DDL}	2	supply voltage LOW
V_{in}	3	inverting input
GND	4	ground, substrate
I_{om}	5	black current measurement output
V_{DDH}	6	supply voltage HIGH
V_{cn}	7	cathode transient output
V_{oc}	8	cathode DC output
V_{of}	9	feedback output

FUNCTIONAL DESCRIPTION

Dissipation

A distinction must first be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6111Q is due to HIGH- and LOW-voltage supply currents and load currents in the feedback network and CRT.

$P_{stat} = V_{DDL} \times I_{DDL} + V_{DDH} \times I_{DDH} + V_{oc} \times I_{oc} - V_{of} \times V_{of}/R_t$

Where $V_{of} = V_{oc} = 100$ V, feedback resistor $R_t = 68$ kΩ, $I_{oc} = 0.6$ mA and other typical conditions as given in the electrical characteristics, the static dissipation $P_{stat} = 2$ W.

The dynamic dissipation equals:

$P_{dyn} = V_{DDH} \times (Cl + Ct + C_{int}) \times f \times V_{O(p-p)} \times b$

With load capacitance $C_L = 10$ pF, feedback capacitance $C_t = 0$, internal load capacitance $C_{int} = 4$ pf, sine wave frequency f = 8 MHz, output voltage (peak-to-peak value) $V_{o(p-p)} = 100$ V and a non-blanking duty-cycle b = 80% the dynamic dissipation P_{dyn} equals 1.8 W. The IC must be mounted on the picture tube base print to minimize the load capacitance C_L.

The total dissipation, $P_{tot} = P_{stat} + P_{dyn}$ thus amounts to 3.8 W under given conditions. From $T_j = T_{amb} + P_{tot} \times R_{th,j\text{-}amb} < T_{j(max)} = 150$ °C, $R_{th,j\text{-}amb}$ of the package and heatsink together must be < 22 K/W.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134). Voltages with respect to pin 4 (ground) unless otherwise specified, currents specified as in Fig.1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDH}	supply voltage HIGH	0	250	V
V_{DDL}	supply voltage LOW	0	14	V
V_I	input voltage	0	V_{DDL}	V
$V_{I,dm}$	differential mode input voltage	−6	6	V
V_{om}	measurement output voltage	0	V_{DDL}	V
V_{oc}, V_{of}	output voltage	V_{DDL}	V_{DDH}	V
I_{in}, I_{ip}	input current	0	1	mA
I_{cn}	repetitive peak output current (pin 7)	−40	40	mA
I_{OCL}	LOW non-repetitive peak cathode output current (50 μC)	0	5	A
I_{OCH}	HIGH non-repetitive peak cathode output current (100 nC)	0	10	A
P_{max}	total power dissipation	0	4	W
T_{stg}	storage temperature range	−55	+150	°C
T_j	junction temperature range	−20	+150	°C
V_{ESD}	peak voltage (ESD–HBM)	–	2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\,j\text{-}case}$	from junction to mounting case	13 K/W
R_{th}	heatsink	10 K/W

Quality specification

Quality specification URV 4-259.602. is applicable.

CHARACTERISTICS

Operating range: T_{amb} = −20 to 65 °C; V_{DDH} = 180 to 210 V; V_{DDL} = 10.8 to 13.2 V; V_{ip} = 2.6 to 5 V; V_{om} = 1.4 V to V_{DDL}.
Test conditions: (unless otherwise specified) R_{th} heatsink = 10 K/W; T_{amb} = 25 °C; V_{DDH} = 200 V; V_{DDL} = 12 V; V_{ip} = 5 V; V_{om} = 6 V); C_L = 10 pF (C_L consists of parasitic and cathode capacitance). See test circuit Fig.3.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DDH}	quiescent HIGH voltage supply current	$V_{oc} = V_{DDH}/2$	7	9	11	mA
I_{DDL}	quiescent LOW voltage supply current	$V_{oc} = V_{DDH}/2$	5	6.8	8	mA
I_{bias}	input bias current	$V_{oc} = V_{DDH}/2$	0	–	40	µA
$I_{i,OFF}$	input offset current	$V_{oc} = V_{DDH}/2$	−6	–	6	µA
$I_{om,off}$	offset current of measurement output	I_{oc} = 0 µA; −1.0 V < V_{1-3} < 1.0 V; 1.4 < V_{om} < V_{DDL}	−10	0	10	µA
$\Delta I_{om} / \Delta I_{oc}$	linearity of current transfer	−10 µA < I_{oc} < 3 mA; −1.0 V < V_{1-3} < 1.0 V; 1.4 < V_{om} < V_{DDL}	0.9	1	1.1	
$V_{i,OFF}$	input offset voltage	$V_{oc} = V_{DDH}/2$	−50	–	50	mV
$V_{oc(min)}$	minimum output voltage	V_{1-3} = −1 V	–	–	20	V
$V_{oc(max)}$	maximum output voltage	V_{1-3} = 1 V	V_{DDH}−12	–	–	V
GB	gain-bandwidth product of Open Loop Gain: $V_{of}/V_{i,dm}$	f = 500 kHz; V_{oc-DC} = 100 V	–	1.75	–	GHz
B_s	small signal bandwidth	V_{oc-AC} = 60 V(p-p); V_{oc-DC} = 100 V	13	16	–	MHz
B_L	large signal bandwidth	V_{oc-AC} = 100 V(p-p); V_{oc-DC} = 100 V	10	13	–	MHz
t_p	cathode output propagation time 50% input – 50% output (see Figs 4 and 5)	V_{oc-AC} = 100 V(p-p); V_{oc-DC} = 100 V; square wave: f < 1 MHz; $t_{r,i}$, $t_{f,i}$ = 22 ns	18	24	30	ns
t_r	cathode output rise time 10% output – 90% output (see Fig.4)	V_{oc} = 50 to 150 V; square wave: f < 1 MHz; t_f, input = 22 ns;	23	30	36	ns
t_f	cathode output fall time 90% output – 10% output (see Fig.5)	V_{oc} = 150 to 50 V; square wave: f < 1 MHz; t_r, input = 22 ns;	23	30	36	ns
t_s	settling time 50% input – (99% < output < 101%) (see Figs 4 and 5)	V_{oc-AC} = 100 V(p-p); V_{oc-DC} = 100 V;; square wave: < 1 MHz; $t_{r,i}$; $t_{f,i}$ = 22 ns	–	–	350	ns
SR	slew rate between 50 V – 150 V	V_{1-3} = 2 V(p-p) square wave: f < 1 MHz; $t_{r,i}$; $t_{f,i}$ = 22 ns	–	3000	–	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
O_V	cathode output voltage overshoot (see Figs 4 and 5)	V_{oc-AC} = 100 V(p-p); V_{oc-DC} = 100 V;; square wave: f < 1 MHz; $t_{r,i}$; $t_{f,i}$ = 22 ns; note 1	–	7	–	%
R_i	differential input resistance		–	100	–	kΩ
SVRRH	HIGH voltage power supply rejection ratio	f < 50 kHz; note 3	–	80	–	dB
SVRRL	LOW voltage power supply rejection ratio	f < 50 kHz; note 3	–	80	–	dB

Notes to the characteristics

The cathode output is protected against peak currents (caused by positive voltage peaks during high-resistance flash) of 5 A maximum with a charge content of 50 μC.

The cathode output is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 10 A maximum with a charge content of 100 nC.

1. If the difference between V_{DDL} and V_{ip} is less then 7 V, overshoot cannot be specified.
2. SVRR: The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

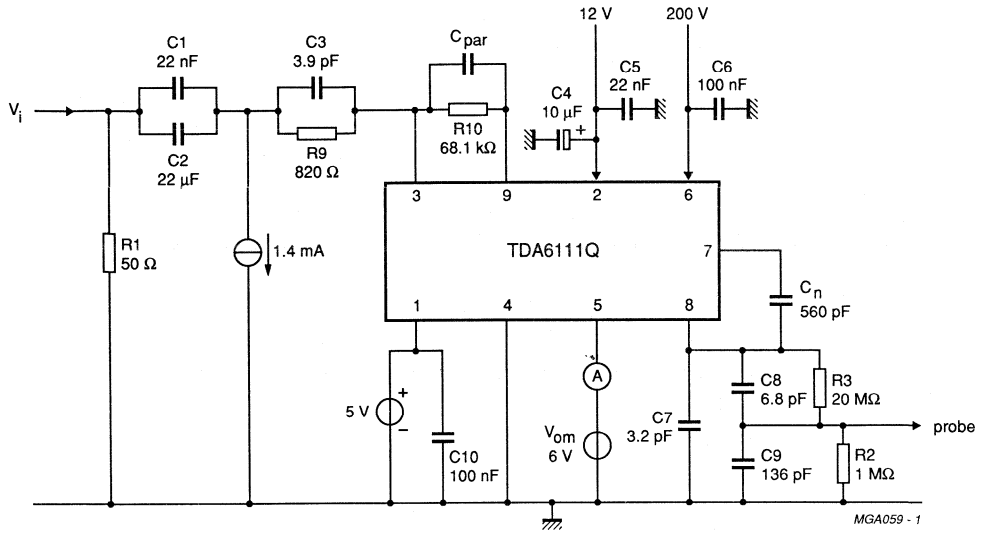


Fig.3 Test circuit with feedback factor 1/83. C_{par} is approximately 150 fF.

Note to Figure 3

FLASHOVER PROTECTION

The TDA6111Q incorporates protection diodes against CRT flashover discharges that clamp the cathode output voltage until maximum $V_{DDH} + V_{diode}$. To limit the diode current, an external 680 Ω carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are needed. For this resistor value the ground connection for the CRT must be connected to the main printed-circuit board. This addition produces an increase in the 'rise' and 'fall' times of approximately 7 ns and a decrease in the overshoot of approximately 5%.

V_{DDH} – GND must be decoupled:

- With a capacitor > 20 nF with good HF behaviour (e.g. foil). This capacitance must be placed as close as possible to pin 6 and pin 4, definitely within 5 mm.
- With a capacitor > 10 µF on the picture tube base print (common for three output stages).

V_{DDL} – GND must be decoupled with a capacitor > 20 nF with good HF behaviour (e.g. ceramic). This capacitance must be placed as close as possible to pin 2 and pin 4, definitely within 10 mm.

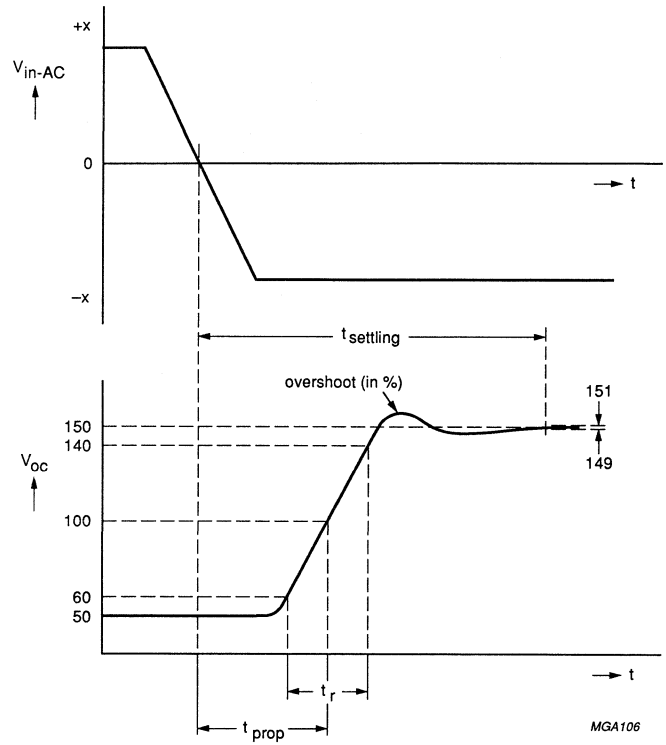


Fig.4 Output rising edge as a function of input signal.

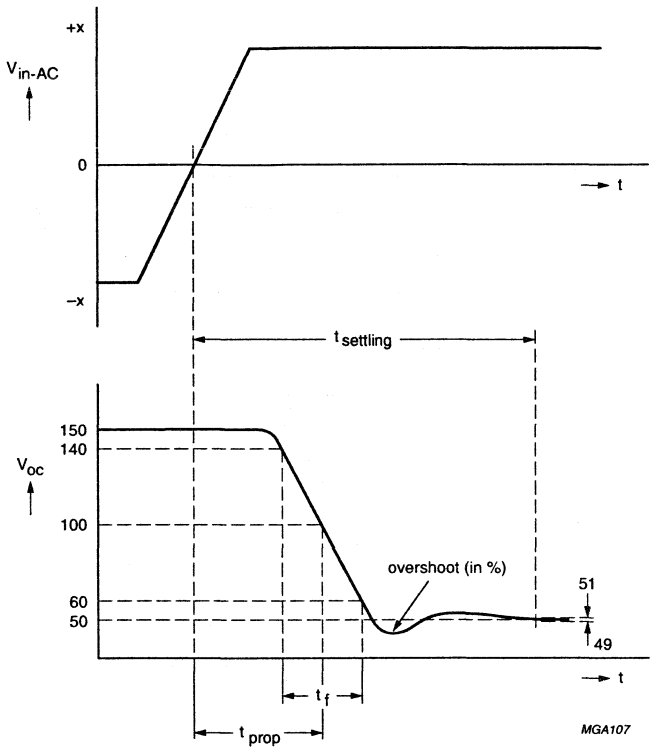


Fig.5 Output falling edge as a function of input signal.

VIDEO MODULATOR CIRCUIT

GENERAL DESCRIPTION

The TDA6800 is a modulator circuit for modulation of video signals on a VHF/UHF carrier. The circuit requires a 5 V power supply and few external components for the negative modulation mode. For positive modulation an external clamp circuit is required. This circuit can be used as a general purpose modulator without additional external components.

Features

- Balanced modulator
- Symmetrical oscillator
- Video clamp circuit for negative modulation
- Frequency range 50 to 800 MHz

QUICK REFERENCE DATA

		min.	typ.	max.	
Supply voltage range	V_{5-4}	4,5	–	5,5	V
Supply current consumption	I_5	–	9	–	mA
Video input voltage	$V_{8(p-p)}$	–	1	–	V
Input impedance	R_8	30	–	–	kΩ
Output voltage (50 MHz)	V_{6-7}	–	13	–	mV
Output voltage (600 MHz)	V_{6-7}	–	10	–	mV
Differential gain	Δ_G	–	–	10	%
Differential phase	Δ_ϕ	–	–	10	deg.
Intermodulation distortion	d_{int}	–	–80	–	dB

PACKAGE OUTLINE

TDA6800 : 8-lead dual in-line; plastic (SOT97A).
TDA6800T: 8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{5-4}	max.	7 V
Input voltage	V_{8-4}	max.	4 V
Output voltage	$V_{6,7-4}$	max.	9 V
Storage temperature	T_{stg}	max.	125 °C
Junction temperature	T_j	max.	125 °C
Operating ambient temperature range	T_{amb}		−25 to + 85 °C

THERMAL RESISTANCE

From junction to ambient in free air

TDA6800T	$R_{th\ j\text{-}a}$	260 K/W
TDA6800	$R_{th\ j\text{-}a}$	120 K/W

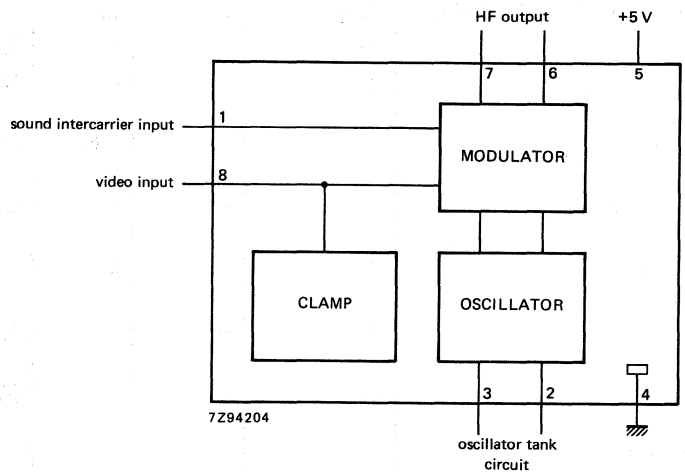


Fig. 1 Block diagram TDA6800 and TDA6800T.

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{5-4}	4,5	–	5,5	V
Supply current consumption	I_5	–	9	13	mA
Video input voltage	$V_{8(p-p)}$	–	1	–	V
Input impedance	R_8	30	–	–	kΩ
Voltage (d.c.) at video input (clamp voltage)	V_8	–	1,4	–	V
Voltage (d.c.) at sound input	V_1	–	2,5	–	V
Output voltage f = 50 MHz; R_L = 75 Ω	V_{6-7}	–	13	–	mV
Output voltage f = 600 MHz; R_L = 75 Ω	V_{6-7}	–	10	–	mV
Differential gain	Δ_G	–	–	10	%
Differential phase	Δ_ϕ	–	–	10	deg.
Intermodulation (1,1 MHz) (note 1)		–	–80	–60	dB
Frequency shift V_b = 5%, f = 600 MHz	Δ_f	–	–	100	kHz
Frequency shift V_b = 5%, f = 800 MHz	Δ_f	–	tbf	–	kHz
Frequency drift 25 to 40 °C	Δ_f	–	–	100	kHz
Frequency drift 15 to 55 °C	Δ_f	–	–	300	kHz
Positive modulation (see Fig. 3)					
Residual carrier voltage	V_r	–	–	2,5	%
Cross modulation (note 2)	α	–	0,1	0,25	%

NOTES TO THE CHARACTERISTICS

1. Input signal: d.c. 0,45 V (V_{8-4} = 1,85 V)
   4,4 MHz; input voltage (p-p) = 0,6 V
   5,5 MHz; input voltage (p-p) = 1,26 V
   measured with respect to picture carrier, at f = 600 MHz.
2. Input signal: d.c. 1 V (V_{8-4} = 3,5 V)
   5,5 MHz AM modulated, f_m = 100 kHz
   m = 0,8; input voltage (p-p) = 2,27 V (including modulation)
   measured with respect to the picture carrier, at f = 600 MHz.

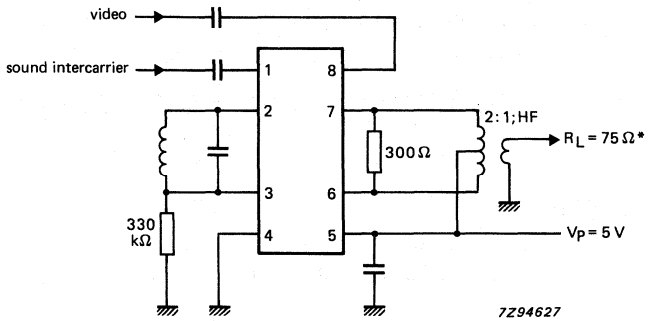


Fig. 2.
Application for negative modulation.

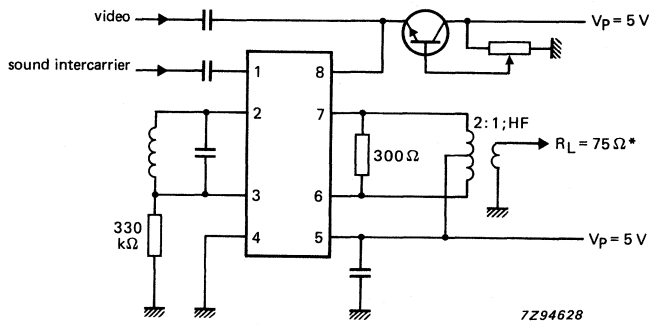


Fig. 3.
Application for positive modulation.

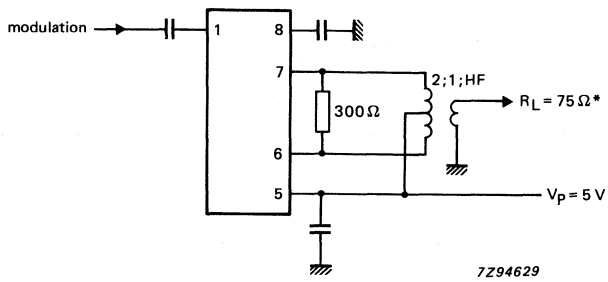


Fig. 4.
Application for general purpose modulation.

* Close to output transformer.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use — mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use — mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8 lead mini-pack; plastic (SO8; SOT96A).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

1 W BTL MONO AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%; 8 Ω	P_o	–	1,2	–	W
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

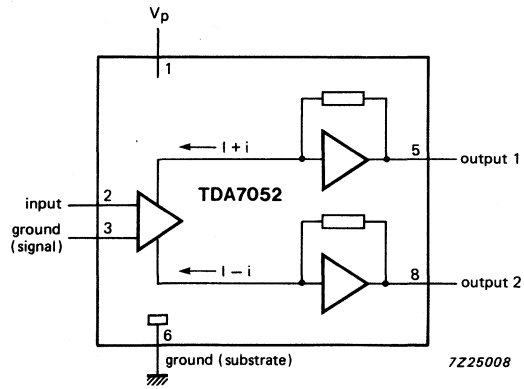


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

1 Watt BTL mono audio amplifier with DC volume control

TDA7052A/AT

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control. They are designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
P_O	output power					
	TDA7052A	$R_L = 8\ \Omega$; $V_P = 6$ V	1.0	1.1	–	W
	TDA7052AT	$R_L = 16\ \Omega$; $V_P = 6$ V	0.5	0.55	–	W
G_v	maximum total voltage gain		34.5	35.5	36.5	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	$V_P = 6$ V; $R_L = \infty$	–	7	12	mA
THD	total harmonic distortion					
	TDA7052A	$P_O = 0.5$ W	–	0.3	1	%
	TDA7052AT	$P_O = 0.25$ W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7052A	8	DIL	plastic	SOT97
TDA7052AT	8	mini-pack	plastic	SOT96A

1 Watt BTL mono audio amplifier with DC volume control

TDA7052A/AT

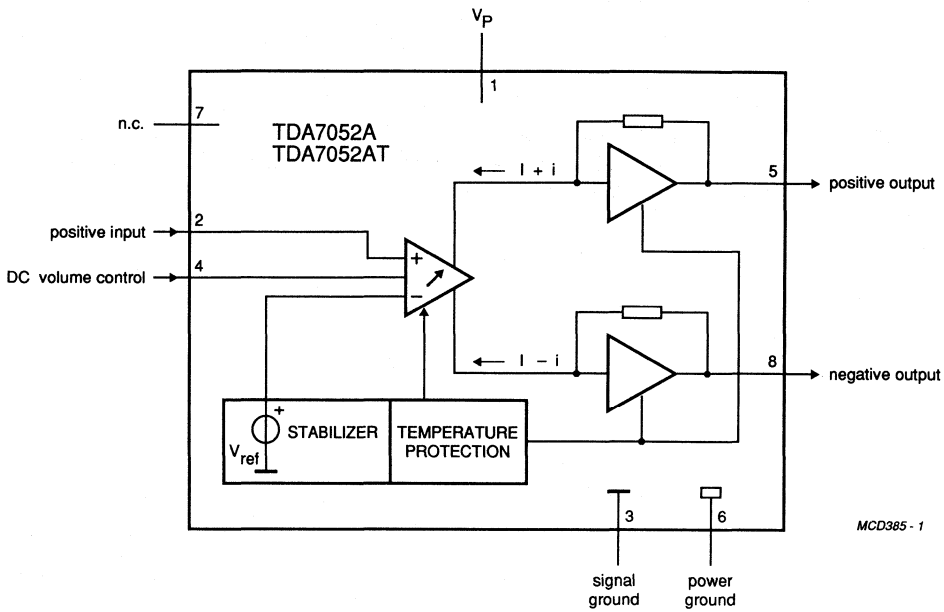


Fig.1 Block diagram.

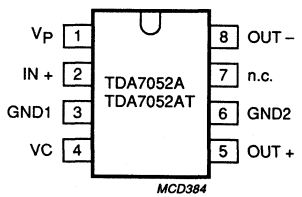


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
IN+	2	positive input
GND1	3	signal ground
VC	4	DC volume control
OUT+	5	positive output
GND2	6	power ground
n.c	7	not connected
OUT−	8	negative output

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

2 × 1 W PORTABLE/MAINS-FED STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7053 is an integrated class-B stereo power amplifier in a 16-lead dual-in-line (DIL) plastic package. The device, consisting of two BTL amplifiers, is primarily developed for portable audio applications but may also be used in mains-fed applications.

Features

- No external components
- No switch-ON/OFF clicks
- Good overall stability
- Low power consumption
- Short-circuit-proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	9	16	mA
Output power	$R_L = 8\ \Omega$; $V_P = 6$ V	P_O	–	1.2	–	W
Internal voltage gain		G_v	38	39	40	dB
Total harmonic distortion	$P_O = 0.1$ W	THD	–	0.2	1.0	%

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

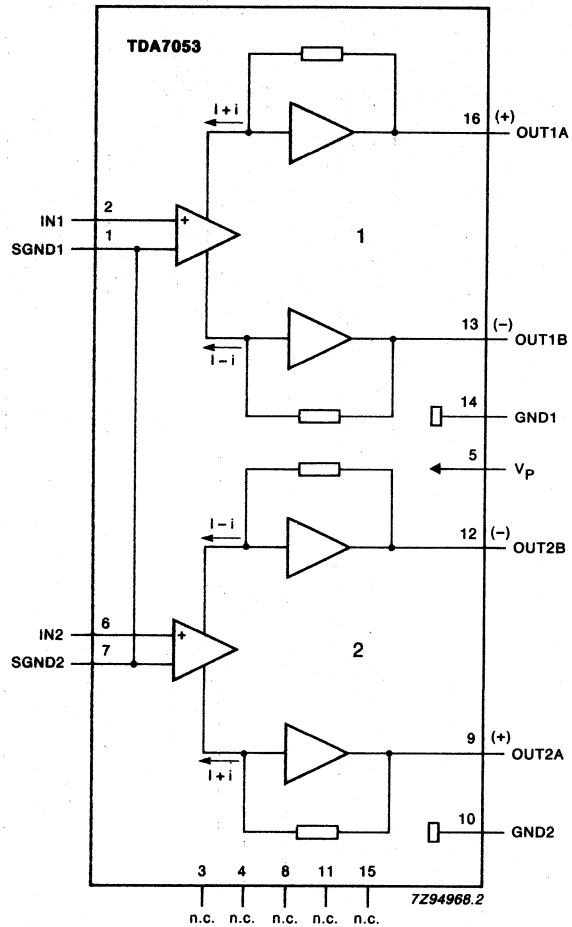


Fig. 1 Block diagram.

PINNING

1.	SGND1	signal ground 1	9.	OUT2A	output 2 (positive)
2.	IN1	input 1	10.	GND2	power ground 2
3.	n.c.	not connected	11.	n.c.	not connected
4.	n.c.	not connected	12.	OUT2B	output 2 (negative)
5.	V_P	supply voltage	13.	OUT1B	output 1 (negative)
6.	IN2	input 2	14.	GND1	power ground 1
7.	SGND2	signal ground 2	15.	n.c.	not connected
8.	n.c.	not connected	16.	OUT1A	output 1 (positive)

Note

The information contained within the parentheses refer to the polarity of the loudspeaker terminal to which the output must be connected.

Data sheet	
status	Product specification
date of issue	May 1992

TDA7056

3 Watt mono BTL audio output amplifier

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

FEATURES

- No external components
- No switch-on/off clicks
- Good overall stability
- Low power consumption
- Short circuit proof
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7056 is a mono output amplifier contained in a 9 pin medium power package.
The device is designed for battery-fed portable mono recorders, radios and television.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		3	11	18	V
P_O	output power in 16 Ω	V_P = 11 V	2.5	3	-	W
G_V	internal voltage gain		39	40.5	42	dB
I_P	total quiescent current	V_P = 11 V; $R_L = \infty$	-	5	7	mA
THD	total harmonic distortion	P_O = 0.5 W	-	0.25	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056	9	SIL	plastic	SOT110

3 Watt mono BTL audio output amplifier TDA7056

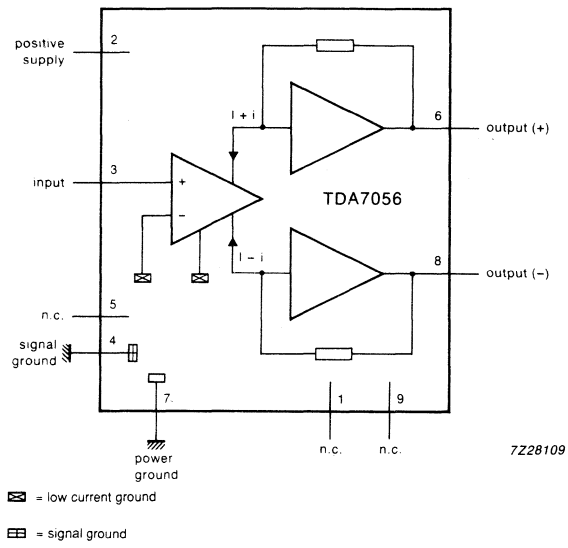


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	n.c.
2	V_P
3	input (+)
4	signal ground
5	n.c.
6	output (+)
7	power ground
8	output (-)
9	n.c.

FUNCTIONAL DESCRIPTION

The TDA7056 is a mono output amplifier, designed for battery-fed portable radios and mains-fed equipment such as television.

For space reasons there is a trend to decrease the number of external components. For portable applications there is also a trend to decrease the number of battery cells, but still a reasonable output power is required.

The TDA7056 fulfills both of these requirements. It needs no peripheral components, because it makes use of the Bridge-Tied-Load (BTL) principle. Consequently it has, at the same supply voltage, a higher output power compared to a conventional Single Ended output stage. It delivers an output power of 1 W into a loudspeaker load of 8 Ω with 6 V supply or 3 W into 16 Ω loudspeaker at 11 V without need of an external heatsink. The gain is internally fixed at 40 dB. Special attention is given to switch-on/off click suppression, and it has a good overall stability. The load can be short circuited at all input conditions.

3 W BTL mono audio output amplifier with DC volume control

TDA7056A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7056A is a mono BTL output amplifier with DC volume control. It is designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
P_O	output power	R_L = 16 Ω; V_P = 12 V	3	3.5	–	W
G_v	voltage gain		34.5	35.5	36.5	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	V_P = 12 V; R_L = ∞	–	8	16	mA
THD	total harmonic distortion	V_P = 0.5 W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056A	9	SIL	plastic	SOT110

3 W BTL mono audio output amplifier with DC volume control

TDA7056A

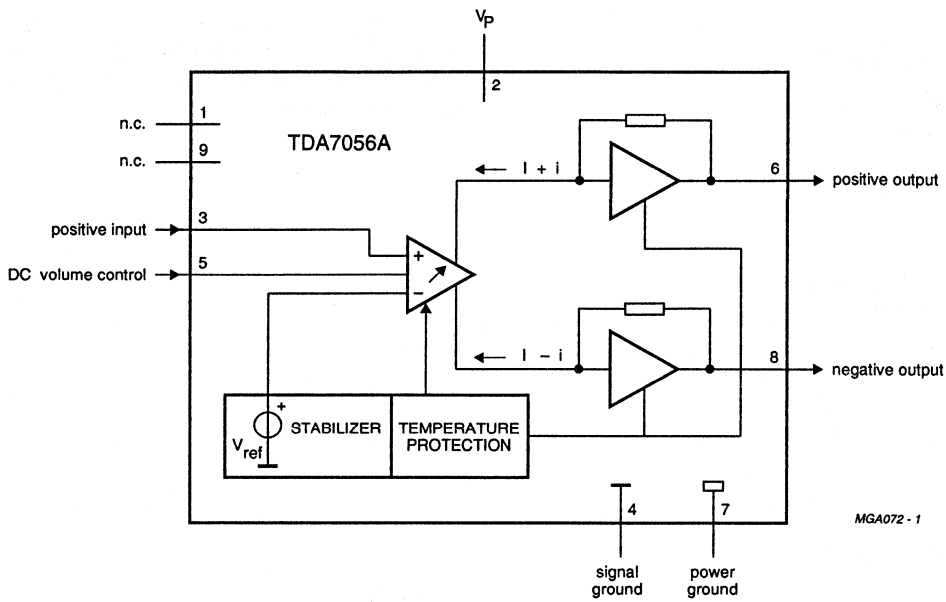


Fig.1 Block diagram.

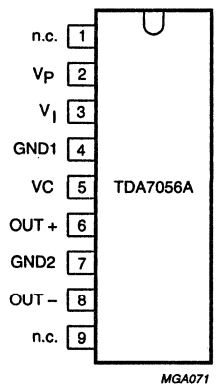


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V_P	2	positive supply voltage
V_I	3	voltage input
GND1	4	signal ground
VC	5	DC volume control
OUT+	6	positive output
GND2	7	power ground
OUT−	8	negative output
n.c.	9	not connected

2 x 3 W stereo BTL audio output amplifier

TDA7057Q

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

FEATURES

- No external components
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Short-circuit proof
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7057Q is a stereo output amplifier in a 13 pin power package. The device is designed for battery-fed portable stereo recorders and radios, but also suitable for mains-fed applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	11	18	V
P_O	output power	V_P = 11 V; R_L = 16 Ω	–	3	–	W
G_v	voltage gain		39	40	41	dB
I_P	total quiescent current	V_P = 11 V; R_L = ∞	–	10	14	mA
THD	total harmonic distortion	P_O = 0.5 W	–	0.25	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7057Q	13	SBD	plastic	SOT141

2 x 3 W stereo BTL audio output amplifier

TDA7057Q

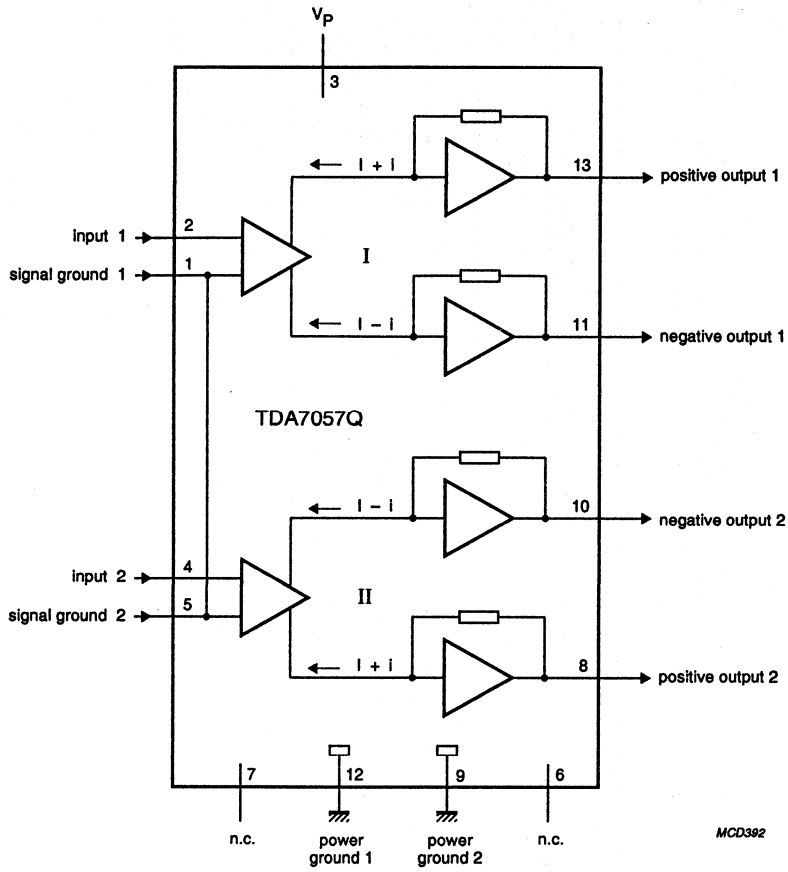


Fig.1 Block diagram.

Smart card coupler TDA8000; TDA8000T

FEATURES

- Two protected I/O lines
- V_{CC} regulation (5 V ±4%, 100 mA (max.), with controlled rise and fall times)
- V_{PP} generation (12.5, 15 or 21 V, ±2.5%, 50 mA (max.), programmable by two bits, with controlled rise and fall times)
- CLOCK generation (up to 6 MHz)
- Short-circuit, thermal and take-off protections
- Two voltage supervisors (digital and analog supplies)
- Automatic activation and de-activation sequences through an independent internal clock
- Enhanced ESD protections on card side (4 kV min.)
- ISO 7816 compatibility

APPLICATIONS

- Pay TV
- Telematics
- Cashless payment
- Multipurpose card-readers, etc.

GENERAL DESCRIPTION

The TDA8000 is a complete, low-cost analog interface which can be positioned between a smart card (ISO7816) and a microcontroller. The complete supply, protection and protocol functions are realized with only some external components, making this product very attractive for consumer applications (see examples in section APPLICATION INFORMATION).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage		6.6	–	18	V
I_{DD}	supply current Idle mode Active modes	 V_{DD}= 12 V unloaded	 – –	 25 32	 – –	 mA mA
V_{TH2}	threshold voltage on V_{SUP}		4.5	–	4.65	V
V_{CC}	card supply voltage		4.8	5.0	5.2	V
I_{CC}	card supply current		–	–	–100	mA
V_H	HIGH voltage supply for V_{PP}		–	–	30	V
I_{PP}	programming current Read mode Write mode	 V_{PP} = 5 V V_{PP} > 5 V	 – –	 – –	 –50 –50	 mA mA
t_{de}, t_{act}	de-activation/activation cycle duration		–	–	500	µs
T_{amb}	operating ambient temperature range		0	–	+70	°C
P_{tot}	continuous total power dissipation	from 0 to +70 °C; see Fig.10; TDA8000T TDA8000	 – –	 – –	 1 2	 W W

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8000T	28	SO28L	plastic	SOT136AH
TDA8000	28	DIL28	plastic	SOT117NG

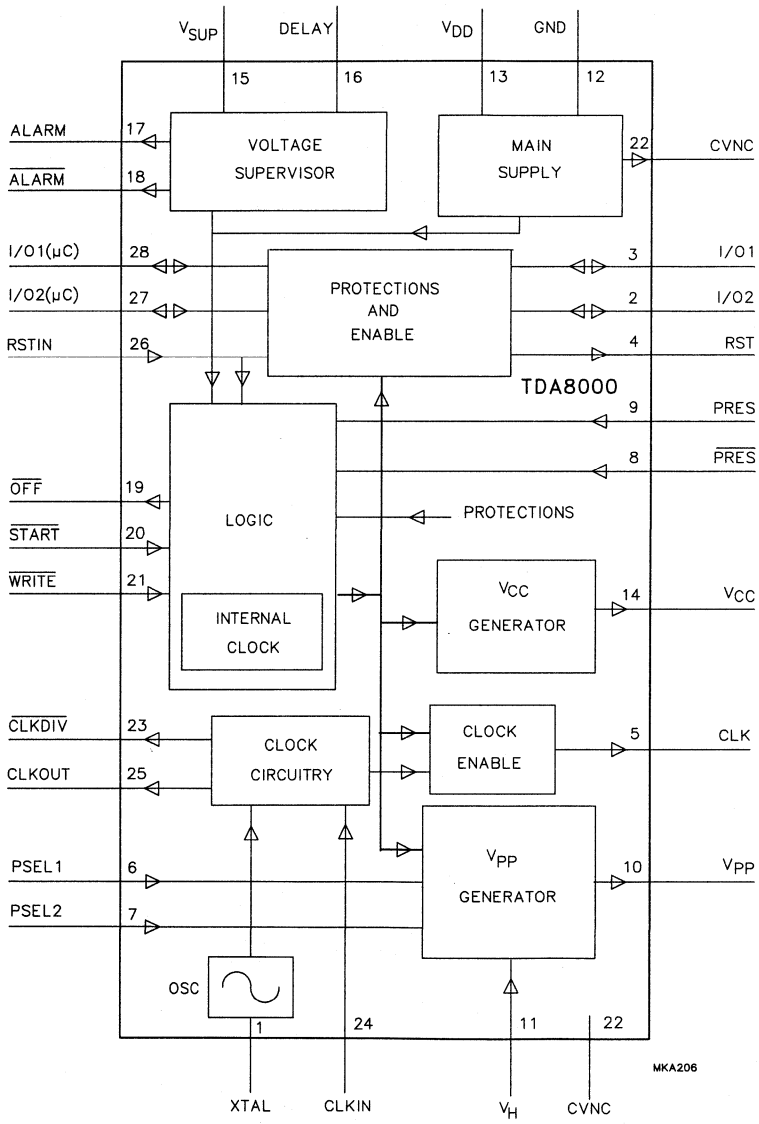


Fig.1 Block diagram.

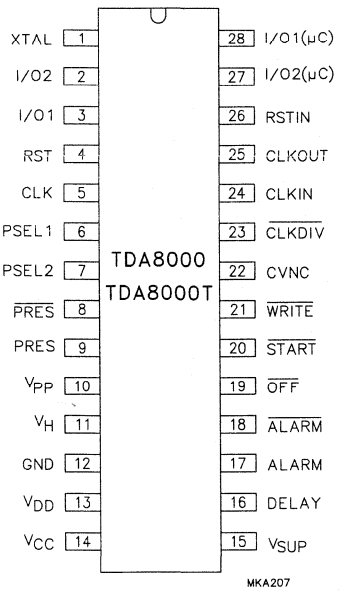


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
XTAL	1	crystal connection
I/O2	2	data line to/from the card
I/O1	3	data line to/from the card
RST	4	card reset output
CLK	5	clock output to the card
PSEL1	6	programming voltage selection input (see Table 1)
PSEL2	7	programming voltage selection input (see Table 1)
$\overline{PRES}$	8	card presence contact input (active LOW)
PRES	9	card presence contact input (active HIGH)
V_{PP}	10	card programming voltage output
V_H	11	high voltage supply for V_{PP} generation
GND	12	ground
V_{DD}	13	positive supply voltage
V_{CC}	14	card supply output voltage
V_{SUP}	15	voltage supervisor input
DELAY	16	external capacitor connection for delayed reset timing
ALARM	17	open-collector reset output for the microcontroller (active HIGH)
$\overline{ALARM}$	18	open-collector reset output for the microcontroller (active LOW)
$\overline{OFF}$	19	interrupt output to the microcontroller (active LOW)
$\overline{START}$	20	microcontroller input for starting session (active LOW)
$\overline{WRITE}$	21	control input for applying programming voltage to the card (active LOW)
CVNC	22	internally generated 5 V reference, present when V_{DD} is on; to be decoupled externally
$\overline{CLKDIV}$	23	input for dividing/not dividing the CLKOUT frequency by two (active LOW)
CLKIN	24	external clock signal input
CLKOUT	25	clock output to the microcontroller, or an other TDA8000.
RSTIN	26	card reset input from the microcontroller (active HIGH)
I/O2(μC)	27	data line to/from the microcontroller
I/O1(μC)	28	data line to/from the microcontroller

FUNCTIONAL DESCRIPTION

Power supply

The circuit operates within a supply voltage range of +6.6 to +18 V. V_{DD} and GND are the supply pins.
All card contacts remain inactive during power-up or power-down, provided V_{DD} does not rise or fall too fast (1 V/ms typically).

POWER UP

The logic part is powered first and is in the reset condition until V_{DD} reaches V_{TH1}.
The sequencer is blocked until V_{DD} reaches $V_{TH4} + V_{HYS4}$.

POWER-DOWN

When V_{DD} falls below V_{TH4}, an automatic de-activation of the contacts is performed.

Voltage supervisor

This block surveys the 5 V supply of the microcontroller (V_{SUP}) in order to deliver a defined reset pulse and to avoid any transients on card contacts during power-up or power-down of V_{SUP}.
The voltage supervisor remains active even if V_{DD} is powered-down.

POWER-UP

When V_{SUP} falls below $V_{TH2} + V_{HYS2}$ the capacitor C_{DEL}, tied to the DELAY pin, will be discharged.
When V_{SUP} rises to the threshold level, C_{DEL} will be recharged.
ALARM and $\overline{\text{ALARM}}$ remain active, and the sequencer is blocked until the voltage on the DELAY line reaches V_{TH3}.

POWER-DOWN (SEE FIG.3)

If V_{SUP} falls below V_{TH2}, C_{DEL} will be discharged, ALARM and $\overline{\text{ALARM}}$ become active, and an automatic de-activation of the contacts is performed.

Clock circuitry (see Fig.4)

The clock signal (CLK) can be applied to the card in two different methods:

1. Generation by a crystal oscillator: The crystal (2 to 12 MHz) is tied to the XTAL pin. Its frequency is divided by two.
2. Use of a signal frequency already present in the system and tied to the CLKIN pin (up to 6 MHz). The XTAL pin has to be tied to GND through a 1 kΩ resistor.

   In both cases the signal is buffered and enabled.

The CLKOUT pin may be used to clock a microcontroller. The signal ($f_{XTAL}/2$ or f_{XTAL} if $\overline{\text{CLKDIV}}$ is HIGH) is available when the circuit is powered up.

State diagram

Once activated, the circuit has six possible modes of operation:

- Idle
- Activation
- Read
- Write
- De-activation
- Fault

Figure 5 shows the way these modes are linked to each other.

IDLE MODE

After reset, the circuit enters the IDLE state. A minimum number of circuits are active while waiting for the microcontroller to start a session:

- All card contacts are inactive
- Voltage generators are stopped
- Oscillator is running, delivering CLKOUT
- Voltage supervisor is active

The $\overline{\text{OFF}}$ line is HIGH if a card is present (PRES and $\overline{\text{PRES}}$ active) and LOW if a card is not present.

ACTIVATION SEQUENCE

From the IDLE mode, the circuit enters the ACTIVATION mode when the microcontroller sets the $\overline{\text{START}}$ line (active LOW). The internal circuitry is activated, the internal clock starts and the following ISO7816 sequence is performed:

- 1 - V_{CC} rises from 0 to 5 V
- 2 - I/Os are enabled
- 3 - V_{PP} rises from 0 to 5 V
- 4 - No change
- 5 - CLK is enabled
- 6 - RST is enabled

The typical time interval between two steps is 32 µs for the two first and 64 µs for the other three. Timing is derived from the internal clock (see Fig.6).

Between steps 3 and 5, a HIGH level on RSTIN enables the CLK signal to be applied to the card. This feature allows a precise count of CLK periods while waiting for the card to respond to a reset.

After step 5, RSTIN has no further action on CLK.
After step 6, RST is set to the complementary value of RSTIN.

READ MODE

When the activation sequence is completed and, after the card has replied to its Answer-to-Reset, theTDA8000 enters the READ mode. Data is exchanged between the card and the microcontroller via the I/O lines.
When it is required to write to the internal memory of the card the circuit is set to the WRITE mode by the microcontroller.
Cards with EPROM memory need a programming voltage (V_{PP}).

V_{PP} GENERATION

The circuit supports cards with V_{PP} of 12.5, 15 or 21 V. The selection of P is achieved by PSEL1 and PSEL2.

	PSEL1	
PSEL2	L	H
L	5	12.5
H	15	21

In order to respect the ISO7816 slopes, the circuit generates V_{PP} by charging and discharging an internal capacitor. The voltage on this capacitor is then amplified by a power stage gain of 5, powered via an external supply pin V_H (30 V max.).

WRITE MODE (SEE FIG.7)

When the microcontroller sets the $\overline{\text{WRITE}}$ line (active LOW), the circuit enters the WRITE mode. V_{PP} rises from 5 V to the selected value with a typical slew rate of 1 V/µs. When the write operation is completed, the microcontroller returns the $\overline{\text{WRITE}}$ line to its HIGH state, and V_{PP} falls back to 5 V with the same slew rate. $\overline{\text{WRITE}}$ has no action outside a session.

DE-ACTIVATION SEQUENCE (SEE FIG.8)

When the session is completed, the microcontroller sets the $\overline{\text{START}}$ line to its HIGH state.

The circuit then executes an automatic de-activation sequence by counting the sequencer back:

- 6 - Card reset (RST falls to LOW)
- 5 - CLK is stopped
- 4 - No change
- 3 - V_{PP} falls to 0 V
- 2 - I/O(µC) become high Z
- 1 - V_{CC} falls to 0 V

The circuit returns to the IDLE mode on the next rising edge of the sequencer clock.

PROTECTIONS

Main fault conditions are monitored by the circuit:

- Short-circuit on V_{CC}
- Short-circuit on V_{PP}
- Over-current on I/Os
- Card take-off during transaction
- Overheating problem

When one of these fault conditions is detected, the circuit pulls the interrupt line $\overline{\text{OFF}}$ to its active LOW state and returns to the FAULT mode.

FAULT MODE (SEE FIG.9)

When a fault condition is written to the microcontroller via the $\overline{\text{OFF}}$ line, the circuit initiates a de-activation sequence.
After the de-activation sequence has been completed, the $\overline{\text{OFF}}$ line is reset to its HIGH state when the microcontroller has reset the $\overline{\text{START}}$ line HIGH, except if the fault condition was due to a card extraction.

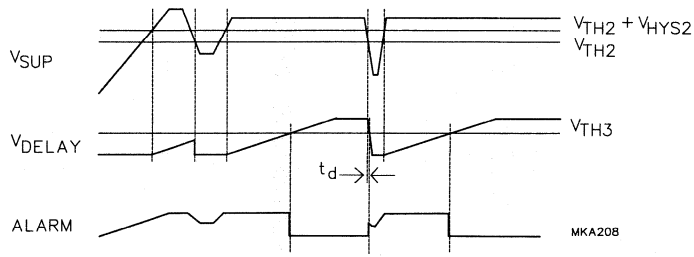


Fig.3 ALARM and DELAY as a function of V_{SUP} (C_{DEL} fixes the pulse width).

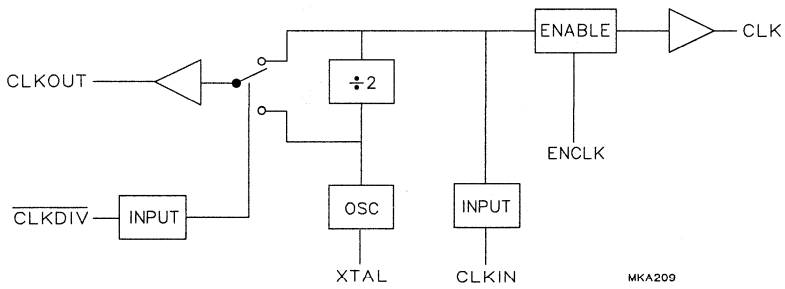


Fig.4 Clock circuitry.

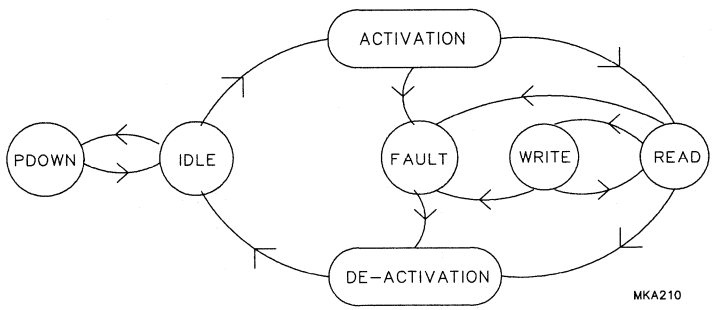


Fig.5 State diagram.

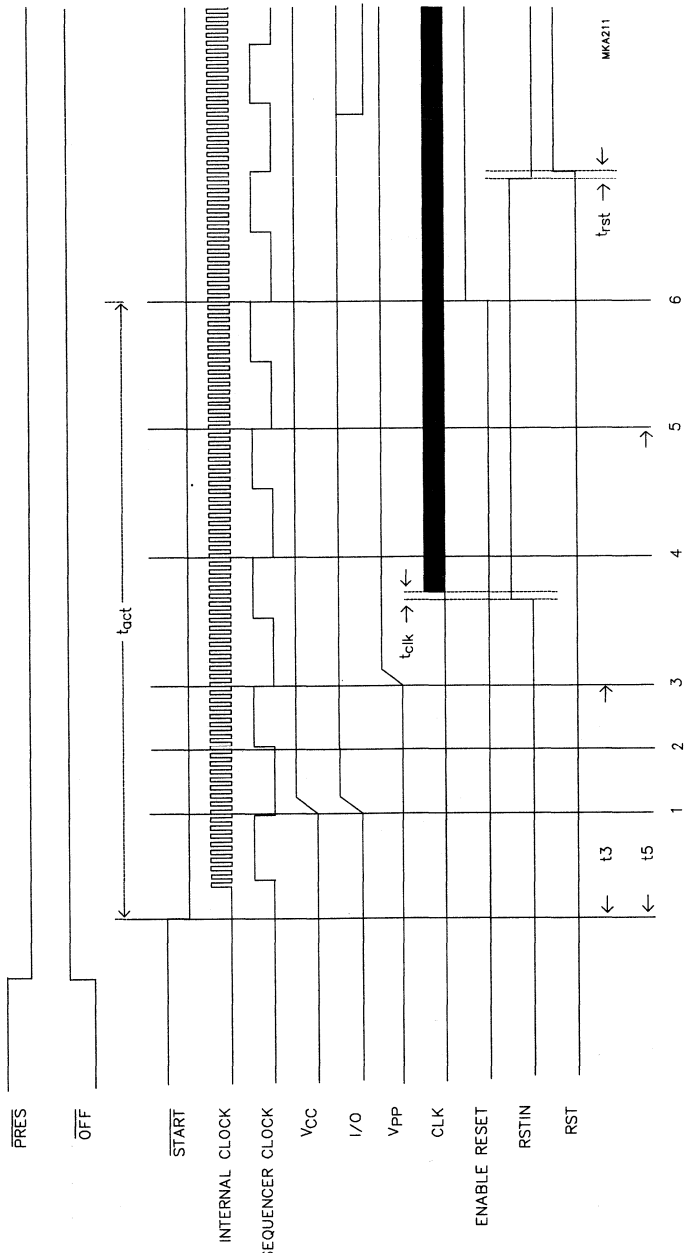


Fig.6 Activation sequence.

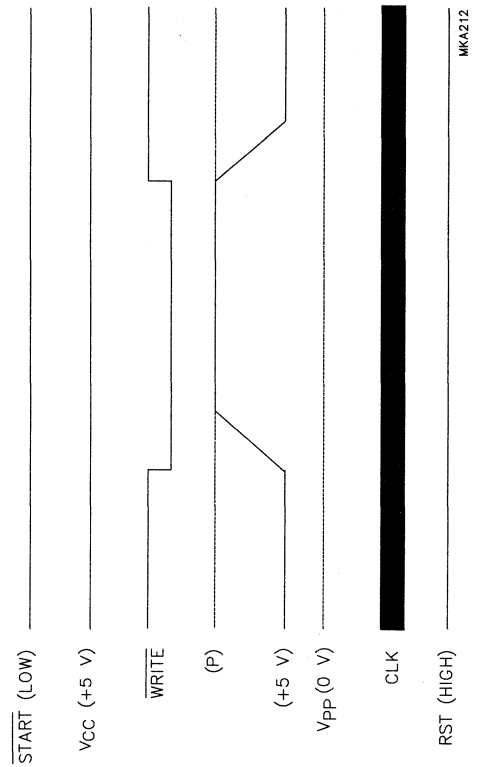


Fig.7 Read/Write, Read mode.

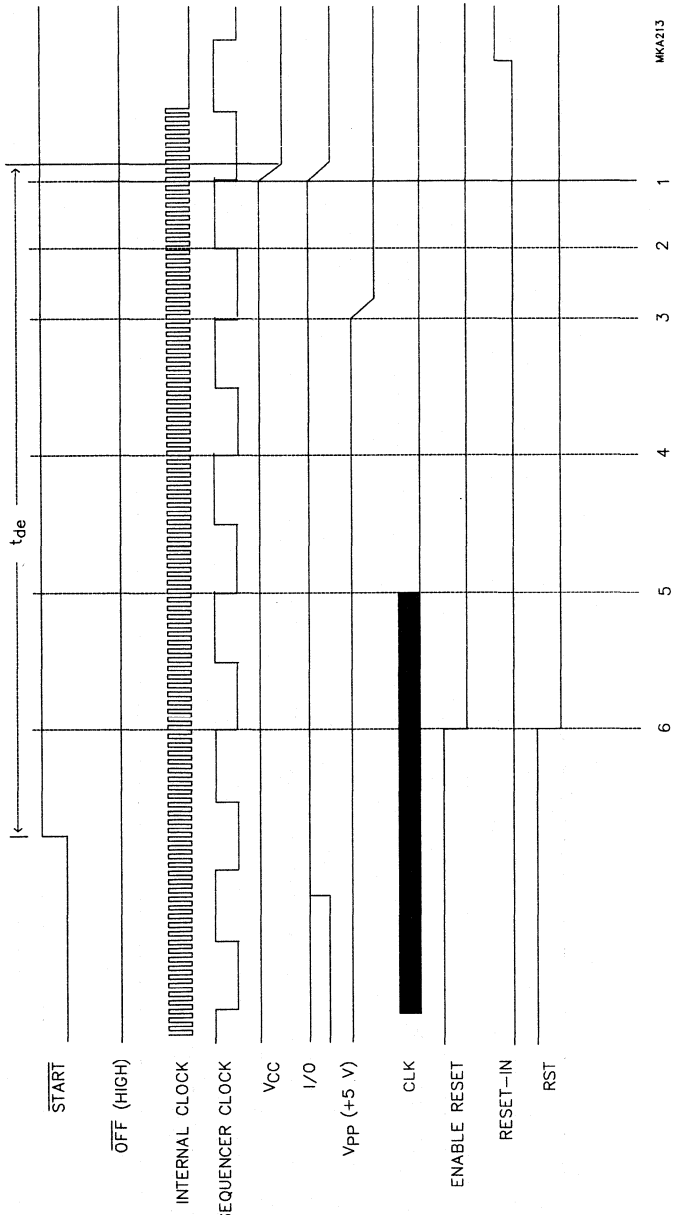


Fig.8 De-activation sequence after a normal session.

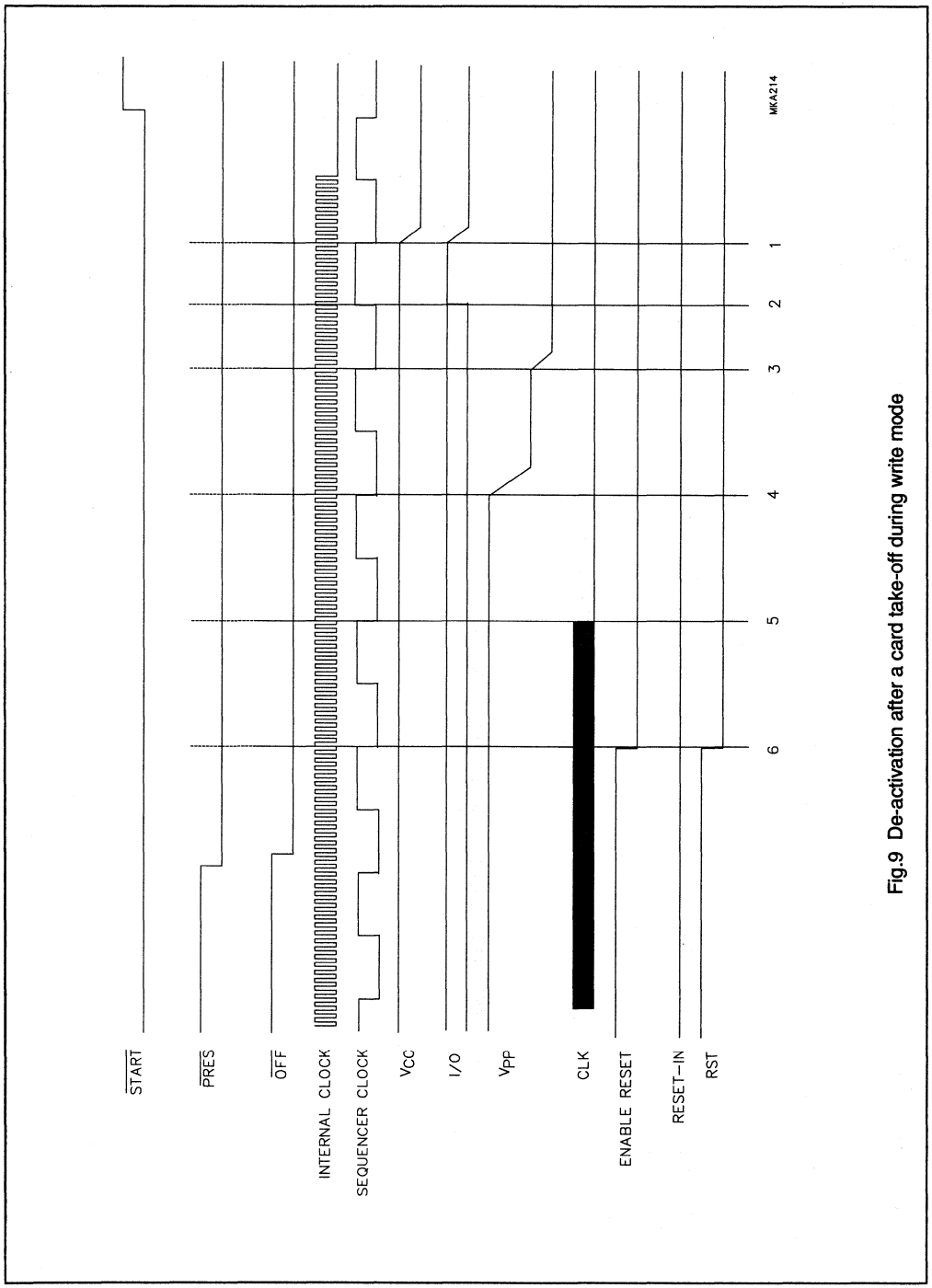


Fig.9 De-activation after a card take-off during write mode

Note

The two other causes of emergency de-activation (Power failure detected on V_{DD} or V_{SUP}) do not act upon $\overline{OFF}$.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage		−0.3	18	V
V_{x1}	voltage on pins PSEL1, PSEL2, PRES, $\overline{PRES}$, $\overline{WRITE}$, $\overline{START}$, $\overline{OFF}$, $\overline{ALARM}$, RSTIN		0	V_{DD}	V
V_H	voltage on pin V_H		0	30	V
V_{PP}	voltage on pin V_{PP}		0	V_H	V
V_{SUP}	voltage on pin V_{SUP}		0	12	V
V_{x2}	voltage on pins ALARM, DELAY		0	V_{SUP}	V
V_{x3}	voltage on pins XTAL, I/O1(µC), I/O2(µC), CLKIN, CLKOUT, $\overline{CLKDIV}$, CVNC		0	6.0	V
V_{x4}	voltage on pins I/O1, I/O2, RST, CLK, V_{CC}	duration < 1ms	0	7.0	V
P_{tot}	continuous total power dissipation	from 0 to +70 °C; note 1 TDA8000T TDA8000	 –	 1	 W
			–	2	W
T_{stg}	storage temperature range		−55	+150	°C
V_{es}	electrostatic voltage on pins I/O1, I/O2, V_{CC}, V_{PP}, RST, PRES, $\overline{PRES}$, CLK	see also handling	−4	+4	kV
	other pins		−2	+2	kV

Note to the limiting values

1. $P_{tot} = V_{DD} \times (I_{DD(unloaded)} + \Sigma I_{signals}) + I_{CC} \times (V_{DD} - V_{CC}) + \max.\{(V_H - V_{PP}) \times I_{PP(read)} + (V_H - V_{PP}) \times I_{PP(write)}\} + V_H \times I_{H(unloaded)} + V_{SUP} \times I_{SUP} + (V_{DD} - CVNC) \times I_{CVNC}$

   Where 'signals' means all signal pins used, excluding the supply pins.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air		
	TDA8000: DIL28	30	K/W
	TDA8000T: SO28	70	K/W

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 3 for card contacts, class 2 for the remaining. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulse − on each pin referenced to ground.

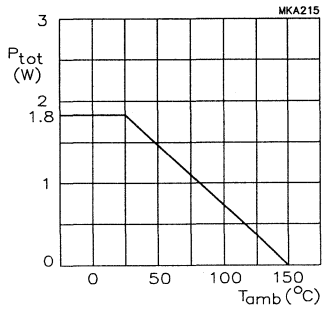


Fig.10 Power derating curve TDA8000 (DIL28).

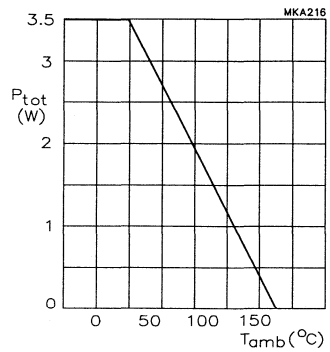


Fig.11 Power derating curve TDA8000T (SO28).

CHARACTERISTICS

V_{DD} = 12 V; V_H = 25 V; V_{SUP} = 5 V; T_{amb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	positive supply voltage		6.6	–	18	V
I_{DD}	positive supply current	Idle mode; V_{DD} = 8 V V_{DD} = 18 V Active mode; unloaded	 16 22 26	 22 28 32	 28 34 38	 mA mA mA
V_{TH1}	threshold voltage for power-on reset		1.5	3.0	4.0	V
V_{TH4}	threshold voltage on V_{DD} (falling)		6.0	–	6.4	V
V_{HYS4}	hysteresis on V_{TH4}		50	–	200	mV
Voltage supervisor						
V_{SUP}	supply voltage for the supervisor		–	5	–	V
I_{SUP}	input current on V_{SUP}		–	1.6	2	mA
V_{TH2}	threshold voltage on V_{SUP} (falling)		4.5	–	4.67	V
V_{HYS2}	hysteresis on V_{TH2}		10	–	80	]mV
V_{TH3}	threshold voltage on DELAY		2.35	–	2.65	V
I_{DEL}	output current on DELAY	pin grounded (charge) V_{DEL} = 4 V (discharge)	–4 6	– –	–2.5 –	µA mA
V_{DEL}	voltage on pin DELAY		–	–	3.5	V
ALARM, $\overline{\text{ALARM}}$ (open-collector outputs)						
I_{OH}	HIGH level output current on pin $\overline{\text{ALARM}}$	V_{OH} = 5 V	–	–	25	µA
V_{OL}	LOW level output voltage on pin $\overline{\text{ALARM}}$	I_{OL} = 2 mA	–	–	0.4	V
I_{OL}	LOW level output current on pin ALARM	V_{OL} = 0 V	–	–	–25	µA
V_{OH}	HIGH level output voltage on pin ALARM	I_{OH} = –2 mA	V_{SUP} – 1	–	–	V
t_D	delay between V_{SUP} and ALARM	C_{DEL} = 47 nF; see Fig.3	–	–	10	µs
t_{pulse}	ALARM pulse width	C_{DEL} = 47 nF	30	–	65	ms
Interrupt line $\overline{\text{OFF}}$ (open-collector)						
I_{OH}	HIGH level output current	V_{OH} = 5 V	–	–	25	µA
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	–	–	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic inputs (RSTIN, $\overline{\text{START}}$, WRITE, CLKDIV, PSEL1, PSEL2, PRES, $\overline{\text{PRES}}$); note 1						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		1.5	–	–	V
I_{IL}	LOW level input current	V_{IL} = 0 V	–	–	–10	µA
I_{IH}	HIGH level input current	V_{IH} = 5 V	–	–	10	µA
Reset output to the card (RST)						
V_{IDLE}	output voltage in IDLE		–	–	0.4	V
V_{OL}	LOW level output voltage	I_{OL} = 200 µA	–	–	0.45	V
V_{OH}	HIGH level output voltage	I_{OH} = –200 µA I_{OH} = –10 µA	4.0 V_{CC} – 0.7	– –	V_{CC} V_{CC}	V V
t_{rst}	delay between RSTIN and RST	RST enabled; see Fig.6	–	–	2	µs
Clock output to card (CLK)						
V_{IDLE}	output voltage in IDLE		–	–	0.4	C]V
V_{OL}	LOW level output voltage	I_{OL} = 200 µA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –200 µA I_{OH} = –20 µA I_{OH} = –10 µA	2.4 0.7V_{CC} V_{CC} – 0.7	– – –	V_{CC} + 0.3 V_{CC} + 0.3 V_{CC} + 0.3	V V V
t_r	rise time	C_L = 30 pF; note 2	–	–	18	ns
t_f	fall time	C_L = 30 pF; note 2	–	–	18	ns
δ	duty cycle	C_L = 30 pF; note 2	45	–	55	%
Card programming voltage (V_{PP})						
P	selected voltage	see Table 1				
V_{PP}	output voltage	Idle mode Read mode Write mode: I_{PP} < 50 mA $\Delta I_{PP}/\Delta t$ < 100 mA/µs	– V_{CC} – 4% P – 2.5% P – 4%	– – – –	0.4 V_{CC} + 4% P + 2.5% P + 4%	V V V V
I_{PP}	output current	Read mode Write mode V_{PP} shorted to GND	– – –	– – –	–50 –50 –400	mA mA mA
SR	slew rate	up or down	0.75	1.0	1.25	V/µs

High-voltage input (V_H)						
V_H	input voltage		–	–	30	V
I_H	input current at V_H	Idle mode Active mode; unloaded P = 5 V P = 12.5 V P = 15 V P = 21 V	2 3 5 6 8	– – – – –	3 7 10 11 13	mA mA mA mA mA
$V_H - V_{PP}$	voltage drop		–	–	2.2	V
Card supply voltage (V_{CC})						
V_{CC}	output voltage	Idle mode Active mode; I_{CC} < 100 mA	– 4.80	– –	0.4 5.20	V V
I_{CC}	output current	– V_{CC} shorted to GND	– –	– –	–100 –400	mA mA
SR	slew rate	up or down	0.75	1.0	1.25	V/µs
5 V reference output (CVNC)						
V_{CVNC}	output voltage at CVNC		4.5	5	5.5	V
I_{CVNC}	output current at CVNC		–	–	–10	mA
Crystal connection (XTAL)						
R_{XTAL}	negative resistance at XTAL	2 MHz < f < 12 MHz; note 3	–	–	–300	Ω
V_{XTAL}	DC voltage at XTAL		3	–	4	V
f_{XTAL}	resonant frequency		2	–	12	MHz
External clock input (CLKIN)						
f_{EXT}	frequency at CLKIN	note 2	0	–	6	MHz
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		1.5	–	5	V
I_{IL}	LOW level input current	V_{IL} = 0 V	–	–	–10	µA
I_{IH}	HIGH level input current	V_{IH} = 2 V	–	–	10	µA
C_I	input capacitance		–	–	5	pF
Clock output (CLKOUT)						
f_{CLKOUT}	frequency on CLKOUT		1	–	8	MHz
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –200 µA I_{OH} = –10 µA	3 4	– –	– –	V V
t_r, t_f	transition times	C_L = 15 pF; note 2	–	–	25	ns
δ	duty cycle	C_L = 15 pF; note 2	40	–	60	%

High-voltage input (V_H)						
Data lines (I/O1, I/O2, I/O1(μC), I/O2(μC))						
V_{OH}	HIGH level output voltage on I/O	$4.5 < V_{SUP} < 5.5$; $4.5 < V_{I/O(\mu C)} < 5.5$ $I_{OH} = -20$ μA $I_{OH} = -200$ μA	 4 2.4	 – –	 $V_{CC} + 0.1$ –	 V V
V_{OL}	LOW level output voltage on I/O	$I_{I/O} = 1$ mA; I/O(μC) grounded	–	–	60	mV
I_{IL}	LOW level input current on I/O(μC)	I/O(μC) grounded	–	–	–500	μA
V_{OH}	HIGH level output voltage on I/O(μC)	$4.5 < V_{I/O} < 5.5$	4	–	$V_{SUP} + 0.2$	V
V_{OL}	LOW level output voltage on I/O(μC)	$I_{I/O(\mu C)} = 1$ mA; I/O grounded	–	–	70	mV
I_{IL}	LOW level input current on I/O	I/O grounded	–	–	–500	μA
V_{IDLE}	voltage on I/O outside a session		–	–	0.4	V
Z_{IDLE}	impedance on I/O(μC) outside a session		10	–	–	MΩ
R_{pd}	internal pull-up resistance between I/O and V_{CC}		17	20	23	kΩ
t_r, t_f	transition times	$C_I = C_O = 30$ pF	–	–	1	μs
Protections						
T_{sd}	shut-down local temperature		–	135	–	°C
I_{CCsd}	shut-down current at V_{CC}		–100	–	–200	mA
I_{PPsd}	shut-down current at V_{PP}		–50	–	–100	mA
I_{IOsd}	shut-down current at I/O's	from I/O to I/O(μC)	3	–	5	mA
Timing						
t_{act}	activation sequence duration	see Fig.6	250	–	500	μs
t_{de}	de-activation sequence duration	see Fig.8	250	–	500	μs
t_3	start of the window for sending CLK to the card	see Fig.6	–	–	155	μs
t_5	end of the window for sending CLK to the card	see Fig.6	205	–	–	μs
t_{st}	maximum pulse width on START before V_{CC} starts rising		–	–	30	μs
t_{clk}	delay between RSTIN and CLK	see Fig.6	–	–	2	μs

Notes to the characteristics

1. $\overline{START}$, $\overline{WRITE}$, $\overline{CLKDIV}$ and $\overline{PRES}$ are active LOW; RSTIN and PRES are active HIGH.
2. The transition time and duty cycle definitions are shown in Fig.11; $\delta = t_1/t_1 + t_2$.

   Caution

   To ensure the specified transition characteristics on the CLK pin, the CLKIN signal has to meet the following criteria: $t_r/t_f < 10$ ns; $47.5\% < \delta < 52.5\%$.
3. This condition ensures proper starting of the oscillator with crystals having series resistance up to 100 Ω.

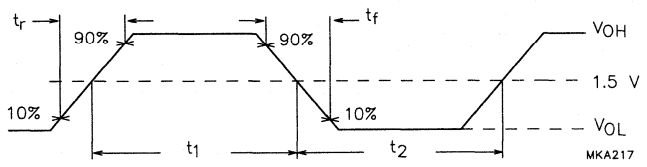


Fig.12 Transition times definition.

INTERNAL CIRCUITRY

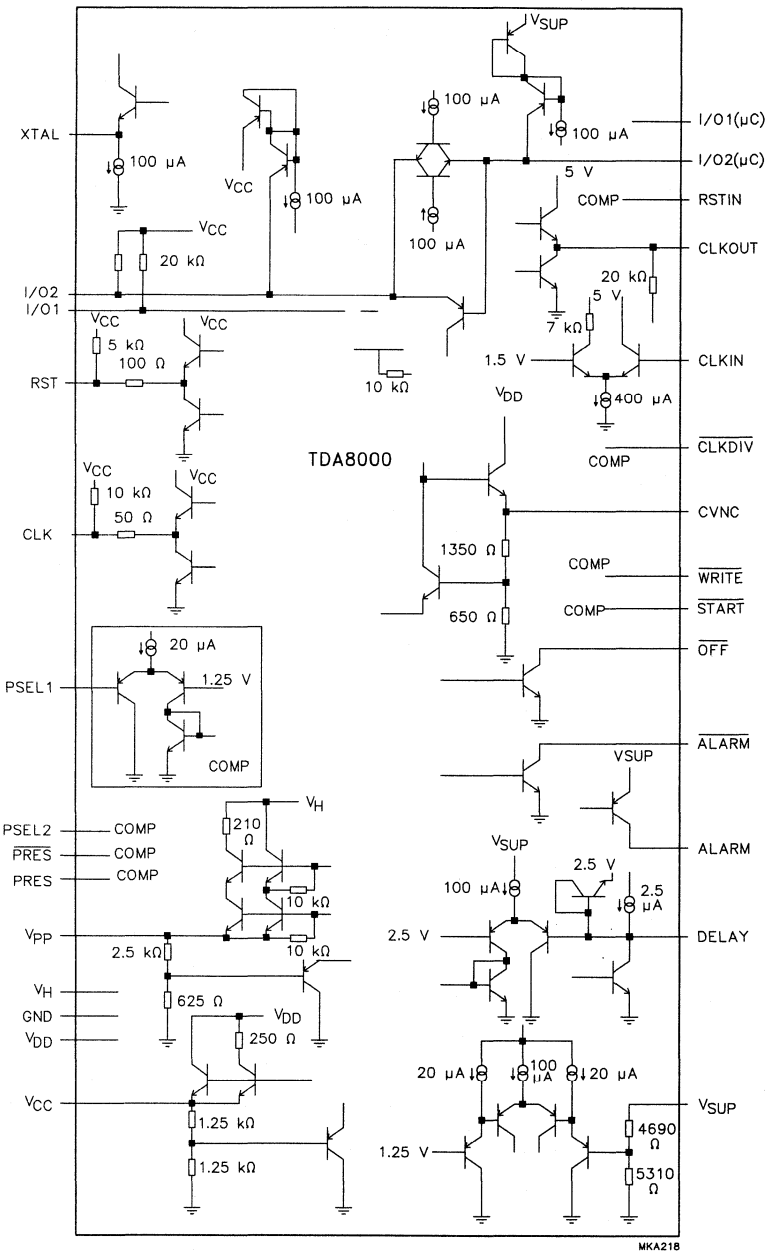


Fig.13 Internal pin configuration.

APPLICATION INFORMATION

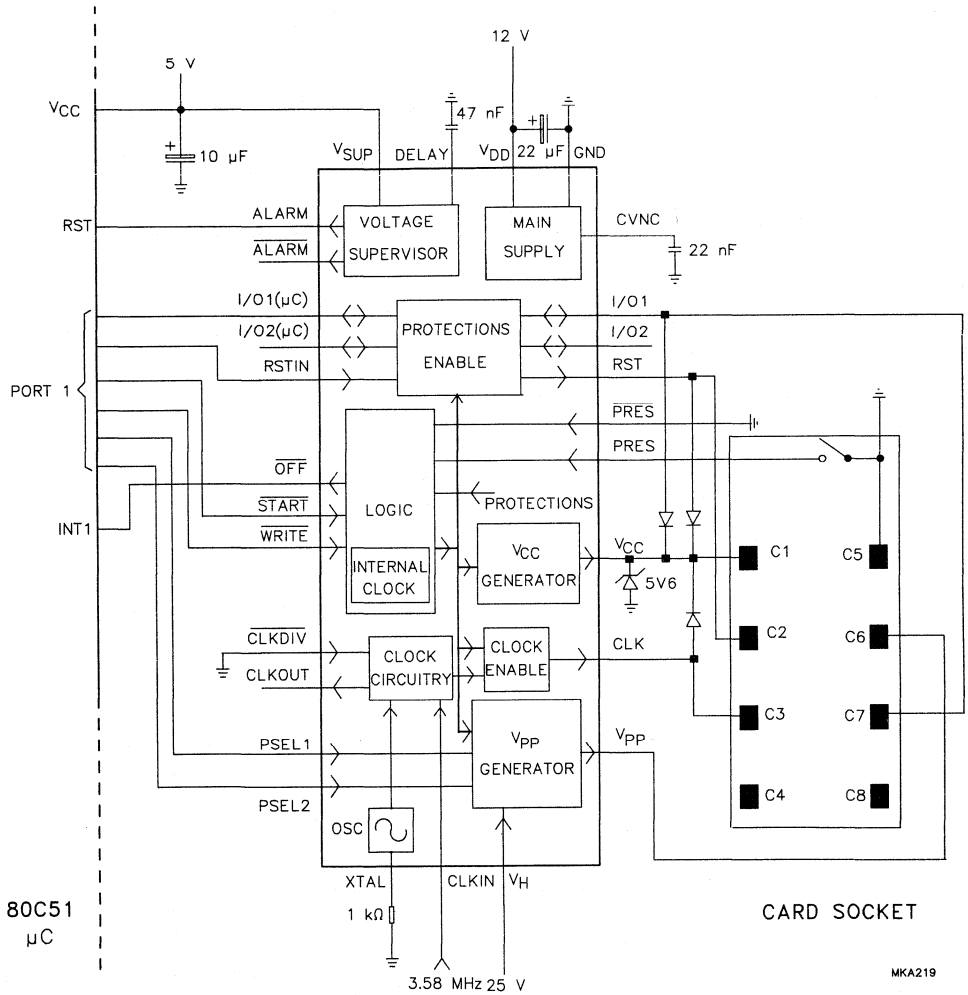


Fig.14 Typical application within a consumer product.

Note

Other examples are available in the application report upon request.

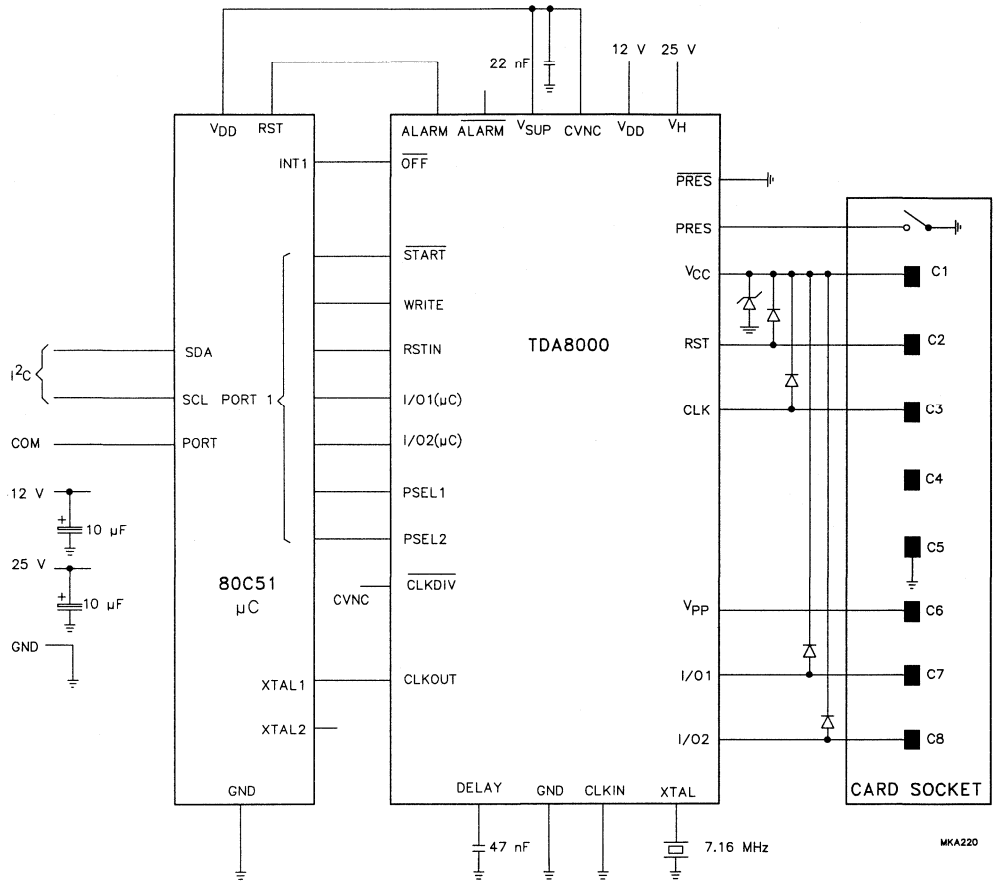


Fig.15 Application in a remote card reader; microcontroller is clocked and powered by the TDA8000; interface is done through I²C bus.

Small signal combination IC for colour TV

TDA8302

FEATURES

- Gain controlled vision IF amplifier
- Synchronous demodulator for negative demodulation
- AGC detector operating on peak sync
- Tuner AGC
- AFC circuit with sample-and-hold and on/off-switch
- Video preamplifier
- Video switch to select either the internal video signal or an external video signal
- Horizontal synchronization circuit with two control loops
- Vertical synchronization (divider system), ramp generator for 60 Hz only
- Transmitter identification (mute)
- Sandcastle pulse generation
- VCR/auto VCR switch.

GENERAL DESCRIPTION

The device includes a three-stage video IF amplifier, AFC and AGC circuitry, integral three-level sandcastle pulse generator, fully synchronized horizontal and vertical time bases with drive circuits, a video switch and a transmitter identification/mute circuit. A functional colour TV receiver can thus be realised with the addition of a tuner, audio demodulator and amplifier, chrominance decoder and respective line and field deflection circuitry.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8302	32	DIL	plastic	SOT201

FUNCTIONAL DESCRIPTION

Video IF amplifier, demodulator and video amplifier

Each of the three AC-coupled IF stages permits the omission of DC feedback and possesses a control range in excess of 20 dB.

The IF amplifier is followed by a passive synchronous demodulator providing a regenerated carrier signal. This is limited by a logarithmic limiter circuit prior to its application to the demodulator. Improved picture synchronization is provided by a wider bandwidth together with improved video amplifier linearity. The video amplifier contains also a white spot inverter and a noise clamp which limits interference pulses to a point below the peak sync level.

AFC-circuit

The reference signal for the AFC quadrature demodulator can also be acquired from the tuned circuit of the IF synchronous demodulator because an accurate 90° phase shift is realised internally. In this way only one tuned circuit needs to be applied and only one adjustment has to be carried out. The AFC output is affected by the asymmetrical frequency spectrum of the signal fed to the quadrature demodulator, which is determined by the SAW filter characteristic. To overcome this video frequency dependency of the AFC output, the demodulator output is followed by a sample-and-hold circuit.
For the reception of negative-going signals, the output is sampled only during peak sync, where a non-modulated carrier is present. Substantial noise will be present on the quadrature demodulator input signal during reception of very weak signals. This noise has an asymmetrical frequency spectrum (with respect to the IF carrier) causing an offset in the AFC output voltage. This effect can be minimized by applying a notch in the demodulator tuned circuit. The sample-and-hold circuit is followed by an amplifier with high output impedance. The steepness of the of the AFC control voltage can be lowered by applying load resistors from the output to the supply and to ground. The AFC output is switched off when the AFC sample pin (22) is connected to ground.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 8)		10	12	13.2	V
I_P	supply current (pin 8)		90	115	140	mA
I_{start}	start current (pin 12)	note 1	-	6.5	9	mA
Video						
$V_{9\text{-}10(rms)}$	IF sensitivity (RMS value)	note 2	25	40	65	µV
$G_{9\text{-}10}$	IF gain control range		-	74	-	dB
S/N	signal-to-noise ratio	input signal = 10 mV	52	58	-	dB
V_{21}	AFC output voltage swing		10.5	-	11.5	V
Video switch						
$V_{16(p\text{-}p)}$	internal video input (peak-to-peak value)	V_O = 2.5 V(p-p)	-	2	-	V
$V_{13(p\text{-}p)}$	external video input (peak-to-peak value)	V_O = 2.5 V(p-p)	-	1	-	V
$V_{15(p\text{-}p)}$	video output signal (peak-to-peak value)		2.3	2.5	2.7	V
Sync						
V_{28}	required sync pulse amplitude	note 3	200	750	-	mV
I_{30}	required input current during flyback pulse		0.1	-	2	mA
V_{30}	sandcastle output during					
	burstkey		8	-	-	V
	horizontal blanking		4	4.4	5	V
	vertical blanking		2.1	2.5	2.9	V
V_{14}	video transmitter identification output					
	no signal condition		-	0.3	-	V
	signal condition		-	12	-	V
V_5	vertical feedback for DC voltage		2.9	3.3	3.7	V
$V_{5(p\text{-}p)}$	vertical feedback for AC voltage (peak-to-peak value)		-	1	-	V

Notes to the quick reference data

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_{cc}) is obtained from the horizontal output stage. The load current of the driver must be added to the value given.
2. On set AGC.
3. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.

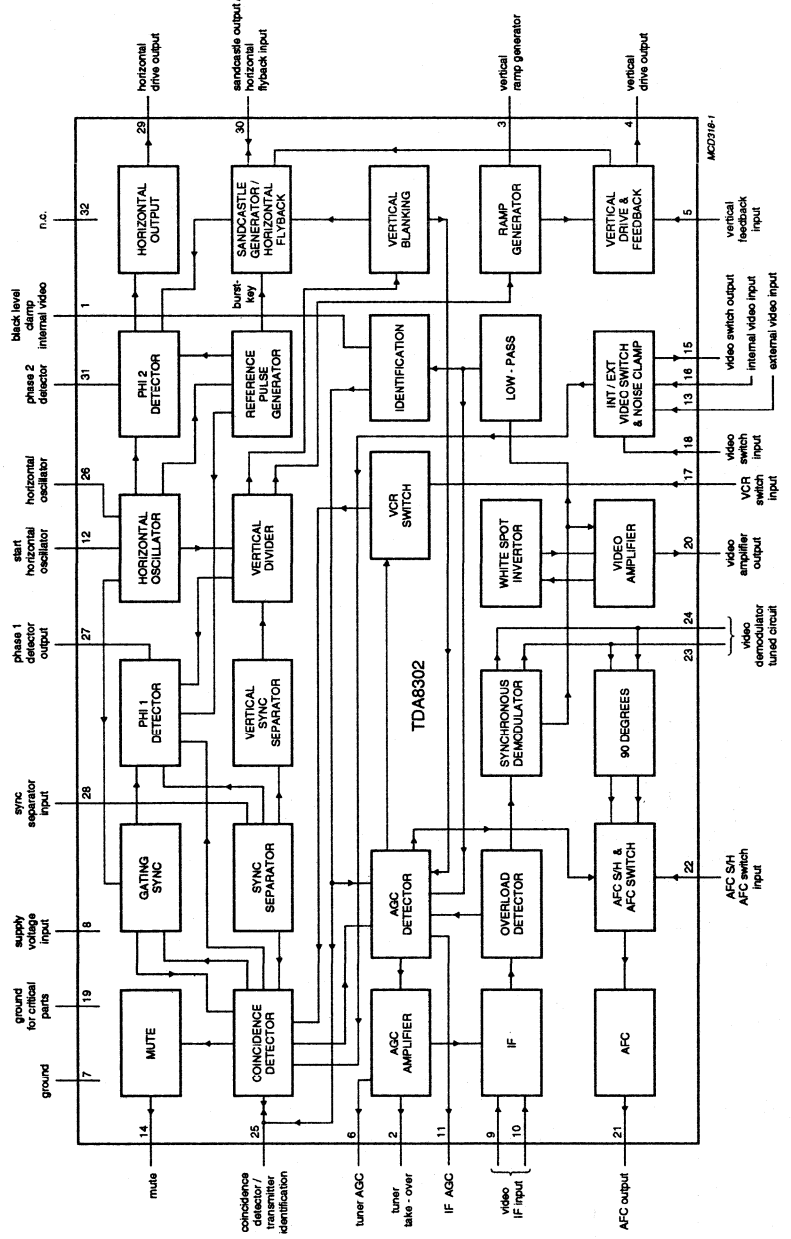


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	black level clamp internal video
2	tuner take-over
3	vertical ramp generator
4	vertical drive
5	vertical feedback
6	tuner AGC
7	ground
8	supply voltage input
9	video IF input
10	video IF input
11	IF AGC
12	start horizontal oscillator
13	external video input
14	mute
15	video switch output
16	internal video input
17	VCR switch input
18	video switch input
19	ground for some critical parts
20	video amplifier output
21	AFC output
22	AFC S/H, AFC switch input
23	video demodulator tuned circuit
24	video demodulator tuned circuit
25	coincidence detector/transmitter identification
26	horizontal oscillator
27	phase 1 detector
28	sync separator input
29	horizontal drive output
30	sandcastle output/horizontal flyback input
31	phase 2 detector
32	not connected

The transmitter identification/coincidence detector

A mute signal (see Table 1) is generated to disable the audio preamplifier of an audio demodulator during the absence of a transmission signal. This prevents the emission of excessive noise from the loudspeaker, particularly when selecting an alternative program channel.

When the video switch is in the internal mode, the coincidence detector will be used as transmitter identification. Pin 25 is HIGH when the horizontal loop is synchronized with the video signal and LOW in the case of no-synchronization. In the external mode the IF part of the circuit has its own identification system. The system relies upon the detection of sync pulses on the incoming IF signal. The separated horizontal sync pulse charges the capacitor on pin 25 which drives the mute output (pin 14).

VCR switch

The TDA8302 has a separate pin (pin 17) for the VCR switch, see tables 2 and 4.

Due to the inherent instability of signals from a VCR, the horizontal time constant should be shorter to prevent loss of horizontal synchronization in the early part of the scan. Provision is therefore incorporated (in the auto VCR mode) to automatically switch the short time constant such that a strong signal instigates the 'VCR' mode and a weak signal triggers the 'TV' mode. The phase detector is gated during the 'TV mode' and operates with a slow time constant.

Video-switch

Video output from the device is filtered to remove the audio carrier and DC-coupled to pin 16. The TDA8302 provides the opportunity for a direct video connection (e.g. via a peritel connector) to be made to the device at pin 13. Selection between internal and external video is made by applying a switching potential to pin 18, see Table 3. The AGC detector is not gated during the external video mode, the first detector is also not gated and operates with a short time constant.

Table 1 MUTE truth Table

INPUT/OUTPUT	STATUS	STATUS	STATUS	STATUS	STATUS
Input signal Pins 9 and 10	60 Hz	none	60 Hz	60 Hz	none
output pin 25	9.5 V	0.3 V	9.5 V	9.5 V	0.3 V
input pin 28	60 Hz	none	60 Hz	none	60 Hz
input pin 18	LOW	LOW/ HIGH	HIGH	HIGH	HIGH
output pin 14	12 V	0.3 V	12 V	12 V	0.3 V

Table 2 VCR switch operation

INPUT	VCR MODE	AUTO VCR MODE	TV MODE
pin 17 (pin 18 = LOW)	HIGH	n.c.	LOW

Table 3 Video switch operation

INPUT	INTERNAL VIDEO	EXTERNAL VIDEO
pin 18	LOW	HIGH

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 8)	-	13.2	V
P_{tot}	total power dissipation	-	2.3	W
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	–25	+65	°C

QUALITY SPECIFICATION

Quality level according to UZW-BQ/FQ-601.

SYMBOL	PARAMETER	RANGE A	RANGE B	UNIT
ESD	protection circuit specification (note 1)	2000	500	V
		100	200	pF
		1500	0	Ω

Note to the Quality specification

1. All pins of the IC are protected against ESD by means of the internal clamping diodes. Range A represents the human body model and range B represents the charge device model.

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	30	35	K/W

Gain-reduction in the external video mode

The TDA8302 has an option to reduce the gain of the IF amplifier to prevent crosstalk from the IF to the horizontal oscillator when the circuit is in the external mode and there is no signal at the RF. The gain of the IF amplifier is reduced with 20 dB when the video-switch (see Table 3) is in the external video mode and pin 17 is connected with a resistor of 39 kΩ to ground. Without this resistor the IF remains at full gain. In the external video mode the 39 kΩ resistor has to be disconnected to achieve the auto VCR mode.

Horizontal synchronization

The horizontal synchronization circuit of the TDA8302 provides the drive pulse for a horizontal deflection stage.

- The phase of the control loop will be adapted automatically to the level of the input signal in order to achieve an optimum performance.
- The control gradient of the control loop will be low at reception of weak signals to reduce the noise bandwidth.
- The phase detector control current is increased during strong or no-signal reception to obtain a short catching time and a good performance during VCR playback.

Vertical synchronization

The TDA8302 embodies a synchronized divider system for generating the vertical sawtooth at pin 3 having several advantages and features such as:

- The advantage of the divider is that the vertical frequency is alignment free, and the provision of a maximum interference/disturbance protection.
- A discriminator-window checks the accuracy of the vertical trigger pulse.
- The divider system operates with a number of different reset windows. The windows are activated via an up/down counter. The counter increases its counter-value by 1 for each time the separated vertical sync pulse appears within the selected window, otherwise the counter value is lowered by 1.

Modes of operation

Large search window: divider ratio between 488 and 576.

This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found does not comply with the narrow window specification limits
- Up/down counter value of the divider system, operating in the narrow window mode, drops below count 10

Narrow window mode: divider ratio between 522 - 528 (60 Hz).

- The divider system switches over to narrow window mode when the up/down counter has reached his maximum value of 15 approved vertical sync pulses.
- When the divider operates in the narrow window mode and a vertical sync pulse is missing in the window, the divider is reset at the end of that window and the counter value is lowered by 1.
- At a counter value below 10 the divider system switches over to the large window mode.
- The divider system generate also the so-called anti-top-flutter pulse which inhibits the phase 1 detector during the vertical sync pulse. The width of this pulse depends on the divider mode. For the large window mode the start is generated at the reset of the divider. In the narrow window mode the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 12.
- The divider is switched to count 525 when out of sync is detected by the coincidence detector. This results in a stable amplitude when no input signal is available.

CHARACTERISTICS

T_{amb} = 25 °C; V_p = 12 V; carrier 38.9 MHz negative modulation, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 8)						
V_8	supply voltage range		10	12	13.2	V
I_8	supply current	no input	90	115	140	mA
I_{12}	start current (pin 12)	note 1	-	6.5	9	mA
V_{12}	start protection level	I_{12} = 12 mA	-	-	16.5	V
IF Amplifier						
$V_{9-10(rms)}$	input sensitivity (RMS value)	note 2	25	40	65	µV
R_{9-10}	differential input resistance	note 3	-	1300	-	Ω
C_{9-10}	differential input capacitance	note 3	-	5	-	pF
G_{9-10}	gain control range		-	74	-	dB
ΔV_{20}	output signal expansion for 46 dB input signal variation	note 4	-	1	-	dB
V_{9-10}	maximum input signal		100	170	-	mV
Video Amplifier (notes 5 and 6)						
V_{20}	zero signal output level		4.7	4.9	5.1	V
V_{20}	peak sync level		2.5	2.7	2.9	V
V_{20}	white spot threshold level		-	5.5	-	V
V_{20}	white spot insertion level		-	4	-	V
Z_{20}	video output impedance		-	25	-	Ω
I_{20}	internal bias current of npn emitter follower output transistor		1.4	1.8	-	mA
I_{source}	maximum source current (pin 20)		10	-	-	mA
B	bandwidth of demodulated output signal		5	6	-	MHz
G_{20}	differential gain	note 7	-	2	5	%
φ	differential phase	note 7	-	2	5	°
NL	video non linearity	note 8	-	2	5	%
	intermodulation	note 9				
	1.1 MHz; blue		50	60	-	dB
	1.1 MHz; yellow		50	60	-	dB
	3.3 MHz; blue		55	65	-	dB
	3.3 MHz; yellow		55	65	-	dB
S/N	signal-to-noise ratio	10 mV input signal	52	58	-	dB
		end of gain control range; note 10; see Fig.5	57	62	-	dB
V_{20}	residual carrier signal		-	2	10	mV
V_{20}	residual 2nd harmonic of carrier signal		-	2	10	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF sync separator						
I_I	input current		0.4	0.6	0.8	mA
I_O	output current (pin 1)		22	27	32	µA
V_1	clamp level		-	3.3	-	V
Tuner AGC						
$V_{9\text{-}10(rms)}$	minimum starting point for tuner take-over (RMS value)		-	-	0.2	mV
$V_{9\text{-}10(rms)}$	maximum starting point for tuner take-over (RMS value)		100	150	-	mV
I_6	maximum tuner AGC output swing	V_6 = 3 V	4	-	-	mA
V_6	output saturation voltage	I_6 = 2 mA	-	-	300	mV
I_6	leakage current		-	-	1	µA
	input signal variation complete tuner control	ΔI_6 = 2 mA	0.2	2	4	dB
V_2	minimum voltage tuner take-over		-	-	1	V
Video Switching Circuit (note 12)						
EXTERNAL POSITIVE VIDEO INPUT						
$V_{13(p\text{-}p)}$	input signal (peak-to-peak value)	V_O = 2.5 V(p-p)	-	1	-	V
I_{13}	input current		-	1.5	5	µA
V_{13}	peak sync clamping level	I_{13} = 1 mA	1.65	1.85	2.05	V
INTERNAL VIDEO INPUT						
$V_{16(p\text{-}p)}$	Internal video input signal (peak-to-peak value	V_O = 2.5 V(p-p)	-	2	-	V
I_{16}	input current		-	1.5	5	µA
V_{16}	noise clamping level	I_{16} = 1 mA	2.2	2.4	2.6	V
POSITIVE VIDEO OUTPUT						
$V_{15(p\text{-}p)}$	video output signal (peak-to-peak value)		2.3	2.5	2.7	V
V_{15}	peak sync signal		-	3	-	V
I_{bias}	internal bias current (pin 15)		1	1.5	-	mA
I_O	maximum output current (pin 15)		5	-	-	mA
α	crosstalk external to internal	notes 12 and 13	-	55	-	dB
α	crosstalk internal to external	notes 12 and 13	-	55	-	dB
Video switch						
V_{18}	input voltage for internal video		-	-	0.8	V
V_{18}	input voltage for external video		2	-	V_P	V
I_{18}	maximum current	V_{18} = 0 V	-	0.05	0.2	mA
		V_{18} = 12 V	-	0.25	1	mA
AFC-circuit (note 14)						
I_{22}	AFC sample and hold switch-off current		0.1	-	-	mA
I_O	output current (pin 22)	V_{22} = 0 V	0.2	0.4	0.8	mA
I_{IL}	leakage current (pin 22)		-	-	1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{21}	AFC output voltage swing		10.5	-	11.5	V
I_{21}	available output current		±0.2	-	-	mA
	control slope		-	100	-	mV/kHz
V_O	output voltage (pin 21)	AFC off	5.5	6	6.5	V
R_O	AFC output resistance		-	40	-	kΩ
$V_{21(p-p)}$	output voltage swing	notes 11 and 15	-	11	-	V
	control slope	notes 11 and 15	-	80	-	mV/kHz
V_{21}	output voltage shift with respect to V_I = 10 mV(RMS)	notes 11 and 15	-	−2	-	V
Sync separator (see Fig.6)						
V_{28}	required sync pulse amplitude	note 16	200	750	-	mV
I_{28}	input current	V_{28} > 5 V	-	8	-	µA
		V_{28} = 0 V	-	−10	-	mA
First control loop						
Δf	PLL holding range		-	±1500	±2000	Hz
Δf	PLL catching range		±600	±1500	-	Hz
	control sensitivity to oscillator	note 17	see Fig.7			
Second control loop (positive edge)						
$\frac{\delta t_d}{\delta t_o}$	control sensitivity, see Fig.6	note 18	-	100	-	
t_d	control range		-	25	-	µs
Phase adjustment (via second control loop)						
	control sensitivity		-	25	-	µA/µs
α	maximum allowed phase shift		-	±2	-	µs
Horizontal oscillator						
	free running frequency	R = 34.3 kΩ; C = 2.7 nF	-	15750	-	Hz
Δf	spread with fixed external components		-	-	4	%
Δf	frequency variations with supply voltage from 9.5 to 13.2 V		-	-	2	%
Δf_T	frequency variation with temperature	note 11	-	−1.6	-	Hz/°C
Δf_{fr}	maximum frequency deviation at start of horizontal output		-	-	10	%
Δf	frequency variation when only noise is received	note 11	-	-	500	Hz
Horizontal output (pin 29; open collector)						
V_{29}	output limiting voltage		-	-	16.5	V
V_{OL}	output voltage LOW	I_{sink} = 10 mA	-	0.3	0.5	V
I_{sink}	maximum sink current		10	-	-	mA
	duty factor of output signal		-	46	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time output pulse		-	260	-	ns
t_f	fall time output pulse		-	100	-	ns
Flyback input and sandcastle output (note 19)						
I_{30}	required input current during flyback pulse		0.1	-	2	mA
V_{30}	output voltage during burstkey horizontal blanking vertical blanking		 8 4 2.1	 - 4.4 2.5	 - 5 2.9	 V V V
t_W	burstkey pulse width		2.9	3.3	3.7	µs
VERTICAL BLANKING						
	divider in search window		-	17	-	lines
	divider in narrow window		-	21	-	lines
t_d	delay between the start of the sync pulse at the video output and the burstkey pulse trailing edge rising edge		 - 4.7	 - 5.4	 9.4 6.1	 µs µs
VCR switch (non-VCR mode; V_{17} < 5 V)						
R_{17}	resistance to ground		-	-	5	kΩ
I_{17}	output current	pin 17 = 0 V	-	-	0.5	mA
VCR switch (auto-VCR mode)						
I_{source}	source current (pin 17)		-	-	30	µA
I_{sink}	sink current (pin 17)		-	-	30	µA
$V_{9-10(rms)}$	IF input signal for switching from fast to slow in auto VCR mode (RMS value)	pin 17 = n.c.	-	2.2	-	mV
VCR switch (VCR mode; V_{17} > 7 V)						
R_{17}	resistance to V_{CC}		-	-	5	kΩ
I_{17}	input current	$V_{17} = V_{CC}$	-	-	1	mA
Vertical ramp generator (note 20)						
I_3	input current during scan		-	-	2	µA
I_3	discharge current during retrace		-	0.8	-	mA
$V_{3(p-p)}$	sawtooth amplitude (peak-to-peak value)		-	1.9	-	V
t	interlace timing of the internal pulses	note 11	30	32	34	µs
Vertical output						
I_4	available output current	V_4 = 4 V	-	-	3	mA
V_4	maximum available output voltage	I_4 = 0.1 mA	4.4	5	-	V
Vertical feedback input						
V_5	DC input voltage		2.9	3.3	3.7	V
$V_{5(p-p)}$	AC input voltage (peak-to-peak value)		-	1	-	V
I_5	input current		-	-	12	µA
	internal pre-correction to sawtooth		-	3	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	temperature dependency of the amplitude	note 11 ΔT = 45 °C	-	-	2	%
Vertical guard						
ΔV_5	active switch level at a deviation with respect to the DC feedback level	note 21				
	guard level LOW		-	1.5	-	V
	guard level HIGH		-	2	-	V
Coincidence detector/transmitter identification (note 22)						
V_{25}	voltage for in-sync condition		-	9.8	-	V
V_{25}	voltage for no-sync condition	no signal	-	0.3	-	V
V_{25}	switching level to the phase detector from fast to slow		6.2	6.7	7.2	V
V_{25}	hysteresis slow to fast		-	0.6	-	V
V_{25}	switching level to activate the mute function (transmitter identification)		2.5	2.8	3.1	V
V_{25}	hysteresis mute function		-	2	-	V
Video transmitter identification output (open collector)						
V_{14}	output voltage active	no sync; I = 1 mA	-	0.3	0.5	V
I_{14}	sink current active		-	-	5	mA
I_{14}	output current inactive (transmitter present)		-	-	1	µA

Notes to the characteristics

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_{cc}) is obtained from the horizontal output stage. The load current of the driver must be added to the value given.
2. On set AGC.
3. The input impedance has been chosen such that a SAW filter can be employed.
4. Measured with 0 dB = 450 µV.
5. Measured at 10 mV RMS 100% input signal.
6. Projected zero point; i.e. with switched demodulator.
7. Measured according to the test line given in Fig.3. The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level. The differential phase is defined as the difference in degrees between the largest and smallest phase angle. The differential gain and phase are measured with a DSB signal.
8. This figure is valid for the complete video signal amplitude (peak white to black). The non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step.
9. The test set-up and input conditions are given in Fig.5. The figures are measured at an input signal of 10 mV RMS.
10. Measured with a source impedance of 75 Ω.

$$\textit{The signal-to-noise ratio} = 20 \log \frac{V_O \ \textit{black-to-white}}{V_{n(rms)} \ \textit{at} \ B = 5 \ \textit{MHz}}$$

11. These figures are based on test samples.
12. When the video switch is in the external mode the first control loop in the synchronization circuit is not switched to a long time constant when weak signals are received.
13. Defined as $20 \log \frac{V_O \text{ unwanted video black-to-white}}{V_O \text{ wanted video-black-to-white}}$; measured at 4.4 MHz.
14. The indicated figures are measured at an input signal of 10 mV RMS. The unloaded Q-factor of the reference tuned circuit is 70. With very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has a asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect a notch filter can be built into the demodulator tuned circuit. The characteristics given for weak signals are measured without a notch circuit, with a SAW filter connected in front of the IC input signal such that the input signal of the IC is 150 μV (RMS value).
15. Measured at an input signal amplitude of 150 μV(RMS) (pin 21).
16. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
17. Frequency control is obtained by supplying a correction current to the oscillator RC network via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by short circuiting the sync separator bias network (pin 28) to $+V_p$. To avoid the need of a VCR switch the time constant of the phase detector at strong input signals is sufficiently short to get a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that the head-errors of the VCR are compensated at the beginning of scan. During conditions of weak signal (information derived from the AGC circuit) the time constant is increased to obtain a better noise immunity.
18. This figure is valid for an external load impedance of 82 kΩ from pin 31 to the phase adjustment potentiometer (of H-shift).
19. The flyback input and sandcastle output have been combined on one pin. The flyback pulse is clamped to a level of 4.5 V. The minimum current to drive the second control loop is 0.1 mA.
20. The vertical scan is synchronized by means of a divider system. Therefore no frequency adjustment is required for the V-ramp generator.
21. To avoid screen burn due to a collapse of the vertical deflection a continuous blanking level (V_{30} = 2.5 V) is inserted in the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
22. The functions in-sync/out-of-sync and transmitter identification have been combined on this pin. The capacitor is charged during the sync pulse and discharged during the time difference between gating (6.5 μs) and the sync pulse in the internal video mode. When the circuit is in the external mode the capacitor is charged by the horizontal sync pulse and discharged continuously with a small current.

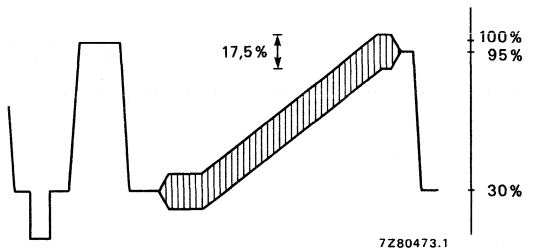


Fig.2 Video output signal.

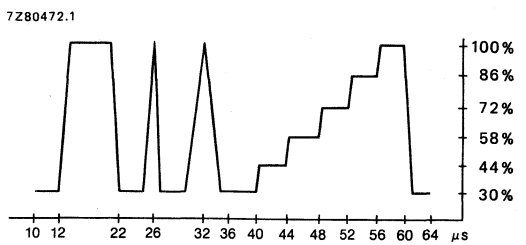
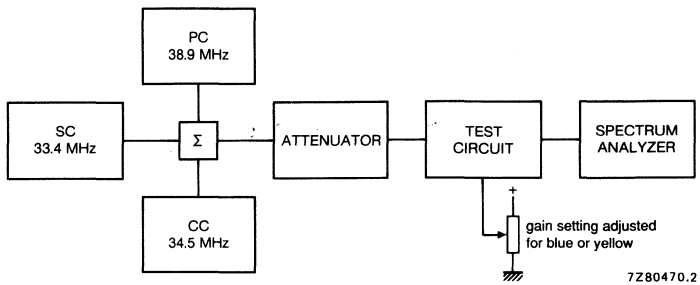
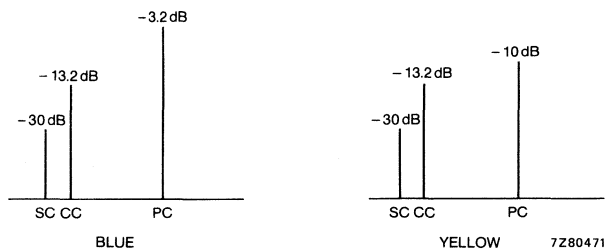


Fig.3 EBU test signal waveform (line 17).





Input signal conditions

SC = Sound carrier

CC = Chrominance carrier

PC = Picture carrier

All with respect to peak sync level

$$\textit{Value at } 1.1\textit{MHz}: 20 \log \frac{V_O \textit{ at } 4.4\textit{MHz}}{V_O \textit{ at } 1.1\textit{MHz}} + 3.6\textit{dB}$$

$$\textit{Value at } 3.3\textit{MHz}: 20 \log \frac{V_O \textit{ at } 4.4\textit{MHz}}{V_O \textit{ at } 3.3\textit{MHz}}$$

Fig.4 Test set-up intermodulation.

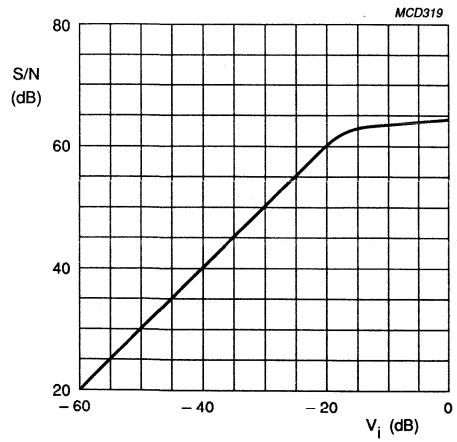
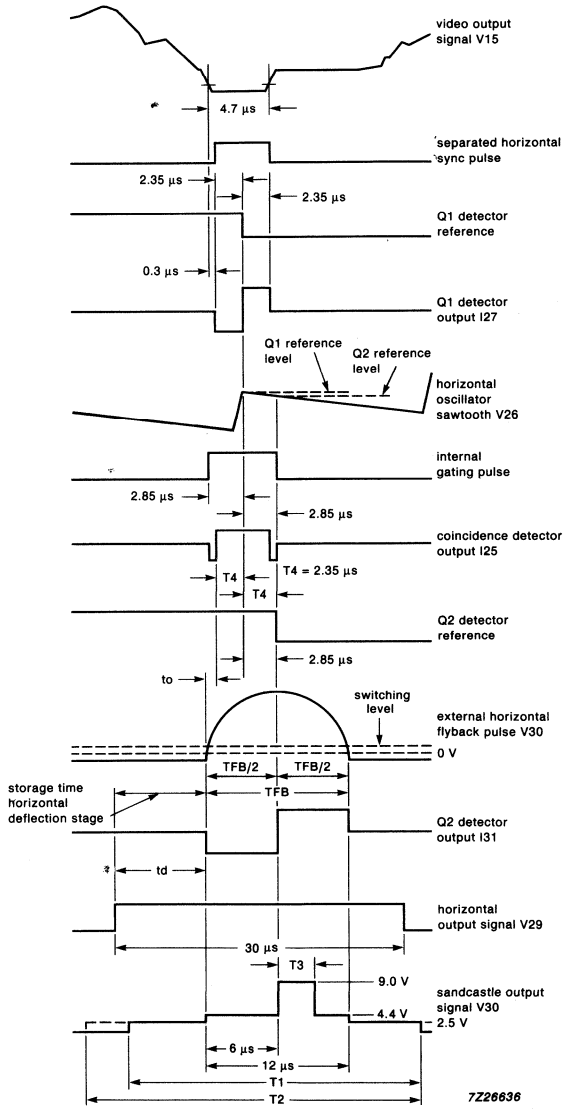


Fig.5 Signal-to noise ratio as a function of the input voltage (0 dB = 100 mV).



T1: divider in search window: 34p; $p = 1/2f_H$

T2: divider in narrow window: 42p

T3: 3.3 µs

Fig.6 Timing diagram.

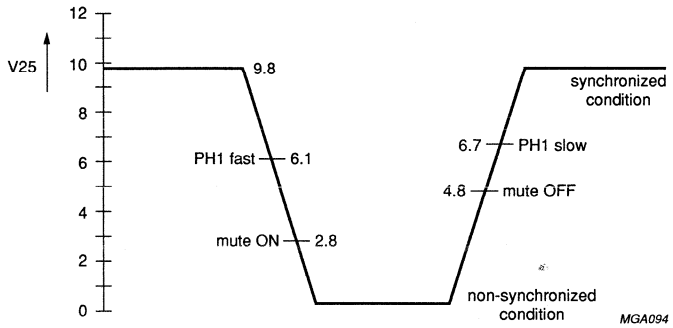


Fig.7 Switching levels coincidence detector.

Table 4

CONDITION PIN 18 VIDEO SWITCH	CONDITION PIN 17 VCR SWITCH	CONDITION V_{25}	CONTROL SENSITIVITY HOR.OSCILLATOR kHz / µs	
			T2 - T1	T3 = SCAN
Low internal video	floating automatic VCR	V_{25} > 6.7 V and strong signal	11.3	7.6
		V_{25} > 6.7 V and weak signal	1.3	1.3
		V_{25} < 6.1 V and strong signal	11.3	7.6
		V_{25} < 6.1 V and weak signal	11.3	7.6
	HIGH forced VCR	don't care	11.3	7.6
	LOW T.V. mode	V_{25} > 6.7 V	1.3	1.3
		V_{25} < 6.1 V	11.3	7.6
HIGH or floating external video	don't care	don't care	11.3	7.6

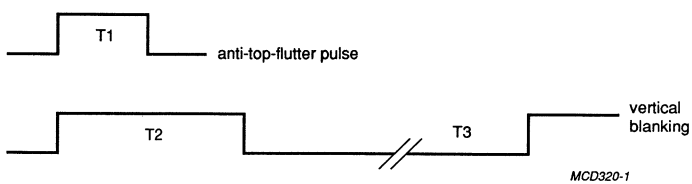


Fig.8 Anti-top-flutter pulse.

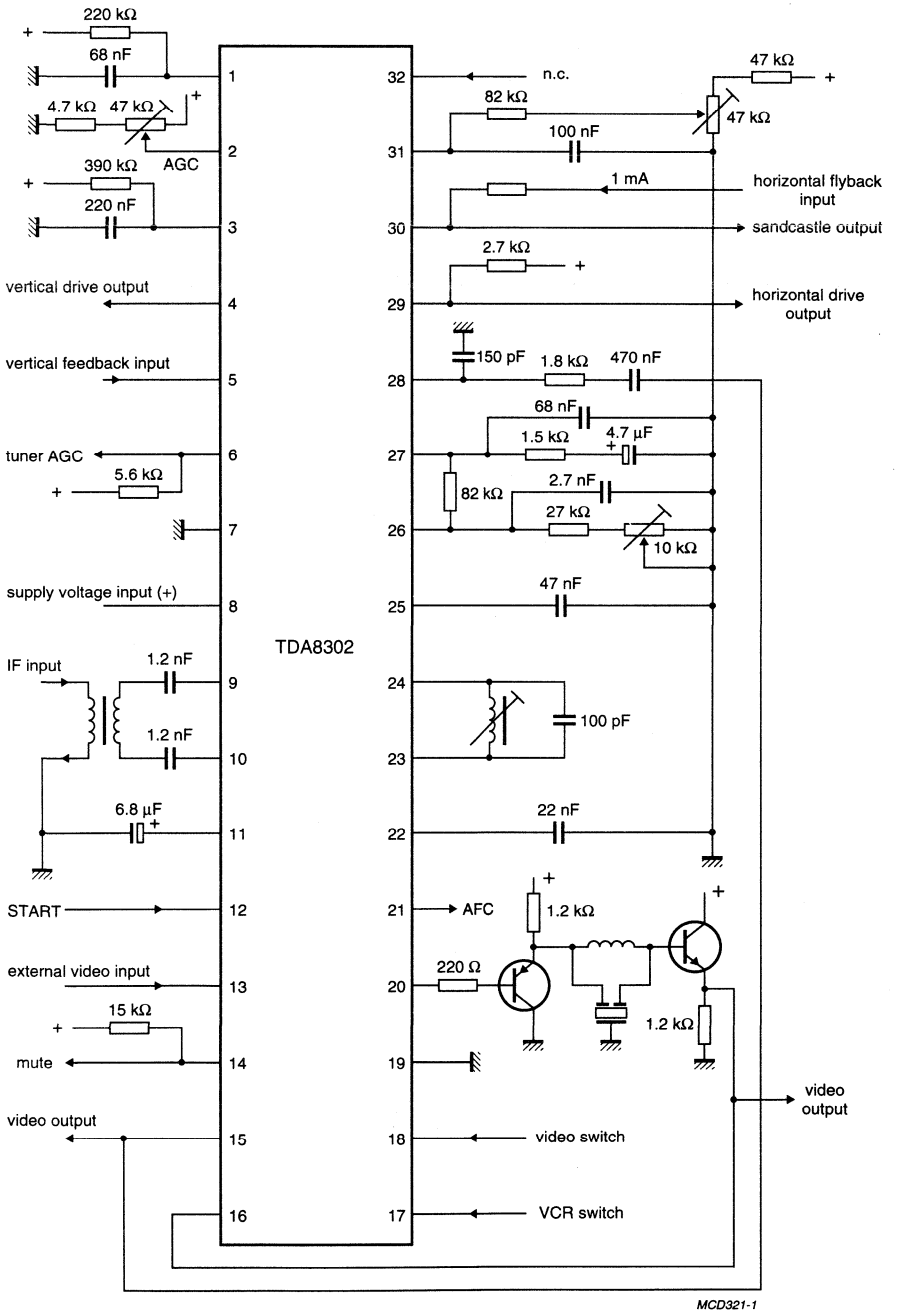


Fig.9 Application diagram.

Small signal combination IC for black/white TV

TDA8303
TDA8303A

FEATURES

- Video IF amplifier with synchronous demodulator
- Automatic gain control (AGC) detector suitable for negative modulation
- AGC tuner
- Automatic frequency control (AFC) circuit with sample-and-hold
- Video preamplifier
- Sound IF amplifier and demodulator
- DC volume control or separate supply for starting the horizontal oscillator
- Audio preamplifier
- Horizontal synchronization circuit with two control loops
- Vertical synchronization (divider system) and sawtooth generation with automatic amplitude adjustment for 50 and 60 Hz
- Transmitter identification (mute)

GENERAL DESCRIPTION

The TDA8303/TDA8303A combines all small signal functions (except the tuner) which are required for a monochrome television receiver. For a complete black and white receiver only the output stages for video, sound, horizontal and vertical deflection and a tuner have to be added.
The TDA8303 is for applications with npn tuners and the TDA8303A for pnp tuners.

FUNCTIONAL DESCRIPTION

Video IF amplifier, demodulator and video amplifier

Each of the three AC-coupled IF stages permits the omission of DC feedback and possesses a control range in excess of 20 dB. An additional advantage is the symmetry of the amplifier which results in a less critical application.

The IF amplifier is followed by a passive synchronous demodulator providing a regenerated carrier signal. This is limited by a logarithmic limiter circuit prior to its application to the demodulator. The limiter has a very low differential phase shift which results in good differential gain and phase figures.

The video amplifier also contains a white spot inverter and a noise clamp which limits interference pulses to a point below the peak sync level. This circuit is more effective than a noise inverter and results in an improved picture stability, with respect to interference.

AFC-circuit

The reference signal for the AFC circuit is obtained from the demodulator tuned circuit. In this way only one tuned circuit needs to be applied and only one adjustment has to be carried out. The disadvantage with this method is that the frequency spectrum of the signal fed to the detector is determined by the SAW filter characteristic. This spectrum is asymmetrical with respect to the picture carrier so that the AFC output voltage is dependent on the video signal.

To overcome this video frequency dependency of the AFC output, the demodulator output is followed by a sample-and-hold circuit which samples during the sync level of the signal. This means that only the carrier signal is available to the AFC and it will not be affected by the video information.

At very weak input signals the drive signal of the AFC circuit will contain substantial noise. This noise has an asymmetrical frequency spectrum causing an offset in the AFC output voltage. This effect can be minimized by applying a notch in the demodulator tuned circuit. The sample-and-hold circuit is followed by an amplifier with high output impedance, therefore the steepness of the of the AFC control voltage is dependent on the load impedance.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8303	28	DIL	plastic	SOT117
TDA8303A	28	DIL	plastic	SOT117

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage (pin 7)		9.5	12	13.2	V
I_P	supply current (pin 7)		90	125	160	mA
I_{start}	start current (pin 11)	note 1	–	6.5	9	mA
Video						
$V_{8\text{-}9(RMS)}$	IF sensitivity (RMS value)	at 38.9 MHz; note 2	20	40	65	μV
$G_{8\text{-}9}$	IF gain control range		–	74	–	dB
S/N	signal-to-noise ratio	input signal = 10 mV	–	57	–	dB
$V_{18(p\text{-}p)}$	AFC output voltage swing (peak-to-peak value)		10.5	–	11.5	V
Sound						
$V_{12(RMS)}$	AF output signal (RMS value)	note 3	400	600	800	mV
AMS	AM suppression	at V_i = 50 mV	–	58	–	dB
THD	total harmonic distortion		–	0.5	–	%
Sync						
V_{25}	required sync pulse amplitude	note 4	200	–	–	mV
I_{27}	required input current during flyback pulse		0.1	–	2	mA
V_{22}	coincidence detector output voltage					
	in synchronized condition		–	9.7	–	V
	in no signal condition		–	1.5	–	V
V_{22}	vertical feedback for DC voltage		2.9	3.3	3.7	V
$V_{22(p\text{-}p)}$	vertical feedback for AC voltage (peak-to-peak value)		–	1.2	–	V

Notes to the quick reference data

1. Pin 11 has a double function. When during switch-on a current of 9 mA is supplied to this pin, it is used to start the horizontal oscillator. The main supply can then be obtained from the horizontal deflection stage. When no current is supplied to this pin it can be used as a volume control.
2. On set AGC.
3. The output signal is measured at Δf = 7.5 kHz and maximum volume control.
4. The minimum value is obtained by connecting a 1.8 kΩ resistor and a 470 nF capacitor in series between the video output and pin 25. The slicing level can be varied by changing the value of this resistor (higher resistance value results in a larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.

Small signal combination IC for black/white TV

TDA8303
TDA8303A

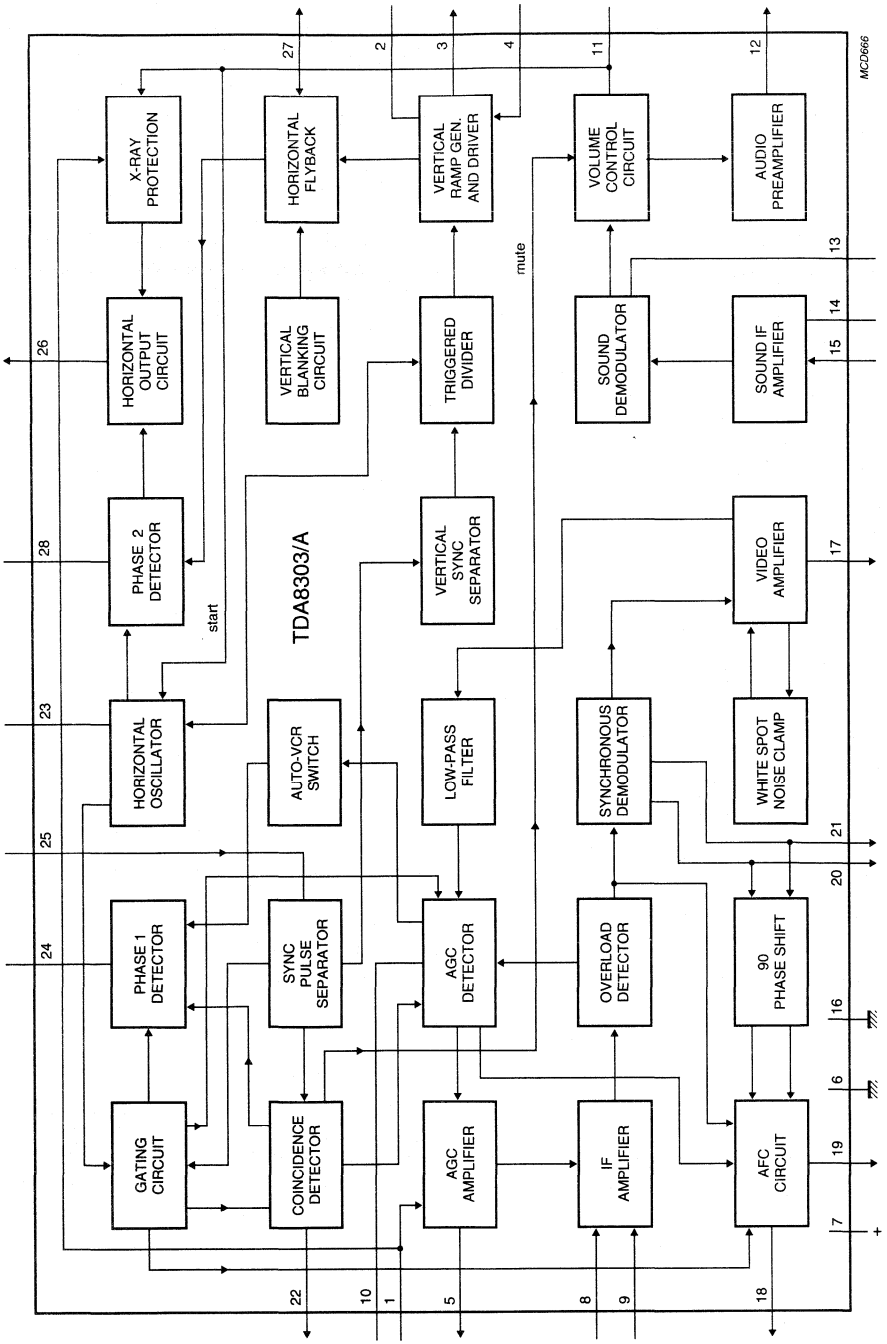


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	AGC take-over
2	vertical ramp generator
3	vertical drive
4	vertical feedback
5	tuner AGC
6	ground
7	supply voltage input
8	video IF input
9	video IF input
10	IF AGC
11	volume control/start horizontal oscillator
12	audio output
13	sound demodulator
14	sound IF decoupling
15	sound IF input
16	ground (for some critical parts)
17	video amplifier output
18	AFC output
19	AFC S/H, AFC switch
20	video demodulator tuned circuit
21	video demodulator tuned circuit
22	coincidence detector
23	horizontal oscillator
24	phase 1 detector
25	sync separator input
26	horizontal drive output
27	horizontal flyback input
28	phase 2 detector

AGC circuit

The AGC circuit of the TDA8303/TDA8303A is a top-sync detector. The video signal coming from the video amplifier passes a 2nd order low-pass filter before it is compared with an internal reference level. The comparator stage is gated when the horizontal oscillator is synchronized with the video signal, such that interference pulses outside the gating time have no influence on the gain control.

Sound circuit

The sound quality of the TDA8303/TDA8303A compared with the predecessors has been improved at weak signal conditions. The improvement has been achieved by the new IF amplifier which is less sensitive for radiation from the sound IF amplifier and by change of the ground and supply connections in the IC. When out-of-sync condition is detected by the coincidence detector the sound output is muted. When no mute is required the minimum voltage level on pin 22 should be clamped to a high level of 5 V. At this level the gating of the AGC is switched off and the phase 1 detector has a high output current for reliable catching of a new transmitter.

Vertical synchronization

The TDA8303/TDA8303A embodies a synchronized divider system for generating the vertical sawtooth at pin 2 having several advantages and features such as:

- The vertical frequency is alignment free. The divider automatically adapts to a vertical frequency of 50 Hz or 60 Hz including automatic amplitude correction and its operating modes offer maximum interference/disturbance protection.
- A discriminator-window checks the accuracy of the vertical trigger pulse. Internally clock pulses are generated by doubling the line frequency. The divider operates in the 60 Hz mode when the trigger pulse appears before count 576, otherwise the 50 Hz mode will be active.
- The divider system operates with two different reset windows for maximum interference/disturbance protection. The windows are activated via an up/down counter. The counter increases its counter-value by 1 for each time the separated vertical sync pulse appears within the selected window, otherwise the counter value is decreased by 1.

Modes of operation

Large search window: divider ratio between 488 and 576.

This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found does not comply with the narrow window specification limits
- Up/down counter value of the divider system, operating in the narrow window mode, drops below count 10

Narrow window mode: divider ratio between 522 and 528 (60 Hz); or 622 and 628 (50 Hz).

- The divider system switches over to narrow window mode when the up/down counter has reached his maximum value of 15 approved vertical sync pulses
- When the divider operates in the narrow window mode and a vertical sync pulse is missing within the window, the divider is reset at the end of that window and the counter value is decreased by 1
- At a counter value below 10 the divider system switches over to the large window mode
- The divider system also generates an anti-top-flutter pulse which inhibits the phase 1 detector during the vertical sync pulse. The pulse width is dependent on the divider mode. For the large window mode the start is generated at the reset of the divider. In the narrow window mode the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 10 for the 50 Hz mode and count 12 for the 60 Hz mode

VCR switch

An extra time constant switch in the horizontal phase detector makes an external VCR switch redundant. The time constant is automatically switched depending on the signal strength of the IF input (pins 8/9) and the coincidence detector.
When a strong signal is detected ($V_{8/9}$ > 2.2 mV) and the circuit is synchronized the time constant of the phase detector is optimum for VCR playback, a fast time constant during the vertical retrace to correct head errors of the VCR and during scan a sufficient time constant to correct fluctuations of the horizontal sync
During weak signal and synchronized conditions the time constant is enlarged and the phase detector is gated. This ensures a stable display which is not disturbed by the noise in the video signal. When the circuit is not synchronized the time constant is fast and not gated to ensure a short catching time.

Combination of DC volume control and start-up feature

Pin 11 of the IC can be used as a DC volume control or as a start-up feature of the horizontal oscillator/output circuit dependent on the application.
Volume control is achieved by connecting a 4.7 kΩ potentiometer or a DC voltage of 0 to 3 V to pin 11.
When a current of 9 mA is supplied to pin 11 the volume control is set to a fixed output signal level and the circuit will generate drive pulses for the horizontal deflection and the main supply can be derived from the deflction.

Application when external video signals require synchronization

The input to the sync separator is externally available via pin 25. For normal application the video output signal at pin 17 is AC-coupled to the sync separator input. It is possible to interrupt this connection and drive the sync separator from other sources.
When external signals are applied to the sync separator the connections between the two parts must be interrupted. This can be achieved by connecting pin 22 to ground, which results in the following conditions:

- AGC detector is not gated
- Mute circuit not active, sound channel remains switched on
- Phase detector 1 has an optimum time constant for external video sources and is not gated

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 7)	–	13.2	V
P_{tot}	total power dissipation	–	2.3	W
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−25	+65	°C

CHARACTERISTICS

V_P = 12 V;T_{amb} = 25 °C; carrier 38.9 MHz negative modulation, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 7)						
V_P	supply voltage range		9.5	12	13.2	V
I_P	supply current	no input	90	125	160	mA
I_{11}	start current (pin 11)	note 1	–	6.5	9	mA
V_{11}	start voltage horizontal oscillator		9.5	–	–	V
V_{11}	start protection level	I_{11} = 12 mA	–	–	16.5	V
IF Amplifier (pins 8 and 9)						
$V_{8\text{-}9(RMS)}$	input sensitivity (RMS value)	at 38.9 MHz; note 2	25	40	65	µV
$V_{8\text{-}9(RMS)}$	input sensitivity (RMS value)	at 45.75 MHz; notes 2 and 25	25	40	65	µV
$R_{8\text{-}9}$	differential input resistance	note 3	–	1300	–	Ω
$C_{8\text{-}9}$	differential input capacitance	note 3	–	5	–	pF
$G_{8\text{-}9}$	gain control range		–	74	–	dB
ΔV_{17}	output signal expansion for 46 dB input signal variation	note 4	–	1	–	dB
$V_{8\text{-}9}$	maximum input signal		100	170	–	mV
Video Amplifier (note 5)						
V_{17}	zero signal output level	note 6	–	5.4	–	V
V_{17}	peak sync level		2.3	2.5	2.7	V
V_{17}	video output signal amplitude	note 7	2.3	2.65	3.0	V
V_{17}	white spot threshold level		–	5.7	–	V
V_{17}	white spot insertion level		–	3.8	–	V
Z_{17}	video output impedance		–	25	–	Ω
I_{17}	internal bias current of npn emitter follower output transistor		1.4	1.8	–	mA
I_{source}	maximum source current (pin 17)		10	–	–	mA
B	bandwidth of demodulated output signal		5	7	–	MHz
G_{17}	differential gain	note 8	–	4	8	%
φ	differential phase	note 8	–	2	5	deg.
NL	video non linearity	note 9	–	2	5	%
	intermodulation	note 10				
	1.1 MHz; blue		50	60	–	dB
	1.1 MHz; yellow		50	60	–	dB
	3.3 MHz; blue		55	65	–	dB
	3.3 MHz; yellow		55	65	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio	10 mV input signal	50	57	–	dB
S/N	signal-to-noise ratio	end of gain control range	50	62	–	dB
V_{17}	residual carrier signal		–	2	10	mV
V_{17}	residual 2nd harmonic of carrier signal		–	2	10	mV
Tuner AGC						
$V_{8\text{-}9(RMS)}$	minimum starting point for tuner take–over (RMS value)		–	–	0.2	mV
$V_{8\text{-}9(RMS)}$	maximum starting point for tuner take–over (RMS value)		100	150	–	mV
I_5	maximum tuner AGC output swing	V_5 = 3 V	4	–	–	mA
V_5	output saturation voltage	I_5 = 2 mA	–	–	300	mV
I_L	leakage current (pin 5)		–	–	1	µA
ΔV_I	input signal variation complete tuner control		0.2	2	4	dB
V_1	minimum voltage tuner take–over		–	–	1	V
AFC circuit						
I_{19}	AFC sample-and-hold switch-off current		0.1	–	–	mA
I_O	output current (pin 19)	V_{19} = 0 V	–	0.1	0.3	mA
I_{LO}	output leakage current (pin 19)		–	–	2	µA
V_{18}	AFC output voltage swing	notes 18 and 19	10.5	–	11.5	V
I_{18}	available output current		0.2	–	–	mA
	control slope		–	100	–	mV/kHz
V_O	output voltage (pin 18)	AFC off	5.5	6	6.5	V
R_O	AFC output resistance		–	40	–	kΩ
V_{18}	output voltage swing	notes 25 and 26	–	11	–	V
	control slope	notes 25 and 26	–	80	–	mV/kHz
V_{18}	output voltage shift with respect to V_I = 10 mV(RMS)	notes 25 and 26	–	–2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sound circuit (note 12)						
V_{15}	input limiting voltage	$V_{O(max)}$ = –3 dB	–	400	800	µV
R_{15}	input resistance		–	2.6	–	kΩ
C_{15}	input capacitance		–	6	–	pF
AMS	AM suppression	note 13	53	58	–	dB
$V_{12(RMS)}$	AF output signal (RMS value)	note 14	400	600	800	mV
$V_{12(RMS)}$	AF output signal when pin 11 is used as a starting pin or connected to V_P (RMS value)	Δf = 50 kHz	500	900	1500	mV
Z_{12}	AF output impedance		–	25	100	Ω
THD	total harmonic distortion	note 15	–	0.5	2	%
RR	ripple rejection	volume control –20 dB; f_k = 100 Hz	–	35	–	dB
V_{12}	output voltage when muted		–	2.5	–	V
V_{12}	output level shift due to muting	volume control –20 dB	–	–	0.5	dB
S/N	signal-to-noise ratio	note 16	–	47	–	dB
V_{11}	voltage with pin 11 disconnected		–	6	–	V
I_{11}	current with pin 11 short-circuited to ground		–	1	–	mA
V_{12}	temperature dependance of the output signal amplitude	T_{amb} = 20 to 65 °C; –30 dB volume control and voltage of pin 11 fixed; note 27	–	2.5	–	dB
Volume control (note 17; see Fig.8)						
R_{11}	external control resistor	note 17	–	4.7	–	kΩ
OSS	suppression of output signal during mute condition		60	66	–	dB
Horizontal synchronization circuit (see Fig.9)						
SYNC SEPARATOR						
V_{25}	required sync pulse amplitude	note 20	200	750	–	mV
I_{25}	input current (pin 25)	V_{25} > 5 V	–	8	–	µA
		V_{25} = 0 V	–	10	–	mA
FIRST CONTROL LOOP						
±Δf	PLL holding range		–	1500	2000	Hz
±Δf	PLL catching range		600	1500	–	Hz
	control sensitivity to oscillator	note 21	see Fig.10			

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{8-9}	IF input signal at which the time constant is switched (RMS value)	strong-to-weak	–	2.2	–	mV
SECOND CONTROL LOOP (POSITIVE EDGE)						
$\frac{\delta t_d}{\delta t_o}$	control sensitivity	note 22	–	100	–	
t_d	control range		–	25	–	µs
PHASE ADJUSTMENT (VIA SECOND CONTROL LOOP)						
	control sensitivity		–	25	–	µA/µs
α	maximum allowed phase shift		–	±2	–	µs
HORIZONTAL OSCILLATOR						
f_{fr}	free running frequency	R = 34.3 kΩ; C = 2.7 nF	–	15625	–	Hz
Δf	spread with fixed external components		–	–	4	%
Δf_{fr}	frequency variations with supply voltage from 9.5 to 13.2 V		–	–	2	%
Δf_T	frequency variation with temperature	note 25	–	–1.6	–	Hz/°C
Δf_{fr}	maximum frequency deviation at start of horizontal output		–	–	10	%
Δf	frequency variation when only noise is received	note 25	–	–	500	Hz
HORIZONTAL OUTPUT (PIN 26; OPEN COLLECTOR)						
V_{26}	output limiting voltage		–	–	16.5	V
V_{OL}	LOW level output voltage	I_{sink} = 10 mA	–	0.2	0.5	V
I_{sink}	maximum sink current		10	–	–	mA
	duty factor of output signal		–	46	–	%
t_r	rise time of output pulse		–	260	–	ns
t_f	fall time of output pulse		–	100	–	ns
HORIZONTAL FLYBACK INPUT (PIN 27)						
I_{27}	required input current during flyback pulse		0.01	–	1.0	mA
COINCIDENCE DETECTOR						
V_{22}	voltage for in-sync condition		–	9.8	–	V
V_{22}	voltage for no-sync condition	no signal	–	1.5	–	V
V_{22}	switching level to the phase detector from fast to slow		6.2	6.7	7.2	V
V_{22}	hysteresis slow to fast		–	0.6	–	V
V_{22}	switching level to activate the mute function (transmitter identification)		2.5	2.8	3.1	V
V_{22}	hysteresis mute function		–	2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_d	delay of mute release after transmitter insertion		–	–	300	µs
	allowable load on pin 22		–	–	10	µA
V_{22}	external video mode		–	–	0.7	V
I_{22}	current at pin 22	V_{22} = 0 V	–	–	0.8	mA
Vertical circuit (note 24)						
VERTICAL RAMP GENERATOR						
I_2	input current during scan		–	–	2	µA
I_2	discharge current during retrace		–	0.8	–	mA
$V_{2(p-p)}$	sawtooth amplitude (peak-to-peak value)		–	1.9	–	V
t	interlace timing of the internal pulses		30	32	34	µs
VERTICAL OUTPUT						
I_3	available output current	V_3 = 4 V	–	–	3	mA
V_3	maximum available output voltage	I_3 = 0.1 mA	4.4	5	–	V
VERTICAL FEEDBACK INPUT						
V_4	DC input voltage		2.9	3.3	3.7	V
$V_{4(p-p)}$	AC input voltage (peak-to-peak value)		–	1	–	V
I_4	input current		–	–	12	µA
Δt_p	internal pre-correction to sawtooth		–	3	–	%
	deviation amplitude	50/60 Hz	–	–	4	%
	temperature dependency of the amplitude	T_{amb} = 20 to 65 °C	–	–	2	%

Notes to the characteristics

1. Pin 11 has a double function. When during switch-on a current of 9 mA is supplied to this pin, it is used to start the horizontal oscillator. The main supply can then be obtained from the horizontal deflection stage. When no current is supplied to this pin it can be used as a volume control.
2. On set AGC.
3. The input impedance has been chosen such that a SAW filter can be employed.
4. Measured with 0 dB = 450 µV.
5. Measured at 10 mV RMS top sync input signal.
6. Projected zero point; i.e. with switched demodulator.
7. White 10% of the top sync amplitude.
8. Measured according to the test line illustrated by Fig.2. The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level. The differential phase is defined as the difference in degrees between the largest and smallest phase angle. The differential gain and phase are measured with a DSB signal.
9. This figure is valid for the complete video signal amplitude (peak white-to-black); see Fig.3. The non–linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step.

10. The test set-up and input conditions are illustrated by Fig.4. The figures are measured at an input signal of 10 mV RMS.
11. Measured with a source impedance of 75 Ω.

$$\textit{The signal-to-noise ratio} = 20 \log \frac{V_o \textit{ black-to-white}}{V_{n(RMS)} \textit{ at } B = 5 \textit{ MHz}}$$

12. The sound circuit is measured (unless otherwise specified) with an input signal of V_{15} of 50 mV RMS, a carrier frequency of 5.5 MHz at a Δf of 27.5 kHz. The QL of the demodulator tuned circuit is 16 and the volume control is connected to the supply. The reference circuit must be tuned in such a way tha the output is symmetrical clipping at maximum volume.
13. The test set-up is illustrated by Fig.6. The AM rejection curve (typical) is illustrated by Fig.7.
14. The output signal is measured at a Δf = 7.5 kHz and maximum volume control.
15. The demodulator tuned circuit must be tuned at minimum distortion.
16. Weighted noise, measured in accordance with CCIR 468.
17. See also note 1. The volume can be controlled by using a potentiometer connected to ground (value 4.7 kΩ) or by means of a variable direct voltage. In the latter event the relatively low input impedance must be taken into account.
18. The AFC control voltage is obtained by multiplying the IF output signal (which is also used to drive the synchronous demodulator) with a reference carrier. This reference carrier is obtained from the demodulator tuned circuit via a 90 degree phase shift network.The IF output signal has an asymmetrical frequency spectrum with respect to the carrier frequency. To avoid problems due to this asymmetrical signal the AFC circuit is followed by a sample-and-hold circuit which samples during the sync level. As a result the AFC output voltage contains no video information. The specified control slope decreases when the AFC oputput is loaded with two resistors between the voltage supply and ground.
19. At very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has an asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. The characteristics given for weak signals are measured with a SAW filter (OFW 1956) connected in front of the IC input signal such that the input signal of the IC is 150 μV RMS.
20. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 17 and 25. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
21. Frequency control is obtained by supplying a correction current to the oscillator RC network via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by short circuiting the sync separator bias network (pin 25) to the voltage supply. To avoid the need of a VCR switch the time constant of the phase detector at strong input signals is sufficiently short to obtain a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that the head-errors of the VCR are compensated at the beginning of scan. During conditions of weak signal (information derived from the AGC circuit) the time constant is increased to obtain a better noise immunity.
22. This figure is valid for an external load impedance of 82 kΩ between pin 28 and the phase adjustment potentiometer.
23. The functions in-sync/out-of-sync and transmitter identification have been combined on pin 22. The capacitor is charged during the sync pulse and discharged during the time difference between gating (6.5 μs) and the sync pulse.
24. The vertical scan is synchronized by means of a divider system. Therefore no frequency adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and corrects the vertical amplitude.
25. These figures are based on test samples.
26. Measured at an input signal amplitude of 150 μV RMS (pin 18).

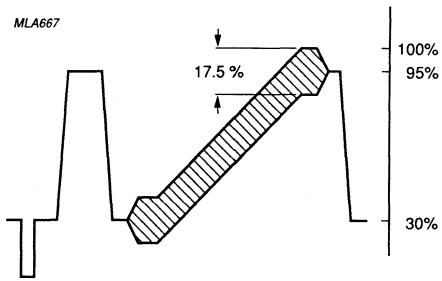


Fig.2 Video output signal.

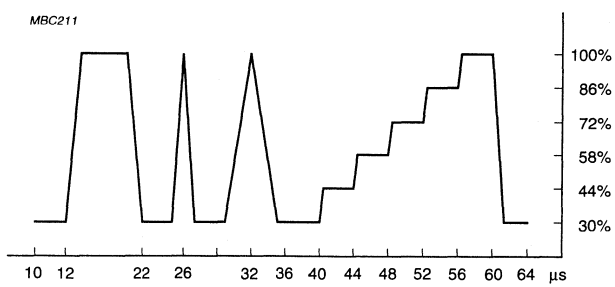
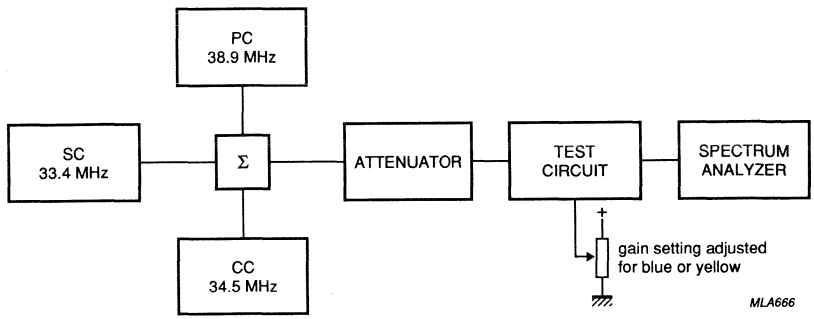
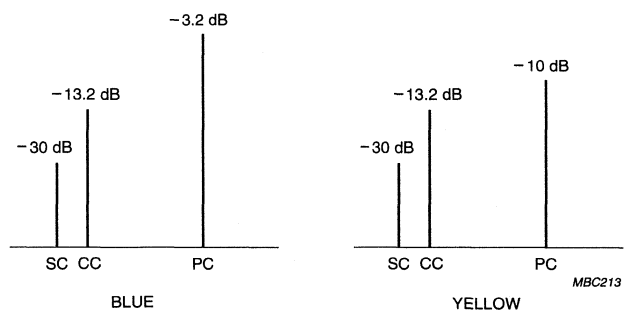


Fig.3 EBU test signal waveform (line 330).





Input signal conditions

SC = Sound carrier

CC = Chrominance carrier

PC = Picture carrier

All with respect to top sync level

$$Value\ at\ 1.1MHz : 20 \log \frac{V_o\ at\ 4.4MHz}{V_o\ at\ 1.1MHz} + 3.6dB$$

$$Value\ at\ 3.3MHz : 20 \log \frac{V_o\ at\ 4.4MHz}{V_o\ at\ 3.3MHz}$$

Fig.4 Test set–up intermodulation.

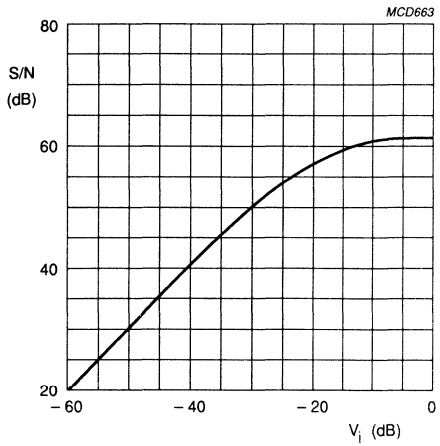


Fig.5 Signal-to-noise ratio as a function of the input voltage (0 dB = 100 mV).

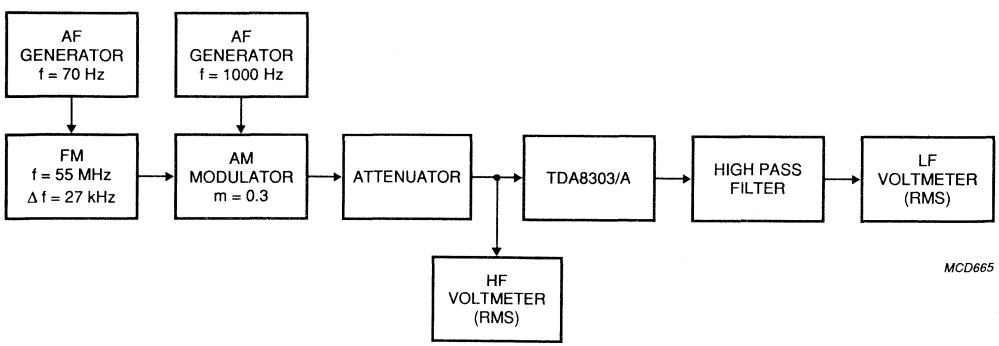


Fig.6 Test set-up AM suppression.

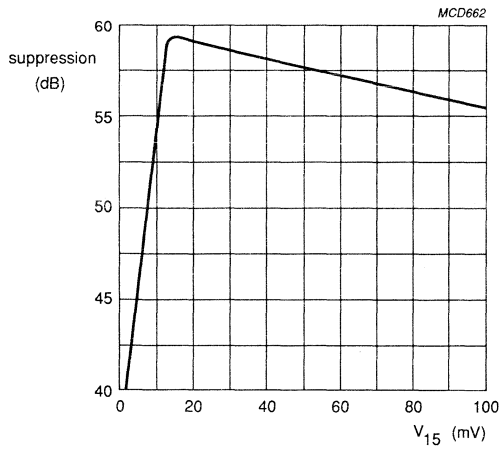


Fig.7 AM suppression.

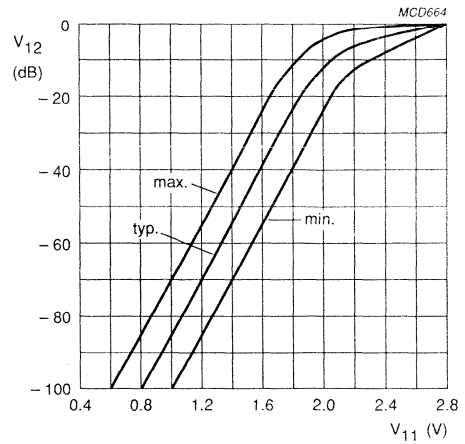


Fig.8 Volume control characteristics.

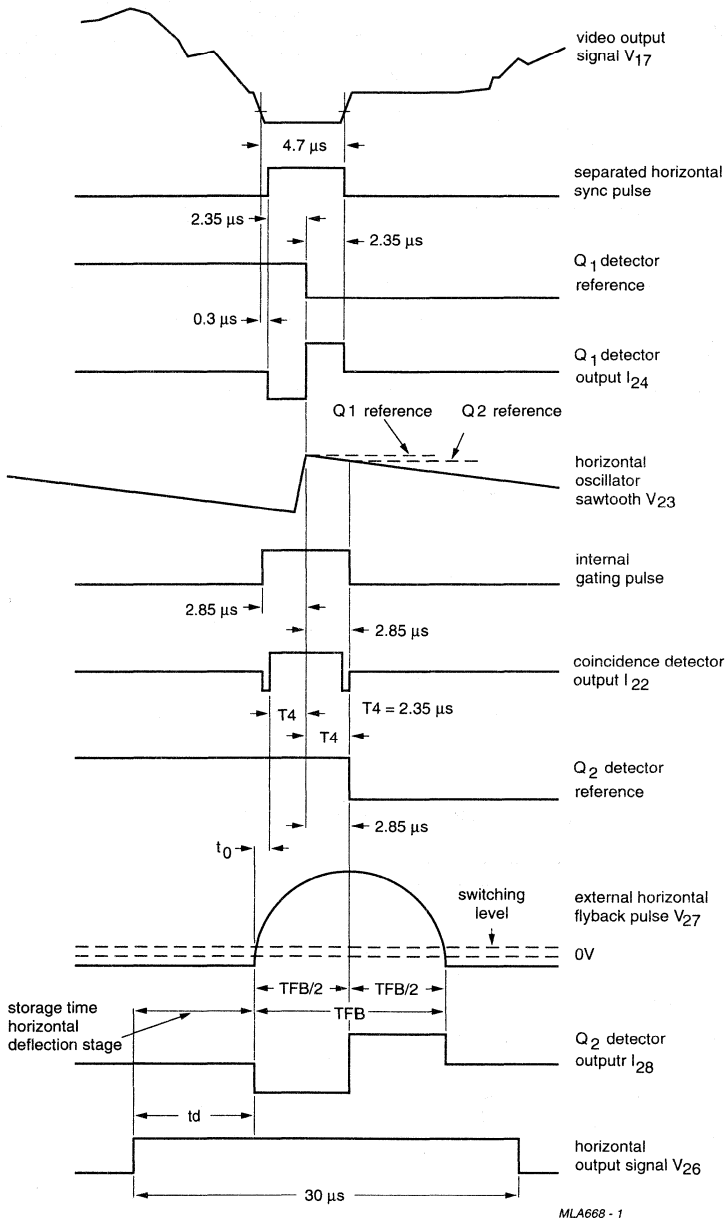


Fig.9 Timing diagram.

Table 1 Switching levels coincidence detector

CONDITION V_{22}	CONTROL SENSITIVITY HORIZONTAL OSCILLATOR (kHz/µs)	
	T2 – T1	T3 = SCAN
$V_{22} > 6.7$ V and strong signal weak signal	 11.3 1.3	 7.6 1.3
$1 < V_{22} < 5.7$ V and strong signal weak signal	 11.3 11.3	 7.6 7.6
$V_{22} < 0.7$	11.3	7.6

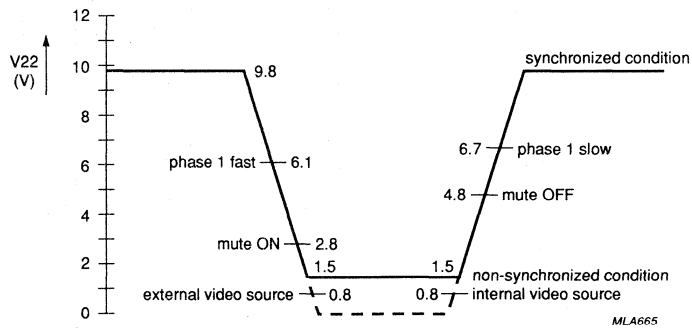


Fig.10 Switching levels coincidence detector.

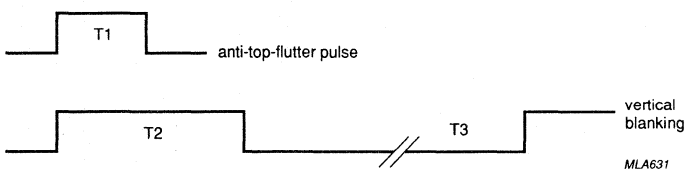


Fig.11 Anti-top-flutter pulse.

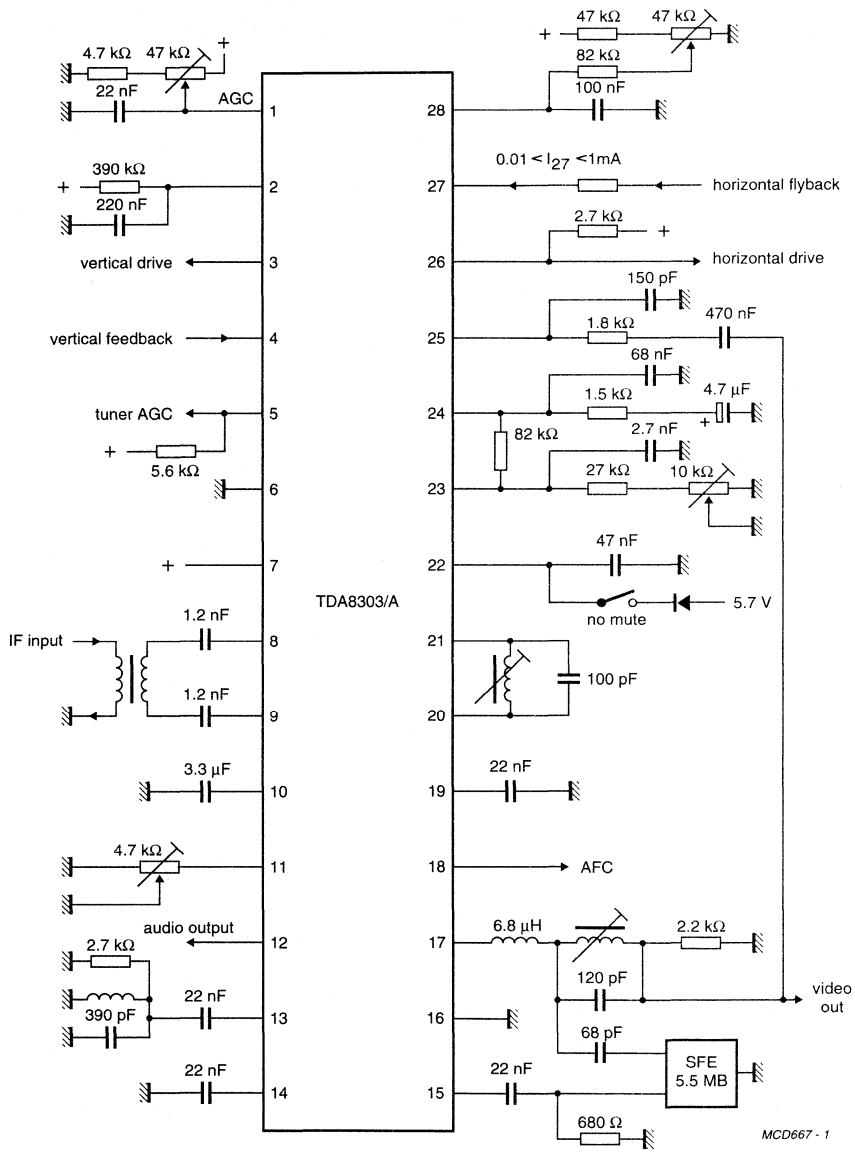


Fig.12 Application diagram.

Small signal combination IC for colour TV

TDA8304

FEATURES

- Gain controlled vision IF amplifier
- Synchronous demodulator for negative and positive demodulation
- AGC detector operating on peak sync amplitude for negative demodulation and on vision peak white level for positive demodulation
- Tuner AGC
- AFC circuit with on/off-switch
- Video preamplifier
- Video switch to select either the internal video signal or an external video signal
- Horizontal oscillator and synchronization circuit with two control loops
- Vertical synchronization (divider system), ramp generator and driver with automatic amplitude adjustment for 50 and 60 Hz
- Transmitter identification (mute)
- Sandcastle pulse generation
- Auto VCR switch
- 50/60 Hz identification

GENERAL DESCRIPTION

The TDA8304 possesses the capability to demodulate IF signals having either positive or negative-going video information. It is housed within a 32-pin encapsulation. The device includes a three-stage video IF amplifier, AFC and AGC circuitry, integral three-level sandcastle pulse generator, fully synchronized horizontal and vertical time bases with drive circuits, a video switch and a transmitter identification/mute circuit. A functional colour TV receiver can thus be realised with the addition of a tuner, audio demodulator and amplifier, chrominance decoder and respective line and field deflection circuitry.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8304	32	DIL	plastic	SOT201

FUNCTIONAL DESCRIPTION

Video IF amplifier, demodulator and video amplifier

Each of the three AC-coupled IF stages permits the omission of DC feedback and possesses a control range in excess of 20 dB.

The IF amplifier is followed by a passive synchronous demodulator providing a regenerated carrier signal. This is limited by a logarithmic limiter circuit prior to its application to the demodulator. Improved picture synchronization is provided by a wider bandwidth together with improved video amplifier linearity. The video amplifier contains also a white spot inverter and a noise clamp which limits interference pulses to a point below the peak sync level.

AFC-circuit

The reference signal for the AFC quadrature demodulator can also be acquired from the tuned circuit of the IF synchronous demodulator because an accurate 90° phase shift is realised internally. In this way only one tuned circuit needs to be applied and only one adjustment has to be carried out. The AFC output is affected by the asymmetrical frequency spectrum of the signal fed to the quadrature demodulator, which is determined by the SAW filter characteristic. To overcome this video frequency dependency of the AFC output, the demodulator output is followed by a sample-and-hold circuit.
For the reception of negative-going signals, the output is sampled only during peak sync (where a non-modulated carrier is present). When receiving signals with positive modulation the AFC is continuously active but extensively filtered. Substantial noise will be present on the quadrature demodulator input signal during reception of very weak signals. This noise has an asymmetrical frequency spectrum (with respect to the IF carrier) causing an offset in the AFC output voltage. This effect can be minimized by applying a notch in the demodulator tuned circuit. The sample-and-hold circuit is followed by an amplifier with high output impedance. The steepness of the of the AFC control voltage can be lowered by applying load resistors from the output to the supply and to ground. The AFC output is switched off when the AFC sample pin (22) is connected to ground.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 8)		10	12	13.2	V
I_P	supply current (pin 8)		90	115	140	mA
I_{start}	start current (pin 12)	note 1	-	6.5	9	mA
Video						
$V_{9\text{-}10(rms)}$	IF sensitivity (RMS value)	note 2	25	40	65	μV
$G_{9\text{-}10}$	IF gain control range		-	74	-	dB
S/N	signal-to-noise ratio	input signal = 10 mV	52	58	-	dB
V_{21}	AFC output voltage swing		10.5	-	11.5	V
Video switch						
$V_{16(p\text{-}p)}$	internal video input (peak-to-peak value)	V_O = 2.5 V(p-p)	-	2	-	V
$V_{13(p\text{-}p)}$	external video input (peak-to-peak value)	V_O = 2.5 V(p-p)	-	1	-	V
$V_{15(p\text{-}p)}$	video output signal (peak-to-peak value)		2.3	2.5	2.7	V
Sync						
V_{28}	required sync pulse amplitude	note 3	200	750	-	mV
I_{30}	required input current during flyback pulse		0.1	-	2	mA
V_{30}	sandcastle output during					
	burstkey		8	-	-	V
	horizontal blanking		4	4.4	5	V
	vertical blanking		2.1	2.5	2.9	V
V_{25}	video transmitter identification output					
	no signal condition		-	0.3	-	V
	signal condition		-	9.8	-	V
V_5	vertical feedback for DC voltage		2.9	3.3	3.7	V
$V_{5(p\text{-}p)}$	vertical feedback for AC voltage (peak-to-peak value)		-	1	-	V

Notes to the quick reference data

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_{cc}) is obtained from the horizontal output stage. The load current of the driver must be added to the value given.
2. On set AGC.
3. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.

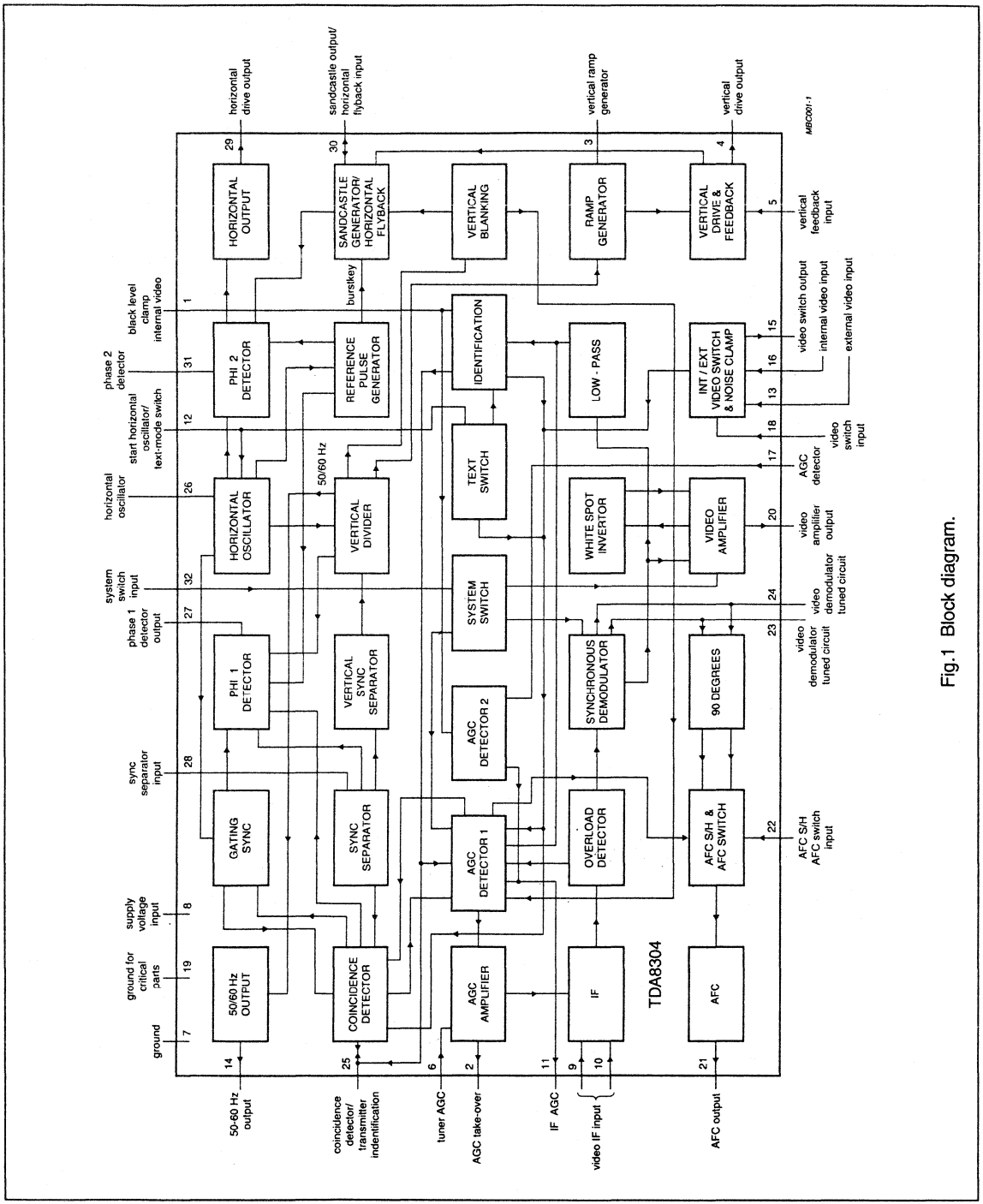


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	black level clamp internal video
2	tuner take-over
3	vertical ramp generator
4	vertical drive
5	vertical feedback
6	tuner AGC
7	ground
8	supply voltage input
9	video IF input
10	video IF input
11	IF AGC
12	start horizontal oscillator/text-mode switch
13	external video input
14	50 - 60 Hz output
15	video switch output
16	internal video input
17	AGC detector
18	video switch input
19	ground for some critical parts
20	video amplifier output
21	AFC output
22	AFC S/H, AFC switch input
23	video demodulator tuned circuit
24	video demodulator tuned circuit
25	coincidence detector/transmitter identification
26	horizontal oscillator
27	phase 1 detector
28	sync separator input
29	horizontal drive output
30	sandcastle output/horizontal flyback input
31	phase 2 detector
32	system switch input

AGC circuit

For signals employing negative modulation the AGC detector operates on peak sync level and on peak white level with those having positive modulation. Selection is facilitated by the system switch (pin 32), see Table 1.

The charge current at positive modulation (see Table 2) is only present during the vertical sync or when the level at pin 1 drops 200 mV below the level of pin 17 as a result of input signal variations. To obtain rapid AGC action when executing a search tuning operation when the circuit is set for peak white AGC, the charge current is increased to 55 μA until the detection of a transmitted signal. With an AGC capacitor of 6.8 μF the video tilt will be < 2% for positive and for negative modulated signals.

VCR switch

The TDA8304 has an auto VCR-switch facility. Due to the inherent instability of signals from a VCR, the horizontal time constant should be shorter to prevent loss of horizontal synchronization in the early part of the scan. Provision is therefore incorporated (in the internal video mode) to automatically switch the short time constant such that a strong signal instigates the 'VCR' mode and a weak signal triggers the 'TV' mode. The phase detector is gated during the 'TV mode' and operates with a long time constant. The phase detector is not gated in the 'VCR' mode and operates with a short time constant. The TDA8304 is active in the 'VCR' mode only at reception of an external video signal.

Video-switch

Selection between internal video (pin 16) and external video (pin 13) is made by applying a switching potential to pin 18 (see Table 3). Video output (pin 20) from the device is filtered to remove the audio carrier and DC-coupled to pin 16. The TDA8304 provides the opportunity for a direct video connection (e.g. via a peritel connector) to be made to the device at pin 13. The AGC detector is not gated during the external video mode, the first phase detector is also not gated and operates with a short time constant. The gain of the

IF amplifier (in the external video mode) is reduced to prevent crosstalk of the video amplifier to the horizontal oscillator during the no-signal condition.

Horizontal synchronization

The horizontal synchronization circuit of the TDA8304 provides the drive pulse for a horizontal deflection stage.

- The phase of the control loop will be adapted automatically to the level of the input signal in order to achieve an optimum performance
- The control gradient of the control loop will be low at reception of weak signals to reduce the noise bandwidth.
- The phase detector control current is increased during strong or no-signal reception to obtain a short catching time and a good performance during VCR playback.

Vertical synchronization

The TDA8304 embodies a synchronized divider system for generating the vertical sawtooth at pin 3 having several advantages and features such as:

- The vertical frequency is alignment free. The divider automatically adapts to a vertical frequency of 50 Hz or 60 Hz including automatic amplitude correction and its operating modes offer maximum interference/disturbance protection.
- A discriminator-window checks the accuracy of the vertical trigger pulse. Internally clockpulses are generated by doubling the line frequency. The divider operates in the 60 Hz mode when the trigger pulse appears before count 576, otherwise the 50 Hz mode will be active.
- The divider system operates with a number of different reset windows. The windows are activated via an up/down counter. The counter increases its counter-value by 1 for each time the separated vertical sync pulse appears within the selected window, otherwise the counter value is lowered by 1.

Modes of operation

Large search window (divider ratio between 488 and 722). This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found does not comply with the narrow window specification limits
- Up/down counter value of the divider system, operating in the narrow window mode, drops below count 10

Narrow window mode: divider ratio between 522 - 528 (60 Hz) or 622 - 628 (50 Hz)

- The divider system switches over to narrow window mode when the up/down counter has reached his maximum value of 15 vertical sync pulses.
- When the divider operates in the narrow window mode and a vertical sync pulse is missing in the window, the divider is reset at the end of that window and the counter value is lowered by 1.
- At a counter value below 10 the divider system switches over to the large window mode.
- The divider system generate also the so-called anti-top-flutter pulse which inhibits the phase 1 detector during the vertical sync pulse. The width of this pulse depends on the divider mode. For the large window mode the start is generated at the reset of the divider. In the narrow window mode the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 10 for 50 Hz and at count 12 for 60 Hz.
- The divider is switched to count 625 when out of sync is detected by the coincidence detector. This results in a stable amplitude when no input signal is available.
- The divider is switched to the large window mode when enlarged vertical sync pulses are detected.

Table 1 AGC circuit operation

STATE	POSITIVE MODULATION	NEGATIVE MODULATION
input pin 32	HIGH/open	LOW

Table 2 AGC detector currents

STATE	POSITIVE MODULATION		NEGATIVE MODULATION	
action	current	condition	current	condition
charge	10 µA	V-sync signal	55 µA	-
charge	55 µA	pin 25 = LOW	-	-
discharge	3 mA	VITS signal	1.5 mA	H-sync signal

Table 3 Video switch operation

STATE	INTERNAL VIDEO	EXTERNAL VIDEO
input pin 18	LOW	HIGH

QUALITY SPECIFICATION

Quality level according to UZW-BQ/FQ-601.

SYMBOL	PARAMETER	RANGE A	RANGE B	UNIT
ESD	protection circuit specification (note 1)	2000	500	V
		100	200	pF
		1500	0	Ω

Note to the Quality specification

1. All pins of the IC are protected against ESD by means of the internal clamping diodes. Range A represents the human body model and range B represents the charge device model.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 8)	-	13.2	V
P_{tot}	total power dissipation	-	2.3	W
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−25	+65	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	30	35	K/W

The transmitter identification/coincidence detector

Pin 25 of the TDA8304 serves as the transmitter identification and/or coincidence detector (see Table 4). Pin 25 is HIGH (= 9.8 V) when a transmitter is present and LOW (= 0.3 V) when of no transmitter signal is detected. When the video switch is in the internal mode, the signal at the sync separator input (pin 28) is the demodulated IF signal, pin 25 will act as a coincidence detector. Pin 25 is HIGH when the horizontal oscillator loop is synchronized with the video signal and LOW in case of no synchronization. In the external video mode and in the text mode, pin 25 will be active as transmitter identification. The system relies upon the detection of sync pulses on the incoming IF signal. Pin 25 is charged with a current of 125 μA by the separated horizontal sync pulse and discharged continuously with a current of 4 μA. The high impedance of pin 25 should be taken into account in the application concept.

The 50/60 Hz identification

The 50/60 Hz information (see Table 5) derived from the divider system is available at the open collector output pin 14.

Table 4 Transmitter identification/coincidence detector

STATE	INTERNAL VIDEO					EXTERNAL VIDEO	
input pin 18	LOW					HIGH	
input pin 12	TV mode = HIGH		Text mode = LOW				
Input signal pins 9 and 10	yes	none	yes	none	none	yes	none
input pin 28	50/60 Hz	none	50/60 Hz	VCS text	none	don't care	don't care
output pin 25	9.8 V	0.3 V	9.8 V	0.3 V	0.3 V	9.8 V	0.3 V

Table 5 50/60 Hz identification

INPUT/OUTPUT	STATUS	STATUS	STATUS
Input signal pins 9 and 10	don't care	don't care	don't care
input pin 28	50 Hz	60 Hz	none
output pin 14	0.3 V	12 V	0.3 V

CHARACTERISTICS

T_{amb} = 25 °C;V_p = 12 V; carrier 38.9 MHz negative modulation, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 8)						
V_8	supply voltage range		10	12	13.2	V
I_8	supply current	no input	90	115	140	mA
I_{12}	start current (pin 12)	note 1	-	6.5	9	mA
V_{12}	start protection level	I_{12} = 12 mA	-	-	16.5	V
IF Amplifier						
$V_{9\text{-}10(rms)}$	input sensitivity (RMS value)	note 2	25	40	65	μV
$R_{9\text{-}10}$	differential input resistance	note 3	-	1300	-	Ω
$C_{9\text{-}10}$	differential input capacitance	note 3	-	5	-	pF
$G_{9\text{-}10}$	gain control range		-	74	-	dB
ΔV_{20}	output signal expansion for 46 dB input signal variation	note 4	-	1	-	dB
$V_{9\text{-}10}$	maximum input signal		100	170	-	mV
$V_{9\text{-}10(rms)}$	input sensitivity in external mode (RMS value)	note 2	250	400	650	μV
Video Amplifier (notes 5 and 6)						
V_{20}	negative modulation, zero signal level		4.7	4.9	5.1	V
V_{20}	positive modulation, zero signal level		2.5	2.7	2.9	V
V_{20}	peak sync (negative modulation)	note 7	2.5	2.75	3.0	V
V_{20}	white level (positive modulation)	note 7	4.7	4.9	5.1	V
V_{20}	white spot threshold level		-	5.7	-	V
V_{20}	white spot insertion level		-	4	-	V
Z_{20}	video output impedance		-	25	-	Ω
I_{20}	internal bias current of npn emitter follower output transistor		1.4	1.8	-	mA
I_{source}	maximum source current (pin 20)		10	-	-	mA
B	bandwidth of demodulated output signal		5	6	-	MHz
G_{20}	differential gain	note 8	-	2	5	%
φ	differential phase	note 8	-	2	5	deg
NL	video non-linearity	note 9	-	2	5	%
	intermodulation	note 10				
	1.1 MHz; blue		50	60	-	dB
	1.1 MHz; yellow		50	60	-	dB
	3.3 MHz; blue		55	65	-	dB
	3.3 MHz; yellow		55	65	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio	10 mV input signal	52	58	-	dB
		end of gain control range; note 11; see Fig.5	57	62	-	dB
V_{20}	residual carrier signal		-	2	10	mV
V_{20}	residual 2nd harmonic of carrier signal		-	2	10	mV
System switch (note 12)						
AGC ON PEAK SYNC LEVEL FOR NEGATIVE MODULATION SIGNALS						
V_{32}	control voltage		0	-	0.8	V
I_{32}	input current		−100	-	−500	µA
AGC ON WHITE LEVEL FOR POSITIVE MODULATION SIGNALS						
V_{32}	control voltage		2	-	12	V
I_{32}	input current		0	-	1	mA
IF sync separator						
I_I	input current		0.4	0.6	0.8	mA
I_O	output current (pin 1)		22	27	32	µA
V_1	clamp level		-	3.3	-	V
Tuner AGC						
$V_{9\text{-}10(rms)}$	minimum starting point for tuner take-over (RMS value)		-	-	0.2	mV
$V_{9\text{-}10(rms)}$	maximum starting point for tuner take-over (RMS value)		100	150	-	mV
I_6	maximum tuner AGC output swing	V_6 = 3 V	4	-	-	mA
V_6	output saturation voltage	I_6 = 2 mA	-	-	300	mV
I_6	leakage current		-	-	1	µA
	input signal variation complete tuner control	ΔI_6 = 2 mA	0.2	2	4	dB
V_2	minimum voltage tuner take-over		-	-	1	V
AGC detection level						
I_{17}	charge current		-	200	-	µA
I_{17}	discharge current		-	20	-	µA
V_{17}	clamp level		-	2.9	-	V
Video switching circuit (note 13)						
EXTERNAL POSITIVE VIDEO INPUT						
$V_{13(p\text{-}p)}$	input signal (peak-to-peak value)	V_O = 2.5 V(p-p)	-	1	-	V
I_{13}	input current		-	1.5	5	µA
V_{13}	peak sync clamping level	I_{13} = 1 mA	1.65	1.85	2.05	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INTERNAL VIDEO INPUT						
$V_{16(p-p)}$	Internal video input signal (peak-to-peak value	V_O = 2.5 V(p-p)	-	2	-	V
I_{16}	input current		-	1.5	5	µA
V_{16}	noise clamping level	I_{16} = 1 mA	2.2	2.4	2.6	V
VIDEO OUTPUT (POSITIVE VIDEO)						
$V_{15(p-p)}$	video output signal (peak-to-peak value)		2.3	2.5	2.7	V
V_{15}	peak sync signal		-	3	-	V
I_{bias}	internal bias current (pin 15)		1	1.5	-	mA
I_O	maximum output current (pin 15)		5	-	-	mA
α	crosstalk external to internal	notes 14 and 24	-	55	-	dB
α	crosstalk internal to external	notes 14 and 24	-	55	-	dB
Video switch						
V_{18}	input voltage for internal video		-	-	0.8	V
V_{18}	input voltage for external video		2	-	V_P	V
I_{18}	maximum current	V_{18} = 0 V	-	0.05	0.2	mA
		V_{18} = 12 V	-	0.25	1	mA
Text/TV switch						
V_{12}	input voltage for text mode		-	-	0.8	V
V_{12}	input voltage for TV mode		2	-	V_P	V
I_{12}	maximum current	V_{12} = 0 V	-	-	0.3	mA
		V_{12} = 11.5 V	-	-	1.5	mA
AFC-circuit (note 15)						
I_{22}	AFC sample and hold switch-off current		0.1	-	-	mA
I_O	output current (pin 22)	V_{22} = 0 V	0.2	0.4	0.8	mA
I_{LI}	leakage current (pin 22)		-	-	1	µA
V_{21}	AFC output voltage swing		10.5	-	11.5	V
I_{21}	available output current		±0.2	-	-	mA
	control slope		-	100	-	mV/kHz
V_O	output voltage (pin 21)	AFC off	5.5	6	6.5	V
R_O	AFC output resistance		-	40	-	kΩ
$V_{21(p-p)}$	output voltage swing	notes 16 and 24	-	11	-	V
	control slope	notes 16 and 24	-	80	-	mV/kHz
V_{21}	output voltage shift with respect to V_I = 10 mV(RMS)	notes 16 and 24	-	–2	-	V
Sync separator (see Fig.6)						
V_{28}	required sync pulse amplitude	note 17	200	750	-	mV
I_{28}	input current	V_{28} > 5 V	-	8	-	µA
		V_{28} = 0 V	-	–10	-	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
First control loop						
Δf	PLL holding range		-	±1500	±2000	Hz
Δf	PLL catching range		±600	±1500	-	Hz
	control sensitivity to oscillator	note 18	see Fig.7			
$V_{9\text{-}10(rms)}$	IF input signal for switching from fast to slow (RMS value)		-	2.2	-	mV
Second control loop (positive edge)						
$\frac{\delta t_d}{\delta t_o}$	control sensitivity, see Fig.6	note 19	-	100	-	
t_d	control range		-	25	-	µs
Phase adjustment (via second control loop)						
	control sensitivity		-	25	-	µA/µs
α	maximum allowed phase shift		-	±2	-	µs
Horizontal oscillator						
	free running frequency	R = 34.3 kΩ; C = 2.7 nF	-	15625	-	Hz
Δf	spread with fixed external components		-	-	4	%
Δf	frequency variations with supply voltage from 10 to 13.2 V		-	-	2	%
Δf_T	frequency variation with temperature	note 24	-	–1.6	-	Hz/°C
Δf_{fr}	maximum frequency deviation at start of horizontal output		-	-	10	%
Δf	frequency variation when only noise is received	note 24	-	-	500	Hz
Horizontal output (open collector; pin 29)						
V_{29}	output limiting voltage		-	-	16.5	V
V_{OL}	output voltage LOW	I_{sink} = 10 mA	-	0.3	0.5	V
I_{sink}	maximum sink current		10	-	-	mA
	duty factor of output signal		-	46	-	%
t_r	rise time output pulse		-	260	-	ns
t_f	fall time output pulse		-	100	-	ns
Flyback input and sandcastle output (note 20)						
I_{30}	required input current during flyback pulse		0.1	-	2	mA
V_{30}	output voltage during					
	burstkey		8	-	-	V
	horizontal blanking		4	4.4	5	V
	vertical blanking		2.1	2.5	2.9	V
t_W	pulse width of burstkey					
	at 60 Hz signals		2.9	3.3	3.7	µs
	at 50 Hz signals		3.2	3.6	4	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Flyback input and sandcastle output (note 20)						
	width of horizontal blanking pulse		flyback pulse width			
	width of vertical blanking pulse					
	divider in search window	50 Hz	-	21	-	lines
		60 Hz	-	17	-	lines
	divider in narrow window	50 Hz	-	25	-	lines
		60 Hz	-	21	-	lines
t_d	delay between the start of the sync pulse at the video output and the burstkey pulse	60 Hz				
	trailing edge		-	-	9.3	µs
	rising edge		4.7	5.4	6.1	µs
Vertical ramp generator (note 22)						
I_3	input current during scan		-	-	2	µA
I_3	discharge current during retrace		-	0.8	-	mA
$V_{3(p-p)}$	sawtooth amplitude (peak-to-peak value)		-	1.9	-	V
t	interlace timing of the internal pulses	note 24	30	32	34	µs
Vertical output						
I_4	available output current	V_4 = 4 V	-	-	3	mA
V_4	maximum available output voltage	I_4 = 0.1 mA	4.4	5	-	V
Vertical feedback input						
V_5	DC input voltage		2.9	3.3	3.7	V
$V_{5(p-p)}$	AC input voltage (peak-to-peak value)		-	1	-	V
I_5	input current		-	-	12	µA
	internal pre-correction to sawtooth		-	3	-	%
	deviation amplitude 50/60 Hz		-	-	2	%
	temperature dependency of the amplitude	note 24 ΔT = 45 °C	-	-	2	%
Vertical guard						
ΔV_5	active switch level at a deviation with respect to the DC feedback level	note 23; V_{30} = 2.5 V				
	guard level LOW		-	1.5	-	V
	guard level HIGH		-	2	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Coincidence detector/transmitter identification (note 21)						
V_{25}	voltage for in-sync condition		-	9.8	-	V
V_{25}	voltage for no-sync condition	no signal	-	0.3	-	V
V_{25}	switching level to switch the phase detector from fast to slow		6.2	6.7	7.2	V
V_{25}	hysteresis slow to fast		-	0.6	-	V
V_{25}	switching level to activate the mute function (transmitter identification)		2.5	2.8	3.1	V
V_{25}	hysteresis mute function		-	2.0	-	V
I_{25}	load (allowed) at pin 25		–2	-	2	μA
50/60 Hz identification (open collector output)						
V_{14}	output voltage at 50 Hz (no signal)		-	0.3	0.5	V
V_{14}	output voltage at 60 Hz		-	V_p	-	V
I_{14}	sink current active		-	-	5	mA
I_{14}	output current inactive (transmitter present)		-	-	1	μA

Notes to the characteristics

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_{cc}) is obtained from the horizontal output stage. The load current of the driver must be added to the value given.
2. On set AGC.
3. The input impedance has been chosen such that a SAW filter can be employed.
4. Measured with 0 dB = 450 μV.
5. Measured at 10 mV RMS 100% input signal.
6. Projected zero point; i.e. with switched demodulator.
7. The output signal amplitude is determined by the AGC detector. For negative modulation the peak sync level is used as reference. With positive modulation the white level is stabilized.
8. Measured according to the test line given in Fig. 3. The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level. The differential phase is defined as the difference in degrees between the largest and smallest phase angle. The differential gain and phase are measured with a DSB signal.
9. This figure is valid for the complete video signal amplitude (peak white-to-black). The non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step.
10. The test set-up and input conditions are given in Fig. 5. The figures are measured at an input signal of 10 mV RMS.
11. Measured with a source impedance of 75 Ω.

$$\textit{The signal-to-noise ratio} = 20 \log \frac{V_O \ \textit{black-to-white}}{V_{n(rms)} \ \textit{at} \ B = 5 \ \textit{MHz}}$$

12. By means of the system switch 2 conditions can be obtained. Negative modulation with peak sync level AGC. This is obtained with pin 32 connected to ground. Positive modulation with peak white AGC. This is obtained with pin 32 connected to the positive supply.

13. When the video switch is in the external mode the first control loop in the synchronization circuit is not switched to a long time constant when weak signals are received.
14. Defined as $20 \log \frac{V_O \text{ unwanted video black-to-white}}{V_O \text{ wanted video-black-to-white}}$; measured at 4.4 MHz.
15. The indicated figures are measured at an input signal of 10 mV RMS. The unloaded Q-factor of the reference tuned circuit is 70. With very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has a asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect a notch filter can be built into the demodulator tuned circuit. The characteristics given for weak signals are measured without a notch circuit, with a SAW filter connected in front of the IC input signal such that the input signal of the IC is 150 μV (RMS value).
16. Measured at an input signal amplitude of 150 μV(RMS) (pin 21).
17. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
18. Frequency control is obtained by supplying a correction current to the oscillator RC network via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by short circuiting the sync separator bias network (pin 28) to $+V_p$. To avoid the need of a VCR switch the time constant of the phase detector at strong input signals is sufficiently short to get a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that the head-errors of the VCR are compensated at the beginning of scan. During conditions of weak signal (information derived from the AGC circuit) the time constant is increased to obtain a better noise immunity.
19. This figure is valid for an external load impedance of 82 kΩ from pin 31 to the phase adjustment potentiometer (of H-shift).
20. The flyback input and sandcastle output have been combined on one pin. The flyback pulse is clamped to a level of 4.5 V. The minimum current to drive the second control loop is 0.1 mA.
21. The functions in-sync/out-of-sync and transmitter identification have been combined on this pin. The capacitor is charged during the sync pulse and discharged during the time difference between gating (6.5 μs) and the sync pulse in the internal video mode. When the circuit is in the external mode the capacitor is charged by the horizontal sync pulse and discharged continuously with a small current.
22. The vertical scan is synchronized by means of a divider system. Therefore no adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and corrects the vertical amplitude.
23. To avoid screen burn due to a collapse of the vertical deflection a continuous blanking level (V_{30} = 2.5 V) is inserted in the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
24. These figures are based on test samples.

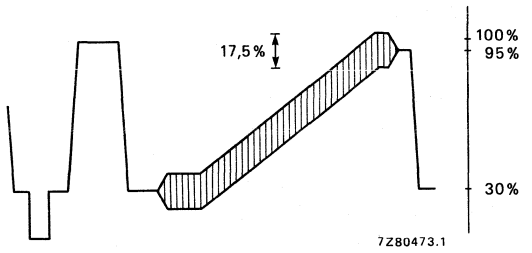


Fig.2 Video output signal.

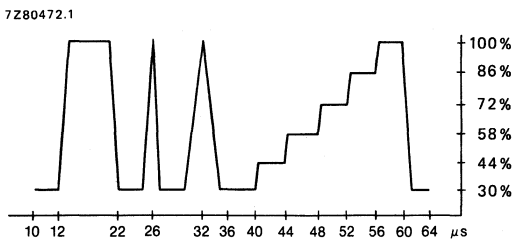
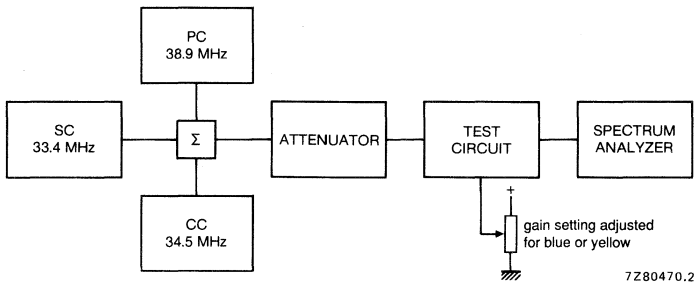
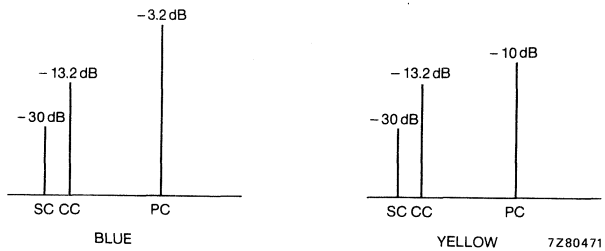


Fig.3 EBU test signal waveform (line 17).





Input signal conditions

SC = Sound carrier

CC = Chrominance carrier

PC = Picture carrier

All with respect to peak sync level

$$Value\ at\ 1.1MHz: 20 \log \frac{V_o\ at\ 4.4MHz}{V_o\ at\ 1.1MHz} + 3.6dB$$

$$Value\ at\ 3.3MHz: 20 \log \frac{V_o\ at\ 4.4MHz}{V_o\ at\ 3.3MHz}$$

Fig.4 Test set-up intermodulation.

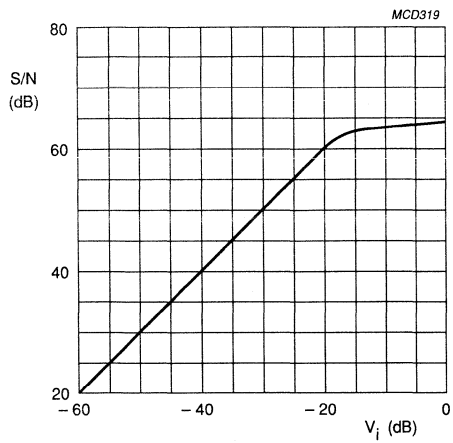
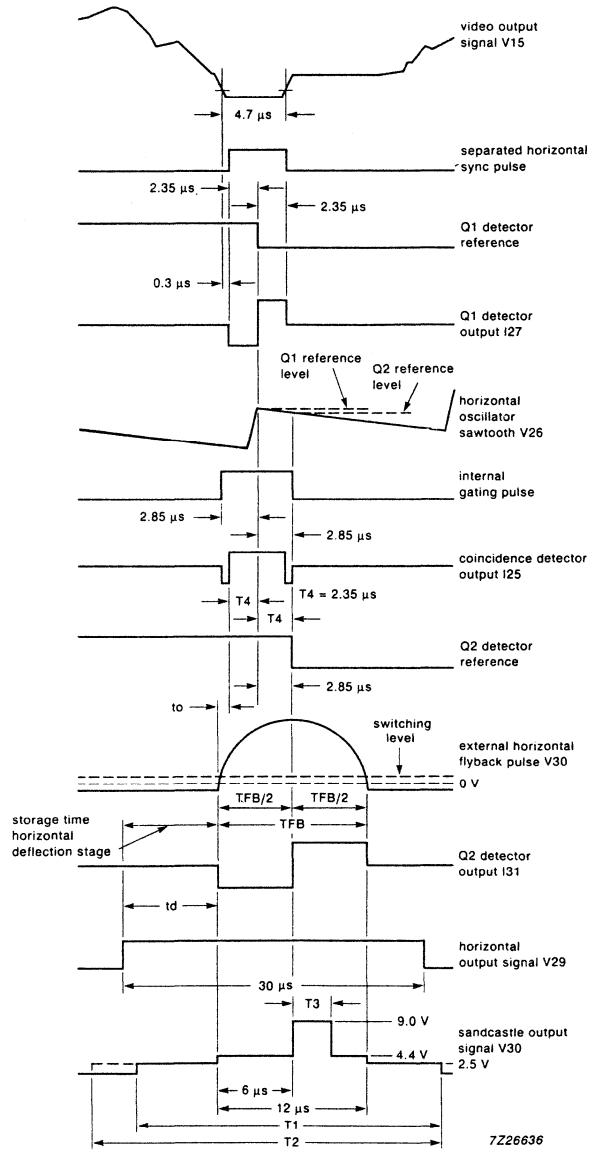


Fig.5 Signal-to noise ratio as a function of the input voltage (0 dB = 100 mV).



T1: divider in search window: 42p (50 Hz); 34p (60 Hz); $p = 1/2f_H$

T2: divider in narrow window: 50p (50 Hz); 42p (60 Hz)

T3: 3.6 µs (50 Hz); 3.3 µs (60 Hz)

Fig.6 Timing diagram.

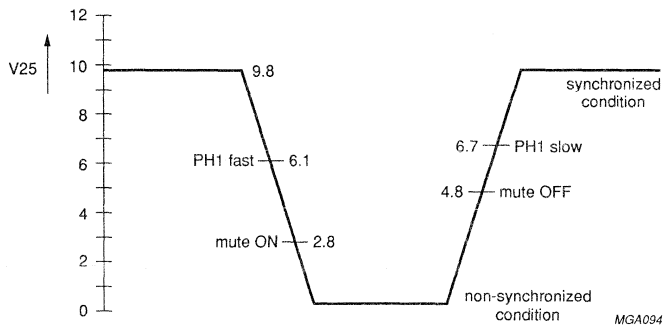


Fig.7 Switching levels coincidence detector.

CONDITION PIN 18 VIDEO SWITCH	CONDITION V_{25}	CONTROL SENSITIVITY HOR.OSCILLATOR kHz / µs	
		T2 - T1	T3 = SCAN
Low internal video	V_{25} > 6.7 V and strong signal	11.3	7.6
	V_{25} > 6.7 V and weak signal	1.3	1.3
	V_{25} < 6.1 V and strong signal	11.3	7.6
	V_{25} < 6.1 V and weak signal	11.3	7.6
HIGH or floating external video	don't care	11.3	7.6

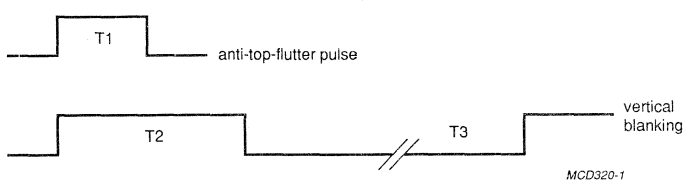


Fig.8 Anti-top-flutter-pulse.

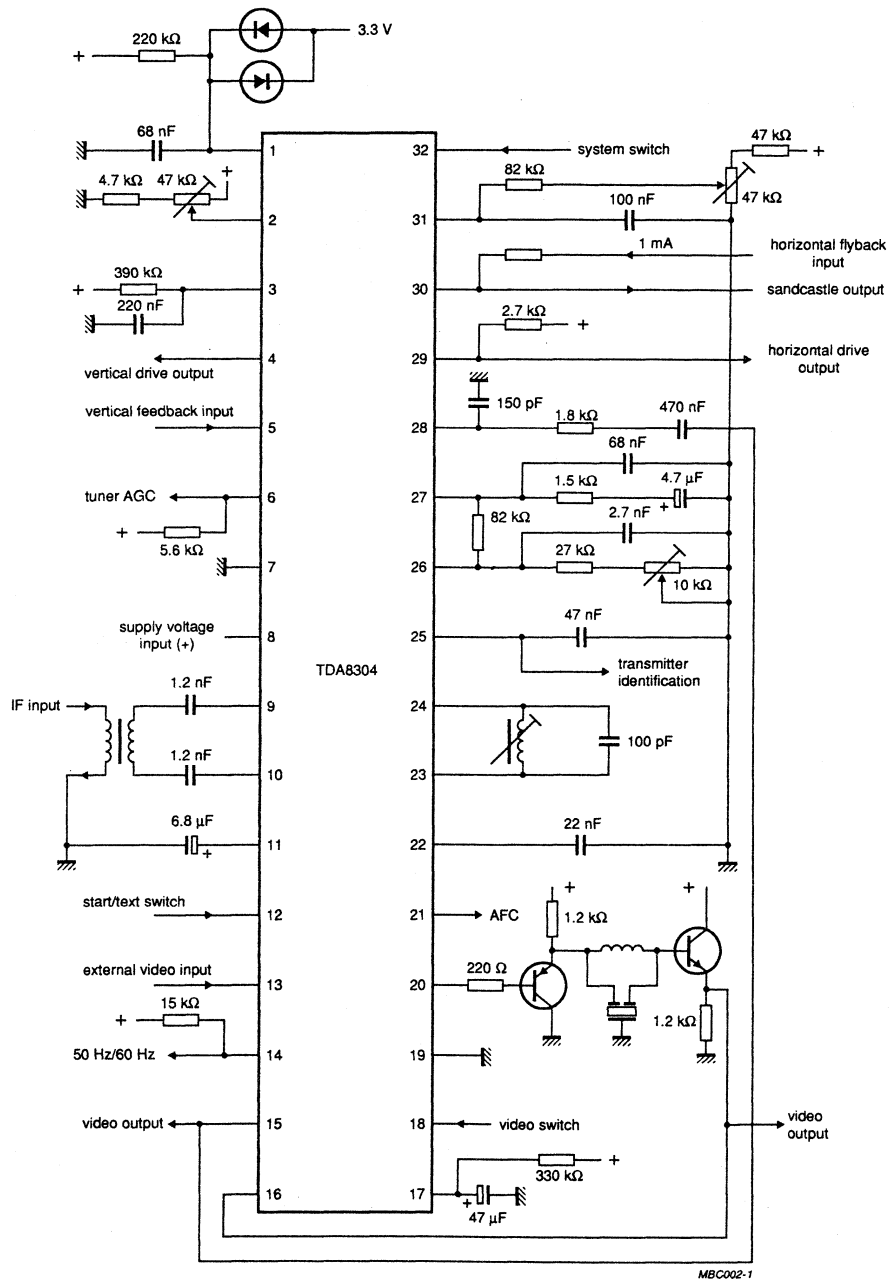


Fig.9 Application diagram.

SMALL SIGNAL COMBINATION IC FOR COLOUR TV

GENERAL DESCRIPTION

The TDA8305A is a TV sub-system circuit, for colour television receivers with the following features.

Features

- Vision IF amplifier with synchronous demodulator
- Automatic gain control (AGC) detector suitable for negative modulation
- AGC tuner
- Automatic frequency control (AFC) circuit with sample-and-hold
- Video preamplifier
- Sound IF amplifier and demodulator
- DC volume control or separate supply for starting the horizontal oscillator
- Audio preamplifier
- Horizontal synchronization circuit with two control loops
- Vertical synchronization (divider system) and sawtooth generation with automatic amplitude adjustment for 50 and 60 Hz
- Transmitter identification (mute)
- Generation of sandcastle pulse

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 7)	V_{7-6}	9.5	12	13.2	V
Supply current (pin 7)	I_7	75	125	165	mA
Start current (pin 11)	I_{11}	–	6.5	9.0	mA
Video					
IF sensitivity at 38.9 MHz (RMS value)		25	40	65	μV
IF gain control range	G_{8-9}	–	74	–	dB
Signal-to-noise ratio at 10 mV input signal	S/N	50	57	–	dB
AFC output voltage swing (peak-to-peak value)	$V_{18-6(p-p)}$	10.5	–	11.5	V
Sound					
AF output signal (RMS value)	$V_{12-6(rms)}$	400	600	800	mV
AM suppression at V_I = 50 mV	AMS	53	58	–	dB
Total harmonic distortion	THD	–	0.5	2	%

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT117)

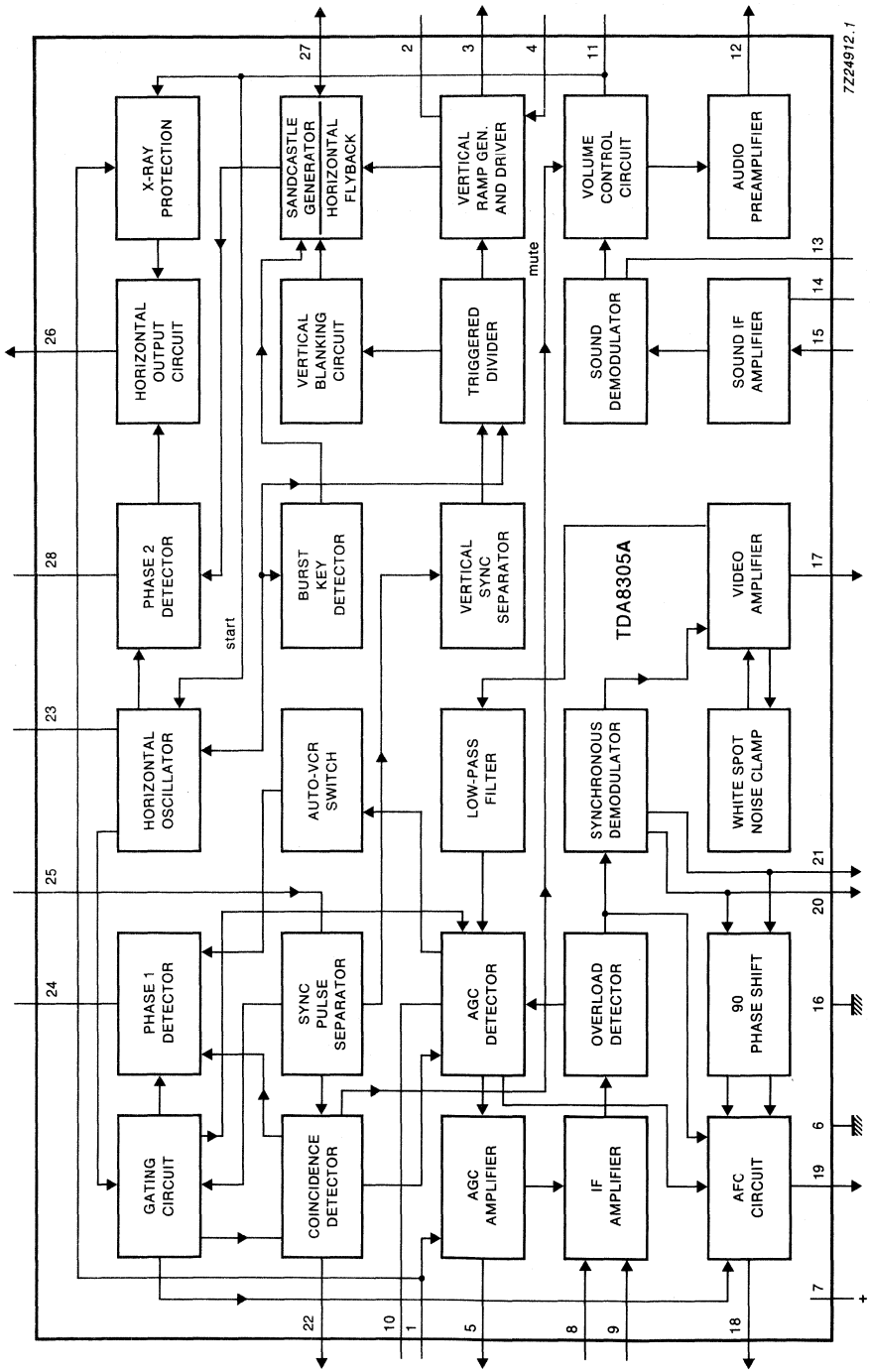


Fig.1 Block diagram.

QUICK REFERENCE DATA (continued)

parameter	symbol	min.	typ.	max.	unit
Sync pulse input amplitude	V_{25}	200	750	–	mV
Flyback input current	I_{27}	0.1	–	2	mA
Sandcastle output					
during burst key	V_{27}	8	–	–	V
during horizontal blanking	V_{27}	4	4.5	5	V
during vertical blanking	V_{27}	2.1	2.5	2.9	V
Coincidence detector voltage					
in synchronized condition	V_{22}	–	9.5	–	V
in no signal condition	V_{22}	–	1.5	–	V
Vertical feedback input					
DC voltage	V_{22}	2.9	3.3	3.7	V
AC voltage (peak-to-peak value)	$V_{22(p\text{-}p)}$	–	1.2	–	V

DEVELOPMENT DATA

PINNING

1. AGC take-over/X-ray protection
2. Vertical ramp generator
3. Vertical drive
4. Vertical feedback
5. Tuner AGC
6. Ground
7. Main supply voltage
8. Vision IF input
9. Vision IF input
10. IF AGC
11. Volume control/start horizontal oscillator
12. Audio output
13. Sound demodulator
14. Sound IF decoupling
15. Sound IF input
16. Ground (for some critical parts)
17. Video output
18. AFC output
19. AFC S/H, AFC switch
20. Vision demodulator tuned circuit
21. Vision demodulator tuned circuit
22. Coincidence detector
23. Horizontal oscillator
24. First phase detector
25. Sync separator
26. Horizontal drive
27. Sandcastle output/horizontal flyback input
28. Second phase detector

FUNCTIONAL DESCRIPTION

Vision IF amplifier, demodulator and video amplifier

The IF amplifier of the TDA8305A has three AC-coupled stages, each stage having a control range that exceeds 20 dB. AC-coupling means that the DC-feedback circuitry of the amplifier (present in the TDA4505) can be omitted, resulting in a saving of one pin. An additional advantage is the symmetry of the amplifier which results in a less critical application.

In the TDA8305A the regenerated carrier signal is limited by a logarithmic limiter circuit before it is passed on to a passive synchronous demodulator. The limiter has a very low differential phase shift which results in good differential gain and phase figures.

The TDA8305A's video amplifier has a higher bandwidth and better linearity compared with that of the TDA4505. A noise clamp is included in the video amplifier that limits the interference pulses to a level just below the top sync. This circuit is more effective than the noise inverter used in the TDA4505 and results in an improved picture stability, with respect to interference.

AFC circuit

In the TDA4505 and TDA8305A, the reference signal for the AFC circuit is obtained from the demodulator tuned circuit which means only one tuned circuit and adjustment are needed. The disadvantage with this method is that the frequency spectrum fed to the detector is determined by the SAW filter characteristic. This spectrum is asymmetrical with respect to the picture carrier so that the AFC output voltage is dependent on the video signal. This was the main problem found with the TDA4505's AFC circuit.

To remove this problem the TDA8305A is equipped with a sample-and-hold circuit which samples during the sync level of the signal. This means that only the carrier signal is available to the AFC and it will not be affected by the video information. The additional pin required for this circuit is provided by the pin that became available when the DC feedback circuit was removed from the IF amplifier (see previous section).

Weak input signals will cause the drive signal of the AFC to contain a lot of noise. This noise signal has an asymmetrical frequency spectrum that causes an offset in the AFC output voltage, this offset can be reduced by applying a notch to the demodulator circuit. The sample-and-hold circuit is followed by a high output impedance amplifier, therefore the AFC's control steepness is dependent on the load impedance.

AGC circuit

The TDA8305A's AGC detector differs from that of the TDA4505 in that it doesn't need the charge resistor but has an internal current source. Also the circuitry between the detector capacitor and the control stages has been changed to improve the signal-to-noise ratio of the video output signal (no dips in the S/N ratio depending on the input signal amplitude). The point of tuner take-over is preset by the voltage level at pin 1.

Sound circuit and horizontal oscillator starting function

The input to the sound IF amplifier is by means of a bandpass filter coupling from the video output (pin 17). The sound is demodulated and passed via a volume control stage to the audio output amplifier. Volume control is obtained by connecting a potentiometer (10 kΩ) between pin 11 and ground, or by supplying pin 11 with a variable voltage. Sound output is suppressed by an internal mute signal when no TV signal is identified.

Improvement of sound quality was one of the main reasons for redesigning the TDA4505. To obtain a better idea of the performance of the various circuits of the TDA4505 the following measurements were carried out:

- Weak signal performance when a TBA120 is driven with an intercarrier signal obtained from the vision IF circuit of the TDA4505 (the sound IF of the latter was not used)
- The same measurement for the sound IF circuit of the TDA4505 driven from another TDA4505 (again without using the sound IF circuit)
- The same measurement as in the first case but with the sound IF of the TDA4505 connected normally

From the results of these measurements it was established that the sound problem was caused by an interaction between vision IF and sound circuits. The improved sound quality of the TDA8305A as compared to the TDA4505 was achieved by:

- A very symmetrical vision-IF amplifier which is less sensitive to radiation from the sound IF amplifier
- A change to the internal ground and supply connections of the IC to reduce coupling between both circuits

DC volume control/Horizontal oscillator start

Horizontal oscillator; the operation depending on the application. During switch-on if no current is supplied to pin 11 this pin will act as a volume control. When a current of 9.0 mA is supplied to pin 11 the volume control is set to a fixed output signal and the device will generate drive pulses for the horizontal deflection. The main supply can then be derived from the horizontal deflection circuit.

Horizontal synchronization

The video input signal (positive video) is connected to pin 25. The horizontal synchronization has two control loops that generate a sandcastle pulse. Using the oscillator sawtooth facilitates accurate timing of the burst key pulse. Therefore, the phase of this sawtooth must have a fixed relationship to the sync pulse, which is achieved by use of the second control loop.

The TDA8305A's horizontal synchronization circuit differs from that of the TDA4505 in that:

- The horizontal oscillator's retrace occurs during the horizontal retrace and not during the scan period. This means that with weak input signals no interference will be visible on the screen. It also prevents video crosstalk from disturbing the picture phase
- The reference signal for the horizontal phase detector is nearer to being symmetrical and is independent of the supply voltage and temperature. As a consequence the frequency shift of the horizontal oscillator during noise is reduced
- The current ratio of the phase detector for strong and weak signals is increased to obtain better behaviour during both VCR-playback and weak signal reception. The switching level is independent of supply voltage and temperature.

FUNCTIONAL DESCRIPTION (continued)

Horizontal phase detector

The circuit has the following operating conditions.

(a) Strong input signal, synchronized or non-synchronized.
(The strong/weak signal condition is obtained from the AGC circuit; the in-sync/out-of-sync from the coincidence detector). In this condition the time constant is optimum for VCR-playback i.e. fast time constant during the vertical retrace (to be able to correct VCR head-errors) and such, that during scan, fluctuations of the sync are corrected. The phase detector is not gated.

(b) Weak signal - synchronized
In this condition the time constant is increased compared to condition (a). Also the phase detector is gated when the oscillator is synchronized. This ensures a stable display which is not disturbed by noise in the video signal.

(c) Weak signal - non-synchronized.
In this condition the time constant during scan and vertical retrace are the same as during scan in condition (a).

Vertical synchronization

The TDA8305A's vertical circuit differs from that of the TDA4505 in that it has:

- Improved interlacing - the timing of the internal pulses is now close to a 50/50 ratio. This timing is independent of supply voltage and temperature
- The temperature drift of the vertical amplitude has been reduced
- Reduction of noise in the vertical output signal so that modulation of the line distance will no longer be visible on large screen sets.
- When out-of-sync is detected by the horizontal circuit the divider is switched to 625 lines. This results in a stable amplitude when no input signal is available. In the TDA4505 the divider remains in the wide window during this condition which means interference may affect stability.

Vertical sync pulse

The vertical sync pulse integrator will not be disturbed when the vertical sync pulses have a width of 10 μs with a separation of 22 μs. These types of vertical sync pulses are sometimes generated by video tapes with anti-copy guard.

Vertical divider system

The TDA8305A embodies a synchronized divider system for generating the vertical sawtooth at pin 2. The divider system has an internal frequency doubling circuit, which allows the horizontal oscillator to operate at its normal line frequency. One line period equals 2 clock pulses.
Use of the divider system avoids the requirement for vertical frequency adjustment. The divider has a discriminator window for automatic switching from 60 Hz to 50 Hz mode. When the trigger pulse comes before line 576 the 60 Hz mode is selected, otherwise the 50 Hz mode is selected.
The divider system operates with 2 different divider reset windows for maximum interference/disturbance protection.
The windows are activated via an up/down counter.
The counter increases its counter value by 1 each time the separated vertical sync pulse is within the search window. When not within the search window this value is decreased by 1.
The operating modes of the divider system are as follows:

Mode A

Large (search) window (divider ratio between 488 and 722)

This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found - not within the narrow window limits
- Up/down counter value of the divider system operating in the narrow window mode drops below count 10

Mode B

Narrow window (divider ratio between 522 to 528, 60 Hz; or 622 to 628, 50 Hz)

The divider system switches over to this mode when the up/down counter has reached its maximum value of 15 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window, the divider is reset at the end of the window and the counter value is decreased by 1. At a counter value below 10 the divider system switches over to the large window mode.

The divider system also generates an anti-topflutter pulse which inhibits the phase 1 detector during the vertical sync pulse. The pulse width is dependent on the divider mode. In Mode A the start is generated by reset of the divider.

In Mode B the anti-topflutter pulse starts at the beginning of the first equalizing pulse.

The anti-topflutter pulse ends at count 10 for the 50 Hz mode and count 12 for the 60 Hz mode.

The vertical blanking pulse is also generated via the divider system. The start is by reset of the divider while the blanking pulse width is 34 (17 lines) for the 60 Hz mode and at count 42 (21 lines) for the 50 Hz mode.

The vertical blanking pulse at the sandcastle output (pin 27) is generated by adding the anti-topflutter pulse to the blanking pulse. Thus the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in Mode B. The length of the vertical blanking in this condition is 21 lines in the 60 Hz mode and 25 lines in the 50 Hz mode.

DEVELOPMENT DATA

Application when external video signals require synchronization

The input to the sync separator is externally available via pin 25. For normal application the video output signal at pin 17 is AC coupled to this input as shown in Fig.11. It is possible to interrupt this connection and drive the sync separator from other sources such as:

- A teletext decoder in serial mode
- An external video signal via a peritelevision connector

When a teletext decoder is applied the IF amplifier and synchronization circuit are operating in the same phase which means that various connections between the two sections (i.e. AGC gating) can remain active. When external signals are applied to the sync separator the connections between the two parts must be interrupted. This can be achieved by connecting pin 22 to ground, which results in the following conditions:

- AGC detector is not gated
- AFC circuit is active
- Mute circuit not active - sound channel remains switched on
- Phase detector 1 has an optimal time constant for external video sources and is not gated.

X-ray protection

By forcing pin 1 below 1 V the horizontal output changes to a high resistance. The protection can be released by switching off the mains.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 7)	$V_P = V_{7-6}$	–	13.2	V
Total power dissipation	P_{tot}	–	2.3	W
Operating ambient temperature range	T_{amb}	−25	+65	°C
Storage temperature range	T_{stg}	−25	+150	°C

CHARACTERISTICS

$V_P = V_{7-6} = 12$ V; $T_{amb} = 25$ °C; carrier 38.9 MHz, negative modulation; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage range (pin 7)		V_{7-6}	9.5	12	13.2	V
Supply current (pin 7)	at no input	I_7	75	125	165	mA
Start current (pin 11)	note 1	I_{11}	–	6.5	9.0	mA
Start voltage horizontal oscillator		V_{11}	9.5	–	–	V
Start protection level	$I_{11} = 12$ mA	V_{11}	–	–	16.5	V
Vision IF amplifier (pins 8 and 9)						
Input sensitivity at 38.9 MHz (RMS value)	note 2	V_{8-9}	25	40	60	μV
Input sensitivity at 45.75 MHz (RMS value)	notes 2, 27	V_{8-9}	25	40	60	μV
Differential input resistance	note 3	R_{8-9}	–	1300	–	Ω
Differential input capacitance	note 3	C_{8-9}	–	5	–	pF
Gain control range		G_{8-9}	–	77	–	dB
Maximum input signal		V_{8-9}	100	170	–	mV
Output signal expansion for 48 dB variation of input signal	note 4	ΔV_{17}	–	1	–	dB
Video amplifier	note 5					
Zero signal output level	note 6	V_{17}	–	5.4	–	V
Top sync level		V_{17}	2.3	2.5	2.7	V
Video output signal amplitude	note 7	V_{17}	2.3	2.65	3.0	V
White-spot threshold level			–	5.7	–	V
White-spot insertion level			–	3.8	–	V
Video output impedance		–	–	25	–	Ω
Internal bias current of output transistor (NPN emitter follower)		$I_{17(int)}$	1.4	1.8	–	mA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Maximum source current		I_{17}	10	–	–	mA
Bandwidth of demodulated output signal		B	5	7	–	MHz
Differential gain	note 8	G_{17}	–	4	8	%
Differential phase	note 8	φ	–	2	5	deg.
Video non-linearity	note 9	NL	–	2	5	%
Intermodulation	note 10					
f = 1.1 MHz (blue)			50	60	–	dB
f = 1.1 MHz (yellow)			50	60	–	dB
f = 3.3 MHz (blue)			55	65	–	dB
f = 3.3 MHz (yellow)			55	65	–	dB
Signal-to-noise ratio	note 11					
V_i = 10 mV		S/N	50	57	–	dB
end of gain control range		S/N	50	62	–	dB
Residual carrier signal		V_{17}	–	2	10	mV
Residual 2nd harmonic of carrier signal		V_{17}	–	2	10	mV
Tuner AGC						
Minimum starting point tuner take-over (RMS value)		$V_{8\text{-}9(rms)}$	–	–	0.2	mV
Maximum starting point tuner take-over (RMS value)		$V_{8\text{-}9(rms)}$	100	150	–	mV
Maximum tuner AGC output swing	V_5 = 3 V	$I_{5(max)}$	4	–	–	mA
Output saturation voltage	I_5 = 2 mA	$V_{5(sat)}$	–	–	300	mV
Leakage current (pin 5)		I_L	–	–	1	μA
Input signal variation complete tuner control		ΔV_i	0.5	2	4	dB
Minimum voltage tuner take-over		V_1	–	–	1	V
Voltage to switch on the X-ray protection	horizontal output high resistance	V_1	–	–	0.8	V
AFC circuit						
AFC sample-and-hold/switch						
AFC switch-off current		I_{19}	0.1	–	–	mA
Output current	V_{19} = 0 V	I_{19}	–	0.1	0.3	mA
Leakage current at pin 19		I_{LO}	–	–	2	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AFC circuit (continued)						
AFC output						
AFC output voltage swing	notes 18, 19	V_{18}	10.5	–	11.5	V
Available output current		I_{18}	0.2	–	–	mA
Control steepness			–	100	–	mV /kHz
AFC output voltage with AFC off		V_{18}	5.5	6	6.5	V
AFC output resistance		R_{18}	–	40	–	kΩ
Measured with an input signal amplitude = 150 μV (RMS value)						
Output voltage swing	note 27	V_{18}	–	11	–	V
Control steepness	note 27		–	80	–	mV /kHz
Output voltage shift with respect to V_i = 10 mV (RMS value)	note 27		–	−2	–	V
Sound circuit	note 12					
Input limiting voltage	$V_{o(max)}$ = −3 dB	V_{15}	–	400	800	μV
Input resistance		R_{15}	–	2.6	–	kΩ
Input capacitance		C_{15}	–	6	–	pF
AM suppression	note 13	AMS	53	58	–	dB
AF output signal (RMS value)	note 14	$V_{12(rms)}$	400	600	800	mV
AF output signal when pin 11 is used as a starting pin or connected to V_P (RMS value)	Δf = 50 kHz	$V_{12(rms)}$	500	900	1500	mV
AF output impedance		Z_{12}	–	25	100	Ω
Total harmonic distortion	note 15	THD	–	0.5	2	%
Ripple rejection	volume control 20 dB; f_k = 100 Hz	RR	–	35	–	dB
Output voltage when muted		V_{12}	–	2.5	–	V
Output level shift due to muting	volume control −20 dB	V_{12}	–	–	0.5	V
Signal-to-noise ratio	note 16	S/N	–	47	–	dB
Voltage with pin 11 disconnected		V_{11}	–	6.0	–	V
Current with pin 11 short circuited to ground		I_{11}	–	1	–	mA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Temperature dependance of the output signal amplitude	T_{amb} = 20 °C to 65 °C; −30 dB volume control and voltage of pin 11 fixed; note 27	V_{12}	–	2.5	–	dB
Volume control	note 17; see Fig.8					
External control resistor	note 17	R_{11}	–	4.7	–	kΩ
Suppression output signal during mute condition		OSS	60	66	–	dB
Horizontal synchronization circuit	see Fig.9					
Sync separator						
Required sync pulse amplitude	note 20	V_{25}	200	750	–	mV
Input current pin 25	$V_{25} > 5$ V	I_{25}	–	8	–	μA
	$V_{25} = 0$ V	I_{25}	–	−10	–	mA
First control loop						
Holding range PLL		± Δf	–	1500	2000	Hz
Catching range PLL		± Δf	600	1500	–	Hz
Control sensitivity to oscillator	note 21			see Fig.10		
IF input signal at which the time constant is switched (RMS value)	strong to weak	V_{8-9}	–	2.2	–	mV
Second control loop						
Control sensitivity	note 22	$\Delta t_d/\Delta t_o$	–	100	–	–
Control range		t_d	–	25	–	μs
Controlled edge				positive		
Phase adjustment (via second control loop)						
Control sensitivity			–	25	–	μA/μs
Maximum allowed phase shift		α	–	±2	–	μs
Horizontal oscillator (pin 23)						
Free running frequency	R = 34.3 kΩ; C = 2.7 nF	f_{fr}	–	15625	–	Hz
Spread with fixed external components		Δf	–	–	4	%
Frequency variation	ΔV_P = 9.5 to 13.2 V	Δf_{fr}	–	–	2	%
Frequency variation with temperature	note 27	TC	–	−1.6	–	Hz/°C

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Horizontal oscillator (pin 23) (continued)						
Maximum frequency deviation at start of horizontal output		Δf_{fr}	–	–	10	%
Frequency variation when only noise is received	note 27	Δf_{fr}	–	–	500	Hz
Horizontal output						
Output limiting voltage		V_{26}	–	–	16.5	V
Output voltage LOW	I_{sink} = 10 mA	V_{26}	–	0.2	0.5	V
Maximum sink current		I_{26}	10	–	–	mA
Duty cycle output signal			–	46	–	%
Rise time of output pulse		t_r	–	260	–	ns
Fall time of output pulse		t_f	–	100	–	ns
Flyback input and sandcastle output	note 23					
Input current required during flyback pulse		I_{27}	0.1	–	2	mA
Output voltage:						
during burst key pulse		V_{27}	8	–	–	V
during horizontal blanking		V_{27}	4	4.4	5	V
during vertical blanking		V_{27}	2.1	2.5	2.9	V
Pulse width:						
burst key pulse	60 Hz	t_W	2.9	3.3	3.7	µs
burst key pulse	50 Hz	t_W	3.2	3.6	4.0	µs
horizontal blanking pulse			flyback pulse width			
Vertical blanking pulse:						
50 Hz divider in search window			–	21	–	lines
60 Hz divider in search window			–	17	–	lines
50 Hz divider in narrow window			–	25	–	lines
60 Hz divider in narrow window			–	21	–	lines
Delay between start of sync pulse at the video output and the burst key pulse						
trailing edge	60 Hz		–	–	9.3	µs
rising edge			4.7	5.4	6.1	µs

parameter	conditions	symbol	min.	typ.	max.	unit
Coincidence detector						
Voltage for:						
synchronized condition		V_{22}	–	9.8	–	V
no signal condition		V_{22}	–	1.5	–	V
Switching level to switch the phase detector from fast to slow		V_{22}	6.2	6.7	7.2	V
Hysteresis slow to fast		V_{22}	–	0.6	–	V
Switching level to activate the mute function (transmitter identification)		V_{22}	2.5	2.8	3.1	V
Hysteresis mute function		V_{22}	–	2	–	V
Delay time of mute release after transmitter insertion					300	μs
Allowable load on pin 22					10	μA
External video mode		V_{22}	–	–	0.7	V
Current at pin 22	V_{22} = 0 V	I_{22}	–	–	0.8	mA
Vertical circuit	note 25					
Vertical ramp generator						
Input current during scan		I_2	–	–	2	μA
Discharge current during retrace		I_2	–	0.8	–	mA
Sawtooth amplitude (peak-to-peak value)		$V_{2(p-p)}$	–	1.9	–	V
Interlace timing of the internal pulses			30	32	34	μs
Vertical output						
Available output current	V_3 = 4 V	I_3	–	–	3	mA
Maximum output voltage	I_3 = 0.1 mA	V_3	4.4	5	–	V
Vertical feedback input						
Input voltage						
DC component		V_4	2.9	3.3	3.7	V
AC component (peak-to-peak value)		$V_{4(p-p)}$	–	1	–	V
Input current		I_4	–	–	12	μA
Internal precorrection to sawtooth		Δt_p	–	3	–	%
Deviation amplitude	50/60 Hz		–	–	2	%
Temperature dependence of the amplitude	T_{amb} = 20 °C to 65 °C		–	–	2	%

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Vertical circuit (continued)						
Vertical guard	note 26					
Active switching level at a deviation with respect to the DC feedback level:	V_{27} = 2.5 V					
guard level LOW		ΔV_4	–	2.1	–	V
guard level HIGH		ΔV_4	–	2	–	V

Notes to the characteristics

1. Pin 11 has a double function. When during switch-on a current of 9.0 mA is supplied to this pin, it is used to start the horizontal oscillator.
   The main supply can then be obtained from the horizontal deflection stage. When no current is supplied to this pin it can be used as a volume control.
2. On set AGC.
3. The input impedance has been chosen such that a SAW-filter can be applied.
4. Measured with 0 dB = 450 μV.
5. Measured at 10 mV (RMS value) top sync input signal.
6. So-called projected zero point; i.e. with switched demodulator.
7. White 10% of the top sync amplitude.
8. Measured according to the test line illustrated by Fig.2:
   - The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   - The differential phase is defined as the difference in degrees between the largest and smallest phase angle. The differential gain and phase are measured with a DSB signal.
9. This figure is valid for the complete video signal amplitude (peak white-to-black); see Fig.3.
   The non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step.
10. The test set-up and input conditions are illustrated by Fig.4. The figures are measured at an input signal of 10 mV (RMS value).
11. Measured with a source impedance of 75 Ω.

$$\text{Signal-to-noise ratio} = 20 \log \frac{V_{\text{out black-to-white}}}{V_{n(\text{rms})} \text{ at } B = 5 \text{ MHz}}$$

12. The sound circuit is measured (unless otherwise specified) with an input signal of V_{15} of 50 mV (RMS value), a carrier frequency of 5.5 MHz at a Δf of 27.5 kHz and an AF frequency of 1 kHz. The QL of the demodulator tuned circuit is 16 and the volume control is connected to the supply. The reference circuit must be tuned in such a way that the output is symmetrical clipping at maximum volume.
13. The test set-up is illustrated by Fig.6. The AM rejection curve (typical) is illustrated by Fig.7.
14. The output signal is measured at aΔf = 7.5 kHz and maximum volume control.
15. The demodulator tuned circuit must be tuned at minimum distortion.
16. Weighted noise, measured according to; CCIR 468.
17. See also note 1. The volume can be controlled by using a potentiometer connected to ground (value 10 kΩ) or by means of a variable direct voltage. In the latter case the relatively low input impedance (pin 11) must be taken into account.

18. The AFC control voltage is obtained by multiplying the IF output signal (which is also used to drive the synchronous demodulator) with a reference carrier. This reference carrier is obtained from the demodulator tuned circuit via a 90 degree phase shift network. The IF output signal has an asymmetrical frequency spectrum with respect to the carrier frequency. To avoid problems due to this asymmetrical signal the AFC circuit is followed by a sample-and-hold circuit which samples during the sync level. As a result the AFC output voltage contains no video information. The specified control steepness is without using an external load resistor. The control steepness decreases when the AFC output is loaded with two resistors between the voltage supply and ground.
19. At very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has an asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect a notch filter can be built in to the demodulator tuned circuit. The characteristics given for weak input signals are measured without a notch circuit, with a SAW filter connected in front of the IC (input signal such that the input signal of the IC is 150 μV (RMS value).
20. The minimum value is obtained with a 1.8 kΩ series resistor connected between pin 17 and pin 25. The slicing level can be varied by changing the value of this resistor (a higher resistance results in a larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
21. Frequency control is obtained by supplying a correction current to the oscillator RC-network. This is achieved via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by:

    - short-circuit the sync separator bias network (pin 25) to the voltage supply.

    To avoid the necessity of a VCR switch, the time constant of the phase detector at strong input signals is sufficiently short to obtain a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that VCR head errors are compensated for at the beginning of the scan. During weak signal conditions (information derived from the AGC circuit) the time constant is increased to obtain a good noise immunity.
22. This figure is valid for an external load impedance of 82 kΩ connected between pin 28 and the shift adjustment potentiometer.
23. The horizontal flyback input and the sandcastle output have been combined on pin 27. The flyback pulse is clamped to a level of 4.5 V. The minimum current to drive the second control loop is 0.1 mA.
24. The functions in-sync/out-of-sync and transmitter identification have been combined on pin 22. The capacitor is charged during the sync pulse and discharged during the time difference between gating and sync pulse.
25. The vertical scan is synchronized by means of a divider system, therefore no adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and corrects the vertical amplitude.
26. To avoid screenburn due to a collapse of the vertical deflection, a continuous blanking level is inserted into the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
27. These figures are based on sampled tests.

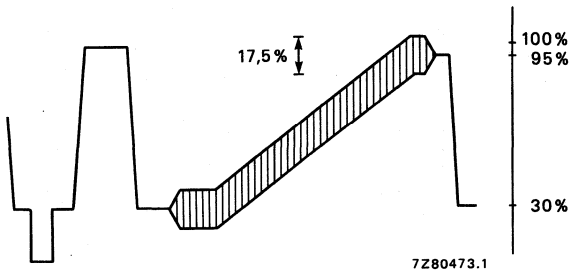


Fig.2 Video output signal.

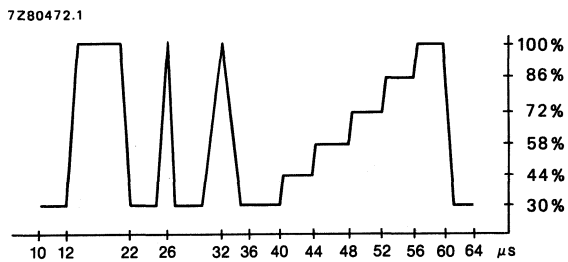
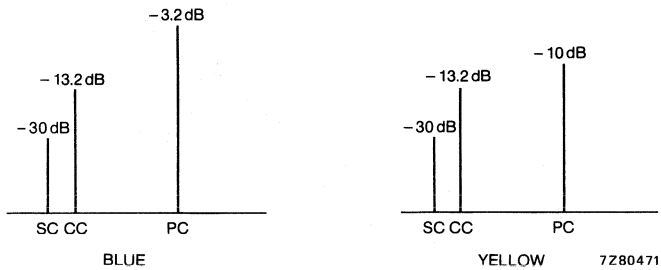


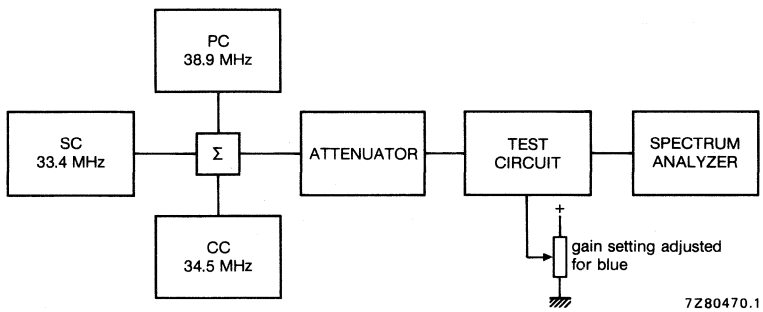
Fig.3 European Broadcasting Union (EBU) test signal waveform (line 330).



Where

SC = sound carrier
CC = chrominance carrier
PC = picture carrier
All values are with respect to the top sync level

DEVELOPMENT DATA



Where

Value at 1.1 MHz: $20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 1.1 \text{ MHz}} + 3.6 \text{ dB}$

Value at 3.3 MHz: $20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 3.3 \text{ MHz}}$

Fig.4 Test set-up intermodulation.

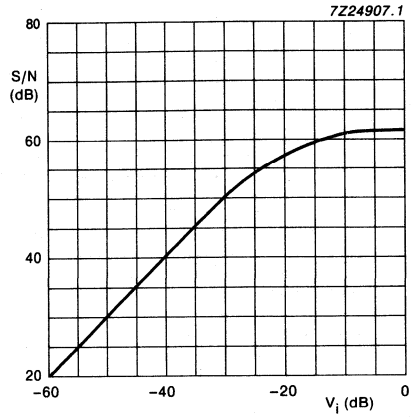


Fig.5 Signal-to-noise ratio as a function of input voltage; 0 dB = 100 mV.

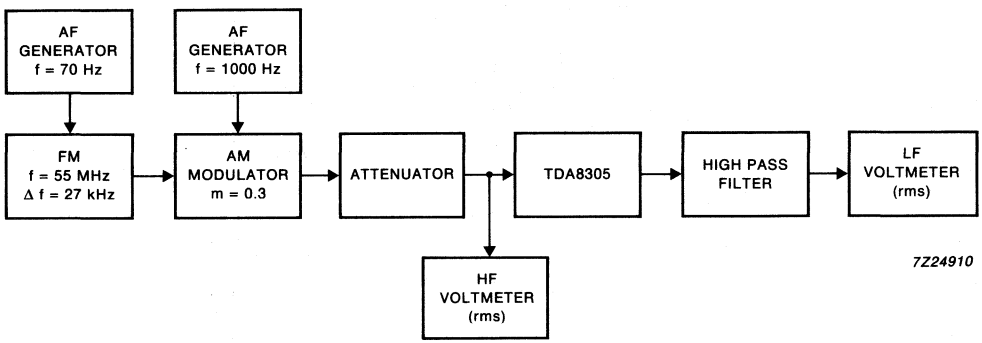


Fig.6 Test set-up AM suppression.

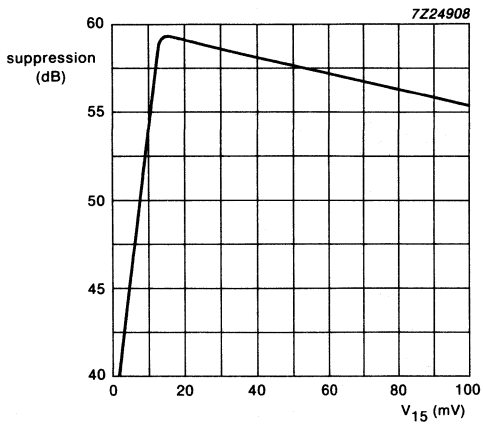


Fig.7 AM suppression.

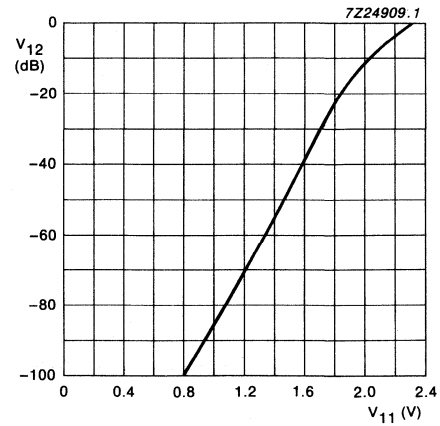
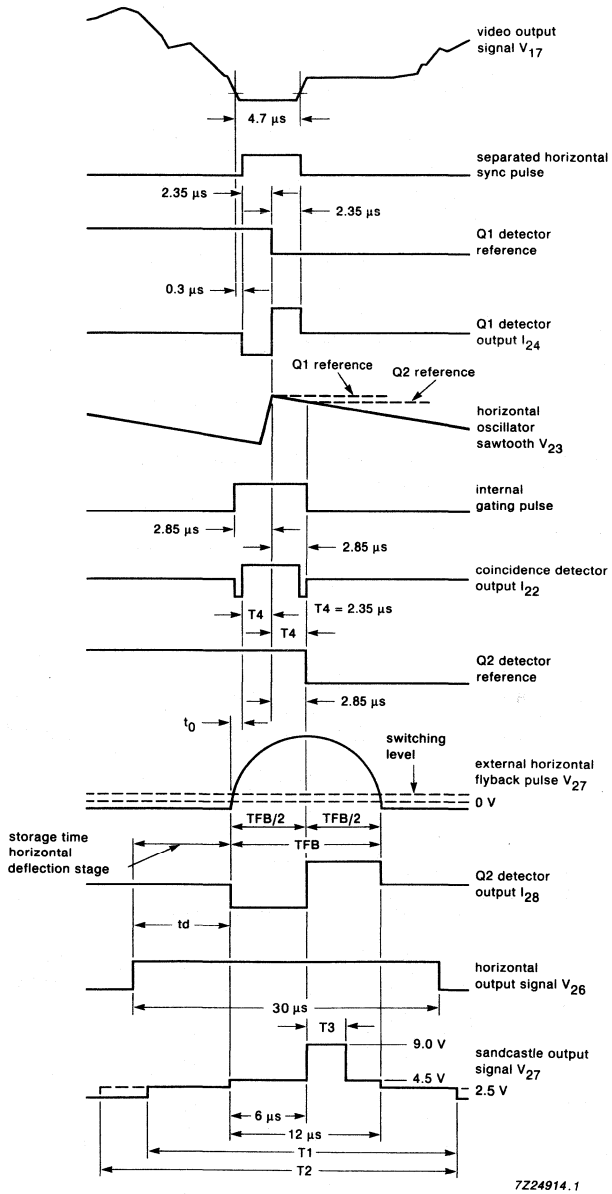


Fig.8 Volume control characteristics.

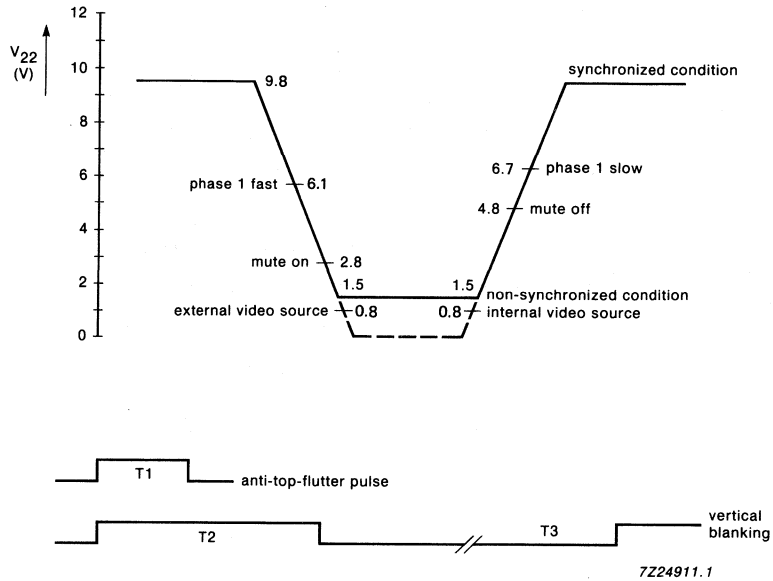
DEVELOPMENT DATA



	50 Hz	60 Hz
T1 – search window –	42P	34P
T2 – narrow window –	50P	42P
T3	3.6 µs	3.3 µs

$$P = \frac{1}{2F_H}$$

Fig.9 Timing diagram.



condition	control sensitivity horizontal oscillator		vertical sync separation pulse after
	T2 – T1	T3 = scan	
$V_{22} > 6.7$ V			
strong signal	11.3 kHz/μs	7.6 kHz/μs	16 μs
weak signal	1.3 kHz/μs	1.3 kHz/μs	16 μs
$1 < V_{22} < 5.7$ V			
strong signal	11.3 kHz/μs	7.6 kHz/μs	16 μs
weak signal	11.3 kHz/μs	7.6 kHz/μs	16 μs
$V_{22} < 0.7$ V	11.3 kHz/μs	7.6 kHz/μs	16 μs

Fig.10 Switching levels coincidence detector.

DEVELOPMENT DATA

APPLICATION INFORMATION

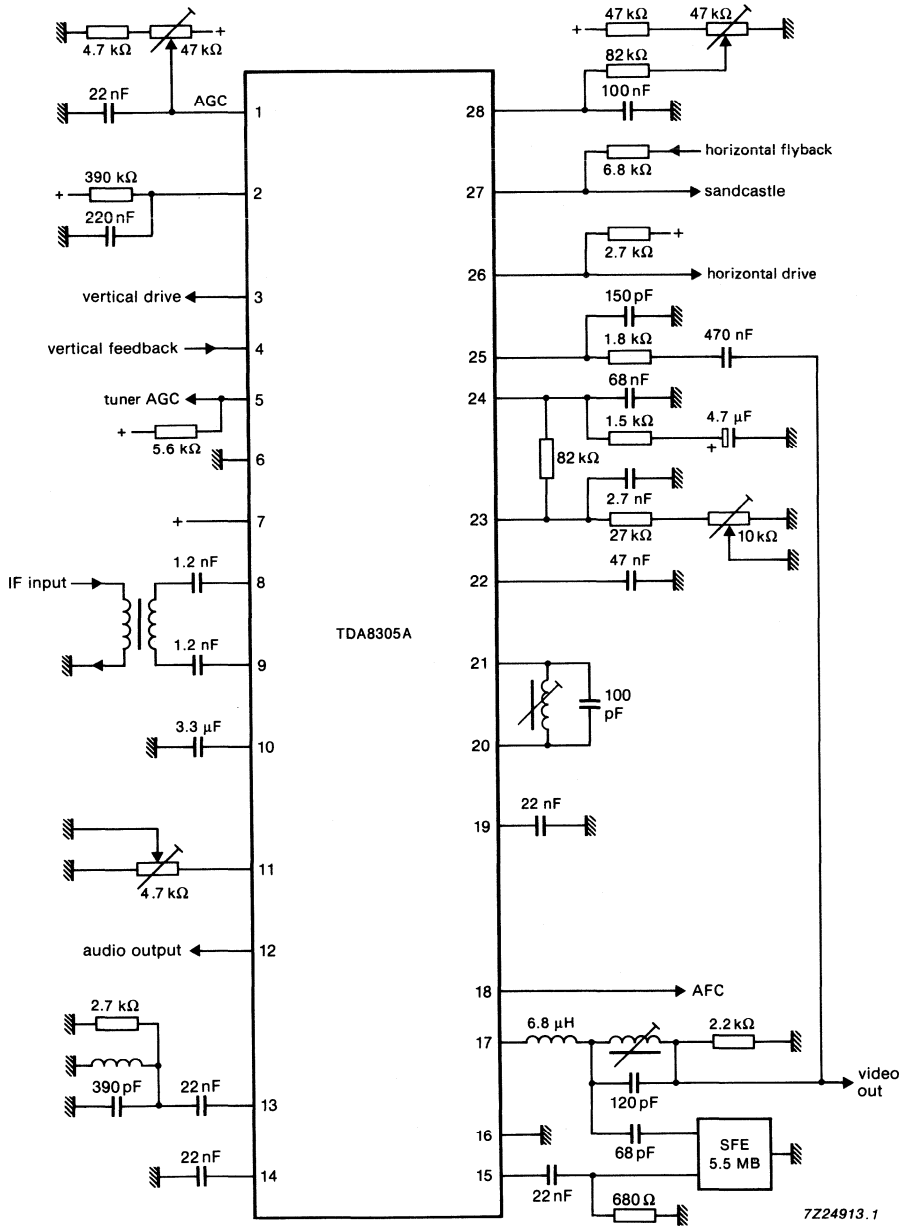


Fig.11 Application diagram.

TELEVISION IF AMPLIFIER AND DEMODULATOR

The TDA8340;Q and TDA8341;Q are integrated IF amplifier and demodulator circuits for colour or black/white television receivers, the TDA8340;Q is for application with n-p-n tuners and the TDA8341;Q for p-n-p tuners.

The TDA8340;Q and TDA8341;Q are pin-compatible successors with improved performance to types TDA2540/2541;Q and TDA3540/3541;Q.

Features

- Full range gain-controlled wide-band IF amplifier
- Linear synchronous demodulator with excellent intermodulation performance
- White spot inverter
- Wide-band video amplifier with noise protection
- AFC circuit with AFC on/off switching and sample-and-hold function
- Low impedance AFC output
- AGC circuit with noise gating
- Tuner AGC output for n-p-n tuners (TDA8340) or p-n-p tuners (TDA8341)
- External video switch for switching-off the video output
- Reduced sensitivity for high sound carriers
- Integrated filter to limit second harmonic IF signals
- Wide supply voltage range
- Requires few external components

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		$V_{CC} = V_{11-13}$	9,4	12	13,2	V
Supply current (pin 11)		I_{11}	30	42	55	mA
IF input sensitivity (r.m.s. value)		$V_{1-16(rms)}$	20	40	80	μV
IF gain control range		G_V	–	67	–	dB
Video output voltage (peak-to-peak value)	white signal; 10% top sync	$V_{12-13(p-p)}$	2,4	2,7	3,0	V
Signal-to-noise ratio	V_i = 10 mV	S/(S+N)	50	58	–	dB
AFC output voltage swing (peak-to-peak value)		$V_{5-13(p-p)}$	–	10	–	V

PACKAGE OUTLINES

TDA8340; TDA8341: 16-lead DIL; plastic (SOT38).
TDA8340Q; TDA8341Q: 16-lead QIL; plastic (SOT58).

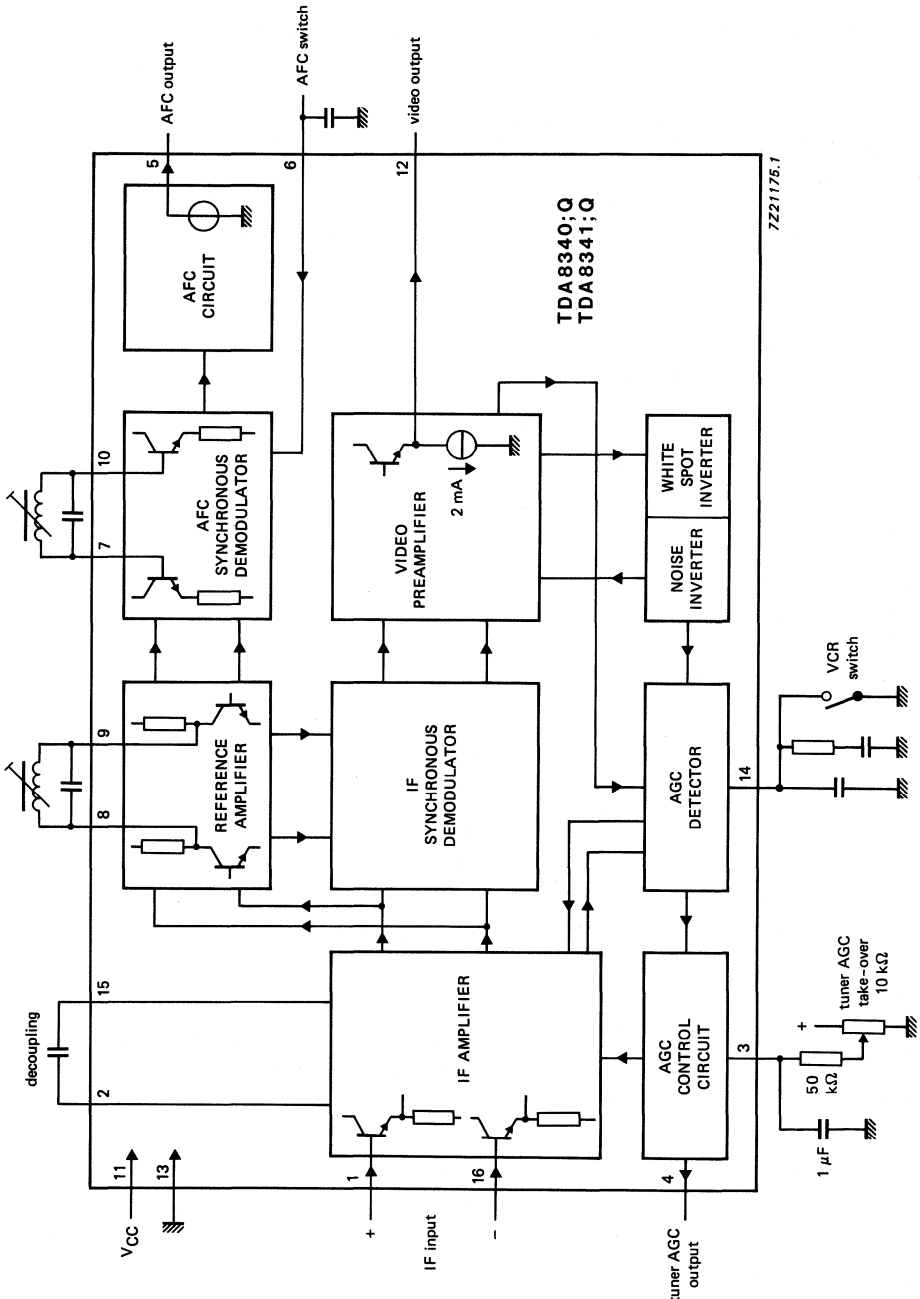


Fig. 1 Block diagram.

PINNING

1 and 16	Balanced IF inputs
2 and 15	IF amplifier decoupling
3	Tuner AGC starting point adjustment
4	Tuner AGC output
5	AFC output
6	AFC on/off switch and sample-and-hold capacitor
7 and 10	Reference carrier $\pi/2$ rad. phase shift
8 and 9	IF picture carrier passive regeneration
11	Positive supply voltage (V_{CC})
12	Video output
13	Ground (V_{EE})
14	IF AGC capacitor and VCR switch

FUNCTIONAL DESCRIPTION

IF amplifier

This is a 3-stage, gain-controlled IF amplifier with a wide dynamic range. On-chip capacitors in the d.c. feedback loop of the amplifier maintain stability at maximum gain. Internal stabilization of the supply voltage ensures the desired sensitivity and gain control range over the whole supply voltage range and also gives very good power supply ripple rejection in this part of the circuit.

Demodulator

The redesigned IF demodulator is a quasi-synchronous circuit that employs passive carrier regeneration and logarithmic clamping to give improved signal handling. The demodulator input is a.c. coupled to the IF amplifier to reduce d.c. offsets and thus minimize residual IF carrier in the output signal.

Video amplifier

The linearity and bandwith of the video amplifier are sufficient to meet all wide band requirements, e.g. for teletext transmissions. Second harmonics of the IF carrier are effectively reduced by a Sallen-Key low pass interstage filter between the demodulator output and the video amplifier input. An integrated filter in the noise inverter reduces the sensitivity of the video amplifier for high sound carriers.

White spot protection comprises a white spot clamp system combined with a delayed-action inverter which is also highly resistant to high sound carriers.

Note. To prevent radiated video output at the input pins, connect a 6,8 μH inductor in series with pin 12 and fit as close as possible to the IC body. Use short leads.

AGC dectector

A Bessel low-pass filter between the video output and the AGC detector improves the detector function in the presence of high sound carriers. No 'hang-up' occurs in the detector after pin 14 has been short-circuited to ground (VCR switch operated). The detector also generates the sample-and-hold pulse for the AFC system.

AGC control circuit

This converts the AGC detector voltage (pin 14) into a current signal which controls the gain of the IF amplifier. It also provides a tuner AGC control output from pin 4, current limiting is incorporated to prevent internal damage. The AGC starting point is adjusted via pin 3.

FUNCTIONAL DESCRIPTION (continued)

AFC circuit

The AFC circuit provides a voltage output which controls the IF frequency of the tuner. Video information on the AFC output (pin 5) is eliminated by a sample-and-hold circuit (external capacitor at pin 6). Coupling between the AFC and reference tuned circuits is via two small capacitors (or parasitic capacitance) between the respective tracks of the printed circuit board. If the capacitance is less than 1 pF, the steepness of the AFC characteristic is reduced.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 11)	$V_{CC} = V_{11-13}$	9,4	13,2	V
IF AGC voltage/VCR switch	V_{14-13}	–	13,2	V
Tuner AGC voltage	V_{4-13}	–	12	V
AFC switch voltage	V_{6-13}	–	13,2	V
Maximum voltage level with VCR switch active	V_{12-13}	–	5,0	V
DC current at video output	I_{12}	–	10	mA
DC current at AFC output	I_5	–	10	mA
Total power dissipation	P_{tot}	–	1,2	W
Storage temperature range	T_{stg}	–55	+150	°C
Operating ambient temperature	T_{amb}	–25	+70	°C

CHARACTERISTICS

Measured in circuit of Fig. 3; V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		$V_{CC} = V_{11-13}$	9,4	12	13,2	V
Supply current	no input signal	I_{11}	30	42	55	mA
IF amplifier (note 1)						
Input sensitivity	at onset of AGC	V_{1-16}	20	40	80	μV
Differential input resistance		R_{1-16}	–	2	–	kΩ
Differential input capacitance		C_{1-16}	–	3	–	pF
Gain control range		G_v	–	67	–	dB
Input signal variation	note 2	V_{12-13}	–	–	0,5	dB
Maximum input signal		V_{1-16}	100	–	–	mV
Tuner AGC (note 1)						
Tuner AGC starting point (note 3)	R_{3-11} = 39 kΩ	V_{1-16}	–	–	3	mV
	R_{3-13} = 39 kΩ	V_{1-16}	70	–	–	mV
Maximum current swing of tuner AGC output		I_4	10	–	–	mA
Input signal variation	note 4; I_4 = 1 to 9 mA	V_{1-16}	–	–	3	dB
Output saturation voltage	I_4 = 7 mA	V_{4-13}	–	200	300	mV
Leakage current	V_4 = 12 V	I_4	–	–	1	μA
Video output (note 4)						
Zero-signal output level	note 5	V_{12-13}	5,7	6,0	6,3	V
Top sync output level		V_{12-13}	2,8	3,0	3,2	V
Video output voltage (peak-to-peak value)	white signal; 10% top sync	$V_{12-13(p-p)}$	2,4	2,7	3,0	V
Internal bias current of emitter follower output transistor			1,4	2,2	3,0	mA
Output impedance		Z_{12}	–	100	–	Ω
Bandwith of demodulated output signal		B	6	7,5	–	MHz
Differential gain	note 6	G_d	–	2	5	%
Differential phase	note 6	φ_d	–	2	5	deg
Luminance non-linearity	note 7		–	2	5	%
Residual carrier signal (r.m.s. value)	note 8	$V_{12-13(rms)}$	–	2	10	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Video output (continued)						
Residual 2nd harmonic of carrier signal (r.m.s. value)	note 8	$V_{12\text{-}13(rms}$	–	2	10	mV
Variation of video voltage for ΔV_{CC} = 1 V		$\frac{\Delta V_{12\text{-}13(p\text{-}p)}}{\Delta V_{11\text{-}13}}$	0,1	0,2	0,3	
Intermodulation	notes 8 and 9;					
	1,1 MHz, blue	α	–	–65	–60	dB
	1,1 MHz, yellow	α	–	–60	–56	dB
	3,3 MHz	α	–	–	–68	dB
Signal-to-noise ratio	note 10;					
	V_i = 10 mV	S/(S+N)	50	58	–	dB
	max. gain	S/(S+N)	54	61	–	dB
Spot inverter (note 11)						
Threshold level		$V_{12\text{-}13}$	6,3	6,8	7,3	V
Insertion level		$V_{12\text{-}13}$	4,2	4,5	4,8	V
Noise inverter (note 11)						
Threshold level		$V_{12\text{-}13}$	1,6	1,8	2,0	V
Insertion level		$V_{12\text{-}13}$	3,5	3,8	4,1	V
VCR switch						
Level below which video output switches off		$V_{14\text{-}13}$	1,8	2,2	2,6	V
Switch current	$V_{12\text{-}13}$ = 0,7 V	$-I_{14}$	40	60	100	μA
AFC circuit (note 12)						
Output voltage swing (peak-to-peak value)		$V_{5\text{-}13(p\text{-}p)}$	–	10	–	V
Change of frequency for an AFC output voltage swing of 10 V		Δf	–	60	120	kHz
AFC output voltage	at f = 38,9 MHz	$V_{5\text{-}13}$	–	6	–	V
	no input signal	$V_{5\text{-}13}$	2	6	10	V
	during AFC off	$V_{5\text{-}13}$	5	6	7	V
AFC output resistance		$R_{5\text{-}13}$	–	500	–	Ω
AFC switch: level below which AFC output switches off		$V_{6\text{-}13}$	1,4	2,0	2,8	V
AFC switch current	during AFC on	I_6	–	200	500	μA
Max. AFC switch current	during AFC off; $V_{6\text{-}13}$ = 0 V	I_6	–	–	5	mA

Notes to the characteristics

1. All input signals are measured r.m.s. at top sync and 38,9 MHz.
2. Measured with 0 dB = 200 μV.
3. Tuner AGC starting point is defined as 'level of input signal when tuner AGC current = 1 mA'.
4. Measured with pin 3 connected via 39 kΩ resistor to V_{CC} (pin 11), with an r.m.s. voltage of 10 mV top sync input signal and with pin 12 not loaded.
5. At the 'projected zero point', e.g. with switched demodulator.
6. Measured in the circuit of Fig. 7:

   the differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level;

   the differential phase is defined as 'the difference (in degrees) between the largest and smallest phase angles'.
7. Measured according to the test line shown in Fig. 9:

   the non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step;

   the mean step is (white level — black level) divided by the number of steps.
8. Measured up to 45 dB gain control.
9. Test set-up and input conditions for intermodulation measurements as in Figs 6 and 7.
10. Measured with a 75 Ω source:

    $$S/(S+N) = 20 \log \frac{V_{\text{out black to white}}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}.$$
11. Video output waveform showing white spot and noise inverter threshold levels.
12. Measured with input signal $V_{1\text{-}16}$ = 10 mV and with no load at AFC output.

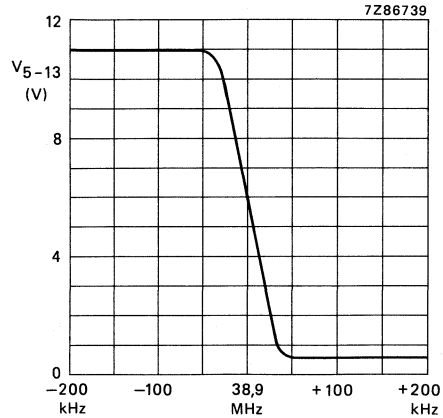


Fig. 2 AFC output voltage as a function of frequency.

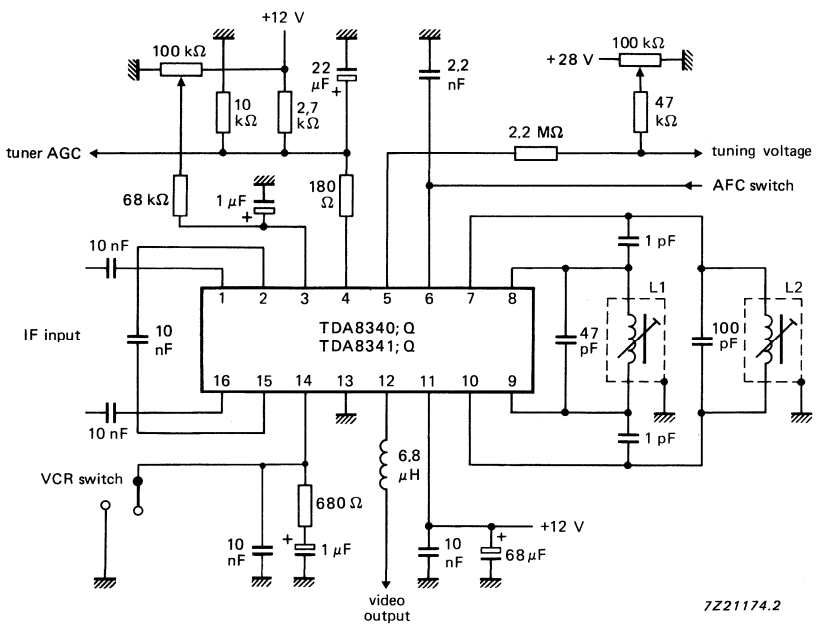


Fig. 3 Typical application circuit diagram;
Q of L1 and L2 = 80; f_o = 38,9 MHz.

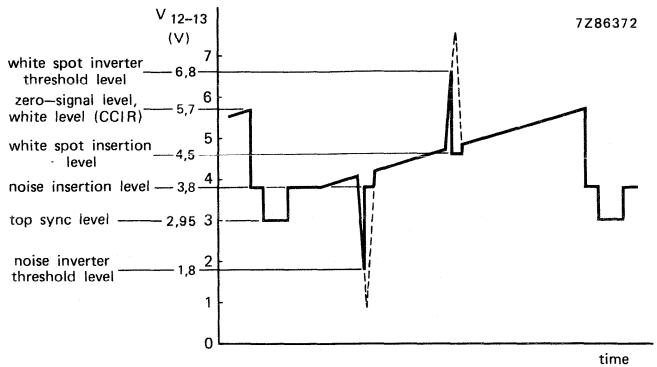


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

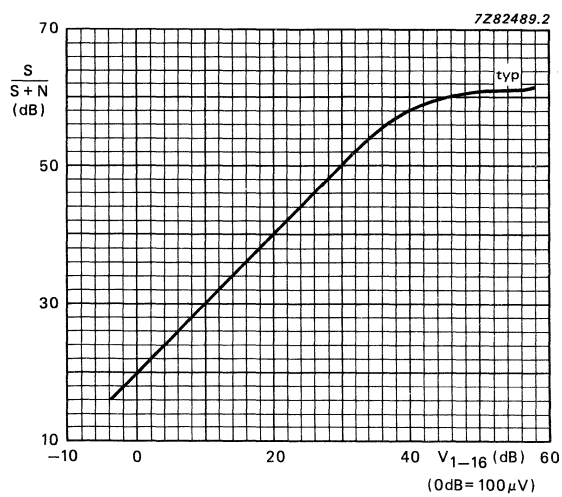
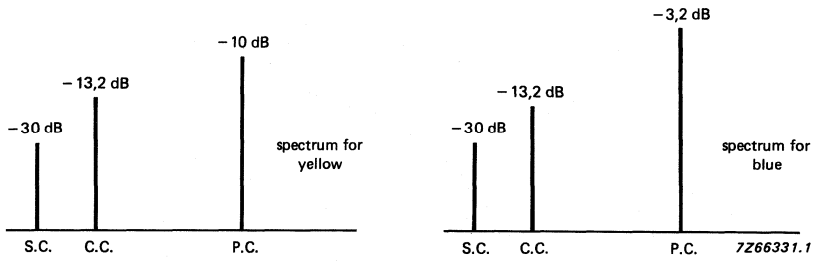


Fig. 5 Signal-to-noise ratio as a function of input voltage.



S.C.: sound carrier level
C.C.: chrominance carrier level
P.C.: picture carrier level
} with respect to top sync level

Fig. 6 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

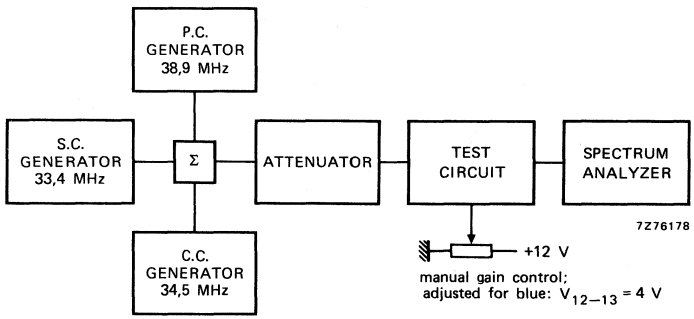


Fig. 7 Test set-up for intermodulation measurements.

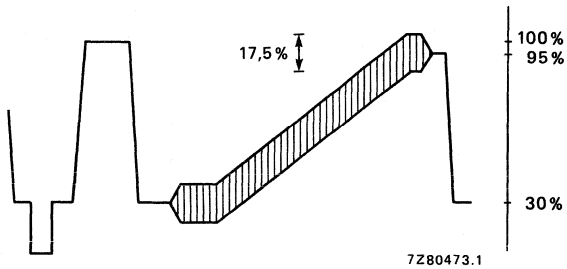


Fig. 8 Video output signal.

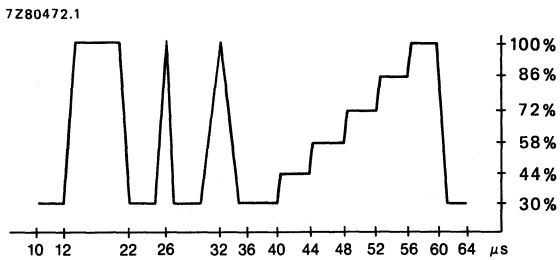


Fig. 9 E.B.U. test signal waveform (line 330).

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	February 1991

TDA8349A

Multistandard IF amplifier and demodulator

GENERAL DESCRIPTION

The TDA8349A is a multistandard IF amplifier and demodulator with AGC and AFC functions for television receivers. The device has a video recognition circuit and a video switch for internal or external video for full SCART applications.

FEATURES

- Full range gain-controlled wide-band IF amplifier up to 60 MHz
- Wide-band video amplifier with good linearity and a class AB output stage to ensure a very low output impedance
- Supply independent video output level
- Small second harmonic IF output
- AGC circuit which operates on top sync level (negative modulation) or on white level (positive modulation) or on top level (MAC) with reduced sensitivity for high sound carriers
- AFC circuit with an internal 90° phase shift circuit, a sample-and-hold circuit for negatively modulated signals to reduce video dependent AFC information and an analog or digital output
- Video recognition possibility based on horizontal pulse duty cycles
- Video switch for selection of internal or external video signals
- Wide supply voltage range and ripple rejection
- Requires few external components
- Tuner AGC output for npn and pnp tuners

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{14-17}	supply voltage (pin 14)		10.2	12	13.2	V
I_{14}	supply current (pin 14)	V_i = 10 mV	40	55	65	mA
$V_{1-2(RMS)}$	IF input sensitivity (RMS value)		-	50	80	µV
G_v	IF gain control range		66	72	-	dB
$V_{11-17(p-p)}$	video output voltage (peak-to-peak value)		1.7	1.9	2.1	V
S/N	signal-to-noise ratio	V_i = 10 mV	54	61	-	dB
$V_{8-17(p-p)}$	AFC output voltage swing (peak-to-peak value)		10	-	11	V

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8349A	20	DIL	plastic	SOT146

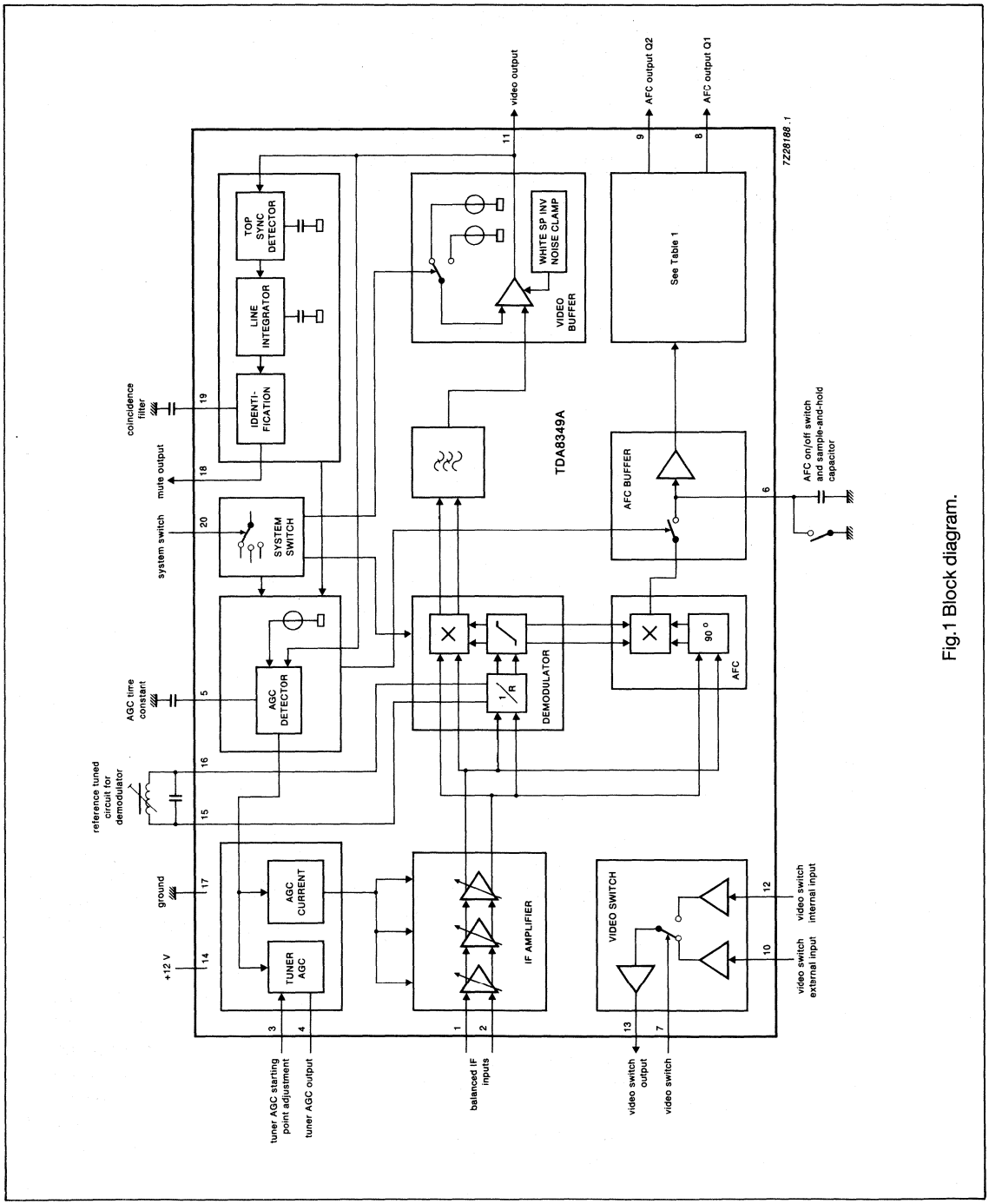


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1,2	balanced IF inputs
3	tuner AGC starting point adjustment
4	tuner AGC output
5	AGC time constant
6	AFC on/off switch and sample-and-hold capacitor
7	video switch
8	AFC output Q1
9	AFC output Q2
10	video switch external input
11	video output
12	video switch internal input
13	video switch output
14	positive supply voltage
15,16	reference tuned circuit for demodulator
17	ground
18	mute output
19	coincidence filter
20	system switch

FUNCTIONAL DESCRIPTION

General

The IC consists of the following parts as illustrated in Fig.1:

- Gain controlled video IF amplifier
- Quasi-synchronous demodulator
- Video amplifier/buffer with white spot clamp/inverter and noise clamp
- AGC circuit which operates either on top sync level (negative modulation) or on white level (positive modulation) or on top level (MAC)
- AFC circuit with sample-and-hold circuit for negatively modulated signals, on/off switch and a digital or analog output (switchable)
- Circuit for switching between positive and negative modulation
- Video recognition circuit for sound muting and tuning indication
- Video switch which facilitates selection between two different video signals, with different gain settings

IF amplifier

The IF amplifier consists of three AC coupled differential gain stages with adjustable feedback in the emitter. The AC coupling allows simple biasing, cascades can be used and no DC feedback is required. This provides a control range above 70 dB with good linearity. The minimum input signal to obtain the nominal output amplitude is 50 μV RMS.

Demodulator

The demodulator is a quasi-synchronous circuit that employs passive carrier regeneration and a tuned circuit for selectivity. The regenerated carrier signal is limited by a clamping circuit before it is fed to the demodulator. Switching between positive and negative modulation is achieved by the system switch which provides currents to the demodulator in a positive or negative direction.

Video amplifier

The video amplifier based on the feedback principle improves the linearity of the video output buffer. It has an internal bandgap reference to ensure a stable video output at different supply voltages and temperatures. This bandgap also reduces the supply ripple on the video output to values less than −30 dB. The video amplifier has a typical bandwidth of 10 MHz which allows application for all new video standards with bandwidths of up to 10 to 12 MHz. The video output signal has an amplitude of 2 V (p-p).

White spot protection comprises a white spot clamp system combined with a delayed-action inverter which is also highly resistant to high sound carriers. A switchable DC shift for positively modulated IF signals ensures correct signal handling. This switching is obtained via pin 20, which is the same pin used for switching the demodulation polarity in the demodulator.
The circuit also has a noise clamp which prevents the video output becoming less than ±400 mV below the top sync level at noise peaks.
The output buffer of the video amplifier consists of a class A/B circuit which can handle large source as well as large sink currents. This makes the circuit more flexible in several applications with one or more ceramic filters connected to this output buffer.

AGC control circuit

This converts the AGC detector voltage (pin 5) into a current signal which controls the gain of the IF amplifier. It also provides a tuner AGC control output from pin 4, current limiting is incorporated to prevent internal damage. The AGC starting point is adjusted by a voltage between 3 and 5 V for pnp tuners and between 7 and 9 V for npn tuners via pin 3.

AGC circuit

A new AGC system has been designed for the AGC. It will be a top sync-detector for negatively modulated signals and a top white level AGC for positively modulated signals.
For optimal flexibility reasons the load and unload currents of the AGC are chosen such that both, a relatively fast set, as well as a set with a low tilt are possible for positive (L) and negative (B/G) modulated signals. For this reason a tilt ratio between positive (L) and negative (B/G) of approximately 3:1 has been chosen. This means that in a fast set the choice of a typical tilt for negatively modulated signals of 2% will obtain a typical tilt for positively modulated signals (L) of 6%. For a digital set which requires a small tilt the choice of tilt can be a factor of 5 or 10 smaller by increasing the AGC capacitor.

The chosen AGC currents:

MODE	UNLOAD CURRENT	LOAD CURRENT	TILT AT 2.2 μF
B/G	50 μA	1.5 mA	typ. 0.5% (line tilt)
L	500 nA*	1.5 mA	typ. 1.5% (field tilt)
MAC(positive)	200 nA	1.5 mA	typ. 1.2% (frame tilt)
MAC(negative)	500 nA	1.5 mA	typ. 1.5% (field tilt)

Switching between the first three modes can be achieved by the system switch. This is a 3-level switch which when grounded selects B/G; open or 5 V selects L, and with pin 20 connected to V_{CC} selects positively modulated MAC. The IC operates in a fourth mode if the identification capacitor at pin 19 is connected to V_{CC}, it can be used for negatively modulated MAC.
During channel switching a situation can occur that requires the AGC to increase the gain more than for example 50 dB. If this increase of gain has to be done for a positively modulated (L) signal, it will be achieved by the 500 nA load current and is therefore extremely slow. Because the identification information can be used to indicate that the signal is too small, in this event the identification circuit will mute, it is possible to increase the positive unload current to the same value as that used for negatively modulated signals. This switching is fully automatic and cannot be switched off.

AFC circuit

The AFC circuit consists of a demodulator stage which is fed with signals 90°out of phase. A very accurate internally realized 90° phase shift circuit makes it possible to use the demodulator IF regenerator tuned circuit for tuning the AFC circuit. To prevent video ripple on the AFC output voltage a sample-and-hold circuit is used for negatively modulated signals. The output signal of the demodulator is sampled during

* As long as no signal has been identified by the identification detector the unload current will be 50 μA.

sync level of the video signal and will be stored with the aid of an external capacitor. This sample-and-hold circuit is not used in the L mode, but it will function as a low-pass filter in this mode and therefore also reduces the video dependency of the AFC. A gain stage amplifies the voltage swing by 5 times. The output of the AFC circuit will be an inverse analog output on pin 8 when pin 9 is connected to a voltage above 8 V. If pin 9 is connected to a voltage above 10 V the output will be a normal analog output. Normally pins 8 and 9 together provide digital AFC information.

Video recognition circuit

For full scart functions it is necessary to implement a second mute function for non-video signals in the whole television concept. This is realized in this IF-IC. With an internal sync separator and an internal integrator it is possible to achieve a very sensitive identification circuit, which measures the mean frequency of the input signal. This is normally approximately 16 kHz. The integrator capacitor will be loaded during the whole line time and unloaded during the sync pulse. The maximum voltage at this internal capacitor is a value for the main frequency of the video signal. By changing the value of an external capacitor it is possible to influence the speed and sensitivity of the recognition circuit. It is possible to gain sensitivity performance at disturbed signals by increasing the value of the external capacitor, however this will reduce the speed of the identification circuit.

Video switch circuit

The video switch also provides application for full SCART functions. The circuit has two inputs, one output and a control pin. The switch selects either internal or external video signals. A x 2 gain stage for the external input provides an equal output level for internal or external video from the SCART. The crosstalk of the unwanted signal is better than –50 dB and the total signal handling meets all the requirements for SCART specifications.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{14-17}	supply voltage (pin 14)	–0.5	13.2	V
P_{tot}	total power dissipation	-	1.2	W
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	–25	+ 75	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; carrier frequency 38.9 MHz; negative modulation; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
supply						
V_{14-17}	supply voltage (pin 14)		10.2	12	13.2	V
I_{14}	supply current	V_i = 10 mV	40	55	65	mA
IF amplifier (note 1)						
V_{1-2}	input sensitivity	note 2	-	50	80	µV
R_{1-2}	differential input resistance	note 3	-	2	-	kΩ
C_{1-2}	differential input capacitance	note 3	-	2	-	pF
ΔG_{1-2}	gain control range		66	72	-	dB
ΔV_{11}	output signal for 50 dB input signal variation	note 4	-	0.5	-	dB
V_{1-2}	maximum input signal		100	-	-	mV
f_{1-2}	maximum operating frequency		60	-	-	MHz
Video output (note 5)						
	zero signal output level	note 6				
V_{11}	negative modulation		-	4.75	-	V
V_{11}	positive modulation		-	2.65	-	V
V_{11}	top sync level (top sync AGC)	note 7	-	2.7	-	V
V_{11}	white level (white level AGC)	note 8	-	4.6	-	V
$V_{11(p-p)}$	amplitude of video output signal (peak-to-peak value)		1.7	1.9	2.1	V
V_{11}	amplitude difference (positive/negative)		-	0	10	%
V_{11}	video output voltage variation	ΔV_P = 1 V	-	−30	-	dB
V_{11}	white spot threshold level	see Fig.3	-	5.6	-	V
V_{11}	white spot insertion level	see Fig.3	-	3.8	-	V
V_{11}	noise clamping level	see Fig.3	-	2.3	-	V
Z_{11}	output impedance		-	-	10	Ω
I_{11}	maximum sink current		5	-	10	mA
I_{11}	maximum source current		5	-	10	mA
B_{11}	bandwidth of demodulated output signal		7.5	10.0	-	MHz
G_d	differential gain	note 9	-	2	-	%
φ_d	differential phase	note 9	-	7	-	deg
Y_{nl}	luminance non-linearity	note 10	-	2	5	%
	intermodulation	see Figs 6 and 7				
α	1.1 MHz blue		-	−66	-	dB
α	1.1 MHz yellow		-	−60	-	dB
α	3.3 MHz blue		-	−60	-	dB
α	3.3 MHz yellow		-	−60	-	dB
	signal-to-noise ratio	note 11				
S/N		V_i = 10 mV	54	61	-	dB
S/N		minimum gain	60	66	-	dB
$V_{1(rms)}$	residual carrier signal (RMS value)		-	10	20	mV
$V_{11(rms)}$	residual 2nd harmonic of carrier signal (RMS value)		-	3	10	mV
System switch (note 12)						
V_{20}	maximum voltage for mode B/G		1.4	-	-	V
I_{20}	input current	V_{20} = 0 V	-	−300	-	µA
V_{20}	minimum voltage for mode L		-	-	3	V
V_{20}	maximum voltage for mode L		7	-	-	V
I_{20}	input current	3 V ≤ pin 20 ≤ 7 V	−150	-	250	µA
V_{20}	minimum voltage for MAC (positive)		-	-	9.5	V
I_{20}	input current	V_{20} = Vp	-	500	-	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AGC control circuit						
t_{11}	response to an amplitude increase of 52 dB of the IF input with the AGC switched to mode B/G	note 13	-	2	-	ms
t_{11}	response to an amplitude decrease of 52 dB of the IF input with the AGC switched to mode B/G	note 14	-	25	-	ms
	allowed leakage current of the AGC capacitor					
I_5	top sync level AGC		-	10	-	μA
I_5	white level AGC		-	200	-	nA
I_5	positive MAC AGC		-	50	-	nA
I_5	negative MAC AGC		-	200	-	nA
Tuner AGC (note 15)						
	input voltage for tuner AGC starting point					
V_3	IF input = 200 μV; negative slope		3.0	3.5	-	V
V_3	IF input = 100 mV; negative slope		-	5.0	5.5	V
V_3	IF input = 200 μV; positive slope		7.0	7.5	-	V
V_3	IF input = 100 mV; positive slope		-	9.0	9.5	V
I_4	maximum current swing of tuner AGC output		3	5	-	mA
V_4	output saturation voltage	I_4 = 2 mA	-	-	300	mV
I_4	leakage current		-	-	1	μA
ΔV_i	input signal variation complete tuner control		0.5	2.0	4.0	dB
V_3	minimum tuner take over voltage		-	-	1	V
Video switching circuit						
EXTERNAL VIDEO INPUT (AC coupled)						
$V_{10(p-p)}$	input signal voltage (peak-to-peak value)	V_O = 2 V(p-p)	-	1.0	-	V
I_{10}	input current		-	3.5	-	μA
V_{10}	top sync clamping level	I_{10} = 1 mA	-	3.3	-	V
INTERNAL VIDEO INPUT (DC coupled)						
$V_{12(p-p)}$	input signal voltage (peak-to-peak value)	V_O = 2 V(p-p)	-	2.0	-	V
$\lvert Z_{12} \rvert$	input impedance		-	2.0	-	kΩ
V_{12}	black level input voltage		-	3.3	-	V
VIDEO OUTPUT						
$V_{13(p-p)}$	output signal voltage (peak-to-peak value)		-	2.0	-	V
V_{13}	top sync level		-	2.7	-	V
V_{13}	noise clamping voltage level	I_{13} = 1 mA	-	2.5	-	V
I_{13}	internal bias current of npn emitter follower output transistor		-	1.5	-	mA
I_{13}	maximum source current		5	-	10	mA
B_{13}	bandwidth of output signal		-	5	-	MHz
	crosstalk of video signal	note 16				
α	external to internal		-	60	55	dB
α	internal to external		-	55	50	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIDEO SWITCH INPUT (note 17)						
V_7	maximum voltage for external video signal		-	-	2	V
V_7	minimum voltage for internal video signal		1	-	-	V
I_7	minimum source current for internal video signal		-	-	300	µA
I_7	input current	$V_7 = 0$ V	-	-	–1	mA
I_7	input current	$V_7 = V_P$	-	-	3	µA
AFC circuit (note 18)						
AFC SAMPLE-AND-HOLD/SWITCH (note 19)						
I_6	AFC switch: current level below which AFC outputs switches off		-	-	–500	µA
I_6	maximum AFC switch current	$V_6 = 0$ V	-	-	–1	mA
I_6	maximum leakage current		-	-	1	µA
AFC ANALOG OUTPUT ($V_9 > 8$ V; see Figs 4 and 5)						
$V_{8(p-p)}$	output voltage swing (peak-to-peak value)		10	-	11	V
I_8	maximum output current		500	-	-	µA
	control steepness		60	75	100	mV/kHz
V_8	AFC output voltage	AFC off	5	6	7	V
AFC DIGITAL OUTPUT (see Table 1)						
$V_{8,9}$	output voltage LOW		-	-	0.5	V
$V_{8,9}$	output voltage HIGH	50 kΩ load	4.5	-	5.5	V
Δf	frequency swing for switching AFC output Q1		65	80	100	kHz
$I_{8,9}$	maximum allowable output current		500	-	-	µA
AFC Analog SWITCH (note 20)						
I_9	minimum sink current for analog AFC		-	-	1.5	mA
V_9	minimum voltage for negative slope		-	-	10.2	V
V_9	minimum voltage for positive slope		-	-	8.0	V
V_9	maximum voltage for positive slope		10.2	-	-	V
I_9	output current	$V_9 = V_P$	-	500	-	µA
I_9	output current	$V_9 = 8$ to 10 V	-	150	-	µA
Video transmitter identification output (note 21)						
V_{18}	output voltage active	no sync; $I_{18} = 1$ mA	-	0.3	0.5	V
I_{18}	output current inactive	sync	-	-	3	µA
t_d	delay time of mute release after sync insertion		-	-	10	ms
I_{19}	allowed leakage current of identification detector capacitor		-	-	50	nA

Notes to the characteristics

1. All input signals are measured in RMS values at 100% carrier level and a frequency of 38.9 MHz.
2. On set AGC.
3. Input impedance selected so that a SAW filter can be applied without extra components.
4. Measured with 0 dB = 200 μV.
5. Measured at 10 mV(RMS) top sync input signal and the video output unloaded.
6. Projected zero point with internally switched demodulator.
7. With the AGC switch switched to ground, for the B/G standard, or with the identification capacitor switched to V_{CC} for the negative MAC standard.
8. With the AGC switch switched open for the L standard, or switched to V_{CC} for the positive MAC standard.
9. Measured in accordance with the test line given in Fig.8.
   - The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   - The differential phase is defined as the difference in degrees between the phase angle of the 4.4 MHz signal at 20% and 80% luminance signal.
10. Measured in accordance with the test line shown in Fig.9.
    - The non-linearity is measured by comparing the differences between adjacent pairs of six luminance levels that make up the 5 step staircase. The measurement result is the largest percentage deviation in adjacent step values. The sign is always positive.
11. Measured with a 75 Ω source:

$$S/N = 20 \log \frac{V_{o\ \text{black-to white}}}{V_{n\ (RMS)\ \text{at}\ B = 5\ MHz}}$$

12. The internal circuit of pin 20 behaves as an internal voltage source of 4.5 V with an input resistance of 15 kΩ. Using the system switch three conditions can be obtained:
    - Negative modulation with top sync level AGC. This is achieved with pin 20 connected to ground.
    - Positive modulation with white level AGC. This is achieved with pin 20 open, or connected to 5 V.
    - Positive modulation with top white AGC and an increased time constant for MAC signals. This is achieved with pin 20 connected to V_{CC}.
13. Measured with a capacitor of 2.2 μF connected to pin 5. A step is made from 200 μV to 80 mV input signals.
14. Measured with a capacitor of 2.2 μF connected to pin 5. A step is made from 80 mV to 200 μV input signals.
15. It is possible to adjust the tuner AGC over the whole AGC range of the IF amplifier for both pnp and npn tuners. Tuner AGC starting point is defined as an output current of 0.2 mA for pnp and 1.8 mA for npn, in an application with a resistance of 6 kΩ to V_P at pin 4.
16. Crosstalk is defined as:

$$20 \log \frac{V_o\ \text{unwanted video black-to-white}}{V_o\ \text{wanted video black-to-white}} \quad \text{measured at 4.4 MHz}$$

17. The video switch is controlled by a voltage on pin 7. The switching level is approximately 1.4 V. With pin 7 open-circuit internal video is selected; with pin 7 pulled to ground external video is selected.
18. Measurement taken with an input 10 mV(RMS). The unloaded Q factor of the reference tuned circuit is 70.
19. Switching off the AFC is obtained by a voltage of less than 2 V on pin 6. Normally this is achieved by pulling pin 6 to ground.

Notes to the characteristics (continued)

20. Switching to the normal analog AFC mode can be done by pulling pin 9 to a voltage above 10.2 V. Normally this is achieved by pulling pin 9 to V_P.
    The inverse analog AFC mode can only be obtained by a voltage of between 8 and 10 V applied to pin 9.
21. All timing figures defined with a capacitor of 2.2 nF at pin 19. The identification can be speeded up by lowering the value of this capacitor, however this makes the circuit also less sensitive if the video signal is disturbed (airplane flutter etc.). If the identification is only used as a sound mute a capacitor of 47 nF is recommended to improve the sensitivity.

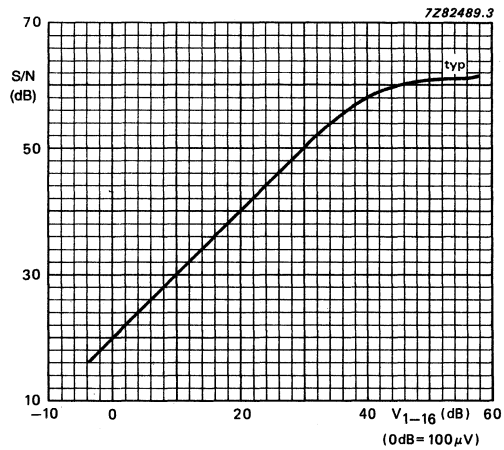


Fig.2 Signal-to-noise ratio as a function of video input.

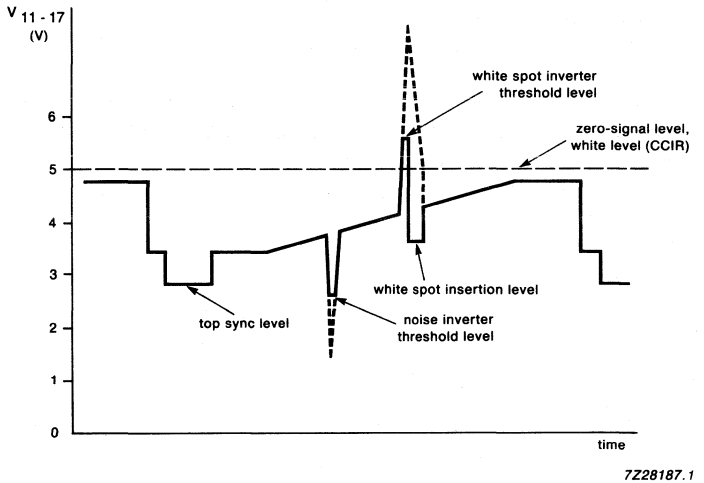


Fig.3 Video waveform showing white spot threshold and insertion levels, and noise clamping level.

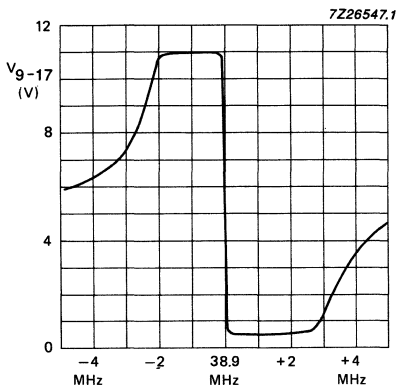


Fig.4 Analog AFC output voltage as a function of frequency pin 9 above 10 V.

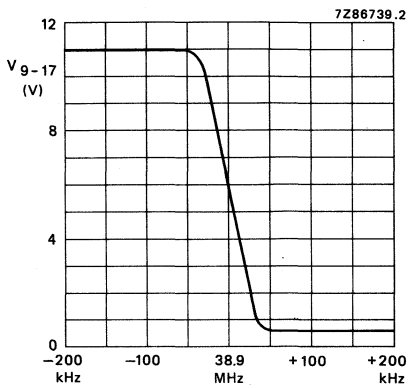
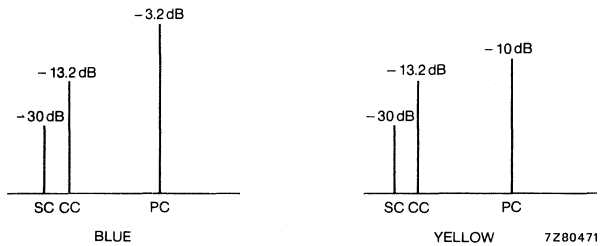


Fig.5 Analog AFC output voltage as a function of frequency pin 9 above 10 V.

Table 1 Digital AFC truth table

INPUT FREQUENCY	Q1	Q2
> IF +40 kHz	0	1
> IF	1	1
< IF	1	0
< IF –40 kHz	0	0



SC = sound carrier
CC = chrominance carrier
PC = picture carrier

all with respect to top sync level

Fig.6 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

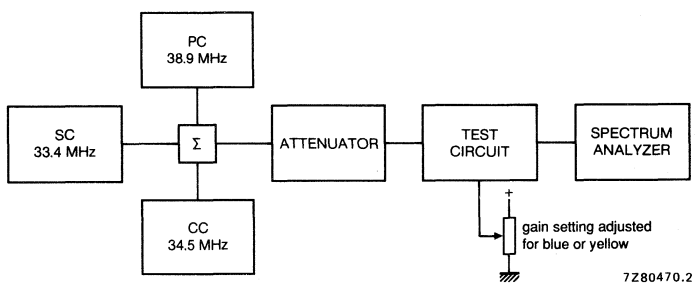


Fig.7 Test set-up intermodulation measurements.

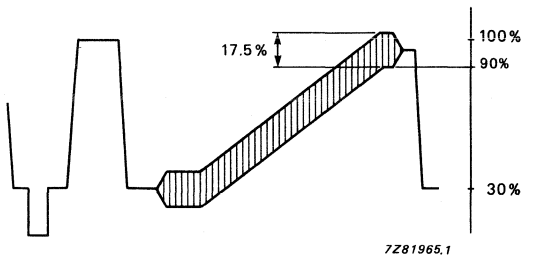


Fig.8 Video output signal.

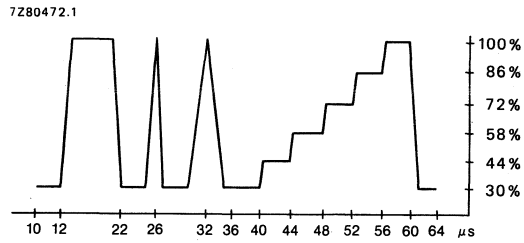


Fig.9 E.B.U. test signal wave form (line 330).

DC-coupled vertical deflection and East-West output circuit

TDA8350Q

FEATURES

- Few external components
- Highly efficient fully DC coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  short-circuit of the output pins
  short-circuit of the output pins to V_P or GND
- Temperature (thermal) protection
- East-West output stage with one single conversion resistor.

DESCRIPTION

The TDA8350Q is a power circuit for use in 90 ° and 110 ° colour deflection systems for frame frequencies of 50 to 120 Hz and line frequencies within 15 to 64 kHz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system and an East-West driver for sinking the diode modulator current.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
DC supply					
V_P	supply voltage range	9	–	25	V
I_P	quiescent current	–	25	–	mA
Vertical circuit					
I_O	output current (peak-to-peak value)	–	–	3	A
$I_{I(diff)}$	differential input current (peak-to-peak value)	–	600	–	µA
$V_{I(diff)}$	differential input voltage (peak-to-peak value)	–	1.8	–	V
Flyback switch					
I_M	peak output current	–	–	±1.5	A
V_{FB}	flyback supply voltage	–	–	60	V
East-West amplifier					
$I_{O(sink)}$	output current (sink only)	–	–	500	mA
$V_{O(sink)}$	peak output voltage ($I_{O(sink)}$ = 10 µA)	–	–	40	V
I_{bias}	input bias current	–	–	1	µA
Thermal data (according to IEC 747-1)					
T_{stg}	storage temperature range	–65	–	150	°C
T_{amb}	operating ambient temperature range	tbf	–	tbf	°C
T_{vj}	virtual junction	–	–	150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8350Q	13	DIL-Bent-Sil	plastic	SOT141

DC-coupled vertical deflection and East-West output circuit

TDA8350Q

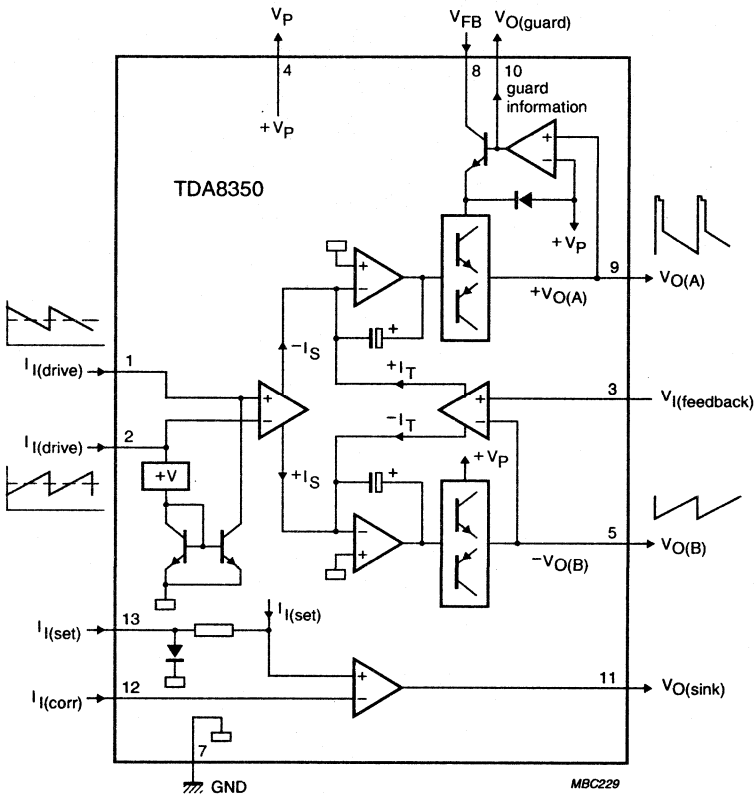


Fig.1 Block diagram.

DC-coupled vertical deflection and East-West output circuit

TDA8350Q

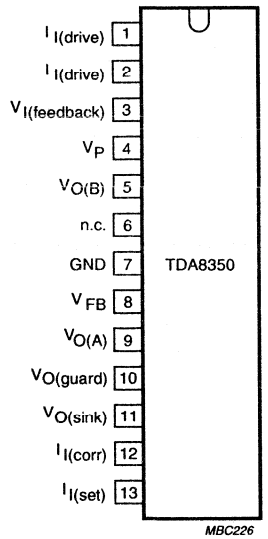


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$I_{I(drive)}$	1	input power-stage (+); includes $I_{I(sb)}$ signal bias
$I_{I(drive)}$	2	input power-stage (−); includes $I_{I(sb)}$ signal bias
$V_{I(feedback)}$	3	feedback voltage
V_P	4	operating supply voltage
$V_{O(B)}$	5	output voltage (B)
n.c.	6	not connected
GND	7	ground
V_{FB}	8	flyback supply voltage
$V_{O(A)}$	9	output voltage (A)
$V_{O(guard)}$	10	guard output
$V_{O(sink)}$	11	East-West amplifier driver (sink) output
$I_{I(corr)}$	12	East-West amplifier input correction (−)
$I_{I(set)}$	13	East-West amplifier set input (+)

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (R_T) connected in series with the deflection coil provides internal feed back information. The differential input circuit is voltage driven. The input circuit is adapted for use with the TDA9150 and TDA9160 which deliver symmetrical current signals. An external resistor (R_{CON}) connected between the differential input determines the output current through the deflection coil. The relationship between the differential input current and the output current is defined by: $I_{I(diff)} \times R_{CON} = I_{(coil)} \times R_T$. The output current is adjustable from 0.5 A (p-p) to 3 A (p-p) by varying R_{CON} (with $R_T = 0.6\ \Omega$).

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_P optimal for the scan voltage and the second supply voltage V_{FB} optimal for the flyback voltage. Using this method, very high efficiency is achieved.

The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected viz.:

- thermal protection
- short-circuit protection of the output pins (5 and 9)
- short-circuit of the output pins to V_P or GND.

A guard circuit $V_{O(guard)}$ is provided. The guard circuit is activated at the following conditions:

- during flyback
- during various short-circuit possibilities at the output pins
- during open loop
- when the thermal protection is activated.

This signal can be used for blanking the picture tube screen.

An East-West amplifier is also provided. This amplifier is an inverting amplifier which is current driven with sink current only capabilities.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
DC supply					
V_P	supply voltage		–	40	V
V_{FB}	flyback supply voltage		–	60	V
Vertical circuit					
I_O	output current (peak-to-peak value)	note 1	–	3	A
$V_{O(A)}$	output voltage (pin 9)		–	60	V
Flyback switch					
I_M	peak output current		–	±1.5	A
East-West amplifier					
$V_{O(sink)}$	output voltage	$I_{O(sink)}$ = 10 µA; note 2	–	40	V
$I_{O(sink)}$	output current	$V_{O(sink)}$ = 2 V; note 2	–	500	mA
Thermal data (according to IEC 747-1)					
T_{stg}	storage temperature range		−65	150	°C
T_{amb}	operating ambient temperature range		tbf	tbf	°C
T_{vj}	virtual junction		–	150	°C
$R_{th\ vj\text{-}c}$	resistance vj-case		–	tbf	K/W
$R_{th\ vj\text{-}a}$	resistance vj-ambient free air		–	40	K/W
T_{sc}	short-circuiting time	note 3	–	1	hr

Notes

1. I_O maximum determined by current protection.
2. The operating area is limited by a straight line between the points $V_{O(sink)}$ = 40 V; $I_{O(sink)}$ = 10 µA and $V_{O(sink)}$ = 2 V; $I_{O(sink)}$ = 500 mA.
3. Up to V_p = tbf (to be fixed).

CHARACTERISTICS

T_{amb} = 25 °C; V_P 16 V; V_{FB} = 45 V; $V_{O(sink)}$ = 20 V; f = 50 Hz and $I_{I(sb)}$ = 400 µA unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_p	operating supply voltage		9	–	25	V
V_{FB}	flyback supply voltage		V_p	–	60	V
I_p	supply current	no signal; no load	–	25	tbf	mA
Vertical circuit						
V_O	output voltage swing (scan)	$I_{I(diff)}$ = 0.6 mA (p-p); $V_{I(diff)}$ = 1.8 V (p-p); I_O = 3 A (p-p)	–	24	tbf	V
LE	linearity error	I_O = 3 A (p-p); I_O = 50 mA (p-p); note 1	– –	– –	1 1	% %
V_O	output voltage swing (flyback) $V_{O(A)}$-$V_{O(B)}$	$I_{I(diff)}$ = +0.3 mA; I_O = +1.5 A (p)	41	–	–	V
V_{DF}	forward voltage of the internal efficiency diode ($V_{O(A)}$- V_{FB})	I_O = –1.5 A (p); $I_{I(diff)}$ = +0.3 mA	–	–	tbf	V
$\|I_{off}\|$	output offset current	$I_{I(diff)}$ = 0; $I_{I(sb)}$ = 50 to 500 µA	–	–	18	mA
$\|V_{off}\|$	offset voltage at the input of the feedback amplifier $V_{I(feedback)}$-$V_{O(B)}$	$I_{I(diff)}$ = 0; $I_{I(sb)}$ = 50 to 500 µA	–	–	10.8	mV
ΔI_{off}	output offset current as a function of temperature	$I_{I(diff)}$ = 0;	–	–	0.12	mA/K
$V_{O(A)}$	DC output voltage	$I_{I(diff)}$ = 0; note 2	–	7.3	–	V
G_{vo}	open loop voltage gain (V9-5/V1-2)	notes 3 and 4	–	60	–	dB
	open loop voltage gain (V9-5/V3-5; V1-2 = 0)	note 3	–	60	–	dB
G	voltage ratio V1-2/V3-5		0	–	–	dB
f	frequency response (–3 dB)	note 5	–	–	tbf	Hz
Gc	current gain ($I_O/I_{I(diff)}$)		–	–	5000	
ΔGc	current gain drift as a function of temperature		–	–	10^{-4}	/K
$I_{I(sb)}$	signal bias current		50	–	500	µA
I_{FB}	flyback supply current	during scan	–	–	100	µA
RR	power supply ripple rejection	note 6	–	tbf	–	dB
I_{ripple}	output ripple current	note 6	–	–	tbf	mA
$V_{I(DC)}$	DC voltage at the input		–	2.6	–	V
$V_{I(CM)}$	common mode input voltage	$I_{I(sb)}$ = 0	0	–	2	V
I_{bias}	input bias current	$I_{I(sb)}$ = 0	–	–	tbf	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
East-West amplifier						
$V_{O(sink)}$	saturation voltage	$I_{O(sink)}$ = 500 mA; $I_{I(corr)}$ = 0 µA; note 7	–	–	2	V
G_{vo}	open loop voltage gain (V11/V12)		–	–	tbf	dB
f	frequency response (–3 dB)		–	–	tbf	Hz
LE	linearity error	$V_{O(sink)}$ = 3 V; $V_{O(sink)}$ = 10 V; note 1	– –	– –	1 0.5	% %
I_{bias}	input bias current (pin 12)		–	–	1	µA
$V_{I(DC)}$	DC input voltage		–	1	–	V
I_{set}	offset voltage set current		–	1	–	mA
V_{13-7}	maximum allowed voltage at pin 13		–	–	0.3	V
Guard circuit						
I_O	output current (not active)	$V_{O(guard)}$ = 0 V	–	–	10	µA
	output current (active)	$V_{O(guard)}$ = 5 V	1	–	–	mA
$V_{O(guard)}$	output voltage allowable voltage on pin 10 (leakage current maximum 10 µA)	I_O = 100 µA note 8	– –	– –	5.5 11	V V

Notes

1. Deviation of the output signal with respect to the input signal.
2. Related to V_P
3. V values within formulae, relate to voltages at or between relative pin numbers, i.e. V9-5/V1-2 = voltage value across pins 9 and 5 divided by voltage value across pins 1 and 2.
4. V3-5 AC short-circuited.
5. Frequency response V9-5/V3-5 is equal to frequency response V9-5/V1-2.
6. At $V_{(ripple)}$ = 500 mV eff., measured across R_T.
7. The output pin 11 requires a capacitor of minimum value 68 nF.
8. This voltage may not exceed + V_P (if + $V_P \leq 11$ V).

DC-coupled vertical deflection and East-West output circuit

TDA8350Q

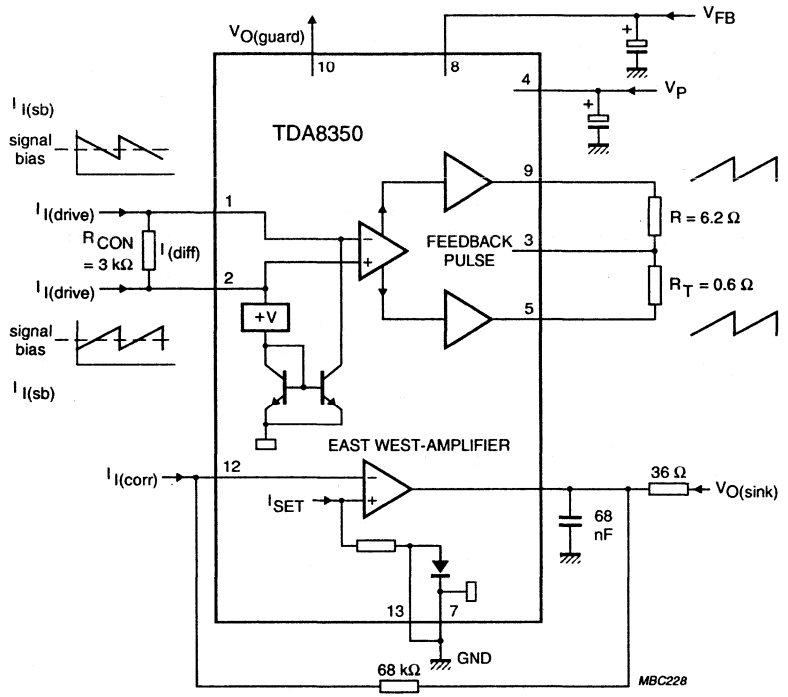
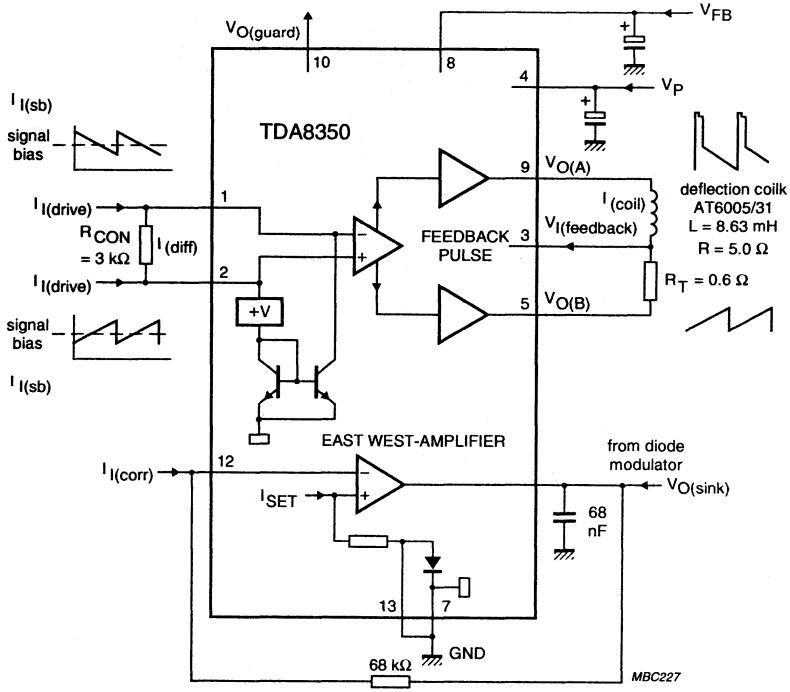


Fig.3 Test diagram.

DC-coupled vertical deflection and East-West output circuit

TDA8350Q



V_P = 13 V
I_O(p-p) = 2.2 A
$I_{I(sb)}$ = 400 µA
$I_{(diff)}$(p-p) = 440 µA
V_{FB} = 42 V
t_{FB} = 0.6 ms

Fig.4 Application diagram.

DC-coupled vertical deflection circuit

TDA8351

FEATURES

- Few external components
- Highly efficient fully DC coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:

  short-circuit of the output pins (7 and 4)

  short-circuit of the output pins to V_P or GND
- Temperature (thermal) protection
- High EMC immunity because of common mode inputs

DESCRIPTION

The TDA8351 is a power circuit for use in 90 ° and 110 ° colour deflection systems for frame frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
DC supply					
V_P	supply voltage range	9	–	25	V
I_P	quiescent current	–	30	–	mA
Vertical circuit					
I_O	output current (peak-to-peak value)	–	–	3	A
$I_{I(diff)}$	differential input current (peak-to-peak value)	–	600	–	µA
$V_{I(diff)}$	differential input voltage (peak-to-peak value)	–	1.8	–	V
Flyback switch					
I_M	peak output current	–	–	±1.5	A
V_{FB}	flyback supply voltage	–	–	50	V
V_{FB}	flyback supply voltage (note 1)	–	–	60	V
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature range	–55	–	150	°C
T_{amb}	operating ambient temperature range	tbf	–	tbf	°C
T_{vj}	virtual junction	–	–	150	°C

Note to the quick reference data

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 470 nF capacitor in series with a 20 Ω resistor has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 100 Ω. See application circuit (Fig.6).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8351	9	SIL	plastic	SOT131

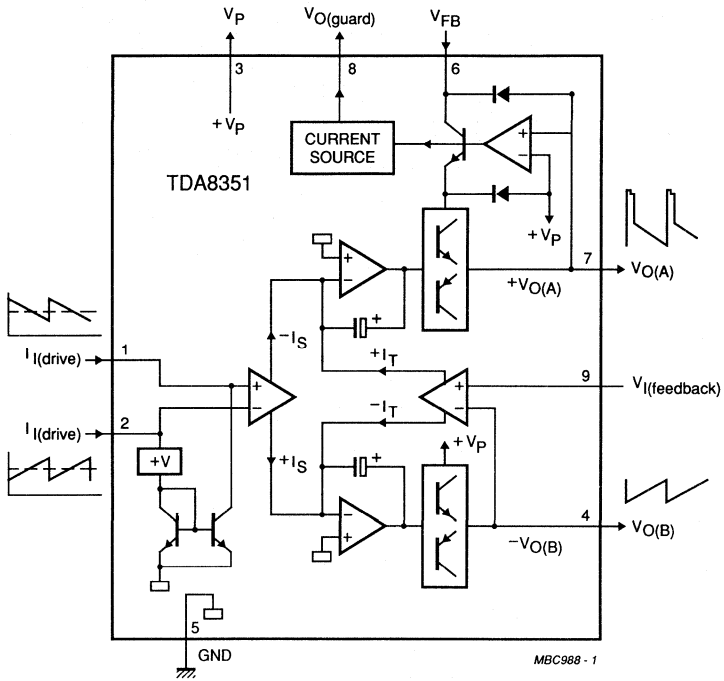
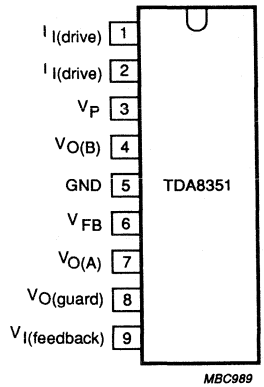


Fig.1 Block diagram.

DC-coupled vertical deflection circuit

TDA8351



metal block connected to substrate (pin 5)

Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
$I_{I(drive)}$	1	input power-stage (+); includes $I_{I(sb)}$ signal bias
$I_{I(drive)}$	2	input power-stage (–); includes $I_{I(sb)}$ signal bias
V_P	3	operating supply voltage
$V_{O(B)}$	4	output voltage (B)
GND	5	ground
V_{FB}	6	flyback supply voltage
$V_{O(A)}$	7	output voltage (A)
$V_{O(guard)}$	8	guard output
$V_{I(feedback)}$	9	feedback voltage

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (R_T) connected in series with the deflection coil provides internal feed back information. The differential input circuit is voltage driven. The input circuit is adapted for use with the TDA9150 and TDA9160 which deliver symmetrical current signals. An external resistor (R_{CON}) connected between the differential input determines the output current through the deflection coil. The relationship between the differential input current and the output current is defined by: $I_{I(diff)} \times R_{CON} = I_{(coil)} \times R_T$. The output current is adjustable from 0.5 A (p-p) to 3 A (p-p) by varying R_{CON} (with $V_{I(diff)} = 1.8$ V).

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_P optimum for the scan voltage and the second supply voltage V_{FB} optimum for the flyback voltage. Using this method, very high efficiency is achieved.

The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected viz.:

- thermal protection
- short-circuit protection of the output pins (4 and 7)
- short-circuit of the output pins to V_P or GND.

A guard circuit $V_{O(guard)}$ is provided. The guard circuit is activated at the following conditions:

- during flyback
- during
  - short-circuit of the coil
  - short-circuit of the output pins 7 and 4 to V_P or ground
- during open loop
- when the thermal protection is activated.

This signal can be used for blanking the picture tube screen.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
DC supply					
V_P	supply voltage		–	40	V
V_{FB}	flyback supply voltage		–	50	V
V_{FB}	flyback supply voltage	note 1	–	60	V
Vertical circuit					
I_O	output current (peak-to-peak value)	note 2	–	3	A
$V_{O(A)}$	output voltage (pin 7)		–	52	V
$V_{O(A)}$	output voltage (pin 7)	note 1	–	62	V
Flyback switch					
I_M	peak output current		–	±1.5	A
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature range		–55	150	°C
T_{amb}	operating ambient temperature range		tbf	tbf	°C
T_{vj}	virtual junction		–	150	°C
$R_{th\ vj\text{-}c}$	resistance vj-case		–	tbf	K/W
$R_{th\ vj\text{-}a}$	resistance vj-ambient in free air		–	40	K/W
T_{sc}	short-circuiting time	note 3	–	1	hr

Notes to the Limiting Values

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 470 nF capacitor in series with a 20 Ω resistor has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 100 Ω. See application circuit (Fig.6).
2. I_O maximum determined by current protection.
3. Up to V_P = tbf (to be fixed).

CHARACTERISTICS

V_P = 16 V; T_{amb} = 25 °C; V_{FB} = 45 V; f = 50 Hz and $I_{I(sb)}$ = 400 µA unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	operating supply voltage		9	–	25	V
V_{FB}	flyback supply voltage		V_P	–	50	V
V_{FB}	flyback supply voltage	note 1	V_P	–	60	V
I_P	supply current	no signal; no load	–	30	tbf	mA
Vertical circuit						
V_O	output voltage swing (scan)	$I_{I(diff)}$ = 0.6 mA (p-p); $V_{I(diff)}$ = 1.8 V (p-p); I_O = 3 A (p-p)	–	20	tbf	V
LE	linearity error	I_O = 3 A (p-p); I_O = 50 mA (p-p); note 2	– –	1 1	tbf tbf	% %
V_O	output voltage swing (flyback) $V_{O(A)}$-$V_{O(B)}$	$I_{I(diff)}$ = +0.3 mA; I_O = +1.5 A (p)	–	39	–	V
V_{DF}	forward voltage of the internal efficiency diode ($V_{O(A)}$- V_{FB})	I_O = −1.5 A (p); $I_{I(diff)}$ = +0.3 mA	–	–	tbf	V
$\|I_{off}\|$	output offset current	$I_{I(diff)}$ = 0; $I_{I(sb)}$ = 50 to 500 µA	–	–	18	mA
$\|V_{off}\|$	offset voltage at the input of the feedback amplifier $V_{I(feedback)}$-$V_{O(B)}$	$I_{I(diff)}$ = 0; $I_{I(sb)}$ = 50 to 500 µA	–	–	10.8	mV
ΔI_{off}	output offset current as a function of temperature	$I_{I(diff)}$ = 0;	–	–	0.12	mA/K
$V_{O(A)}$	DC output voltage	$I_{I(diff)}$ = 0; note 3	–	7.3	–	V
G_{vo}	open-loop voltage gain (V7-4/V1-2)	notes 4 and 5	–	80	–	dB
	open loop voltage gain (V7-4/V9-4; V1-2 = 0)	note 4	–	80	–	dB
G	voltage ratio V1-2/V9-4		–	0	–	dB
f	frequency response (−3 dB)	open loop; note 6	–	40	–	Hz
Gc	current gain ($I_O/I_{I(diff)}$)		–	5060	–	
ΔGc	current gain drift as a function of temperature		–	–	10^{-4}	/K
$I_{I(sb)}$	signal bias current		50	–	500	µA
I_{FB}	flyback supply current	during scan	–	–	100	µA
RR	power supply ripple rejection	note 7	–	40	–	dB
I_{ripple}	output ripple current	note 7	–	–	tbf	mA
$V_{I(DC)}$	DC voltage at the input		–	2.7	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{I(CM)}$	common mode input voltage	$I_{I(sb)} = 0$	0	–	1.6	V
I_{bias}	input bias current	$I_{I(sb)} = 0$	–	0.1	0.5	µA
$I_{O(CM)}$	common mode output current	$\Delta I_{I(sb)}$ = 300 µA (p-p); f = 50 Hz; $I_{I(diff)} = 0$	–	tbf	–	mA
Guard circuit						
I_O	output current (not active)	$V_{O(guard)} = 0$ V	–	–	50	µA
	output current (active)	$V_{O(guard)} = 5$ V	1	–	–	mA
$V_{O(guard)}$	output voltage	I_O = 100 µA	–	–	5.5	V
	allowable voltage on pin 8 (leakage current maximum 10 µA)	note 8	–	–	11	V

Notes to the characteristics

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 470 nF capacitor in series with a 20 Ω resistor has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 100 Ω. See application circuit (Fig.6).
2. Deviation of the output signal with respect to the input signal.
3. Related to V_P.
4. V values within formulae, relate to voltages at or between relative pin numbers, i.e. V_{7-4}/V_{1-2} = voltage value across pins 7 and 4 divided by voltage value across pins 1 and 2.
5. V_{9-4} AC short-circuited.
6. Frequency response V_{7-4}/V_{9-4} is equal to frequency response V_{7-4}/V_{1-2}.
7. At $V_{(ripple)}$ = 500 mV eff., measured across R_T.
8. This voltage may not exceed $+V_P$ (if $+V_P \leq 11$ V).

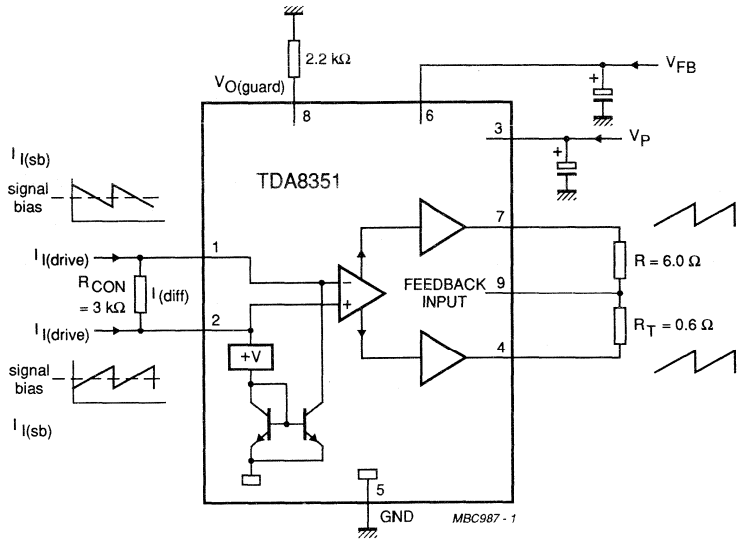


Fig.3 Test diagram.

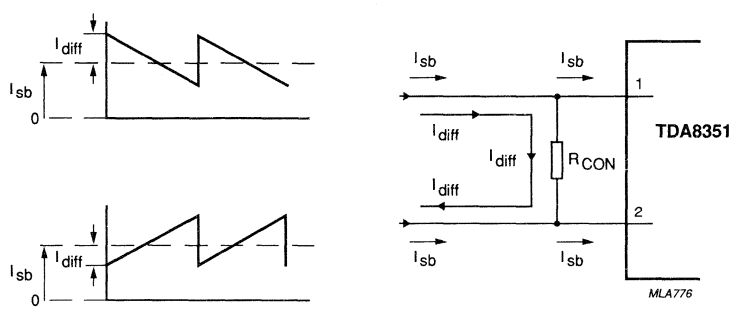
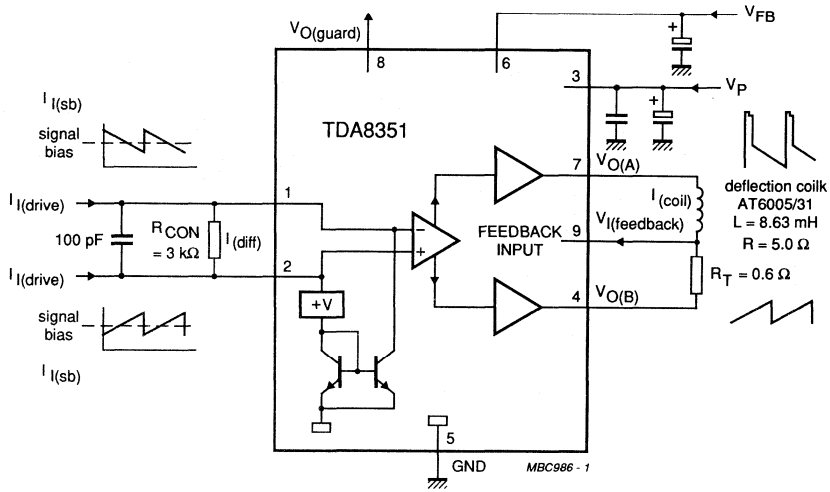


Fig.4 Input currents.

APPLICATION INFORMATION

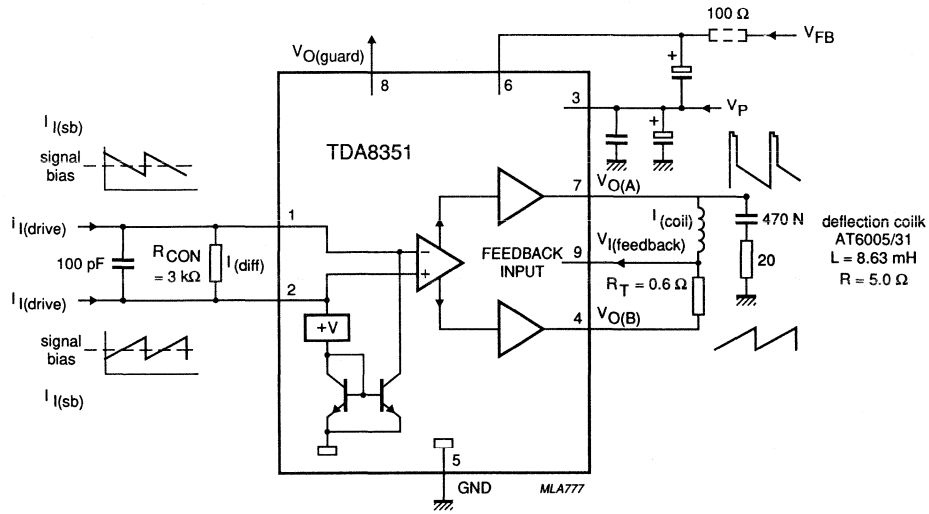


V_P = 14 V
$I_{O(p-p)}$ = 2.14 A
$I_{I(sb)}$ = 400 µA
$I_{(diff)(p-p)}$ = 428 µA
V_{FB} = 42 V
t_{FB} = 0.6 ms

Fig.5 Application diagram.

DC-coupled vertical deflection circuit

TDA8351



V_P = 14 V
$I_{O(p-p)}$ = 2.14 A
$I_{I(sb)}$ = 400 µA
$I_{(diff)(p-p)}$ = 428 µA
V_{FB} = 60 V
t_{FB} = 0.4 ms

Fig.6 Application diagram.

Multistandard TV processor TDA8362

FEATURES

- Multistandard vision IF circuit (positive and negative modulation)
- Multistandard FM sound demodulator (4.5 MHz to 6.5 MHz)
- Video and audio switches (CVBS internal/external, S-VHS and audio internal/external)
- Integrated chrominance trap and bandpass filters (automatically calibrated)
- Integrated luminance delay line
- PAL/NTSC colour decoder with automatic search system
- Easy interfacing with the TDA8395 (SECAM decoder) for multistandard applications
- RGB control circuit with linear RGB inputs and fast blanking
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Vertical count-down circuit and vertical preamplifier
- Low dissipation (600 mW)
- Small amount of peripheral components compared with competition ICs
- Only one adjustment (video IF demodulator)

GENERAL DESCRIPTION

The TDA8362 contains nearly all small signal functions that are required for a colour television receiver. For a complete receiver the following circuits need to be added: a base-band delay line (TDA4661), a tuner and output stages for audio, video and horizontal and vertical deflection.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage	–	8.0	–	V
I_P	positive supply current	–	80	–	mA
Input voltages					
$V_{45/46(RMS)}$	video IF amplifier sensitivity (RMS value)	–	70	–	μV
$V_{5(RMS)}$	sound IF amplifier sensitivity (RMS value)	–	1.0	–	mV
$V_{6(RMS)}$	external audio input (RMS value)	–	350	–	mV
$V_{15(p-p)}$	external CVBS input (peak-to-peak value)	–	1.0	–	V
$V_{21(p-p)}$	RGB inputs (peak-to-peak value)	–	0.7	–	V
Control voltages					
$V_{control}$	control voltages for Volume, Contrast, Saturation, Brightness, Hue and Peaking	0	–	5.0	V
Output signals					
$V_{O(p-p)}$	demodulated CVBS output (peak-to-peak value)	–	2.5	–	V
V_{47}	tuner AGC control voltage range	0	–	10	V
V_{44}	AFC output voltage swing	–	6.0	–	V
$V_{50(RMS)}$	audio output voltage	–	700	–	mV
$V_{18-20(p-p)}$	RGB output signal amplitudes (peak-to-peak value)	–	4.0	–	V
I_{37}	horizontal output current	10	–	–	mA
I_{43}	vertical output current	1	–	–	mA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8362	52	SDIL	plastic	SOT247

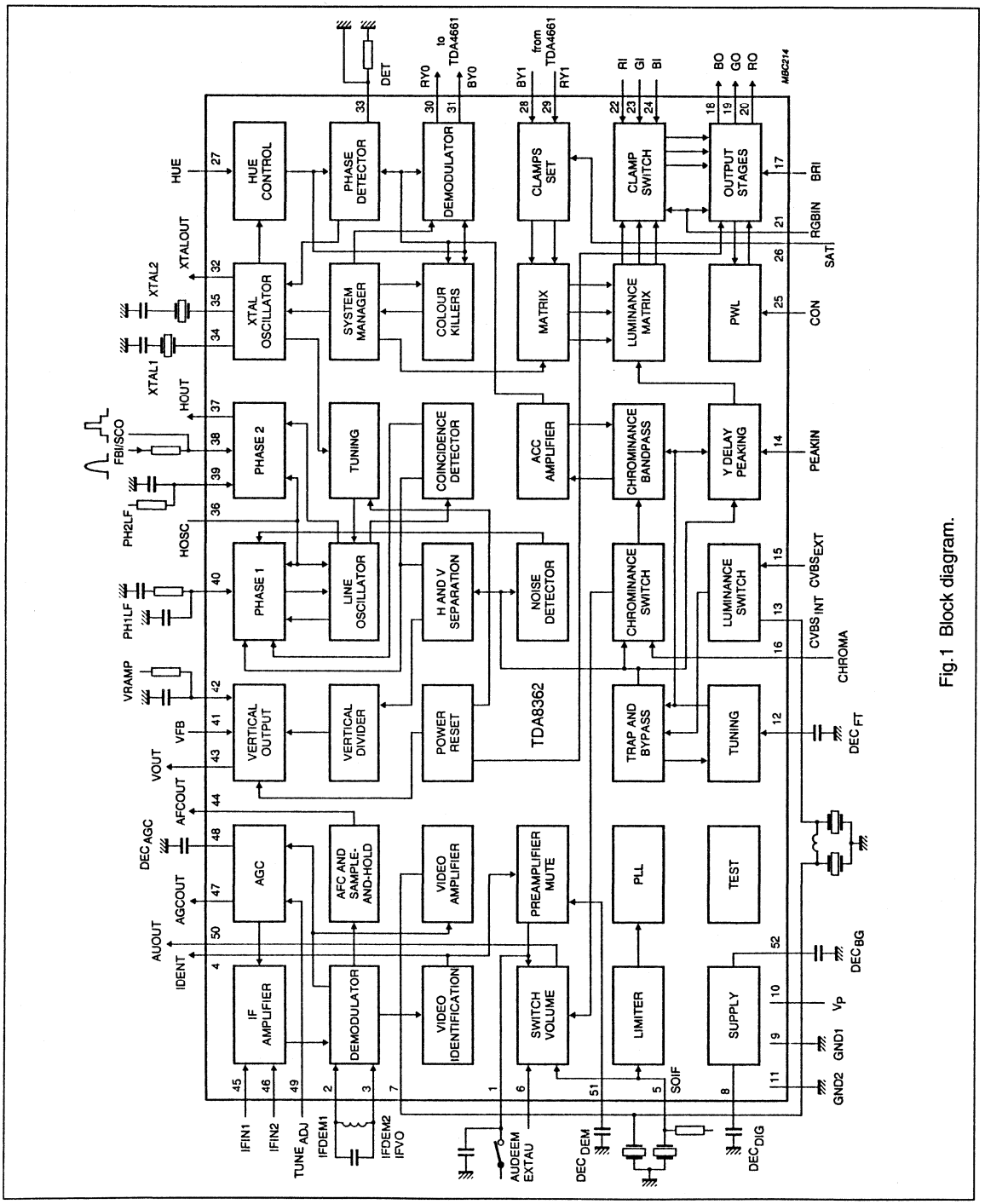


Fig.1 Block diagram.

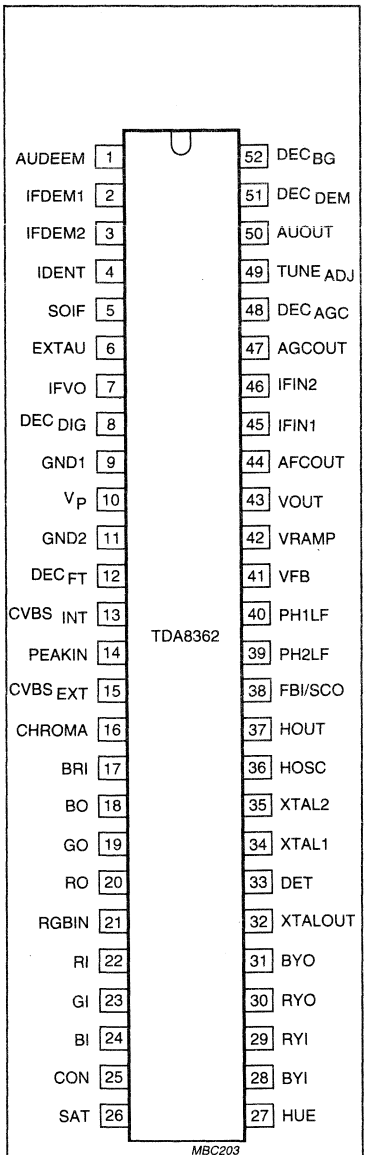


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AUDEEM	1	audio de-emphasis
IFDEM1	2	IF demodulator tuned circuit
IFDEM2	3	IF demodulator tuned circuit
IDENT	4	video identification output
SOIF	5	sound IF input and volume control
EXTAU	6	external audio input
IFVO	7	IF video output
DEC_{DIG}	8	decoupling digital supply
GND1	9	ground 1
V_P	10	positive supply voltage (+8 V)
GND2	11	ground 2
DEC_{FT}	12	decoupling filter tuning
$CVBS_{INT}$	13	internal CVBS input
PEAKIN	14	peaking control input
$CVBS_{EXT}$	15	external CVBS input
CHROMA	16	chrominance and A/V switch input
BRI	17	brightness control input
BO	18	blue output
GO	19	green output
RO	20	red output
RGBIN	21	RGB insertion and blanking input
RI	22	red input
GI	23	green input
BI	24	blue input
CON	25	contrast control input
SAT	26	saturation control input
HUE	27	hue control input (or chrominance output)
BYI	28	B-Y input signal
RYI	29	R-Y input signal
RYO	30	R-Y output signal
BYO	31	B-Y output signal
XTALOUT	32	4.43 MHz output for TDA8395
DET	33	loop filter burst phase detector
XTAL1	34	3.58 MHz XTAL connection
XTAL2	35	4.43 MHz XTAL connection
HOSC	36	start horizontal oscillator
HOUT	37	horizontal output
FBI/SCO	38	flyback input/sandcastle output

SYMBOL	PIN	DESCRIPTION
PH2LF	39	phase 2 loop filter
PH1LF	40	phase 1 loop filter
VFB	41	vertical feedback input
VRAMP	42	vertical ramp generator
VOUT	43	vertical output
AFCOUT	44	AFC output
IFIN1	45	IF input 1
IFIN2	46	IF input 2
AGCOUT	47	tuner AGC output
DEC_{AGC}	48	AGC decoupling capacitor
$TUNE_{ADJ}$	49	tuner take-over adjustment
AUOUT	50	audio output
DEC_{DEM}	51	decoupling sound demodulator
DEC_{BG}	52	decoupling bandgap supply

FUNCTIONAL DESCRIPTION

Video IF amplifier

The IF amplifier contains 3 AC-coupled control stages with a total gain control range of greater than 60 dB. The sensitivity of the circuit is comparable with that of modern IF ICs. The reference carrier for the video demodulator is obtained by means of passive regeneration of the picture carrier. The external reference tuned circuit is the only remaining adjustment of the IC.
The polarity of the demodulator can be switched so that the circuit is suitable for both positive and negative modulated signals.

The AFC circuit is driven with the same reference signal as the video demodulator. To ensure that the video content does not disturb the AFC operation a sample-and-hold circuit is incorporated; the capacitor for this function is internal. The AFC output voltage range is 6 V.

The AGC detector operates on top-sync or top white-level, depending on the position of the demodulator. The AGC detector time constant capacitor is connected externally. This is mainly because of the flexibility of the application. The time constant of the AGC system during positive modulation is slow, this is to avoid any visible picture variations. This, however, causes the system to react very slowly to sudden changes in the input signal amplitude. To overcome this problem a speed-up circuit has been included which detects whether the AGC detector is activated every frame period. If, during a 3-frame period, no action is detected the speed of the system is increased.

The circuit contains a video identification circuit which is independent of the synchronization circuit. Consequently search tuning is possible when the display section of the receiver is used as a monitor. The identification output voltage is LOW when no transmitter is identified (in this condition the sound demodulator is switched off, mute function). When a transmitter is identified the output voltage goes HIGH. The voltage level is dependent on the frequency of the incoming chrominance signal.

Sound circuit

The sound bandpass and trap filters have to be connected externally. The filtered intercarrier signal is fed to a limiter circuit and is demodulated by means of a PLL demodulator. The PLL circuit tunes itself automatically to the incoming signal, consequently, no adjustment is required.

The volume is DC controlled. The composite audio output signal has an amplitude of 700 mV(RMS) at the maximum volume control setting. The de-emphasis capacitor has to be connected externally. The non-controlled audio signal can be obtained from this pin (pin 1) via a buffer stage. This signal, and the external audio input signal, must have an amplitude of 350 mV(RMS). The audio/video switch is controlled via the chrominance input (pin 16).

Synchronization circuit

The sync separator is preceded by a voltage controlled amplifier which adjusts the sync pulse amplitude to a fixed level. The sync pulses are then fed to the slicing stage (separator) which operates at 50% of the amplitude.
The separated sync pulses are fed to the first phase detector and to the coincidence detector. The coincidence detector is used for transmitter identification and to detect whether the line oscillator is synchronized. The first PLL has a very high static steepness, this ensures that the phase of the picture is independent of the line frequency.

The line oscillator operates at twice the line frequency (the oscillator capacitor is internal). Because of the spread of internal components an automatic adjustment circuit has been added to the IC. The circuit compares the oscillator frequency with that of the crystal oscillator, in the colour decoder, which results in a free-running frequency that deviates less than 2% from the typical value.
The circuit employs a second control loop to generate the drive pulses for the horizontal driver stage.

X-ray protection can be realised by switching the pin of the second control loop (pin 39) to the positive supply line. The detection circuit must be connected externally. When the X-ray protection is active the horizontal output voltage goes HIGH. When the voltage on this pin (pin 37) returns to its normal level the horizontal output is released again.

The IC contains a start-up circuit for the horizontal oscillator. When this feature is required a current of 5.5 mA should be applied to pin 36. For an application without start-up both supply pins (10 and 36) must be connected to the 8 V supply line.

The drive signal for the vertical ramp generator is generated by means of a divider circuit. The RC network for the ramp generator is external.

Integrated video filters

The circuit contains a chrominance bandpass and trap circuit. The filters are realised by means of gyrator circuits and are automatically tuned by comparing the tuning frequency

with the crystal frequency of the decoder. The chrominance trap is only active when a separate chrominance input pin is connected to ground or to V_P. When this pin is left open-circuit the trap is switched off to enable the circuit be used also for S-VHS applications.

The luminance delay line and the delay for the peaking circuit are also realised by means of gyrator circuits.

Colour decoder

The colour decoder contains an alignment-free crystal oscillator, a colour killer circuit and colour difference demodulators. The 90° phase shift for the reference signal is achieved internally. The demodulation angle and gain ratio for the colour difference signals (PAL and NTSC) are switched to the required standards depending on the incoming signal.

The colour decoder is very flexible, together with the SECAM decoder (TDA8395) an automatic multistandard decoder can be designed. It is also possible to use it for only one standard when just one crystal is connected to the IC.
The following applications are possible:

PAL ONLY

Connect one, or two crystals to the IC (when only one crystal is used the other crystal pin has to be connected to the positive supply rail via a 30 kΩ resistor) and the hue control pin to the positive supply via a 30 kΩ (approximate) resistor. In this condition the decoder will not search for NTSC signals.

PAL/NTSC

Connect one, or two crystals to the IC and connect a control voltage of between 0 and 5 V to the hue control pin. The decoder will identify PAL and NTSC signals at one or two frequencies. For the reception of PAL-N and the PAL-M standards the two 3.6 MHz crystals must be connected to pin 34; switching between the crystals must be made externally. The circuit will indicate whether a PAL signal has been identified via the identification pin (pin 4). The conditions are:

- Signal identified at f_{osc} = 3.6 MHz; V_o = 6 V
- Signal identified at f_{osc} = 4.4 MHz (or no colour); V_o = 8 V

The information from the identification pin can also be used to switch the sound bandpass filter.

PAL/SECAM

The chrominance input signal for the SECAM decoder must be identical to that of the PAL decoder. This can be realised by means of an external switch which is connected in parallel with the internal video switch. In the TDA8362, when the NTSC option is not required, the output signal from the switch can be obtained from the hue control input when it is connected to the positive supply line via a suitable resistor.

PAL/SECAM/NTSC

In this application the hue control must be active. Therefore, an external video switch has to be added so that the previous application (PAL/SECAM) is not possible.

RGB output circuit

The colour difference signals are matrixed with the luminance signal to obtain the RGB signals. Linear amplifiers have been chosen for the RGB inputs so that the circuit is suitable for incoming signals from the SCART connector. The contrast and brightness controls operate on internal and external signals.
The fast blanking pin has a second detection level at 4 V. When this level is exceeded the RGB outputs are blanked so that "On-Screen-Display" signals can be applied to the outputs.
The ouput signal has an amplitude of approximately 4 V, black-to-white, with nominal input signals and nominal control settings.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	–	9.0	V
T_{stg}	storage temperature range	−25	+150	°C
T_{amb}	operating ambient temperature range	−25	+70	°C
T_s	soldering temperature for 5 s	–	260	°C
T_j	maximum junction temperature (operating)	–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage (pin 10)		7.2	8.0	8.8	V
I_P	positive supply current (pin 10)		–	80	–	mA
I_{HOSC}	horizontal oscillator start current (pin 36)	note 1	6.5	–	–	mA
P_{tot}	total power dissipation		–	0.64	–	W
IF circuit						
VISION IF AMPLIFIER INPUTS (PINS 45 AND 46)						
$V_{i(RMS)}$	input sensitivity (RMS value)	note 2				
	at 38.9 MHz		–	70	100	μV
	at 45.75 MHz		–	70	100	μV
	at 58.75 MHz		–	70	120	μV
R_i	Input resistance (differential)		–	2	–	kΩ
C_i	Input capacitance differential)		–	3	–	pF
G_{CR}	gain control range		64	–	–	dB
E_O	output signal expansion for 50 dB input signal variation	note 3	–	1	–	dB
$V_{I(RMS)}$	maximum input signal (RMS value)		100	150	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIDEO AMPLIFIER OUTPUT; NOTE 4 (PIN 7)						
V_7	zero signal output level	note 5				
	negative modulation		–	4.8	–	V
	positive modulation		–	2.0	–	V
V_7	top sync level	negative modulation	1.9	2.0	2.1	V
V_7	white level	positive modulation	–	4.5	–	V
ΔV_7	difference in amplitude between negative and positive modulation		–	0	15	%
Z_O	video output impedance		–	–	50	Ω
I_{bias}	internal bias current of npn emitter follower output transistor		1	–	–	mA
I_{source}	maximum source current		–	–	5	mA
B	bandwidth of demodulated output signal	at –3 dB	6	9	–	MHz
G_{diff}	gain differential	note 6	–	2	5	%
φ_{diff}	phase differential	note 6	–	1	5	deg
NL_{vid}	video non-linearity	note 7	–	–	5	%
V_{th}	white spot threshold level		–	4.8	–	V
V_{ins}	white spot insertion level		–	3.7	–	V
N_{clamp}	noise invertor clamp level		–	1.3	–	V
δ	intermodulation	note 8				
	at 0.92/1.1 MHz blue		60	66	–	dB
	at 0.92/1.1 MHz yellow		56	62	–	dB
	at 2.66/3.3 MHz blue		60	66	–	dB
	at 2.66/3.3 MHz yellow		60	66	–	dB
S/N	signal-to-noise ratio	note 9				
	at 10 mV input signal		52	60	–	dB
	at end of control range		52	61	–	dB
V_7	residual carrier signal		–	5.5	–	mV
V_7	residual 2nd harmonic of carrier signal		–	2.5	–	mV
IF AND TUNER AGC						
timing of IF-AGC (C48 = 2.2 μF)						
	modulated video interference	30% AM for 1 mV to 100 mV; 0 to 200 Hz (system B/G)	–	–	10	%
t_{inc}	response time for an IF input signal amplitude increase of 52 dB for positive and negative modulation		–	2	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{dec}	response time for an IF input signal amplitude decrease of 52 dB					
	for negative modulation		–	25	–	ms
	for positive modulation		–	100	–	ms
I_{leak}	allowed leakage current of the AGC capacitor					
	for negative modulation		–	–	10	µA
	for positive modulation		–	–	200	nA
Tuner take-over adjustment (pin 49)						
$V_{49min(RMS)}$	minimum starting level for tuner take-over (RMS value)		–	0.2	0.5	mV
$V_{49max(RMS)}$	maximum starting level for tuner take-over (RMS value)		100	150	–	mV
V_{CR}	voltage control range		0.5	–	4.5	V
Tuner control output (pin 47)						
V_{47}	maximum tuner AGC output voltage	maximum gain	–	–	V_P+1	V
$V_{47(sat)}$	output saturation voltage	minimum gain; I_{47} = 2 mA	–	–	300	mV
I_{47}	maximum tuner AGC output swing		5	–	–	mA
I_{leak}	leakage current RF AGC		–	–	1	µA
ΔV_{47}	input signal variation for complete tuner control		0.5	2	4	dB
AFC OUTPUT; NOTE 10 (PIN 44)						
V_{44}	output voltage swing		–	6	–	V
f_{sl}	AFC slope frequency		–	160	–	kHz
f_{os}	AFC offset frequency		–	–	50	kHz
V_O	output voltage at centre frequency		–	4.0	–	V
Z_O	output impedance		–	50	–	kΩ
SWITCHING TO POSITIVE MODULATION; NOTE 11 (PIN 1)						
V_1	voltage on pin 1 to switch the video demodulator and AGC to positive modulation		–	–	V_P–1	V
I_1	input current		–	0.1	–	mA
VIDEO IDENTIFICATION OUTPUT (PIN 4)						
V_O	output voltage	video not identified	–	–	0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Z_O	output impedance		–	20	–	kΩ
V_O	output voltage	video identified; colour signal available; f_{osc} = 3.5 MHz	–	6.0	–	V
		video identified; colour signal available/unavailable; f_{osc} = 4.4 MHz	–	8.0	–	V
t_d	delay time of identification after the AGC has stabilized on a new transmitter		–	–	10	ms
Sound circuit						
DEMODULATOR INPUT; NOTE 12 (PIN 5)						
$V_{5(RMS)}$	input limiting for PLL catching range (RMS value)		–	1.0	2.0	mV
Δf	catching range PLL	note 13	4.2	–	6.8	MHz
R_I	input resistance		–	8.5	–	kΩ
C_I	input capacitance		–	–	5	pF
AMR	AM rejection	V_I = 50 mV(RMS); note 13	60	tbf	–	dB
DE-EMPHASIS (PIN 1)						
$V_{O(RMS)}$	output signal amplitude (RMS value)	note 13	–	350	–	mV
R_O	output resistance		–	15	–	kΩ
V_1	DC output voltage		–	3.0	–	V
AUDIO ATTENUATOR OUTPUT (PIN 50)						
$V_{50(RMS)}$	controlled output signal amplitude (RMS value)	at –6 dB; note 13	500	700	900	mV
R_O	output resistance		–	250	–	Ω
V_{50}	DC output voltage		–	3.3	–	V
THD	total harmonic distortion	note 15	–	–	0.5	%
SVRR	supply voltage ripple rejection		–	tbf	–	dB
S/N	signal-to-noise ratio					
	internal		–	60	–	dB
	external		tbf	–	–	dB
ΔT	temperature dependancy of output level	note 16	–	–	tbf	dB
VOL_{CR}	control range	see also Fig.3	–	80	–	dB
OSS	suppression of output signal when mute is active		–	80	–	dB
ΔV_{50}	DC shift of the output when mute is active	note 16	–	10	50	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EXTERNAL AUDIO INPUT; NOTE 17 (PIN 6)						
$V_{6(RMS)}$	input signal amplitude (RMS value)		–	350	700	mV
R_I	input resistance		–	25	–	kΩ
ΔG_V	voltage gain difference between input and output	maximum volume	–	12	–	dB
α	crosstalk between internal and external audio signals		–	60	–	dB
CVBS/On-Screen Display and CD inputs						
INTERNAL AND EXTERNAL CVBS INPUTS (PINS 13 AND 15)						
$V_{13(p-p)}$	internal CVBS input voltage (peak-to-peak value)	note 18	–	2.0	2.8	V
I_{13}	internal CVBS input current		–	4	–	μA
I_{15}	external CVBS input current		–	4	–	μA
$V_{15(p-p)}$	external CVBS input voltage (peak-to-peak value)		–	1.0	1.4	V
ISS	suppression of non-selected CVBS input signal		50	–	–	dB
COMBINED CHROMINANCE AND SWITCH INPUT (PIN 16)						
$V_{16(p-p)}$	chrominance input voltage (peak-to-peak value)	note 19	–	0.3	–	V
$V_{16(p-p)}$	input signal amplitude before clipping occurs (peak-to-peak value)		1.0	–	–	V
R_I	chrominance input resistance		–	15	–	kΩ
C_I	chrominance input capacitance		–	–	5	pF
V_{16}	DC input voltage to switch the A/V switch to internal mode		–	–	0.5	V
V_{16}	DC input voltage to switch the A/V switch to external mode		V_P–0.5	–	–	V
V_{16}	DC input voltage for chrominance insertion		3.0	$V_P/2$	5.0	V
SS	suppression of non-selected chrominance signal from CVBS input		50	–	–	dB
RGB INPUTS FOR ON-SCREEN DISPLAY (PINS 22, 23 AND 24)						
$V_{22,23\ 24(p-p)}$	input signal amplitude for an output signal of 4 V (black-to-white)(peak-to-peak value)	note 20	–	0.7	0.8	V
$V_{22,23\ 24(p-p)}$	input signal amplitude before clipping occurs (peak-to-peak value)		1.0	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{diff}	difference of black level of internal and external signals at the outputs		–	–	200	mV
$I_{22,23,24}$	input currents		–	0.1	–	µA
t_d	delay difference for the three channels		–	0	–	ns
FAST BLANKING (PIN 21)						
V_I	input voltage	no data insertion data insertion	– 0.9	– –	0.3 –	V V
$V_{21\ max}$	maximum input pulse	insertion	–	–	3	V
t_d	delay of data insertion		–	–	20	ns
I_{21}	input current		–	–	0.2	mA
SS_{int}	suppression of internal RGB signals	insertion = 0 to 5 MHz	46	–	–	dB
SS_{ext}	suppression of external RGB signals	insertion = 0 to 5 MHz	46	–	–	dB
V_I	input voltage to blank the RGB-outputs so that "On-Screen-Display" signals can be applied to these outputs	note 21	4.5	–	–	V
t_d	delay between the input pulse and the blanking at the output		–	30	tbf	ns
COLOUR DIFFERENCE INPUT SIGNALS (PINS 28 AND 29)						
$V_{29(p-p)}$	input signal amplitude –(R-Y) (peak-to-peak value)		–	1.05	–	V
$V_{28(p-p)}$	input signal amplitude –(B-Y) (peak-to-peak value)		–	1.35	–	V
$I_{28,29}$	input current		–	0.1	1.0	µA
Chrominance filters						
CHROMINANCE TRAP CIRCUIT						
f_{trap}	trap frequency		–	f_{osc}	–	MHz
QF_{tr}	trap quality factor	note 22	–	2	–	
SR	colour subcarrier rejection		20	–	–	dB
CHROMINANCE BANDPASS CIRCUIT						
f_C	centre frequency		–	f_{osc}	–	MHz
QF_{bp}	bandpass quality factor		–	1.5	–	
Delay line and peaking circuit						
Y DELAY LINE						
t_d	delay time	note 23	–	260	–	ns
B	bandwidth of internal delay line		8	–	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PEAKING CONTROL; (PIN 14) NOTE 24, SEE ALSO FIG.4						
t_W	width of preshoot or overshoot	at 50% of pulse	–	130	–	ns
S_{cth}	peaking signal compression threshold		–	50	–	IRE
Horizontal and vertical synchronization circuits						
SYNC INPUT (VIDEO) (PINS 13 AND 15)						
V_{13}	sync pulse amplitude	referenced to pin 15	50	300	–	mV
	slicing level	note 25	–	50	–	%
VERTICAL SYNC						
t_W	width of the vertical sync pulse without sync instability	note 26	10	–	–	µs
HORIZONTAL OSCILLATOR						
f_{fr}	free running frequency		–	15625	–	Hz
Δf_{fr}	spread on free running frequency		–	–	±2	%
$\Delta f_{osc}/\Delta V_P$	frequency variation with respect to the supply voltage	V_P = 8.0 V ±10 %	–	0.2	0.5	%
$\Delta f_{osc}/\Delta T$	frequency variation with temperature		–	–	tbf	Hz/K
$\Delta f_{osc\ max}$	maximum frequency deviation at the start of the horizontal output		–	–	+60	%
FIRST CONTROL LOOP (FILTER CONNECTED TO PIN 40)						
f_{HR}	holding range PLL		–	±0.9	±1.2	kHz
f_{CR}	catching range PLL		±0.6	±0.9	–	kHz
S/N	signal-to-noise ratio of the video input signal at which the time constant is switched		–	20	–	dB
H	hysteresis at the switching point		–	3	–	dB
SECOND CONTROL LOOP; NOTE 27 (CAPACITOR CONNECTED TO PIN 39)						
$\Delta\varphi_i/\Delta\varphi_o$	control sensitivity		–	150	–	µs/µs
t_{CR}	control range from start of horizontal output to flyback		11	12	–	µs
t_{SHIFT}	horizontal shift range		±2	–	–	µs
$\Delta\varphi_i/\Delta\varphi_o$	shift control sensitivity		–	3	–	µA/µs
V_{39}	voltage to switch on the X-ray protection		6.0	–	–	V
I_I	input current during protection		–	–	tbf	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HORIZONTAL OUTPUT (PIN 37)						
V_{OL}	LOW level output voltage	I_O = 10 mA	–	–	0.3	V
$I_{O\ max}$	maximum allowed output current		10	–	–	mA
$V_{O\ max}$	maximum allowed output voltage		–	–	V_P	V
δ	duty cycle		–	50	–	%
FLYBACK INPUT/SANDCASTLE OUTPUT (PIN 38)						
I_{38}	required input current during flyback pulse		100	–	300	µA
V_O	output voltage					
	during burst key		4.8	5.3	5.8	V
	during blanking		1.8	2.0	2.2	V
V_{icl}	clamped input voltage during flyback		2.6	3.0	3.4	V
t_W	pulse width					
	burst key pulse		3.3	3.5	3.7	µs
	vertical blanking		–	14	–	lines
t_d	delay of start of burst key to start of sync		5.2	5.4	5.6	µs
VERTICAL SECTION; NOTE 28						
f_{fr}	free running frequency		–	50/60	–	Hz
f_{lock}	locking range		45	–	64.5	Hz
	divider value not locked		–	625/525	–	
	locking range (lines/frame)		488	–	722	
VERTICAL RAMP GENERATOR (PIN 42)						
I_{42}	input current during scan		–	–	2	µA
I_{dis}	discharge current during retrace		–	0.4	–	mA
$V_{saw(p-p)}$	sawtooth amplitude (peak-to-peak value)	in 50 Hz mode	–	1.5	–	V
t_d	delay from field to field		–	–	1.6	µs
VERTICAL OUTPUT (PIN 43)						
I_O	available output current		1	–	–	mA
I_{int}	internal bias current of npn emitter follower		–	0.2	–	mA
$V_{O(max)}$	maximum available output voltage		4.0	–	–	V
$V_{O(min)}$	minimum available output voltage		–	–	0.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL FEEDBACK INPUT (PIN 41)						
V_{41}	input voltage (DC component)		2.0	2.5	3.0	V
$V_{41(p-p)}$	input voltage (AC component) (peak-to-peak value)		–	1.0	–	V
I_{41}	input current		–	–	15	μA
Δt_p	internal precorrection to sawtooth	note 29	–	3	–	%
$\Delta T/\Delta V$	temperature dependency on amplitude	ΔT = 40 °C	–	–	1	%
	vertical guard switching level with respect to the DC feedback level					
V_{GL}	switching level LOW		–	–	−1.5	V
V_{GH}	switching level HIGH		–	–	+1.5	V
t_d	delay of scan start	power-on at 60 Hz	–	140	–	ms
Colour demodulation part						
CHROMINANCE AMPLIFIER						
ACC_{CR}	ACC control range	note 30	26	–	–	dB
ΔV	change in amplitude of the output signals over the ACC range		–	–	2	dB
TH_{on}	threshold colour killer ON		−23	−26	−29	dB
H_{off}	hysteresis colour killer OFF		–	+3	–	dB
ACL CIRCUIT						
	chrominance burst ratio at which the ACL starts to operate		2.3	–	2.7	
REFERENCE PART						
Phase-locked loop; note 31						
f_{CR}	catching range		400	500	–	Hz
$\Delta\varphi$	phase shift for a ±400 Hz deviation of the oscillator frequency		–	–	2	deg
Oscillator						
TC	temperature coefficient of the oscillator frequency	note 31	–	2.0	2.5	Hz/K
Δf_{osc}	frequency deviation with respect to the supply	note 31; V_P = 8 V ±10%	–	–	250	Hz
R_I	input resistance (pin 34)	at 3.58 MHz	–	1.5	–	kΩ
R_I	input resistance (pin 35)	at 4.43 MHz	–	1.3	–	kΩ
C_I	input capacitance (pins 34 and 35)		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R	required resistor to forcethe oscillator into one crystal mode		–	tbf	–	kΩ
HUE CONTROL AND CHROMINANCE OUTPUT; NOTE 32 (PIN 27)						
CR_{HUE}	hue control range	see also Fig.5	±45	±50	–	deg
ΔHUE	hue variation for ±10 % V_P		–	0	–	deg
ΔHUE/ΔT	hue variation with temperature	T_{amb} = 0 to +70°C	–	0	–	deg
R	value of resistor connected to V_P to switch the PAL decoder and to obtain a chrominance input signal for the TDA8395		–	22	–	kΩ
$V_{O(p-p)}$	chrominance output signal to the TDA8395 (peak-to-peak value)		–	330	–	mV
DEMODULATORS						
$V_{30(p-p)}$	–(R-Y) output signal amplitude (peak-to-peak value) (pin 30)	note 33	–	0.525	–	V
$V_{31(p-p)}$	–(B-Y) output signal amplitude (peak-to-peak value) (pin 30)	note 33	–	0.675	–	V
G	gain ratio of both demodulators G–(B-Y)/G–(R-Y)		1.6	1.78	1.96	
	spread of signal amplitude ratio	PAL/NTSC	–1	–	+1	dB
Z_O	output impedance –(R-Y)/–(B-Y) output		–	–	250	Ω
B	bandwidth of demodulators	–3 dB	–	1	–	MHz
$V_{30,31(p-p)}$	residual carrier output (peak-to-peak value)	f = f_{OSC}				
	–(R-Y) output		–	–	tbf	mV
	–(B-Y) output		–	–	tbf	mV
$V_{30,31(p-p)}$	residual carrier output (peak-to-peak value)	f = $2f_{OSC}$				
	–(R-Y) output		–	–	tbf	mV
	–(B-Y) output		–	–	tbf	mV
$V_{30(p-p)}$	H/2 ripple at –(R-Y) output (peak-to-peak value)		–	–	25	mV
$\Delta V_O/\Delta T$	change of output signal amplitude with temperature		–	0.1	–	%/K
$\Delta V_O/\Delta V_P$	change of output signal amplitude with supply voltage		–	–	±0.1	dB
φ_e	phase error in the demodulated signals		–	–	5	deg

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
COLOUR DIFFERENCE MATRICES IN CONTROL CIRCUIT						
PAL/SECAM mode with TDA8395 (–(R-Y) and –(B-Y) not affected)						
	G-Y/–(R-Y)		–	–0.51 ±10%	–	
	G-Y/–(B-Y)		–	–0.19 ±25%	–	
NTSC mode; the CD matrix results in the following signals (nominal hue setting)						
	–(B-Y): 1.14/–10° = $1.12U_R$ – $0.20V_R$ –(R-Y): 1.14/100° = $-0.20U_R$ + $1.12V_R$ G-Y: 0.30/235° = $-0.25V_R$ – $0.17U_R$					
REFERENCE SIGNAL OUTPUT FOR TDA8395 (PIN 32)						
f_{ref}	reference frequency		–	4.43	–	MHz
$V_{32(p-p)}$	output signal amplitude (peak-to-peak value)		0.2	0.25	0.3	V
V_O	output level	PAL/NTSC identified	–	1.5	–	V
		no PAL/NTSC; SECAM (by TDA8395) identified	–	5.0	–	V
I_{32}	required current to stop PAL/NTSC identification circuit during SECAM		150	–	–	µA
Control part						
SATURATION CONTROL; NOTE 20 (PIN 26)						
CR_{SAT}	saturation control range	see also Fig.6	52	–	–	dB
ΔSAT/ΔV	saturation level change	V_P = ±10%	–	0	–	%
CONTRAST CONTROL; NOTE 20 (PIN 25)						
CR_{CON}	contrast control range	see also Fig.7	–	20	–	dB
	tracking between the three channels over a control range of 10 dB		–	0.3	0.5	dB
BRIGHTNESS CONTROL (PIN 17)						
CR_{BRI}	brightness control range	see also Fig.8	–	±1.0	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB AMPLIFIERS (PINS 18, 19 AND 20)						
$V_{18,19\ 20(p-p)}$	output signal amplitude (peak-to-peak value)					
	at nominal luminance input signal and nominal contrast	note 20	tbf	4.0	tbf	V
	for the RED channel with nominal settings for contrast and saturation control and no luminance signal to the –(R-Y) input (PAL)		tbf	4.2	tbf	V
$V_{18,19,20bl}$	blanking level at the RGB outputs		0.7	0.8	0.9	V
$V_{18,19,20b}$	black level at the RGB outputs	note 20	–	1.3	–	V
V_{max}	maximum peak white level	note 34	–	6.0	–	V
I_O	available output current		5.0	–	–	mA
Z_O	output impedance		–	100	–	Ω
I_{source}	current source of output stage		2.0	tbf	–	mA
	relative spread between the RGB output signals		–	–	7	%
S/N	signal-to-noise ratio of output signals	note 35				
	for RGB input		–	60	–	dB
	for CVBS input		50	–	–	dB
$f_{res(p-p)}$	residual frequency (peak-to-peak value)					
	at f_{OSC} in the RGB outputs		–	–	25	mV
	at 2 x f_{OSC} plus higher harmonics in the RGB outputs		–	–	25	mV
V_{diff}	difference in black level between the three outputs at nominal brightness		–	–	50	mV
V_b	black level shift with picture content		–	0	–	mV
$\Delta b/\Delta T$	variation of black level with temperature		–2	–	0	mV/K
$\Delta b/\Delta_{CON}$	variation of black level over contrast range at nominal saturation		–	–	tbf	mV
$\Delta b/\Delta_{SAT}$	variation of black level over saturation range at nominal contrast		–	–	tbf	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Δb	relative variation in black level between the three channels during variations of:					
	supply voltage (±10%) at nominal saturation		–	–	tbf	mV
	saturation (50 dB) at nominal contrast		–	–	tbf	mV
	contrast (20 dB) at nominal saturation		–	–	tbf	mV
	brightness (±0.5 V) at nominal controls		–	–	tbf	mV
	±45° tint, nominal saturation and contrast		–	–	tbf	mV
V_{diff}	differential drift of black level over a temperature range of 40 °C		–	–	10	mV
B	bandwidth of output signals	at –3 dB				
	for RGB input		8	–	–	MHz
	for CVBS input	f_{osc} = 3.58 MHz	–	2.8	–	MHz
	for CVBS input	f_{osc} = 4.43 MHz	–	3.5	–	MHz
	for S-VHS input		8	–	–	MHz

Notes to the characteristics

1. It is possible to start the horizontal oscillator when a current of 5.5 mA is supplied to this pin. In this condition the main part of the IC is not active and this results in the frequency of the oscillator not being controlled at the correct value. Consequently, the oscillator frequency will be higher than normal, the maximum deviation will be 60%. When the start-up function is used the maximum voltage on pin 36 must be limited to 8.8 volts.
2. On set AGC.
3. Measured with 0 dB = 500 µV.
4. Measured at 10 mV (RMS) top sync input signal.
5. So called projected zero point, i.e. with switched demodulator.
6. Measured according to the test line given in Fig.9. For the differential phase test the peak white setting is reduced to 87%.
   - the differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   - the phase difference is defined as the difference in degrees between the largest and smallest phase angle.
7. This figure is valid for the complete video signal amplitude (peak white-to-black), see Fig.10.
8. The test set-up and input conditions are given in Fig.11. The figures are measured at an input signal of 10 mV (RMS).
9. Measured with a source impedance of 75 Ω, where:

$$S/N = 20 \log \frac{V_O\,(black\text{–}to\text{–}white)}{V_{n\,RMS)}\,(B = 5\ MHz)}$$

10. The AFC slope is directly related to the Q-factor of the demodulator tuned circuit. The given AFC steepness is obtained with a Q-factor of 60. When a lower steepness is required this can be obtained by connecting an external resistor to the AFC output (the output impedance is 50 kΩ). The AFC off-set is tested with a double sideband input signal and with the reference tuned circuit tuned to minimum AGC voltage (optimal tuning for the demodulator).
11. For positive modulated signals the FM sound demodulator is not required. This is because the sound signal is amplitude modulated. The circuit is therefore switched to positive modulation via the de-emphasis pin (pin 1). When switched to positive modulation the audio switch is set to "external" so that the demodulated audio signal can be supplied to the input. The option between AM sound and SCART audio signals is achieved by means of an external switch.
12. The sound IF input is combined with the AF volume control. The IF signal is internally AC coupled to the limiter amplifier. The volume control voltage must be supplied to this pin via a resistor.
13. V_i = 100 mV (RMS); FM: 1 kHz, $\Delta f = \pm 50$ kHz.
14. V_i = 50 mV (RMS), 5.5 MHz;
    FM: 70 Hz ±50 kHz deviation
    AM: 1 kHz at 30% modulation
15. V_i = 100 mV (RMS), 5.5 MHz; FM: 1 kHz, ±17.5 kHz deviation; 15 kHz bandwidth; audio attenuator at – 6 dB.
16. Audio attenuator at – 20 dB; temperature range 10 to 50 °C.
17. The audio and CVBS switches are controlled via the chrominance input pin. Table 1 lists the various possibilities.

    When the DC voltage has a value between 3 and 5 V the switches are set to the S-VHS position. The chrominance trap is then switched off and separate Y and chrominance signals have to be applied to the inputs (the audio switch is set to external in this condition). The audio switch is also set to external when the IF amplifier is switched to positive modulation (see also note 11).
18. Signal with negative-going sync. Amplitude includes sync pulse amplitude.
19. Burst amplitude; for a colour bar with 75% saturation the chrominance signal amplitude is 660 mV (p-p).
20. Nominal contrast is specified as maximum contrast –3 dB. Nominal saturation as maximum –10 dB. The nominal brightness control voltage is 2.5 V.
21. When the data blanking input pulse exceeds a level of 4 V the RGB outputs are blanked. In this condition it is possible to supply "On-Screen-Display" signals to the outputs. This blanking overrules both the internal and external RGB signals.
22. The –3 dB bandwidth of the circuit can be calculated by means of the following equation:

    $$f_{-3\ dB} = f_{OSC}\left(1 - \frac{1}{2Q}\right)$$
23. When SECAM signals are received (only valid when the TDA8395 is applied) the luminance delay time is increased to 360 ns to compensate for the delay in the SECAM decoder.
24. The amplitude response curve can be expressed as follows:

    $A(f) = 1 + K1 - \cos(180\ x\ f/3.8\ MHz)$

    and is realised with a transversal peaking filter having delay sections of 130 ns (during SECAM reception 200 ns) each.
    In the "neutral" setting K = 0 and in the minimum setting K = –0.5.

    The peaking signal amplifier is linear for 250 ns step input signals up to 50 IRE units (With a standard signal 100 IRE units = 700 mV black-to-white at 1 V top sync level). For higher amplitudes the marginal gain is reduced.
25. Slicing level independent of sync pulse amplitude.

26. The horizontal and vertical sync are stable while processing Copy Guard signals and signals with phase shifted sync pulses (stretched tapes). Trick mode conditions of the VCR will also not disturb the synchronization.
27. Picture shift can be obtained by means of a variable external load on the second phase detector. The control range is ±2 μs; the required current for this phase shift is ±6 μA.
28. The timing pulses for the vertical ramp generator are obtained from the horizontal oscillator via a divider circuit. This divider circuit has 2 search modes of operation;

    The 'large window' mode is switched on when the circuit is not synchronized or, when a non-standard signal is received (the number of lines per frame in the 50 Hz mode is between 311 and 314 and in the 60 Hz mode between 261 and 264). In the search mode the divider can be triggered between line 244 and line 361 (approximately 45 to 64.5 Hz)

    The 'narrow window' mode is switched on when more than 15 successive vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the retrace of the vertical ramp generator is started at the end of the window. Consequently, the disturbance of the picture is very small. The circuit will switch back to the search window when, for 6 successive vertical periods, no sync pulses are found within the window.
29. This precorrection is intended to compensate for non-linearity of AC coupled vertical output stages. The value given indicates the amplitude of the correction waveform with respect to the sawtooth amplitude.
30. At the given chrominance input voltage (related to CVBS2) of 660 mV (p-p) (colour bar with 75% saturation i.e. burst signal amplitude 300 mV (p-p)) the dynamic range of the ACC is +6 and −20 dB.
31. All frequency variations are referred to 3.58/4.43 MHz carrier frequency.
32. The hue control pin has a double function. When the control voltage has a value of 0 to 5 V (normal control range) the hue can be controlled when NTSC signals are decoded. When this voltage is increased to a value greater than 5.5 V the decoder is forced to the PAL standard. When this pin is connected to the positive supply line via a 22 kΩ resistor the selected CVBS signal, of the CVBS switch, is available. This signal can be applied to the SECAM decoder TDA8395.
33. The −(R-Y) and −(B-Y) signals are demodulated with the 90° phase difference of the reference carrier and a gain ratio −(B-Y)/−(R-Y) = 1.78. The matrixing to the required signals is achieved in the control part.
34. When one of the three output signals exceeds this level the gain of the amplifiers is reduced. This is achieved by a reduction of contrast and thus avoids clipping of the output signals. The discharge current at pin 25 is 100 μA. When the black level exceeds a value of 2 V the maximum peak-to-peak value of the video output signal will be less than 4 V (p-p); this is due to the operation of the peak-white limiter.
35. The signal-to-noise ratio is specified as a peak-to-peak signal with respect to RMS noise (bandwidth 5 MHz).

Table 1 Audio and CVBS switch selection

LEVEL (pin 16)	INTERNAL CVBS	EXTERNAL CVBS/Y	CHROMINANCE	CHROMINANCE TRAP	AUDIO
DC ≤ 0.5 V	ON	OFF	OFF	ON	internal
3 ≤ DC ≤ 5 V	OFF	ON (Y)	ON	OFF	external
DC ≥ 7.5 V	OFF	ON (CVBS)	OFF	ON	external

QUALITY SPECIFICATION

Quality level according to URV 4-2-59/601.

SYMBOL	PARAMETER	RANGE A	RANGE B	UNIT
ESD	protection circuit specification note 1	2000	500	V
		100	200	pF
		1500	0	Ω

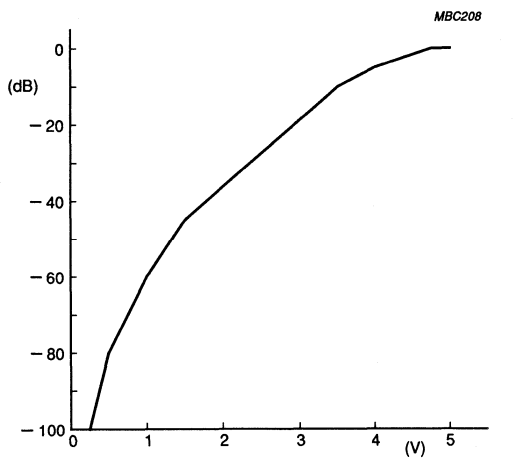


Fig.3 Volume control curve.

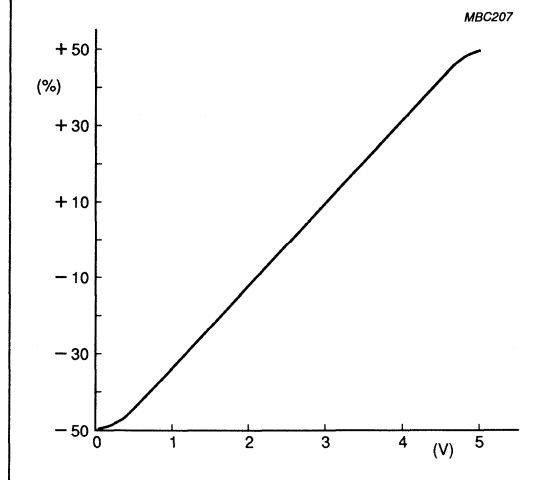


Fig.4 Peaking control curve.

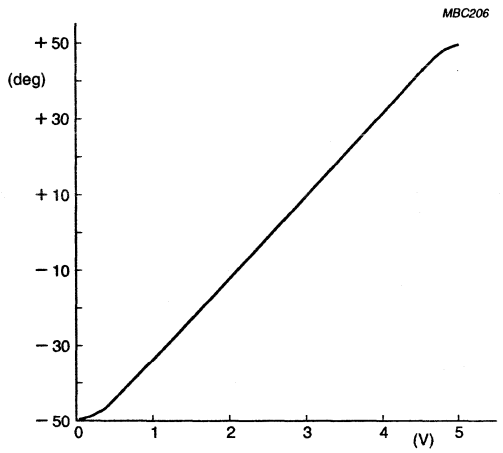


Fig.5 Hue control curve.

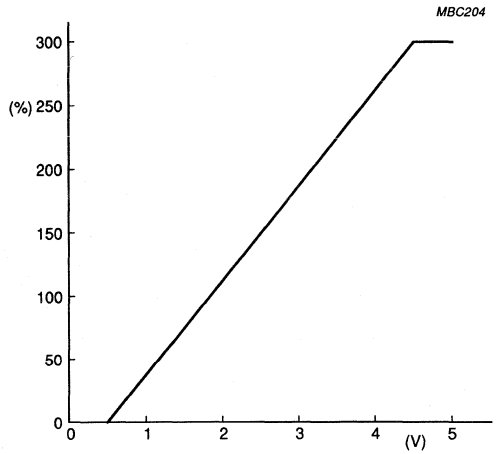


Fig.6 Saturation control curve.

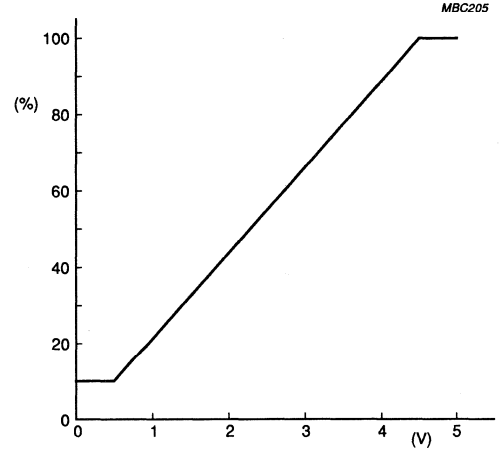


Fig.7 Contrast control curve.

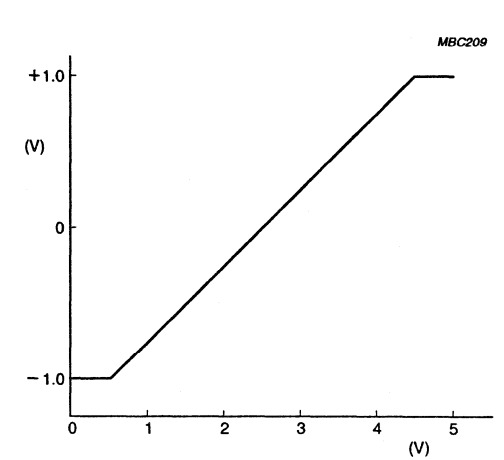


Fig.8 Brightness control curve.

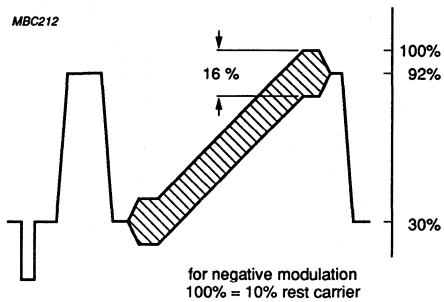


Fig.9 Video output signal.

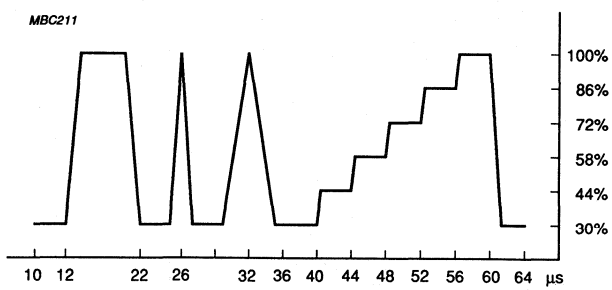
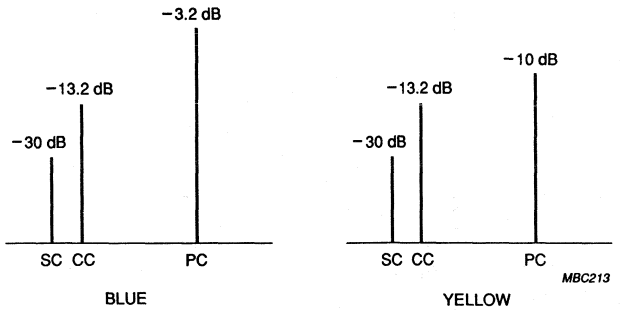
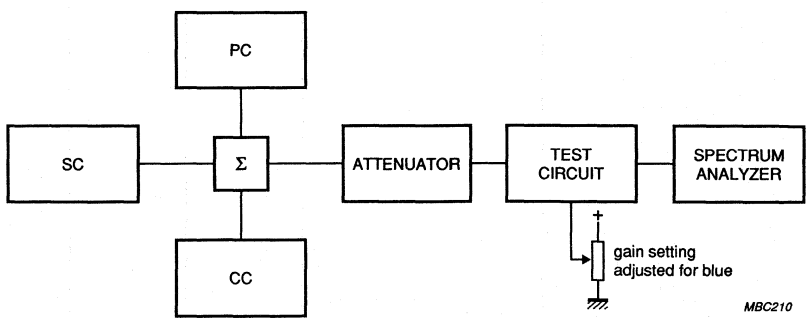


Fig.10 Test signal waveform.



Input signal conditions; SC = sound carrier; CC = colour carrier; PC = picture carrier
All amplitudes with respect to top sync level



$$\text{Value at } 0.92 \text{ or } 1.1 \text{ MHz} = 20 \log \frac{V_o \text{ at } 3.58 \text{ or } 4.4 \text{ MHz}}{V_o \text{ at } 0.92 \text{ or } 1.1 \text{ MHz}} + 3.6 \text{ dB}$$

$$\text{Value at } 2.66 \text{ or } 3.3 \text{ MHz} = 20 \log \frac{V_o \text{ at } 3.58 \text{ or } 4.4 \text{ MHz}}{V_o \text{ at } 2.66 \text{ or } 3.3 \text{ MHz}}$$

Fig.11 Test set-up intermodulation.

CONTROL CIRCUIT FOR SWITCHED MODE POWER SUPPLIES

GENERAL DESCRIPTION

The TDA8380 is an integrated circuit intended for use as a control circuit in low-cost switched mode power supplies for television, monitors and small industrial equipment. The TDA8380 operates using duty factor regulation in the fixed frequency mode.

Features

- A low-current initialization circuit (maximum 150 μA) which can be switched off
- A bandgap reference generator
- Circuitry for slow-start combined with an accurate setting of the maximum duty factor (D_{max})
- Programmable low supply voltage protection with one default value
- High supply protection circuitry
- Error amplifier with a transfer characteristic generator (TCG)
- Protection against open- and short-circuited feedback loop
- An overload voltage foldback
- Primary current protection circuitry for both cycle-by-cycle and trip mode
- Protection against transformer saturation
- A direct drive output stage (sink current 2.5 A, source current 0.75 A)
- Anti-double pulse logic
- Protected against damage as a result of a short-circuited high-voltage transistor
- RC oscillator with synchronization input

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	–	14	–	V
Supply current	I_{CC}	–	–	15	mA
Output pulse repetition frequency range	f_o	10	–	100	kHz
Operating ambient temperature range	T_{amb}	−25	–	+ 70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

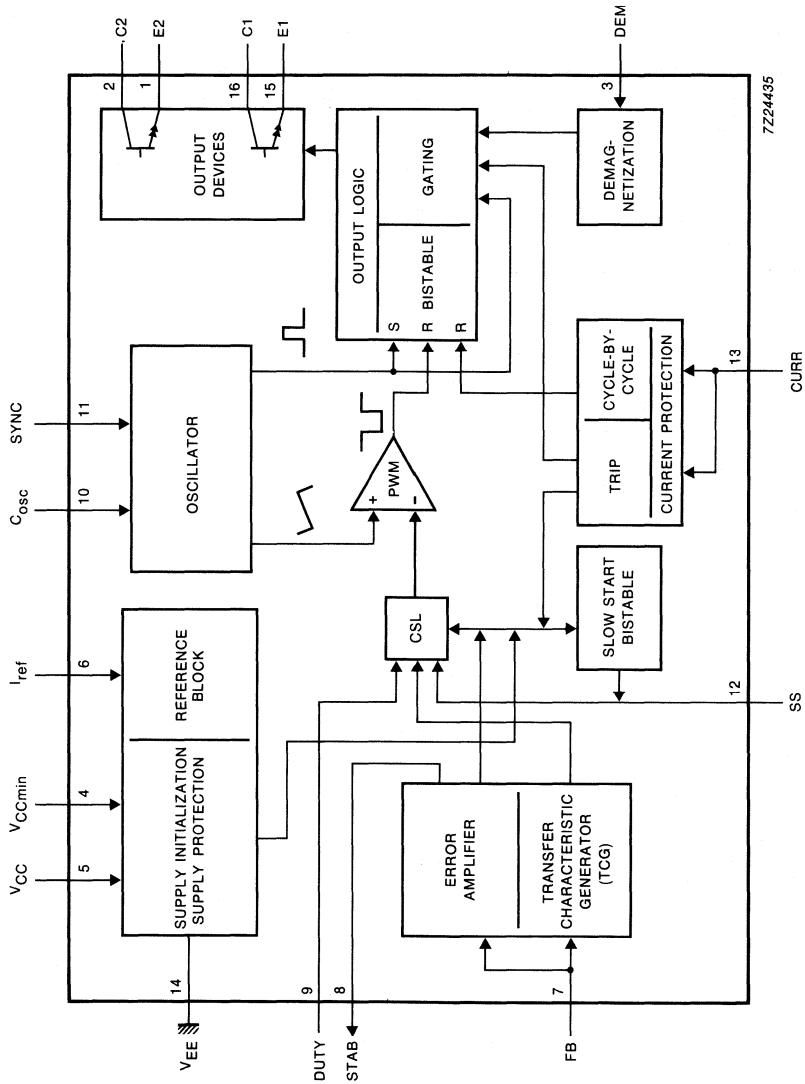


Fig.1 Block diagram.

PINNING

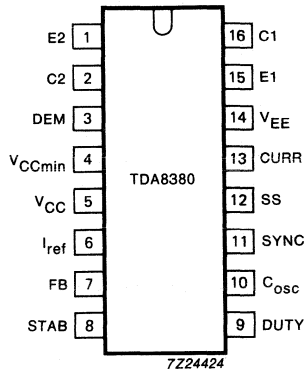


Fig.2 Pinning diagram.

DEVELOPMENT DATA

1	E2	Emitter of output source transistor
2	C2	Collector of output source transistor
3	DEM	Demagnetization sense input
4	V_{CCmin}	Minimum V_{CC} threshold setting
5	V_{CC}	Supply voltage
6	I_{ref}	Reference current setting
7	FB	Feedback input
8	STAB	Output error amplifier
9	DUTY	Pulse width modulator input
10	C_{OSC}	Oscillator capacitor
11	SYNC	Synchronization input
12	SS	Maximum duty factor (D_{max}) setting plus slow-start
13	CURR	Input current protection
14	V_{EE}	Ground
15	E1	Emitter of output sink transistor
16	C1	Collector of output sink transistor

FUNCTIONAL DESCRIPTION

The TDA8380 is a control circuit which generates the pulses required to drive the switching transistor in a switched mode power supply (SMPS).

Supply

This device is intended to be used on the primary side of the power supply and can be supplied via a take-over (auxiliary) winding on the transformer.

The device is initialized via a high value resistor connected between the rectified mains voltage and the device's supply pin (pin 5), which causes the capacitor connected to this pin to charge slowly. When the voltage exceeds the initialization level (typically 17 V) the device will start up and the duty cycle will be slowly increased by the slow-start circuit. After a short period the take-over winding will supply the device. The value of the resistor is normally defined by the time taken to charge the capacitor. A one second delay between switching on and operation of the power supply is acceptable in most cases.

The operating voltage range is from 9 to 20 V. The supply pin is protected by a 23 V Zener diode. The supply protection circuit is activated once the Zener diode is conducting. The slow-start procedure begins after initialization, until then the output is off. The current drawn by the device during the initialization period is less than 150 μA.

When the supply voltage falls below the minimum trip level, the device switches off and the start-up procedure is repeated. The minimum voltage supply threshold setting (V_{CCmin}) can be set externally with a resistor connected between the V_{CCmin} pin (pin 4) and ground (pin 14) (see Fig.3).

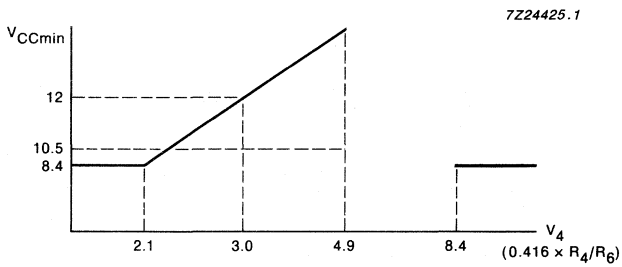


Fig.3 Trip level setting of minimum V_{CC} protection level.

V_{CCmin} can be set between 8.4 V (an internally fixed overriding protection level) and 17 V by means of an external resistor connected to pin 4.

When choosing the initialization and minimum supply voltages the following should be taken into account:

- The difference between the two voltages should be large enough to enable a supply voltage dip during start-up.
- The value of the minimum supply voltage should be high enough to ensure that the high-voltage transistor is correctly driven. A high protection level makes it possible to have a large resistor value in series with the base drive.

For battery line input operation, the V_{CCmin} pin is connected to V_{CC}, the start-up circuit is then inhibited and the device starts operating when V_{CC} exceeds the 8.4 V protection level (this level has a hysteresis of approximately 50 mV). The device draws current continuously under these conditions.

Reference block

A bandgap based reference generates a stabilized voltage of 7 V to supply most of the device's internal circuits, this decreases chip size and increases reliability. The only circuits connected to V_{CC} are:

- The initialization circuit
- The output circuitry
- The series transistor of the stabilized voltage

By means of a resistor (R_6) connected to the I_{ref} input a reference current is defined which determines six other device settings.

Part of the reference current is used to charge the oscillator capacitor (C_{10}), therefore, the charging time is proportional to $R_6 \times C_{10}$. The maximum duty factor (D_{max}) is set by the resistor connected to pin 12 (R_{12}) and is defined by the ratio R_6/R_{12}. The minimum supply voltage (pin 5) set by the resistor (R_4) at input V_{CCmin} is defined by: $4/6 \times V_6 \times R_4/R_6$.

Oscillator

The oscillator capacitor is charged and discharged between the high and low voltage levels as defined by the bandgap reference (high voltage typically 5 V and low voltage typically 1.4 V). The charge current is 1/6 of the reference current, the discharge current having the same value as the reference current. The period is therefore defined by $10 \times R_6 \times C_{10}$.

The oscillator flyback pulse is used to set the bistable in the output logic, however the output remains low until the positive ramp starts (see Fig.4). The oscillator can be synchronized by means of the SYNC pin. When this pin is connected to V_{CC}, the oscillator is free running. When it is between 0.85 and 5.6 V, the oscillator stops at the low voltage level prior to the next positive ramp.

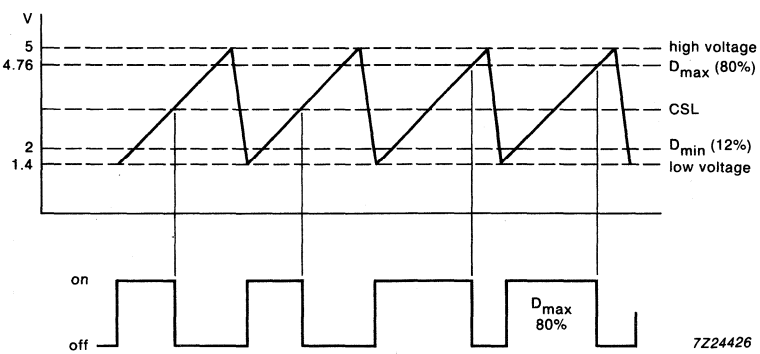


Fig.4 Oscillator levels.

FUNCTIONAL DESCRIPTION (continued)

Synchronization

The synchronization input (pin 11) can be driven by either an optocoupler or a loosely coupled pulse transformer.

Figure 5(a) illustrates synchronization using the 0.85 V threshold and a digital signal connected to the SYNC input (for example, an optocoupler between pin 11 and V_{CC}); the duty factor of the pulse is not very important. The oscillator starts at the first negative going edge of the sync. signal after the low voltage level has been reached. The synchronization frequency must be lower than the free running frequency. Synchronization must never affect the period time as this will corrupt the setting of the maximum duty factor.

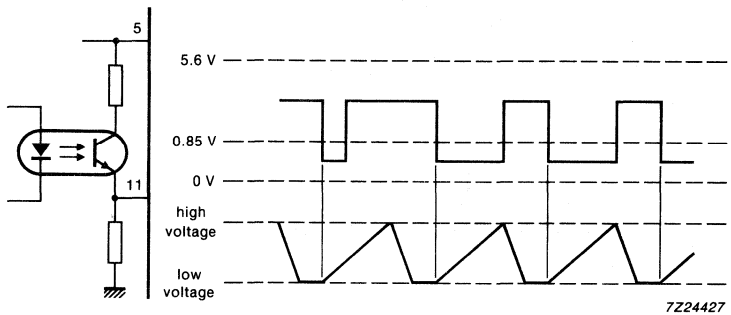


Fig. 5(a) DC coupled synchronization using the 0.85 V level.

In Fig.5(b) the disabling threshold (5.6 V) is used for synchronization. In this case the oscillator starts at the positive going edge of the sync. signal.

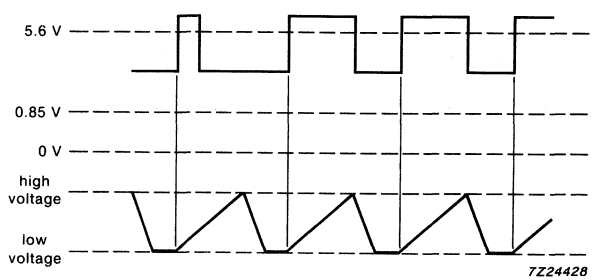
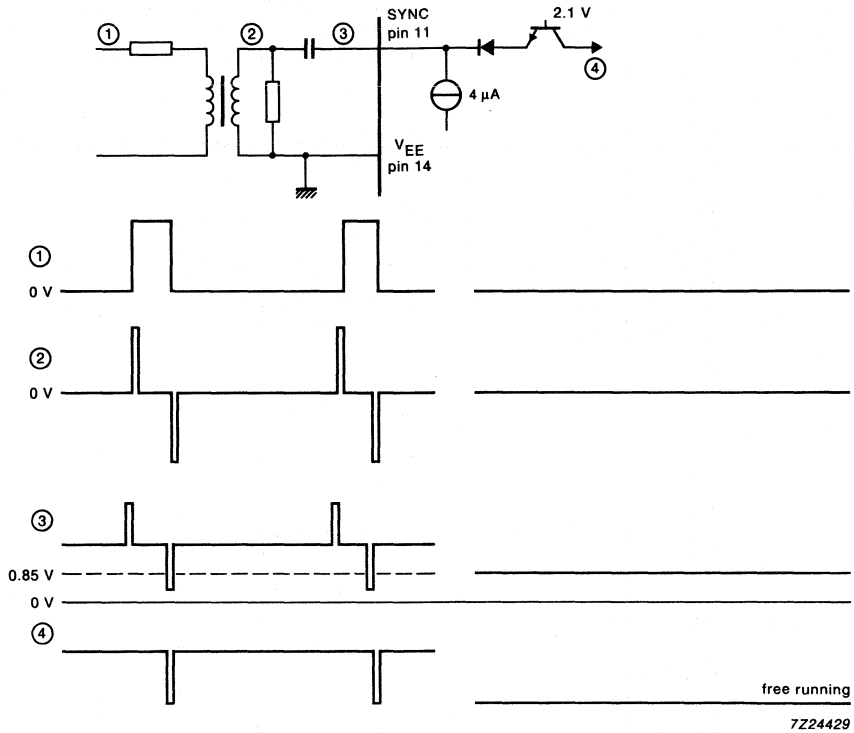


Fig.5(b) DC coupled synchronization using the 5.6 V level.

Figure 6 illustrates synchronization using a pulse transformer. Internal circuitry causes a DC shift which informs the device that synchronization pulses are present (spikes around 0 V at the output of the pulse transformer) or not present (DC 0 V at the output of the pulse transformer). When synchronization is not used the SYNC pin must be connected to V_{CC}, it must not be connected directly to ground or left open.



Synchronization pulses present. Synchronization pulses not present.

Fig.6 Synchronization using a pulse transformer.

FUNCTIONAL DESCRIPTION (continued)

Error amplifier

The error amplifier compares the feedback voltage of the SMPS with a reference voltage (nominally 2.5 V). The amplifier output at pin 8 enables gain setting. The amplifier is stable for a gain greater than 20 dB.

The output of the error amplifier is not internally connected to the Pulse Width Modulator (PWM). One input to the PWM is available at the DUTY input (pin 9) via the Control Slicing Level (CSL) circuit. Normally the STAB and DUTY pins are connected together, but direct driving of pin 9 via an optocoupler from the secondary side is also possible. A type of current mode control can be achieved by mixing the STAB signal with the primary current signal before applying it to the DUTY input.

The feedback (FB) input (pin 7) is used as the input to the Transfer Characteristic Generator (TCG) circuit which ensures well defined duty factors at low FB voltages; a voltage foldback is an inherent characteristic. In Fig.7, the duty factor is shown as a function of the voltages at the FB, DUTY and SS inputs. The input which gives the lowest duty factor overrides the others.

The left hand curve is passed through during a slow-start (via the slow-start input pin 12) when the duty cycle slowly increases linearly with respect to V_{12}. The right-hand curve is passed through at start-up. The FB voltage slowly increases from zero and the duty factor, starting at 12%, increases until the maximum duty factor (D_{max}) is reached. A few hundred millivolts later, the FB voltage reaches the start of the regulation curve which is at approximately 2.5 V. The plateau area between reaching D_{max} and starting the regulation curve is kept as small as possible (typically 200 mV).

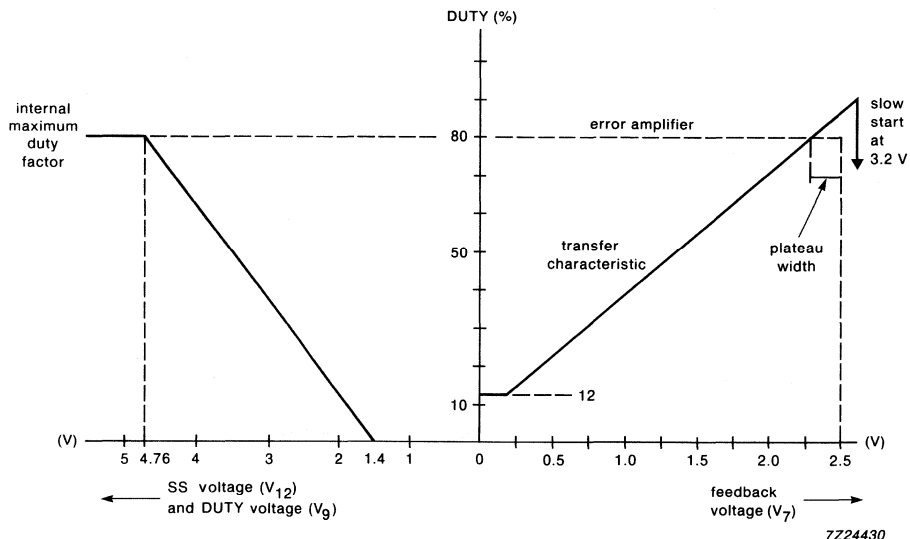


Fig.7 The duty factor as a function of the FB, SS and DUTY voltages.

Due to the characteristics of the TCG, and the fact that an open FB input results in a low voltage at the FB input, open- and short-circuit feedback loops will result in low duty factors. When DC feedback is used across the error amplifier, the current capability of the error amplifier must be considered when determining the feedback resistor value.

When the input to the PWM (pin 9) is driven by an optocoupler, the TCG can be used when a rough primary voltage is applied to the FB input. In this situation an open feedback loop will cause an increase in the FB voltage as the duty factor rises to its maximum. As soon as the FB voltage exceeds the reference by 0.7 V, the slow-start is triggered.

Demagnetization sense circuit

To enable the SMPS to be kept in the non-continuous mode, an input is available which delays switch-on of the high-voltage transistor until the transformer currents have decayed to zero. This is an effective way of avoiding transformer saturation. The waveforms illustrated by Fig.8 show demagnetization with respect to the application diagram of Fig.12.

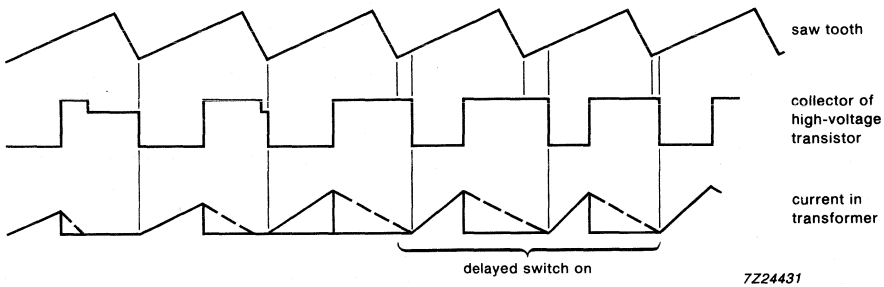


Fig.8 Demagnetization function.

As long as the voltage of the take-over (auxiliary) winding (also used for supplying the device) is above 0.6 V (V_3) the output will be prevented from switching on.

Over-current protection

The over-current protection circuit (pin 13) senses the voltage across resistor R_s (see Fig.12), which reflects the primary current. This generated voltage is negative-going as the emitter of the high-voltage power transistor is grounded (this circuit arrangement provides the IC with the best safeguard against a possible collector-emitter short-circuit in the power transistor). At pin 13, the negative voltage signal is shifted to a positive level by a voltage across resistor R_{13}. This voltage is set by the reference current at pin 13 and is defined by resistor R_6 at the I_{ref} input (pin 6) and = $1/6 \times V_{ref}/R_6$.
Therefore $V_{shift}(V_{R13}) = V_{ref}/6 \times R_{13}/R_6$ or nominal $0.416 \times R_{13}/R_6$ (V).

The positive current monitor voltage at pin 13 is compared with two voltage levels: the first level = 0.2 V and the second level = 0 V (see Fig.9).

The first trip level only switches off the high-voltage transistor for a cycle and puts the SMPS in a continuous cycle-by-cycle current protection mode.

The second trip level is only activated when the primary current rise is very fast which can occur during a short-circuited output. In this mode the high-voltage transistor is quickly switched off and the slow-start procedure is activated.

The difference between the first and second primary current peak levels is set by R_s:

$I_2 - I_1 = 0.2/R_s$.

The absolute peak values are set by R_6 and R_{13}:

$I_2 \times R_s = 0.416 \times R_{13}/R_6$ or

$I_1 \times R_s = (0.416 \times R_{13}/R_6) - 0.2$

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Over-current protection (continued)

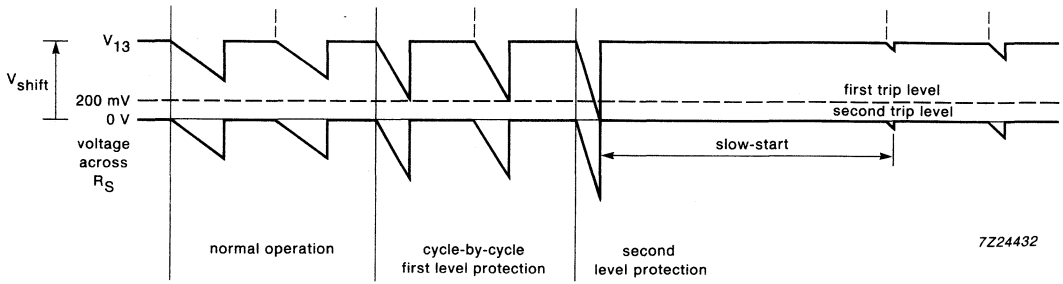


Fig.9 Current protection.

Slow-start circuit

A slow-start occurs:

- At Switch-on of the SMPS
- After a current trip as described in the section **Over-current protection**
- After a low or high V_{CC} trip.

The capacitor at the SS input is discharged and the slow-start bistable is reset when the voltage at the SS input falls below 0.5 V after which the circuit is ready for a slow-start. The dead time (during which the capacitor at the SS input is being charged to the 1.4 V lower level of the sawtooth) before duty cycle regulation starts is minimal. The SS input can also be used for D_{max} setting by connecting a resistor to ground. The voltage across this resistor is then limited to $1/6 \times V_{ref} \times R_{12}/R_6$.

Output stages

The output stage consists of two NPN darlington transistors, their collector and emitter connected to separate pins (see Fig.12). The top transistor is capable of sourcing a maximum of 0.75 A to the high-voltage transistor while the bottom transistor can sink peak currents up to 2.5 A.

For low currents up to 10 mA, the saturation voltage of the sink darlington transistor is similar to that of a single transistor (see Fig.10). During switching of this transistor dV/dt is internally limited to reduce interference.

Care should be taken with the external wiring of the output pins to avoid oscillation or interference due to parasitic inductance and wire resistance.

During start-up a small current flows from V_{CC} to E2 to precharge the series capacitor at the output (see Fig.12).

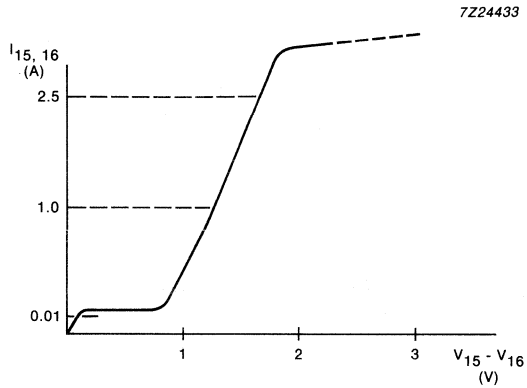


Fig.10 Saturation curve.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Voltage					
pin 5 (V_{CC})		−0.5	–	20	V
pins 1, 2, 4 and 16		−0.5	–	V_{CC}	V
pins 3 and 13		−0.5	–	0.5	V
pins 7 and 9		−0.5	–	6.5	V
pin 11		0.6	–	V_{CC}	V
Currents					
pin 5 (V_{CC})		0	–	20	mA
pin 1		−0.75	–	0	A
pin 2		0	–	0.75	A
pins 3, 4, 6 to 8 and 10 to 12		−10	–	10	mA
pin 13		−200	–	10	mA
pin 15		−2.5	–	0	A
pin 16		0	–	2.5	A
Total power dissipation	P_{tot}	see Fig.11			
Operating ambient temperature range (for dissipation $\leqslant$ 1 W)	T_{amb}	−25	–	+ 70	°C
Storage temperature range	T_{stg}	−55	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a(max)} = 55$ K/W

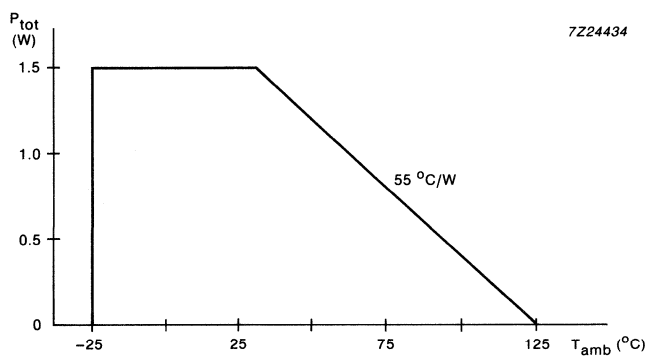


Fig.11 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C; reference resistor = 5 kΩ unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{CC}	9	–	20	V
Supply initialization level		V_5	15	17	18	V
High voltage protection		V_5	21	23	25	V
Internal fixed minimum protection level		V_5	7.9	8.4	8.9	V
Hysteresis		dV_{CC}	–	50	–	mV
Supply current operational		I_{CC}	–	–	15	mA
before initialization		I_{CC}	–	100	150	μA
Reference current (pin 4)	note 1	I_4	I_6/5.7	I_6/6	I_6/6.4	mA
Trigger level V_{CCmin} setting		V_5	$3.6V_4$	$3.8V_4$	$4.2V_4$	V
Clamp voltage	at 20 mA		21.5	23.5	25.5	V
Reference (pin 6)						
Reference voltage		V_{ref}	2.4	2.5	2.6	V
Current range		I_{ref}	200	–	800	μA
Reference voltage over I_6 range		dV_{ref}	–20	–	+ 20	mV
Error amplifier						
Error amplifier threshold	V_{CC} = 8.5 to 20 V	V_7	2.4	2.5	2.6	V
Input current		I_7	0	–	5	μA
Sink current output	at 1.2 V	I_8	1	–	–	mA
Source current output	at 5.5 V	I_8	80	100	130	μA
Open loop gain		A0	–	100	–	dB
Unity gain bandwidth		BW	–	5	–	MHz
Input DUTY current	note 1	I_9	I_6/5.7	I_6/6	I_6/6.3	mA
High FB protection level		V_7	2.95	3.1	3.25	V
Temperature coefficient of error amplifier threshold		dV_7/dT	–	100	–	10^{-6}/K
TCG function (see Fig.7)						
Transfer characteristic		dD/dV_7	–	32	–	%/V
Minimum duty factor		D_{min}	–	12	–	%
Plateau width		V_7	–	200	–	mV

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Slow-start function						
Transfer characteristic		dD/dV_{12}	–	23.8	–	%/V
Input current	note 1	I_{12}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Sink current during faults	at 0.5 V	I_{12}	8	–	–	mA
Internally fixed maximum duty factor		D_{max}	75	80	85	%
Clamp current	at V_{12} = 0.5 V	I_{12}	–	–2	–	mA
Output stage						
Source transistor						
Voltage drop with respect to V_{CC}	at 0.75 A	$V_{CC}-V_1$	–	2	–	V
Pull-up current	$V_{CC} - V_1$ = 15 V	$-I_1$	25	–	100	μA
Operating current range		$-I_1$	0	–	0.75	A
Sink transistor (see Fig.10)						
Saturation voltage						
at 2.5 A		$V_{16} - V_{15}$	–	2	–	V
at 1 A		$V_{16} - V_{15}$	–	1.5	–	V
at 10 mA		$V_{16} - V_{15}$	–	0.3	–	V
Leakage current	$V_{16} - V_{15}$ = 20 V	I_{16}	–	–	1	μA
Falling edge		$dV_{16\text{-}15}/dt$	–	0.2	–	V/ns
Operating current range						
Peak		I_{16}	0	–	2.5	A
Average		I_{16}	–	–	250	mA
Oscillator						
High level voltage		V_{10}	–	5	–	V
Low level voltage		V_{10}	–	1.4	–	V
Charge current	note 1	I_{10}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Frequency range		f_o	10	–	100	kHz
Frequency	R_6 = 5 kΩ C_{10} = 680 pF	f_o	27	28.5	30	kHz
Temperature coefficient of the frequency		df/dT	–	100	–	10^{-6}/K

parameter	conditions	symbol	min.	typ.	max.	unit
Synchronization						
Minimum synchronization pulse width		t_{11}	–	–	0.5	μs
Switching threshold		V_{11}	0.7	0.85	0.9	V
Input current		I_{11}	2.5	5.0	7.5	μA
Disabling threshold		V_{11}	4.2	5.6	6.0	V
Input voltage	at −700 μA	V_{11}	390	–	550	mV
Demagnetization input						
Pin voltage	at 0 A	V_3	–	690	–	mV
Input current	at 0 V	I_3	−30	−40	−55	μA
Current range of clamp circuits		I_3	−10	–	+ 10	mA
Clamp level positive	at 10 mA	V_3	–	950	–	mV
Clamp level negative	at −10 mA	V_3	–	−800	–	mV
Current protection						
Input current	note 1	I_{13}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
First threshold		V_{13}	190	200	210	mV
Second threshold		V_{13}	−10	0	10	mV
Delay to switch output via level 1	pulse at pin 13 from 300 mV to 100 mV; I_O = 500 mA	–	–	350	–	ns
Delay to switch output via level 2	pulse at pin 13 from 300 mV to −200 mV; I_O = 500 mA	–	–	300	500	ns
First threshold including R_{13} (12 kΩ)	R_6 = 5 kΩ	–	–	−800	–	mV
Threshold for open pin detection		V_{13}	–	3.5	–	V

Note to the characteristics

1. Over the current range of I_6; 200 to 800 μA.

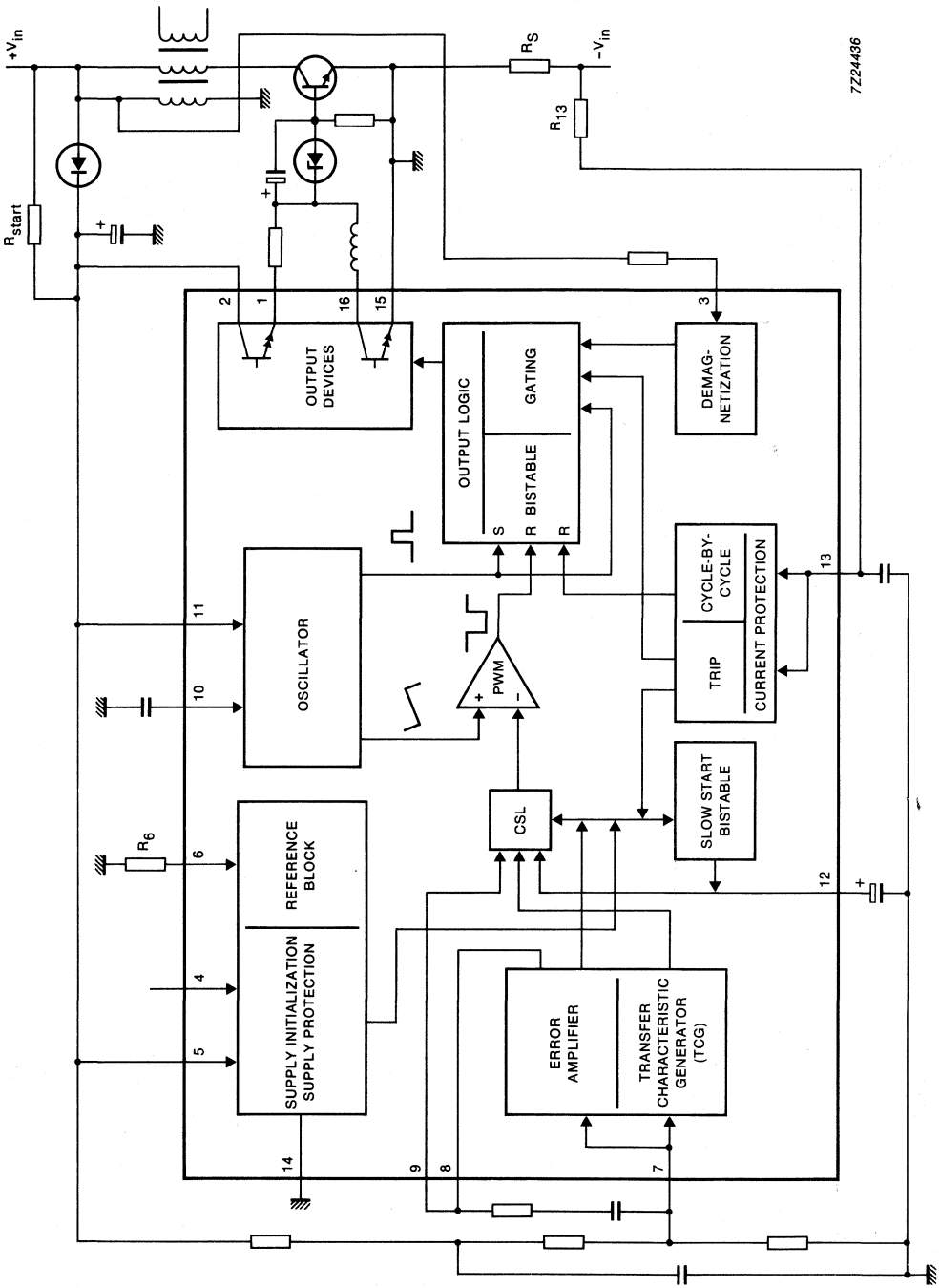


Fig.12 Simplified application diagram.

DEVELOPMENT DATA

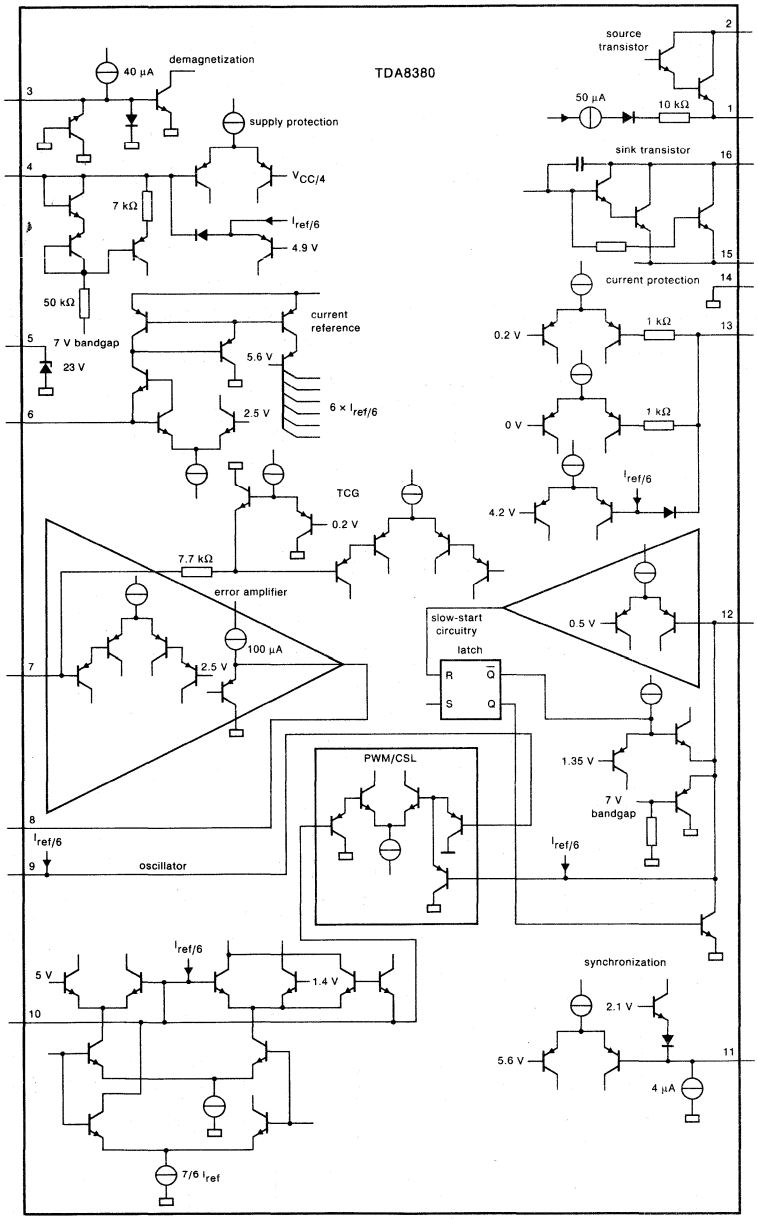


Fig.13 Input and output loading diagram.

Control circuit for a self-oscillating power supply (SOPS)

TDA8385

FEATURES

- Bandgap reference generator
- Slow-start circuitry
- Low-loss peak current sensing
- Overvoltage protection
- Hysteresis controlled stand-by function
- Error amplifier with gain setting
- Programmable transfer character generator
- Protection against open- and short-circuited feedback loop
- Overload current fold back characteristic
- LED driver
- Demagnetization protection
- Programmable determination of switch-on moment of switching transistor for low-switching losses
- Feed-forward input
- Regulation-indicator output
- Programmable minimum on-time of switching transistor
- Accurate peak-current setting

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8385	16	DIL	plastic	SOT38

GENERAL DESCRIPTION

The TDA8385 is an integrated circuit which is intended to be used in combination with the opto-coupler (CNR50) as a control unit for a self-oscillating power supply.

Control circuit for a self-oscillating power supply (SOPS)

TDA8385

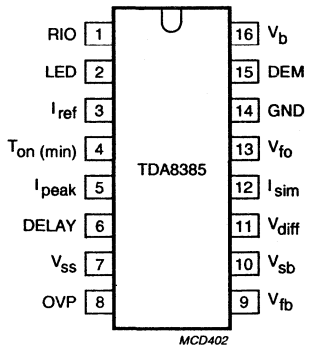


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RIO	1	regulation indicator output
LED	2	LED driver output
I_{ref}	3	current reference
$T_{on(min)}$	4	transistor on setting input
I_{peak}	5	peak current setting input
DELAY	6	delay setting
V_{ss}	7	slow start voltage input
OVP	8	over voltage protection
V_{fb}	9	feed back voltage input
V_{sb}	10	stand-by voltage input
V_{diff}	11	differential amplifier output
I_{sim}	12	current simulation input
V_{fo}	13	feed forward input
GND	14	0 V ground
DEM	15	demagnetization input
V_b	16	positive supply voltage

FUNCTIONAL DESCRIPTION

The TDA8385 can be divided into 10 functional blocks as shown in Fig.1.

I supply references
II sawtooth generator
III control part
IV pulse width modulator
V LED control
VI LED driver
VII slow start circuitry
VIII over voltage protection
IX stand-by circuit
X regulation-indicator output

These 10 functional blocks of Fig.1 contain sub-sections numbered 1 to 28 which are cross-referenced in the following description.

Supply references (Block I)

The TDA8385 is intended to be used on the secondary side of the self-oscillating power supply. It can be supplied either by an auxiliary winding of the transformer or an external supply e.g. 50 Hz transformer. Charging of the capacitor C_b (see Fig.15) takes place during transistor on-time (T_{on}; see Fig.16). During stand-by the IC is supplied by the stand-by voltage V_{sb} (pin 10). The operating voltage range is from 7.5 to 20 V. The supply current, inclusive drive current for the LED, is less than 20 mA. A bandgap based reference (2.5 V) generates a stabilized voltage V_{stab} of 3.9 V to supply all internal circuits of the IC except the LED driver. The LED driver is directly supplied by V_b. The reference block generates all the reference voltages in the circuit. By means of a resistor connected to pin 3, a reference current (I_{ref}) is defined. This current is reflected several times and is used to obtain IC-independent settings e.g. $T_{on(min)}$ setting, delay setting, charging and discharging of slow-start capacitor C_{ss}.

The power supply is released by the opto-coupler IC at an input voltage level, which is high enough to guarantee correct operation of the TDA8385 e.g. V_b = 10 V by sensing the mains voltage V_I. As soon as the SOPS switching transistor is conductive the capacitor C_b is charged. As long as the IC supply voltage is below 7.5 V the LED driver is blocked (see latch output Fig.1 block 28) in order to guarantee start-up of SOPS.

During the initialisation phase the quick-discharge-switch (Fig.1 block 27) set input of flip-flop 13 and reset input of flipflop 23 are also activated. As soon as the voltage of 7.5 V is reached the control functions of the IC are operative.
Hysteresis on the initialization level is 2.3 V as shown in Fig.3.

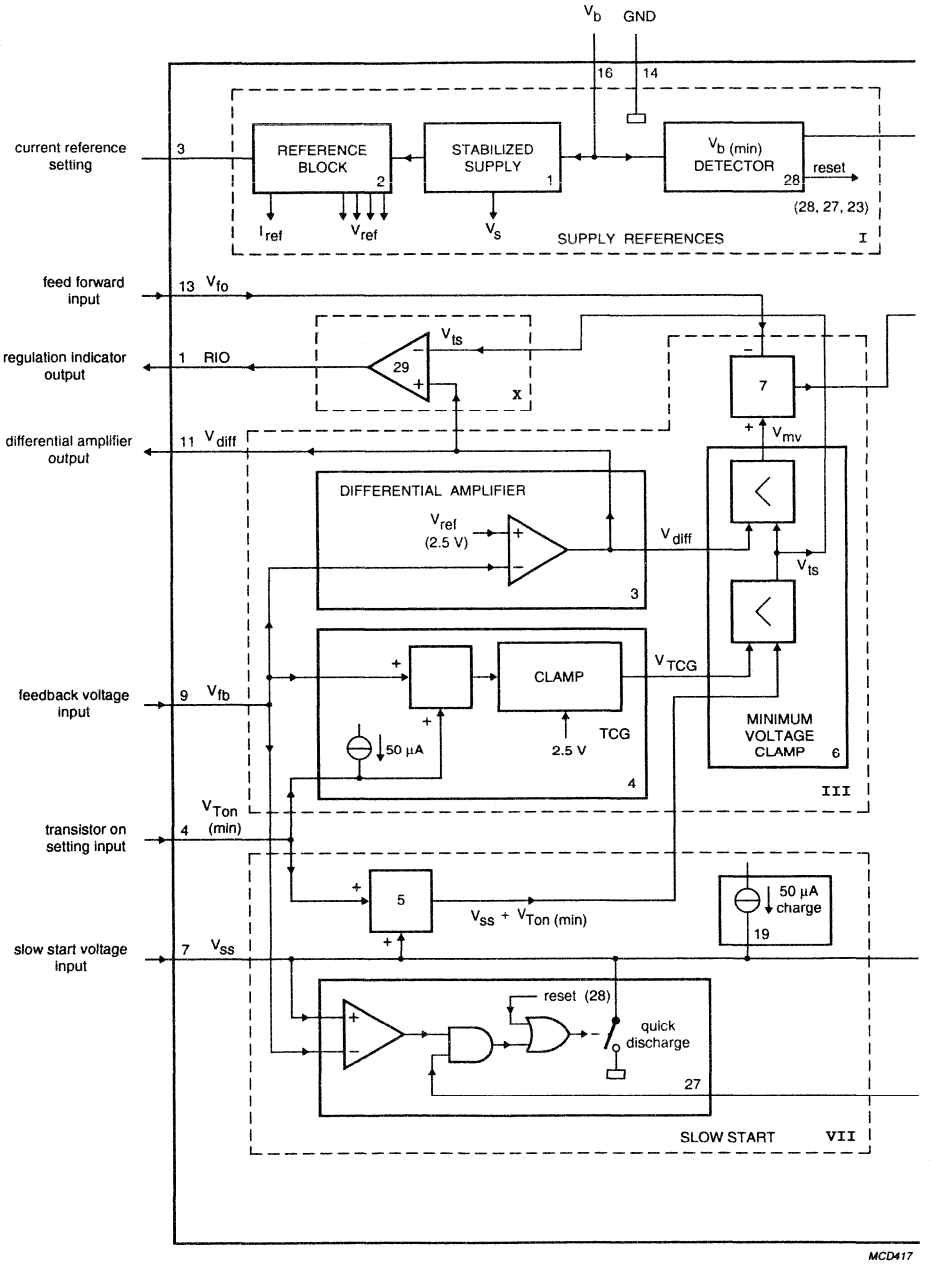


Fig.1 Block diagram.

Control circuit for a self-oscillating power supply (SOPS)

TDA8385

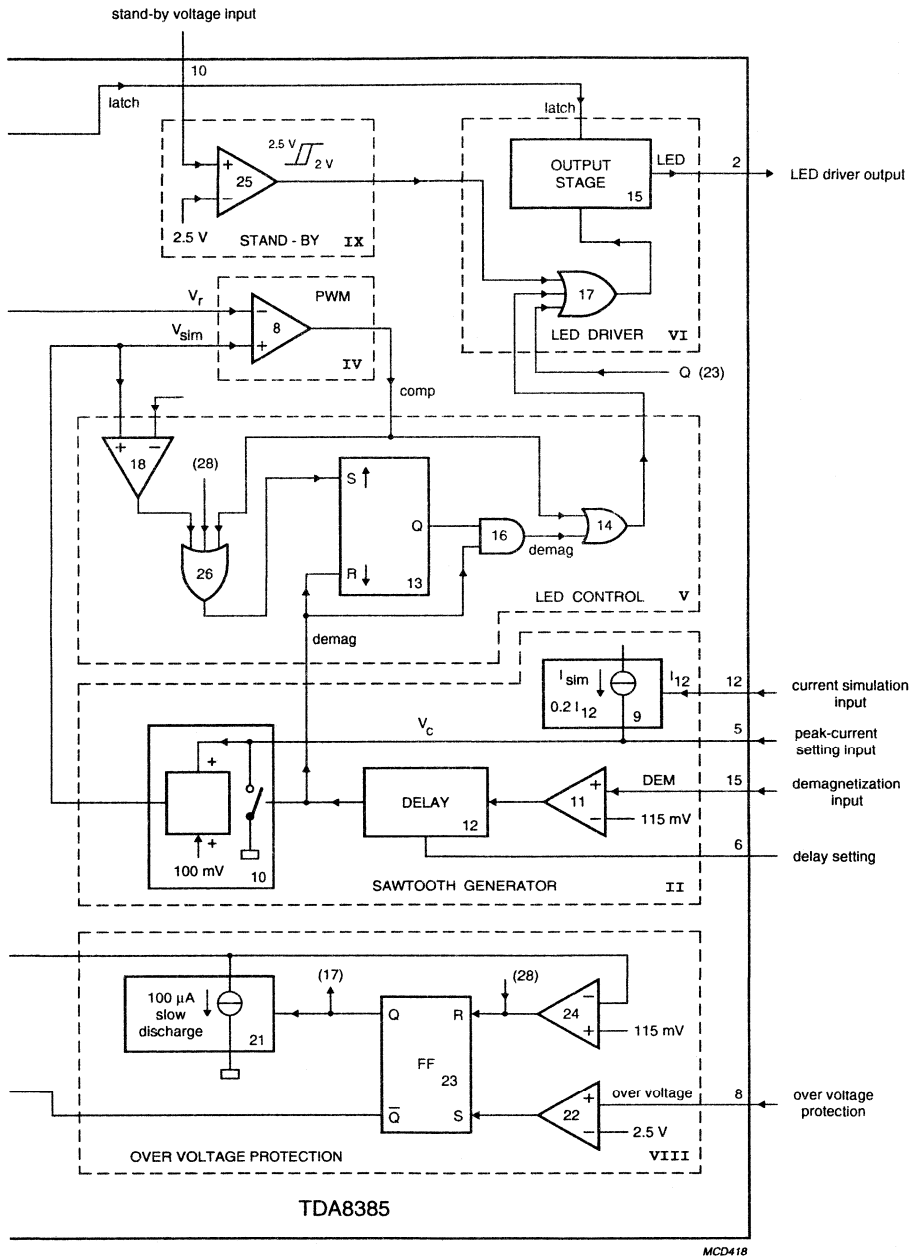


Fig.1 Block diagram.

Sawtooth generator (Block II)

CURRENT SIMULATION

The current of the power supply switching transistor is detected on the secondary side by an indirect way of current sensing. Information of the collector current (I_c) is obtained by integrating the voltage of an auxiliary winding of the transformer during transistor on-time (T_{on}). An external capacitor C on pin 5 is charged during T_{on} by the current source I_{sim}. The current I_{sim} is the reflection of the current which flows into pin 12. This current is obtained by connecting an external resistor R12 to the auxiliary transformer winding. During transistor on-time this current is related to the input voltage V_I. During transistor off time (T_{off}) the capacitor C is discharged by switch 10. This switch is active during the total T_{off} time. In this way a sawtooth voltage V_c is formed across C (see Fig.4 and Fig.16). This sawtooth is a measure for the collector current of the switching transistor T1.

For the voltage V_c (Fig.4) yields:

(1)

$$V_c = \frac{I_{sim} \times T_{on}}{C}$$

(2)

$$I_{sim} = p \times \frac{n_h}{n_p} \times \frac{V_I}{R12}$$

Where: p = reflection factor;

$$p = \frac{I_{sim}}{I12} = 0.2$$

(2) → (1) gives:

(3)

$$V_c = \frac{p}{C} \times \frac{n_h}{n_p} \times \frac{VI}{R12} \times T_{on}$$

For "T_{on}" yields:

(4)

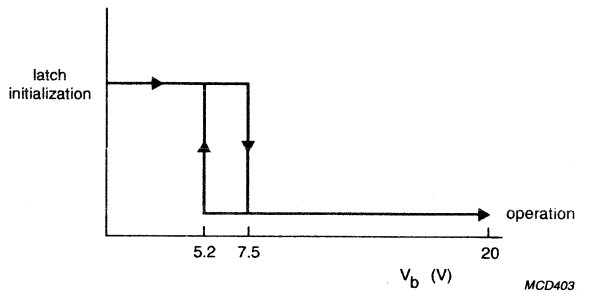


Fig.3 Latch initialization as a function of supply voltage V_b.

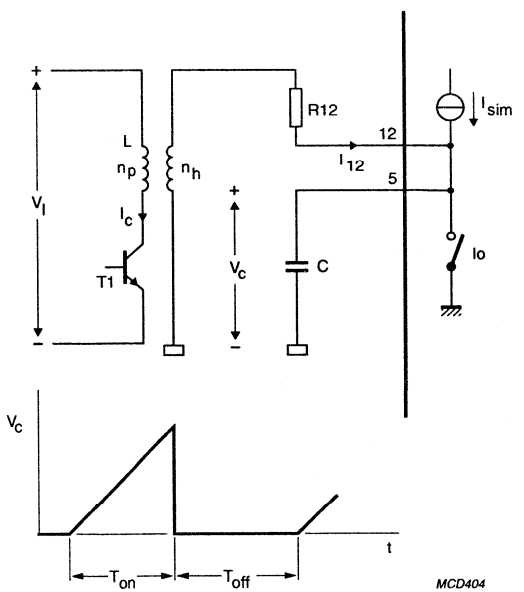


Fig.4 Determination of the peak current I_c.

$$T_{on} = \frac{V_c \times C \times n_p \times R12}{p \times n_h \times V_l}$$

For the primary current I_c yields:

(5)

$$I_c = \frac{V_l}{L} \times T_{on}$$

Substitution (4) into (5):

(6)

$$I_c = \frac{C}{L} \times \frac{1}{p} \times \frac{n_p}{n_h} \times R12 \times V_c$$

Formula (6) shows that by limiting the voltage V_c the collector peak current can be limited. The peak current is limited by means of the clamping circuit in the transfer character generator (TCG); see Fig.1 block 4.
The clamping level can be externally influenced by means of a resistor on pin 7.
The collector peak current can be influenced in several ways:

- resistor R12 on pin 12
- capacitor C on pin 5
- capacitor on pin 7
- transfer ratio nh/np
- inductance L

Before comparing the sawtooth voltage V_c with the control voltage V_r in the pulse width modulator, a voltage of 100 mV is added to V_c. In this way it will be possible for V_r to become smaller than V_{sim}, which is important for a stabilized no-load operation (see Fig.5 area 3).

DEMAGNETIZATION INPUT (PIN 15)

This input prevents the switching transistor from conducting during demagnetization of the transformer in order to prevent the transformer from going into saturation. The output of comparator 11 is HIGH as soon as the voltage of the transformer winding is above 115 mV.

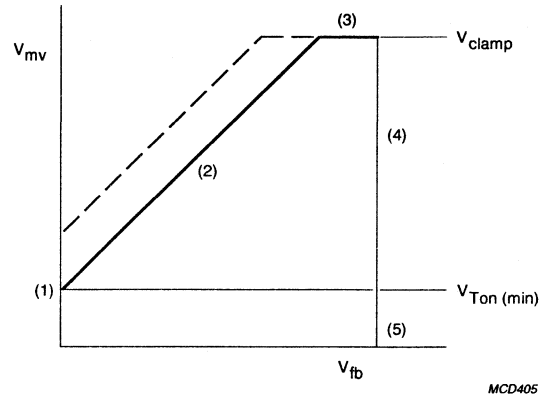


Fig.5 Reference voltage (V_{mv}) as a function of feedback voltage (V_{fb}).

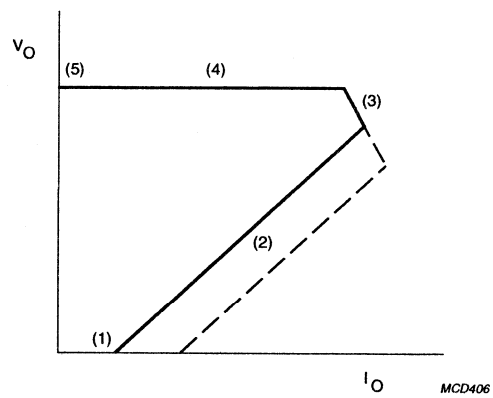
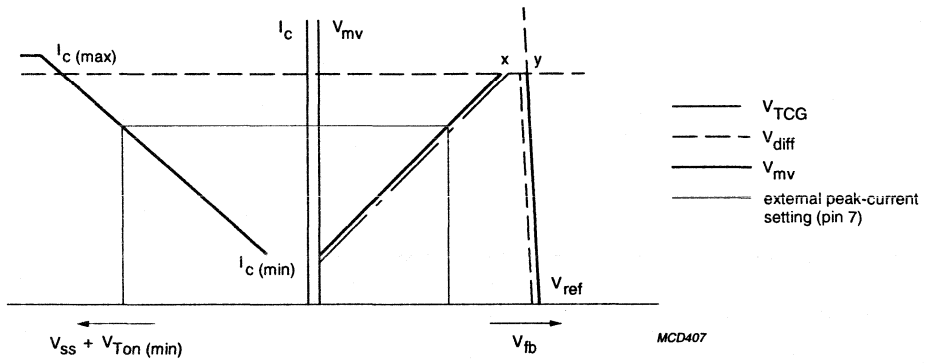


Fig.6 Current foldback characteristic; stabilized output voltage (V_O) as function of load current (I_O).



The voltage V_{mv} determines the collector peak current I_c of transistor T1. The right-hand curve is passed through at start-up. When the feedback voltage slowly increases from zero, the peak current starts at $I_{c(min)}$ and rises along the straight line until $I_{c(max)}$ is reached. At a slightly higher feedback voltage the regulation slope is reached, which is approximately V_{ref}.
The plateau of the top between the points x and y has to be kept as small as possible.
The voltage V_{diff} decreases with the decreasing load. For good no-load operation the peak current has to be made zero with V_{diff}.
Due to the characteristic of the TCG open- and short-circuited feedback loop will result in low peak current.
An additional signal on pin 13 can be supplied which is subtracted from the signal V_{mv}. This input can be used for feed forward information.
If no feed forward information is used, pin 13 should be connected to ground.

Fig.7 Characteristics of the control part.

DELAY SETTING (PIN 6)

The output of block 11 is extended by the delay circuit of block 12. The starting (reference) point of the delay circuit is the falling edge of the output of demagnetizing comparator 11. The delay can be determined externally by capacitor (C6) on pin 6. By means of the capacitor C6 the switch-on moment of the switching transistor can be determined.
A minimum delay time is required to prevent transistor T1 from switching during demagnetization of the transformer because of oscillations caused by the leakage inductance.

Control part (Block III)

The differential amplifier, block 3, compares the feedback voltage (V_{fb}) with the reference voltage V_{ref}. The output of the differential amplifier is available on pin 11 to allow gain setting. The differential amplifier is internally compensated for 0 dB feedback stability.
The feedback input (pin 9) is also used as the input for the TCG (see Fig.5) with which a current foldback characteristic can be obtained as shown in Fig.6.

The voltage $VT_{on(min)}$ determines the minimum on-time of the switching transistor. This voltage can be determined externally with a resistor on pin 4. With this resistor the current foldback characteristic can be influenced (see --- Figs 5 and 6).

The minimum on-time is of importance for:

- stand-by operation
- starting-up of power supply
- overload and short-circuited conditions

The output of the differential amplifier (V_{diff}), the output of the TCG (V_{TCG}) and the voltage V_{ss} + $VT_{on(min)}$ are compared in a minimum voltage clamping circuit (see block 6).
The output voltage of this block is equal to the lowest input voltage.

Some relevant characteristics of the control part are depicted in Fig.7.

Pulse width modulator (Block IV)

The pulse width modulator compares the control voltage V_r with the sawtooth voltage V_{sim}. If $V_{sim} > V_r$ output block 8 is HIGH and the LED is switched on then the switching transistor is switched off. In this way the output voltage is controlled.

Example: If the load decreases, V_O increases and therefore V_r decreases. This causes the LED to start conducting prematurely, which implies that the switching transistor is turned off sooner. The consequence is that the collector peak current decreases and hence less energy is stored in the transformer and V_O will decrease.

LED control (Block V)

If either output of block 8 or output of block 16 are HIGH the LED is conductive. In order to improve the start-up behaviour of the power supply, the demagnetization signal of block 12 will only activate the LED driver if flipflop 13 has previously been set. The set signal is generated in three ways:

(a) pulse width modulator (block 8)

(b) comparator 18

(c) $V_{b(min)}$ detector

Set signal (b) and (c) are added as extra security to guarantee a demagnetization pulse in the event of the switching transistor not having enough base current. In that situation e.g. at start-up, no comparator signal, set signal (a), is generated by block 8.

LED driver (Block VI)

The LED driver (pin 2) is blocked if the supply voltage V_b is in the initialization phase (see Fig.3). The output stage is a push-pull stage, which can sink 5 mA and source 10 mA.

Slow start circuitry (Block VII)

The slow start circuitry is active at start-up, overvoltage protection or after an overload, (short-circuited) and stand-by mode. The voltage V_{ss} and therefore the voltage V_{mv} and the peak current I_c slowly increase at start-up.
By means of block 27 the slow start voltage V_{ss} is clamped to the voltage V_{fb}. If the feedback voltage is reduced, e.g. as overload, the slow start capacitor is discharged to the level of V_{fb}. In this way a slow start-up is also guaranteed after an overload, short circuited situation or after a stand-by mode. The circuit of block 27 is not active during an over voltage protection.
When the supply voltage V_b is below the reset-level of 5.2 V (block 28) the slow start capacitor is quickly discharged.
The slow start input (pin 7) can also be used for $I_{c(max)}$ setting by connecting a resistor to this pin.

Over voltage protection (Block VIII)

The operation of the over voltage protection circuitry is, in the case of the IC being SOPS-supplied, quite different from when the IC is externally supplied.

- Operation when the IC is externally supplied

When the voltage on pin 8 exceeds 2.5 V the slow start capacitor is slowly discharged. During discharging the LED is permanently conducting. Discharging is stopped when V_{ss} is below 115 mV. Flipflop 23 will then be reset and the circuit is ready again for a new slow start procedure.
During an over voltage block 27 is not active so that the output voltage V_O cannot influence the slow start discharge procedure.

- Operation when IC is SOPS-supplied (see Figs 8 and 9)

When the voltage on pin 8 exceeds 2.5 V the slow start capacitor is slowly discharged. During discharging of C_{ss} the supply capacitor C_b is also discharged. Because the capacitors C_b and C_{ss} have almost the same value and the supply current I_b ($\approx$ 15 mA) is much larger than the slow discharge current ($\approx$ 50 µA), the LED will be switched off by means of the V_b(min) detection circuit (5.2 V). At that moment the switching transistor will be switched on again until the 7.5 V level is reached. During this hysteresis interval the slow charge capacitor is quickly discharged. At the 7.5 V level the LED will be switched on again because flipflop 23 output is still HIGH.
The same procedure will be repeated several times until the slow start capacitor reaches the 115 mV reset level. At that moment the slow start procedure is started again.
If there is still an over voltage the procedure will be repeated.
Fig.9 is a detailed exposure of Fig.8.

Stand-by circuit (Block IX)

During stand-by operation the voltage V_{sb} is supplied from the SOPS via a thyristor (see Fig.15). In the stand-by state, SOPS operates in a burst mode. When the voltage on pin 10 exceeds 2.5 V the LED driver is permanently activated. The LED driver is released again if the voltage is below 2 V (see Fig.10).

Regulation indicator output (Block X)

Pin 1 can be used to reset the logic circuitry in the TV receiver at power on and off. Block 29 has an open-collector output. The output of this block is LOW during the regulation mode ($V_{diff} < V_{ts}$; see Fig.11).

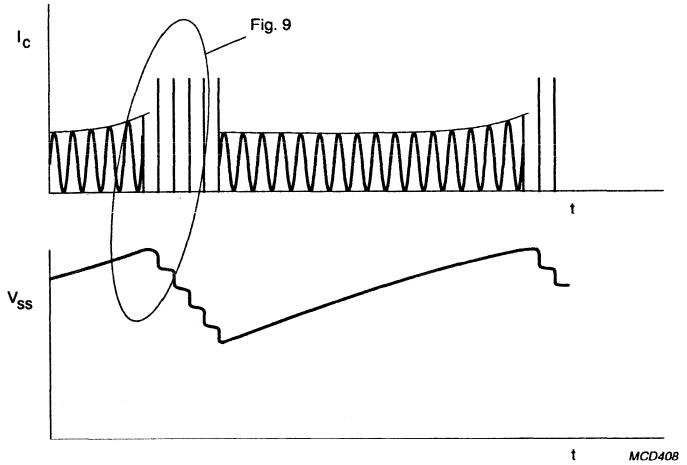


Fig.8 Over voltage protection.

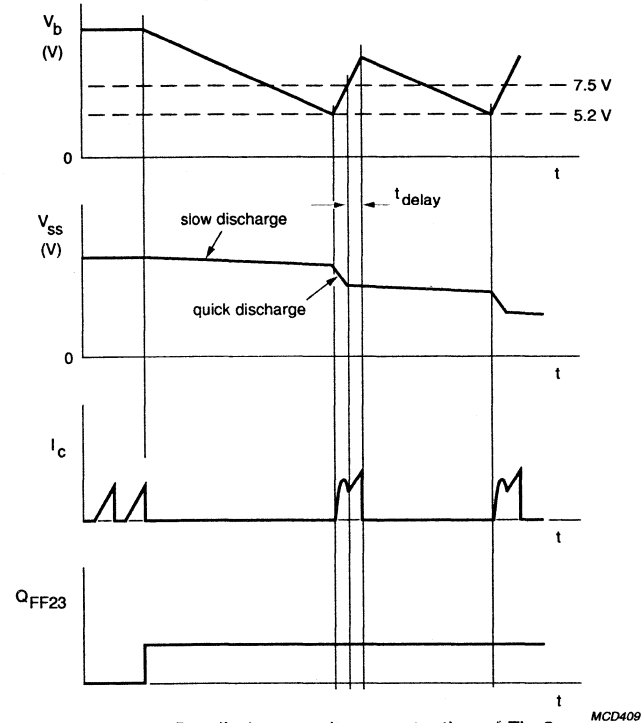


Fig.9 Detailed over voltage protection of Fig.8.

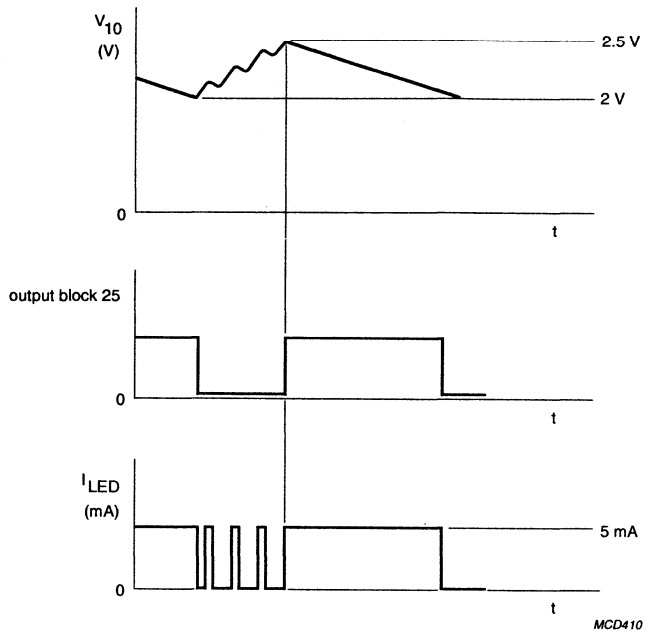
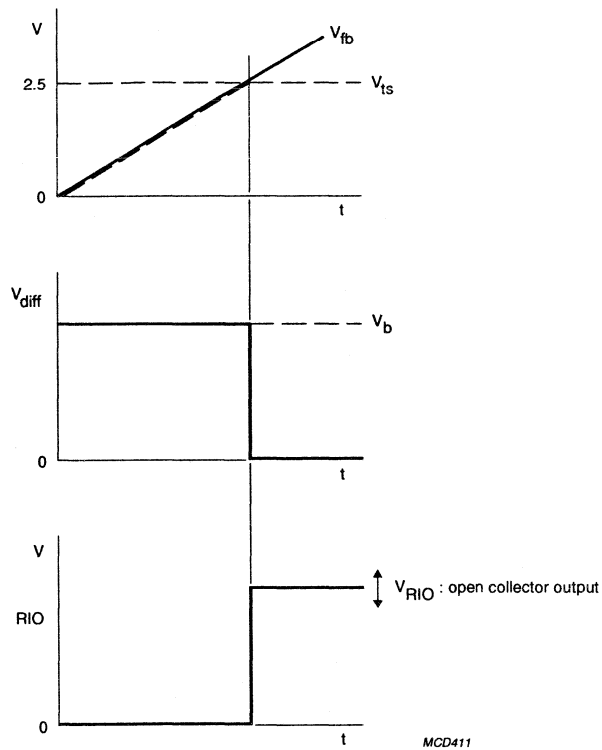


Fig.10 Stand-by operation; burst mode.



A desired delay at power-on reset can be made externally.

Fig.11 Regulation indicator output; pin 1.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134. All voltages with respect to ground; positive current flow into the IC; all pins not mentioned in the voltage list are not allowed to be voltage driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the power rating is not violated.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Voltages				
V_b	supply voltage (pin 16) with pin 2 connected with pin 2 = open-circuit	 −0.5 −0.5	 20 18	 V V
V_n	pins 1, 2, 4, 7, 9 and 13	−0.5	+18	V
V_3	pin 3	−0.5	+6	V
$V_{8,10}$	pin 8 and 10	−0.5	+3.9	V
V_{12}	pin 12	−0.1	+0.5	V
V_{15}	pin 15	−0.5	+0.5	mA
Currents				
I_1	pin 1	0	2	mA
I_n	pins 2, 12 and 15	−10	+10	mA
I_3	pin 3	−1	0	mA
$I_{5, 6}$	pins 5 and 6	−1	+1	mA
I_7	pin 7	−1	+25	mA
I_{11}	pin 11	−10	+0.5	mA
I_{16}	pin 16	0	20	mA
T_{amb}	operating ambient temperature range	−25	+70	°C
T_{stg}	storage temperature range	−55	+150	°C
P_{tot}	total power dissipation	−	500	mW

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
R_{th}	thermal resistance	−	55	K/W

CHARACTERISTICS

V_{16} = 15 V; I_3 = 200 µA; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{16}	supply voltage range		7.9	–	20	V
V_{16}	supply initialization level		7.1	7.5	7.9	V
δV_{16}	internal fixed hysteresis		2.5	–	2.55	V
I_{16}	supply current at active LED output		–	–	20	mA
V_{11}	supply voltage ripple rejection	see Figs 12 and 13	–	60	–	mV
Reference voltage						
V_3	reference voltage at pin 3		0.52	0.55	0.58	V
Error amplifier						
V_9	threshold voltage error amplitude		2.4	2.5	2.6	V
I_9	input current feedback input		–	–	0.5	µA
I_{11}	sink current output	V_{11} = 80 mV	400	–	–	µA
I_{11}	source current output	V_{11} = 2.5 V	500	–	–	µA
A_o	open loop gain		–	100	–	dB
B	unity gain bandwidth		–	600	–	kHz
$\Delta V_9/\Delta T$	temperature coefficient		–	±300	–	10^{-6}/°C
V_5	threshold for switching output	V_{diff} = 1.25 V; V_4 = 2 V; V_{13} = 0; $V_7 > V_9$; I_2 = 2 mA	–	V_{diff}-V_{os}; note 1	–	V
Transfer characteristic generator						
I_4/I_3	current ratio	V_4 = 0.5 V	0.23	0.25	0.27	
V_5	threshold for switching output	V_4 = 0.5 V; V_{13} = 0 V; $V_7 > V_9$; I_2 = 2 mA				
	$T_{on(min)}$	V_9 = 0 V	0.4–V_{os}; note 1	0.5–V_{os}	0.6–V_{os}	V
	V_{fb} = 20%	V_9 = 0.4 V	–	0.9–V_{os}	–	V
	V_{fb} = 50%	V_9 = 1 V	1.4–V_{os}	1.5–V_{os}	1.6–V_{os}	V
	V_{fb} = 80%	V_9 = 1.6 V	–	2.1–V_{os}	–	V
	clamp	V_9 = 2.25 V	2.4–V_{os}	–	2.6–V_{os}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transfer characteristic generator						
	response time pulse width modulation pin 5 to pin 2	V_5 pulse = 1 V; V_4 = 0.5 V; V_9 = V7 = 3 V; V_{11} = 0.5 V; V_{13} = 0 V; I_2 = 2 mA				
t_{PLH}	LOW-to-HIGH		–	–	700	ns
t_{PHL}	HIGH-to-LOW		–	–	1	µs
Feed forward						
V_5	threshold for switching output	V_4 = 0.5 V; V_{13} = 0.3 V; V_7 = V9 = 3 V; I_2 = 2 mA; V_{11} = 1 V				
	V_{fo}		0.6–V_{os}	0.7–V_{os}	0.8 –V_{os}	V
I_{13}	input bias current	V_{13} = 0 V	–	–	1	µA
Slow start						
I_7/I_3	charge current ratio	V_7 = 0.5 V	0.22	0.24	0.26	
I_7	quick discharge current	V_7 = 1 V V_7 = 100 mV	20 50	– –	– –	mA µA
V_7	clamping level	at 100 µA	2.8	3.0	3.2	V
V_5	threshold for switching output	V_4 = 0.5 V; V_{13} = 0 V; V_7 = 1 V; I_2 = 2 mA; V_9 = 2 V				
	V_{ss}	note 1	1.4–V_{os}	1.5–V_{os}	1.6–V_{os}	V
Output stage						
V_2	saturation voltage	I_2 = 2 mA	–	–	300	mV
I_2	source current	V_2 = 2 V				
	operating		4.8	5.3	6.3	mA
	initialization phase		–	–	50	µA
V_2	open output voltage HIGH	I_2 = 5 mA	12	–	–	V
Current simulation						
I_5/I_{12}	current ratio	V_5 = 1 V; I_{12} = 0.5 mA	0.19	0.2	0.21	
V_{12}	voltage simulation input	I_{12} = 0.5 mA	–	–	1.1	V
V_5	saturation voltage	V_{15} = V_6 = 0 V				
		I_5 = 1 mA	–	–	300	mV
		I_5 = 200 µA	–	–	200	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current simulation						
V_5-V_{11}	threshold for switching output	V_4 = 0.5 V; V_{13} = 0 V; V_7 = V_9 = 3 V; I_2 = 2 mA; V_{11} = 0.5 V				
	offset simulation voltage (V_{os})	note 1	60	100	140	mV
Demagnetization input						
	delay from pin 15 to pin 5	see Fig.14				
t_{demL-H}	LOW-to-HIGH	pin 6 not connected	–	–	500	ns
t_{demH-L}	HIGH-to-LOW		–	–	1	µs
V_{15}	positive clamping level	I_{15} = 10 mA	–	–	1.2	V
V_{15}	negative clamping level	I_{15} = 10 mA	–	–	–1	V
V_{15}	demagnetization threshold		90	115	140	mV
C_{15}	input capacitance		–	–	10	pF
I_{15}	input bias current	V_{15} = 60 mV	–	–	0.5	µA
Delay setting						
I_6/I_3	charge current ratio	V_6 = 1 V	1.1	1.2	1.3	
I_6	charge current initialization phase	V_6 = 1 V; V_{16} = 5 V	2	–	–	mA
V_6	clamping level		2.8	–	3.2	V
V_6	saturation level	V_{15} = 140 mV	–	50	100	mV
	delay from pin 6 to pin 2	C_6 = 470 pF;				
	V_6 crossing the 2.5 V level	V_5 = 0 V; I_2 = 2 mA; V_{15} see Fig.14				
t_{dL-H}	LOW-to-HIGH	excluding capacitive tolerance	–	–	1.2	µs
t/c	delay setting (t = C_6 x V/I)	V_6 = 2.5 V; I_3 = 250 µA	–	10	–	ns/pF
Stand-by						
V_{10}	threshold level HIGH		2.4	2.5	2.6	V
ΔV_{10}	hysteresis		450	500	550	mV
	delay to output from pin 10 to pin 2					
$t_{stbyL-H}$	LOW-to-HIGH		–	–	1	µs
$t_{stbyH-L}$	HIGH-to-LOW		–	–	1	µs
I_{10}	input current	V_{10} = 2.3 V	–	–	5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Over voltage protection						
V_8	threshold level		2.4	2.5	2.6	V
	delay to output from pin 8 to pin 2					
t_{L-H}	LOW-to-HIGH		–	–	1	µs
t_{H-L}	HIGH-to-LOW		–	–	1	µs
V_7	reset level		90	–	140	mV
I_7/I_3	slow discharge current ratio	V_7 = 1 V	0.12	0.2	0.28	
I_8	input current	V_8 = 3 V	–	–	1	µA
Regulation indicator output						
V_1	saturation voltage	I_1 = 1 mA	–	–	300	mV
I_1	leakage current	V_1 = V16	–	–	1	µA

Note to the characteristics

1. $V_{os} = V_{offset}$; see **Current simulation**.

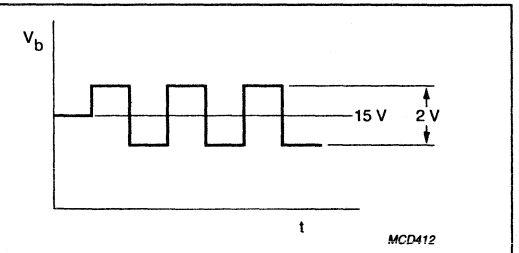


Fig.12 Supply voltage ripple rejection; V_b as a function of time.

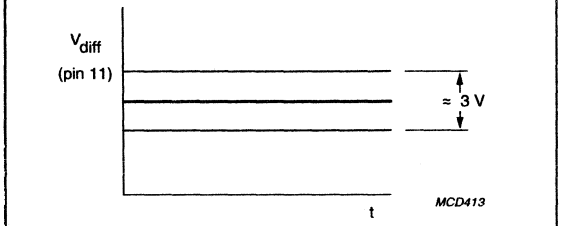


Fig.13 Supply voltage ripple rejection; V_{diff} as a function of time.

Notes to Fig.12 and Fig.13

1. Frequency = 50 kHz; Slew rate = 0.2 µs.

CONDITION OF TEST CIRCUIT

PINS	STATUS
1, 2, 4 to 6, 12, 13	not connected
8 to 10, 14, 15	ground
3	R_{ref} = 2.7 kΩ
7	C_{ss} = 4.7 µF
16	V_b; see Fig.12 input
11	V_{diff}; see Fig.13 output

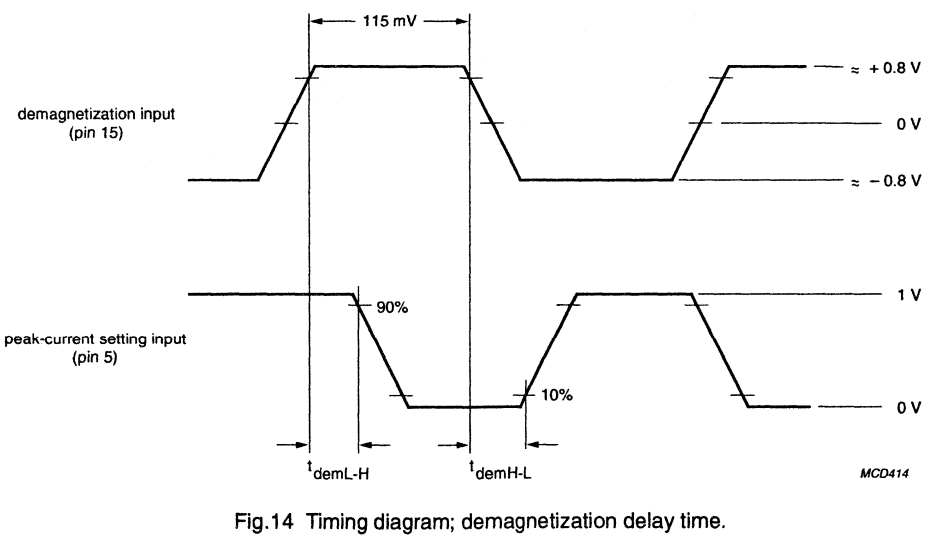


Fig.14 Timing diagram; demagnetization delay time.

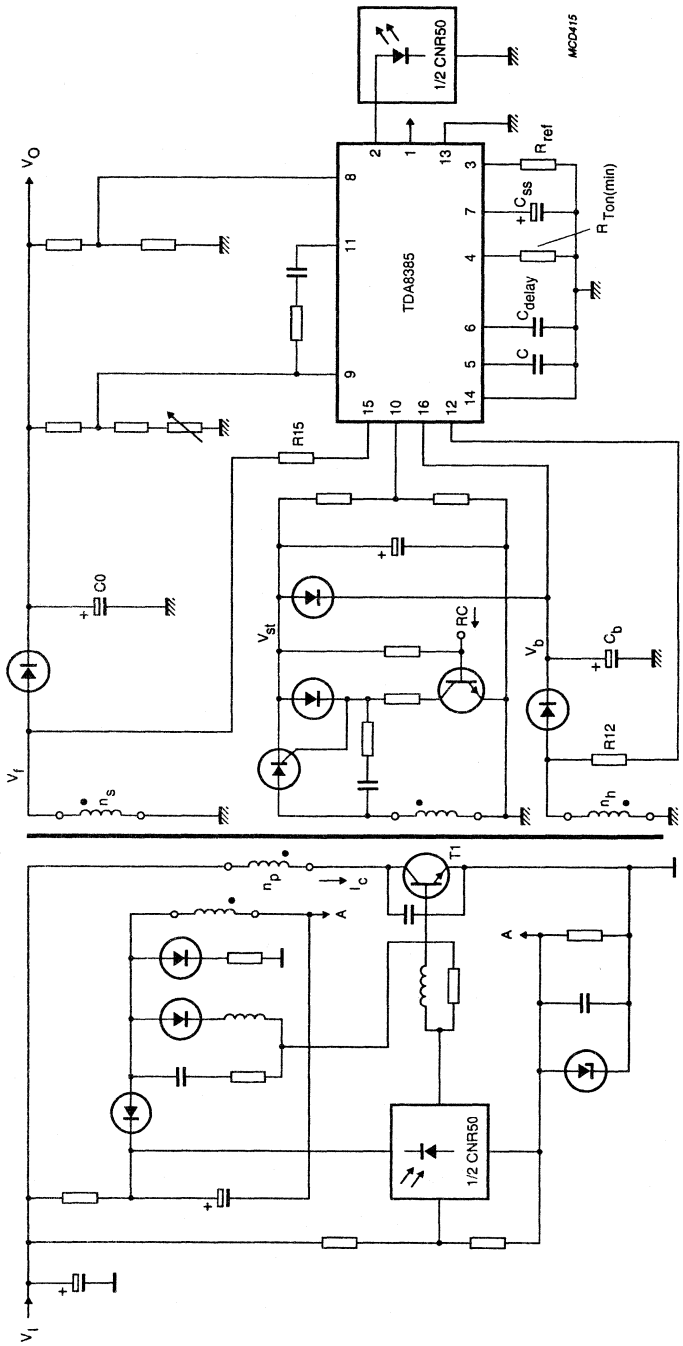


Fig.15 Application circuit of SOPS with stand-by facility.

APPLICATION INFORMATION

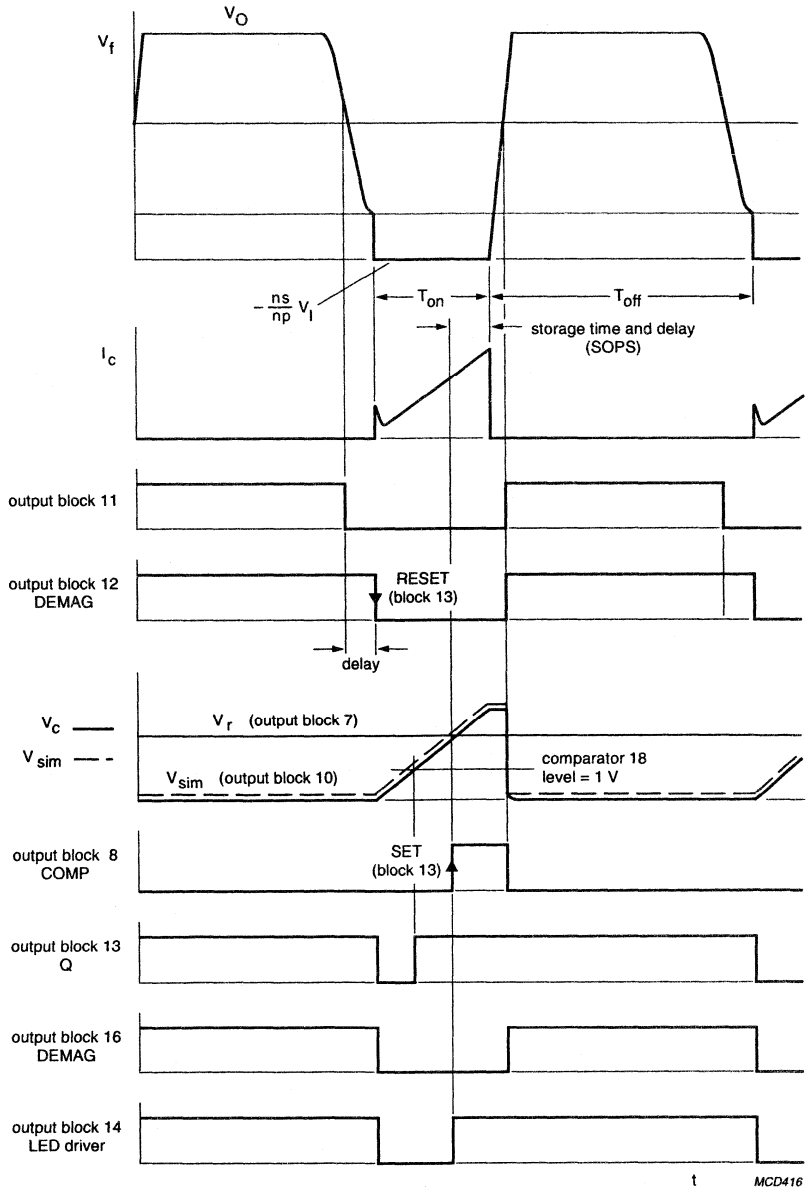


Fig.16 Application timing diagram.

One-chip PAL decoder and RGB matrix TDA8391

FEATURES

- A black-current stabilizer which controls the black currents of the three electron guns
- Contrast and brightness control of inserted RGB signals
- Self aligned oscillator
- Capacitive coupling with black level clamping of the luminance, colour difference and RGB inputs
- Equal black levels for internal TV and external signals
- 12 MHz bandwidth
- Emitter follower outputs for driving the RGB output stages

GENERAL DESCRIPTION

The TDA8391 is a one-chip PAL colour decoder which is designed to be used in combination with the P2CCD Delay Line (TDA8451A) and the Filter Combination (TDA8452A or TDA8453). The device combines the circuits that are required for the identification and demodulation of pulse signals, RGB matrixing and amplification. Inductive components are not required due to the integration of the filters and the delay lines. The TDA8391 provides a crystal-precise reference signal for the clock generator circuits in TDA8451A and TDA8452A/8453; therefore, no adjustments are required to the filters and delay times.

The TDA8391 is functionally identical to the TDA8390, it has the same pinning and its application is almost identical.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 23)		10.8	12	13.2	V
I_P	positive supply current (pin 23)		55	70	100	mA
$V_{25(p-p)}$	luminance input voltage (peak-to-peak value)		–	0.45	–	V
C_{CR}	contrast control range (pin 7)		–	20	–	dB
$V_{30(p-p)}$	chrominance input voltage (peak-to-peak value)		–	465	–	mV
	demodulator output voltages (pins 26 and 27) (peak-to-peak value)					
$V_{26(p-p)}$	–(R-Y) (peak-to-peak value)		0.55	0.65	0.77	V
$V_{27(p-p)}$	–(B-Y) (peak-to-peak value)		0.70	0.82	0.97	V
S_{CR}	saturation control range (pin 6)		50	–	–	dB
	colour difference input signals					
$V_{21(p-p)}$	–(R-Y) (peak-to-peak value)		–	0.65	–	V
$V_{22(p-p)}$	–(B-Y) (peak-to-peak value)		–	0.82	–	V
$V_{14,16\ 18(p-p)}$	RGB input signal for an output signal of 4 V black-to-white at nominal contrast (peak-to-peak value)		–	0.7	0.8	V
V_9	video switching	external RGB	0.9	–	–	V
$V_{13,15\ 17(p-p)}$	RGB output voltage at nominal luminance input and nominal contrast; black-to-white (peak-to-peak value)		3.5	4.0	4.5	V
B_{CR}	brightness control range (pin 5)		–	±1.3	–	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8391	32	DIL	plastic	SOT201

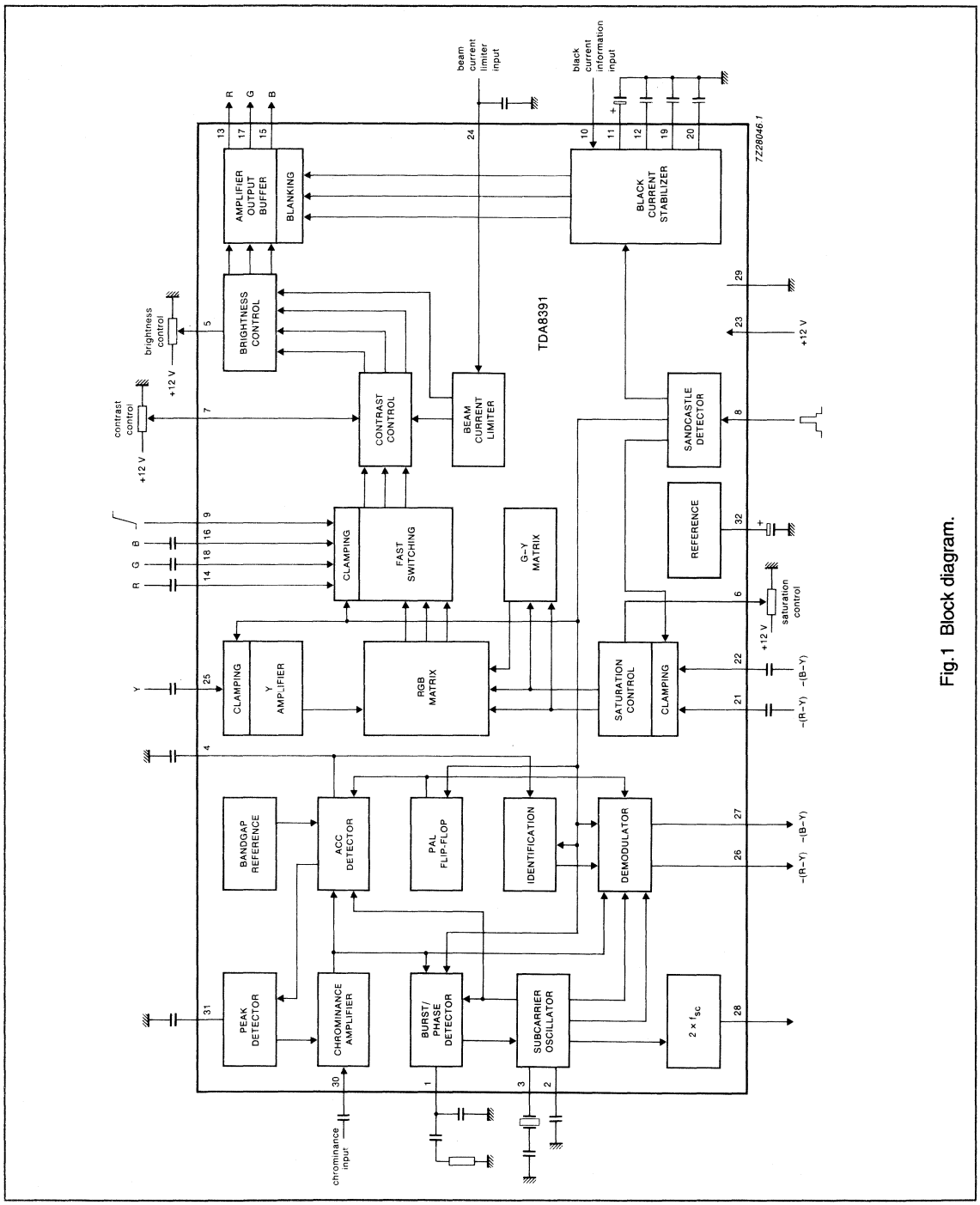


Fig.1 Block diagram.

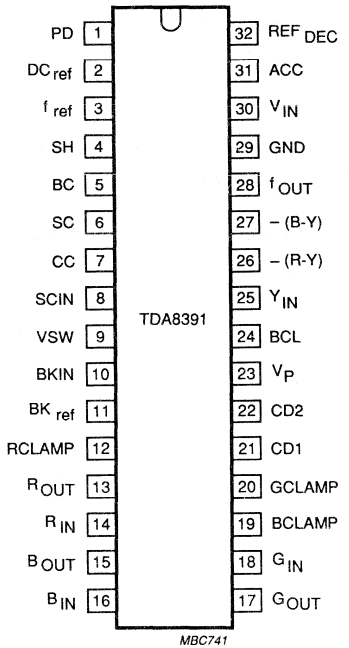


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
PD	1	phase detector
DC_{ref}	2	90° phase shift DC reference
f_{ref}	3	4.43 MHz PAL reference frequency input
SH	4	sample-and-hold (PAL identification)
BC	5	brightness control
SC	6	saturation control
CC	7	contrast control
SCIN	8	sandcastle pulse input
VSW	9	video switch input
BKIN	10	black current input
BK_{ref}	11	black current reference
RCLAMP	12	red clamping circuit
ROUT	13	red signal output
RIN	14	red insertion input
BOUT	15	blue signal output
BIN	16	blue insertion input
GOUT	17	green signal output
GIN	18	green insertion input
BCLAMP	19	blue clamping circuit
GCLAMP	20	green clamping circuit
CD1	21	–(R-Y) colour difference input
CD2	22	–(B-Y) colour difference input
V_P	23	positive supply voltage
BCL	24	beam current limiter input
YIN	25	luminance input
–(R-Y)	26	–(R-Y) signal output
–(B-Y)	27	–(B-Y) signal output
f_{OUT}	28	frequency doubler output
GND	29	ground
VIN	30	chrominance input
ACC	31	automatic colour control
REF_{DEC}	32	reference decoupling

FUNCTIONAL DESCRIPTION

Colour decoder

The input chrominance signal is amplified and applied to the burst phase detector (reference signal R-Y phase), the ACC and identification detector (reference signal ±(R-Y) phase) and the two demodulators. The burst phase detector controls the oscillator which operates at a frequency of 4.43 MHz. By connecting pin 6 to 12 V, the free-running frequency of the oscillator can be adjusted (phase detector and colour killer switched off). The gain control stage of the oscillator is biased in such a way that sinewave signals are generated. The output from the oscillator is fed to a Miller integrator in order to obtain the required 90° phase shift. The reference signals obtained from the oscillator and 90° phase shift network are applied to the various demodulators.

The output signal from the ACC and identification detector is peak detected to generate the ACC voltage and detected in a sample and hold circuit to obtain the identification and killer information.

Because the P²CCD filter combination (TDA8452A/8453) requires a reference signal ($2 \times f_{sc}$) the oscillator frequency is doubled, internally, and is made available at pin 28.

The demodulated signals, with the correct amplitude ratio, are applied to the TDA8451A. The TDA8391 can be combined with the SECAM decoder TDA8490 (Fig.4) by direct connection of their outputs. The output DC levels have been chosen so that the PAL decoder has priority (output level during PAL is higher than output level during SECAM).

Control circuit

The luminance and colour difference signals together with the RGB inputs and fast switching pulse form the inputs to the control circuit. The required luminance input signal (from TDA8452A/8453) has a peak-to-peak value of 0.45 V (including sync). The colour difference input signals (from TDA8451A) have a negative phase with a 0.72 V –(R-Y) and 0.93 V –(B-Y) peak-to-peak value. After amplification, the luminance signal is applied to the RGB matrix.

The colour difference signals are fed to the saturation control circuit before being applied to the RGB matrix (the G-Y signal is generated after the saturation control circuit).

The normal matrix for PAL is:
(G-Y) = –0.51 –(R-Y) –0.19 –(B-Y).
The signals from the RGB matrix are applied to a fast switching circuit from where external RGB signals can be selected. The fast switching circuit is controlled by the video switching input. After amplification the RGB signals (internal or external video) are controlled on the contrast and brightness before being fed to the outputs. A typical output signal amplitude is 4 V black-to-white (nominal controls).

The black level of the RGB output signals is determined by the black current stabilization circuit. The information regarding the black current level of the picture tube is obtained in the same manner as the TDA3562A. The beam current limiter input is used to reduce the output signal amplitude via the contrast and brightness control circuits.

A block diagram is given in Fig.1. Figure 3 illustrates the PAL decoder configuration and Figure 4 the PAL-SECAM configuration. Figures 5, 6 and 7 illustrate the Saturation, Contrast and Brightness control curves respectively.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{23}	positive supply voltage		–	13.2	V
P_{tot}	total power dissipation		–	1.5	W
T_{amb}	operating ambient temperature range		–25	+70	°C
T_{stg}	storage temperature range		–25	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; all voltages are referenced to ground (pin 29) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{23}	positive supply voltage		10.8	12.0	13.2	V
I_{23}	supply current		55	70	100	mA
P_{tot}	total power dissipation		–	0.85	–	W
DEMODULATOR PART						
CHROMINANCE AMPLIFIER (PIN 30)						
$V_{30(p-p)}$	input signal amplitude (peak-to-peak value)	note 1	–	465	–	mV
$V_{30(p-p)}$	input signal amplitude before clipping occurs in the input stage (peak-to-peak value)		–	–	1100	mV
$V_{30(p-p)}$	minimum burst signal amplitude within the ACC control range (–1 dB) (peak-to-peak value)		30	–	–	mV
R_{30}	input resistance		9	12	15	kΩ
C_{30}	input capacitance		–	–	4	pF
CR_{ACC}	ACC control range		30	–	–	dB
ΔV_O	change in amplitude of the output signals (pins 26 and 27) over the ACC range		–	+1	±1.5	dB
REFERENCE PART						
PHASE LOCKED LOOP						
Δf	catching range	note 2	±450	–	–	Hz
$\Delta\Phi$	phase shift for ±400 Hz deviation of the oscillator frequency	note 2	–	–	5	deg
OSCILLATOR (PIN 3)						
TC_{osc}	temperature coefficient of the oscillator frequency	note 2	–	–2	–	Hz/K
Δf	frequency deviation for a supply voltage change from 10 V to 13.2 V	note 2	–	40	–	Hz
R_3	input resistance (pin 3)		400	650	900	Ω
C_3	input capacitance (pin 3)		–	–	6	pF

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ACC AND IDENTIFICATION DETECTORS (PINS 4 AND 31)						
V_4	voltage at the PAL identification output pin 4					
	nominal input signal for PAL		–	5.0	–	V
	without burst input		–	2.9	–	V
V_4	colour OFF voltage		–	3.3	–	V
V_4	colour ON voltage		–	3.5	–	V
V_{31}	voltage at peak detector output (pin 31)					
	voltage at nominal input signal		–	5.8	–	V
	voltage without input signal		–	2.7	–	V
DEMODULATORS (PINS 26 AND 27)						
$V_{26(p-p)}$	output signal amplitude –(R-Y) output (peak-to-peak value) (pin 26)		0.54	0.65	0.76	V
$V_{27(p-p)}$	output signal amplitude –(B-Y) output (peak-to-peak value) (pin 27)		0.68	0.82	0.97	V
$V_{26,27}$	ratio of amplification of both demodulators G–(B-Y)/G–(R-Y)		1.6	1.78	1.96	
t_d	internal delay between chrominance input and –(R-Y)/–(B-Y) output		140	200	260	ns
f	frequency response between 0 and 1 MHz		–	–3	–	dB
$R_{26,27}$	output resistance (pins 26 and 27)		–	100	–	Ω
$V_{26,27}$	output DC level when a PAL signal is identified		–	8.3	–	V
$V_{26,27}$	output level during killing		–	1.3	–	V
	unwanted signals at –(R-Y) and –(B-Y) outputs	note 3	–	–	–40	dB
$V_{26,27(p-p)}$	4.4 MHz residual carrier at the –(R-Y) and –(B-Y) outputs (peak-to-peak value)		–	–	10	mV
$V_{26,27(p-p)}$	8.8 MHz + harmonics residual carrier at the –(R-Y) and –(B-Y) outputs (peak-to-peak value)		–	–	20	mV
$V_{26(p-p)}$	H/2 ripple at –(R-Y) output without input signal (peak-to-peak value)		–	–	50	mV

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta V/\Delta T$	change in amplitude –(R-Y/B-Y) with temperature		–	–0.1	–	%/K
$\Delta V/\Delta V$	change in amplitude for a supply voltage change from 10.8 V to 13.2 V		–	–	±0.3	dB
FREQUENCY DOUBLER OUTPUT (PIN 28)						
$V_{28(p-p)}$	output signal amplitude (peak-to-peak value)		200	300	–	mV
R_{28}	output resistance		–	50	–	Ω
V_{28}	DC output level		–	4.5	–	V
REFERENCE DECOUPLING (PIN 32)						
V_{32}	DC level		–	9.0	–	V
CONTROL PART						
LUMINANCE INPUT (PIN 25)						
$V_{25(p-p)}$	input voltage (peak-to-peak value)	note 4	–	0.45	–	V
$V_{25(p-p)}$	input voltage before clipping occurs (peak-to-peak value)		–	–	0.8	V
I_{25}	input current		–	0.1	1	µA
f	frequency response of the total luminance and RGB amplifier circuits between 0 and 12 MHz		–	–3	–	dB
COLOUR DIFFERENCE INPUT SIGNALS (PINS 21 AND 22)						
$V_{21(p-p)}$	input signal amplitude –(R-Y) (peak-to-peak value) (pin 21)		–	0.65	–	V
$V_{22(p-p)}$	input signal amplitude –(B-Y) (peak-to-peak value) (pin 22)		–	0.82	–	V
$I_{21,22}$	input current (pins 21 and 22)		–	–	0.2	µA
RGB INPUTS (PINS 14, 16 AND 18) (NOTE 5)						
$V_{14,16\ 18(p-p)}$	input signal amplitude for an output signal of 4 V black-to-white at nominal contrast (peak-to-peak value)	notes 6 and 7	–	0.7	0.8	V
$\Delta V_{13,15,17}$	difference between the black level of the RGB signals and the black level of the inserted signals at the outputs		–	–	100	mV
f	frequency response of RGB amplifier between 0 and 12 MHz		–	–2	–	dB
t_d	delay difference for the three channels		–	0	–	ns

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB INPUTS (PINS 14, 16 AND 18) (NOTE 5)						
$I_{14.16.18}$	input current		–	–	10	μA
VIDEO SWITCHING (PIN 9)						
V_9	input voltage	no insertion	–	–	0.3	V
		insertion of external RGB	0.9	–	4.0	V
t_d	switching delay		–	–	50	ns
R_9	input resistance		8	10	12	kΩ
	suppression of the internal RGB signals with reference to 4 V(p-p) at the RGB outputs	V_9 > 0.9 V; 0 to 5 MHz	46	50	–	dB
	suppression of the external RGB signals with reference to 4 V(p-p) at the RGB outputs	V_9 < 0.3 V; 0 to 5 MHz	40	–	–	dB
SANDCASTLE INPUT (PIN 8)						
V_8	detection level for:					
	vertical blanking		1.0	1.5	2.0	V
	horizontal blanking		3.0	3.5	4.0	V
	upper part of pulse		6.5	7.0	7.5	V
I_8	input current					
		V_I = 0 to 1.5 V	–	–0.4	–0.5	mA
		V_I = 1.5 to 3.5 V	–	–13	–	μA
		V_I = 3.5 to 7.0 V	–	–3.3	–	μA
		V_I = 7.0 to 12 V	–	–0.1	–	μA
t_d	internal delay between black level clamping and burst gating pulse (leading edge)		1.5	2.0	2.5	μs
SATURATION CONTROL INPUT (PIN 6); (SEE FIG.5)						
SC	saturation control range		50	–	–	dB
I_6	Input current saturation control	V_6 < 4.5 V	–	–	10	μA
R_6	input resistance	V_6 = 4.5 to 6 V	–	10	–	kΩ
		V_6 = 6 to 12 V	–	7	–	kΩ
CONTRAST CONTROL INPUT (PIN 7); (SEE FIG.6)						
CC	contrast control range		–	20	–	dB
	tracking of contrast control between the three channels over a control range of 10 dB		–	0.3	1.0	dB
I_7	input current contrast control	V_7 < 6 V	–	–	10	μA
R_7	input resistance	V_7 > 6 V	–	10	–	kΩ

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BRIGHTNESS CONTROL INPUT (PIN 5); (SEE FIG.7)						
V_5	brightness control voltage range	note 8	–	±1.3	–	V
I_5	input current brightness control		–	–	–50	μA
Colour difference matrices						
	G-Y/R-Y		–	–0.51	±10%	
	G-Y/B-Y		–	–0.19	±25%	
RGB amplifiers (pins 13 15 17)						
$V_{13,15\ 17(p-p)}$	output signal amplitude at nominal luminance input and nominal contrast; black-to-white (peak-to-peak value)	notes 1 and 6	3.5	4.0	4.5	V
$V_{15(p-p)}$	output signal amplitude for the blue channel at nominal contrast and saturation and no luminance signal at the input (pin 15) (peak-to-peak value)		4.3	5.4	6.5	V
V_{max}	maximum peak white level		10.0	10.5	11.0	V
$\Delta V_{13,15,17}$	difference in black level between the three outputs at nominal brightness	note 9	–	20	100	mV
	control range of black current stabilization at V black = 3 V and nominal brightness control		–	–	±2	V
ΔV	black level shift with picture content		–	–	40	mV
$V_{13,15,17}$	output voltage during the 4L pulse after switch-ON		7.0	7.5	8.0	V
$\Delta V/\Delta T$	variation of black level with temperature		–	1.0	–	mV/K
ΔV	variation of black level over contrast range at nominal saturation		–	–	100	mV
ΔV	variation of black level over saturation range at nominal contrast		–	–	50	mV
	relative spread between the three output signals		–	–	10	%

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB amplifiers (pins 13 15 17)						
V_B	relative variation in black level between the three channels during variations of the following conditions:	note 8				
	supply voltage ±10%) at nominal controls		–	–	100	mV
	contrast (20 dB) at nominal saturatioin		–	–	100	mV
	saturation (50 dB) at nominal contrast		–	–	100	mV
	brightness (±1 V) at nominal controls		–	–	100	mV
ΔV	differential drift of the black level over a temperature range of 40 K	note 8	–	50	70	mV
V_{bl}	blanking level at the RGB outputs		–	1.0	–	V
Δbl	difference in blanking level of the three channels		–	0	10	mV
$\Delta V/\Delta T$	differential drift of the blanking levels over a temperature range of 40 K		–	0	10	mV
$(\Delta V_{bl} \div V_{bl})$ x $(V_P \div \Delta V_P)$	tracking of the output black levels with supply voltage		0.9	1.0	1.1	
S/N	signal-to-noise ratio of output signals	note 3	–	60	–	dB
$R_{13.15.17}$	output resistance		–	150	–	Ω
$I_{13.15.17}$	available output current		5	–	–	mA
I_O	current source at output stage		–	2.5	–	mA
BLACK CURRENT STABILIZATION (PIN 10)						
V_{10}	DC bias voltage		3.5	5.0	7.0	V
ΔV	difference between input voltage for black current and leakage current		0.35	0.5	0.65	V
I_{10}	input current during black current		–	–	1	µA
I_{10}	input current during scan		–	–	10	mA
V_{10}	internal limiting level		8.5	9.0	9.5	V
V_{10}	switching threshold for black current control ON		7.6	8.0	8.4	V
R_{10}	input resistance during scan		1.0	1.5	2.0	kΩ

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BLACK CURRENT STABILIZATION (PIN 10)						
$I_{12,19,20}$	DC input current during scan at pins 12, 19 and 20		–	–	50	nA
$I_{11,12,19,20}$	maximum charge/discharge current during measuring time of clamping pulse at pins 11, 12, 19 and 20		0.3	–	–	mA
BEAM CURRENT LIMITER (PIN 24)						
V_{24}	voltage when beam current limiter function is not active	note 9	5.0	6.0	–	V
V_{24}	trigger level for beam current limiter function		3.8	4.2	4.6	V

Notes to the characteristics

1. The value indicated is a signal for a colour bar with 75% saturation (chrominance/burst ratio = 2.2 : 1).
2. All frequency variations are referred to 4.43 MHz carrier frequency and to the Philips 4.43 MHz crystal catalogue number 4322 143 04043.The specification is given for nominal crystal parameters. However, the load capacitance is fixed at a standard value of 18 pF for these crystal series.
3. The ratio between unwanted and wanted signals (e.g. crosstalk, phase errors and noise) is specified as the output signal amplitude (peak-to-peak value at nominal conditions) with respect to the RMS value of the unwanted signal.
4. Signal with negative going sync. Amplitude includes sync pulse amplitude.
5. When not used pins 14, 16 and 18 should be connected to ground via a 100 nF capacitor; pin 9 may be left open-circuit or connected to ground
6. Nominal contrast is specified as maximum contrast –3 dB. Nominal saturation as maximum saturation –6 dB.
7. Maximum input on pins 14, 16 and 18 is 1V(p-p).
8. With respect to the measuring pulse.
9. With respect to the measuring pulse. At nominal brightness the black level of an output is identical to the measuring level.
10. Pin 24 is connected internally to a high-resistance voltage divider (2 x 100 kΩ).

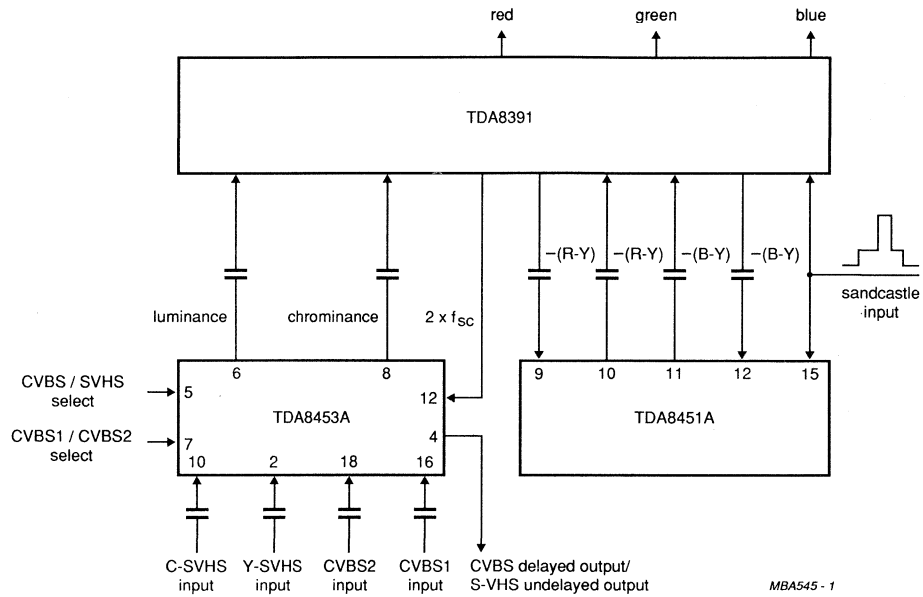


Fig.3 PAL decoder configuration.

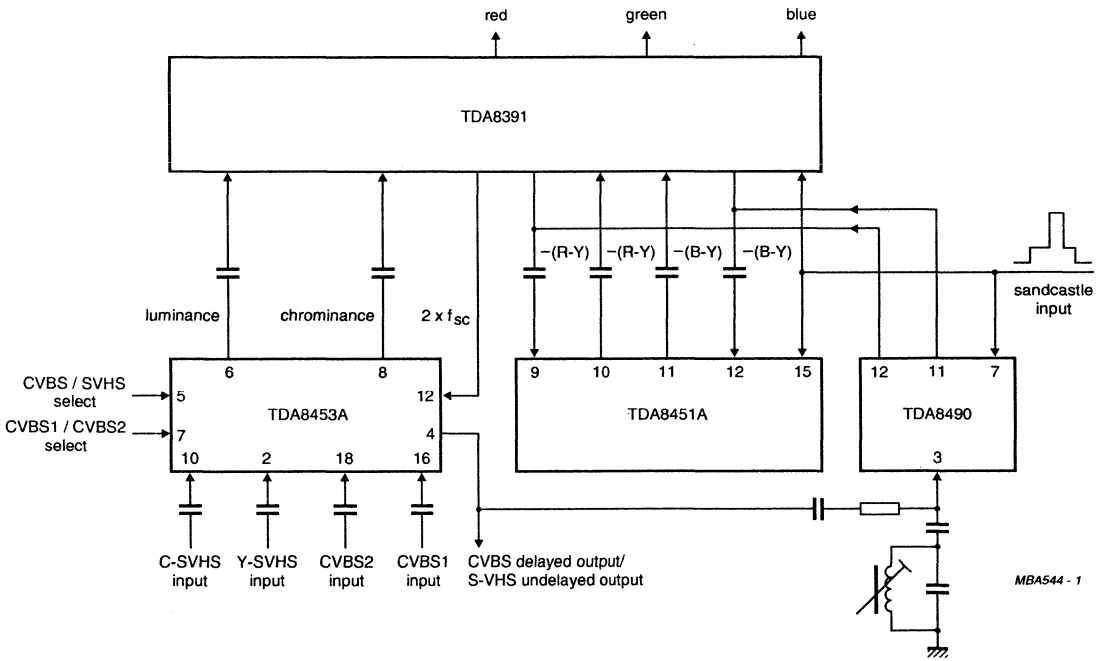


Fig.4 PAL-SECAM decoder configuration.

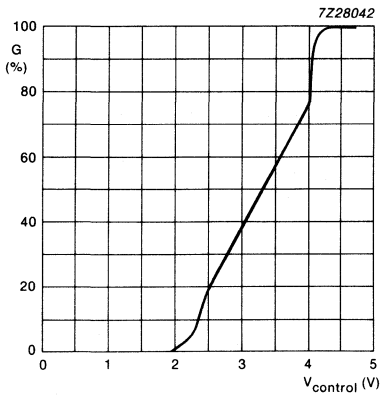


Fig.5 Typical saturation control curve.

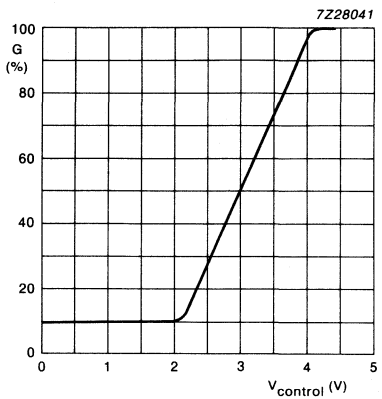
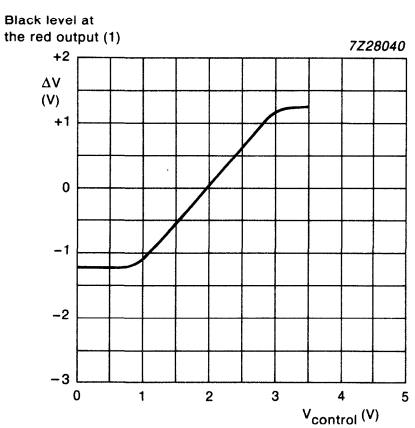


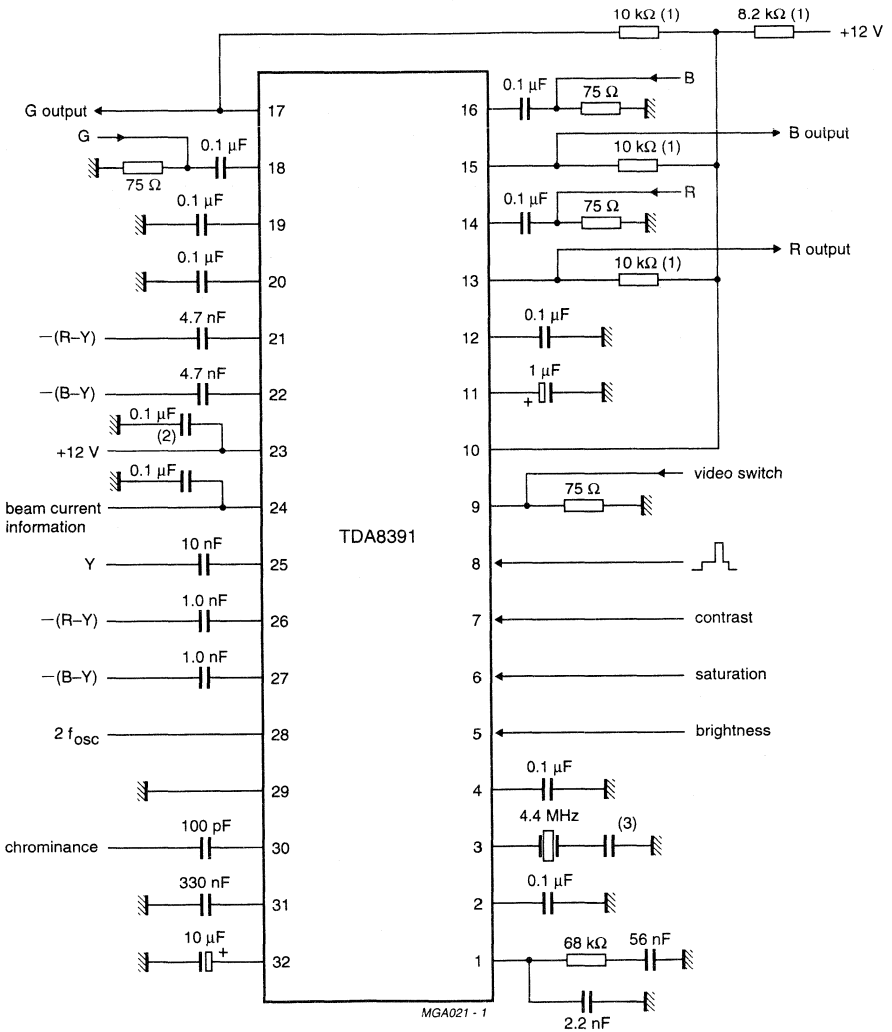
Fig.6 Typical contrast control curve.



(1) with respect to the measuring pulse.

Fig.7 Typical brightness control curve.

APPLICATION INFORMATION



(1) Artificial black current is to be removed for real black current from the video output stages. (2) It is recommended to decouple to pin 29 via the shortest possible way. (3) Dependent on type of crystal used.

Fig.8 Application diagram.

SECAM decoder TDA8395

FEATURES

- Fully integrated filters
- Alignment free
- For use with baseband delay

GENERAL DESCRIPTION

The TDA8395 is a self-calibrating, fully integrated SECAM decoder. The IC should preferably be used in conjunction with the PAL/NTSC decoder TDA8362 or TDA8366 and with the switched capacitor baseband delay circuit TDA4660. The IC incorporates HF and LF filters, a demodulator and an identification circuit (luminance is not processed in this IC). The IC needs no adjustments and very few external components are required. A highly stable reference frequency is required for calibration and a two-level sandcastle pulse for blanking and burst gating.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage; pin 3	7.2	-	8.8	V
P_{tot}	total power dissipation	-	-	220	mW
$V_{16(p-p)}$	composite video input voltage (peak-to-peak value); pin 16	-	1.0	1.5	V
$V_{O(p-p)}$	-(R-Y) output voltage amplitude (peak-to-peak value); pin 9	-	1.05	-	V
$V_{O(p-p)}$	-(B-Y) output voltage amplitude (peak-to-peak value); pin 10	-	1.33	-	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8395	16	DIL	plastic	SOT38GE1

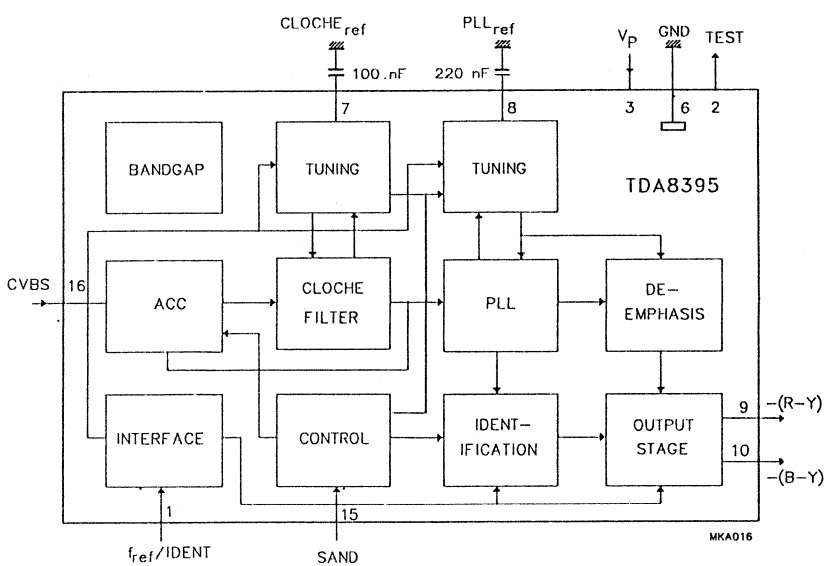


Fig.1 Block diagram.

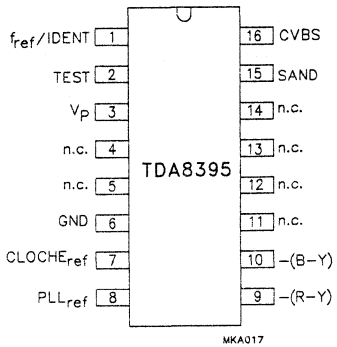


Fig.2 Pin configuration

PINNING

SYMBOL	PIN	DESCRIPTION
f_{ref}/IDENT	1	reference frequency input/identification input
TEST	2	test output
V_P	3	positive supply voltage
n.c.	4	not connected
n.c.	5	not connected
GND	6	ground
$CLOCHE_{ref}$	7	Cloche reference filter
PLL_{ref}	8	PLL reference
-(R-Y)	9	-(R-Y) output
-(B-Y)	10	-(B-Y) output
n.c.	11	not connected
n.c.	12	not connected
n.c.	13	not connected
n.c.	14	not connected
SAND	15	sandcastle pulse input
CVBS	16	video (chrominance) input

FUNCTIONAL DESCRIPTION

The TDA8395 is a self-calibrating SECAM decoder designed for use with a baseband delay circuit.

During frame retrace a 4.433619 MHz reference frequency is used to calibrate the filters and the demodulator. The reference frequency should be very stable during this period.

The Cloche filter is a gyrator-capacitor type filter the resonance frequency of which is controlled during the calibration period and offset during scan; this ensures the correct frequency during calibration.

The demodulator is a Phase-Locked Loop (PLL) type demodulator which uses the frequency reference and the bandgap reference to force the PLL to the required demodulation characteristic.
The low frequency de-emphasis is matched to the PLL and is controlled by the tuning voltage of the PLL.

A digital identification circuit scans the incoming signal for SECAM (only line-identification is implemented). The identification circuit needs to communicate with the TDA8362 to guarantee that the output signal from the decoder is only available when no PAL signal has been identified. If a SECAM signal is decoded a request for colour-on is transmitted to pin 1 (current is sunk). If the signal request is granted (i.e. pin 1 is HIGH therefore no PAL) the colour difference outputs (-(B-Y) and -(R-Y)) from the TDA8362 are high impedance and the output signals from the TDA8395 are switched ON.

If no SECAM signal is decoded during a two-frame period the demodulator will be initialized before another attempt is made also during a two-frame period. The CD outputs will be blanked or high-impedance depending on the logic level at pin 1.

A two-level sandcastle pulse generates the required blanking periods and, also, clocks the digital identification pulse on the falling edge of the burst gate pulse. To enable the calibration period to be defined the vertical retrace is discriminated from the horizontal retrace, this is achieved by measuring the width of the blanking period.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	-	8.8	V
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	–25	+70	°C

CHARACTERISTICS

V_P = 8.0 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 3)						
V_P	positive supply voltage		7.2	8.0	8.8	V
I_P	supply current		-	18	25	mA
P_{tot}	total power dissipation		-	144	220	mW
CVBS input (pin 16)						
$V_{16(p-p)}$	composite video input voltage (peak-to-peak value)		-	1.0	1.5	V
$V_{16(p-p)}$	chrominance input voltage (peak-to-peak value)	note 1	15	-	300	mV
Z_I	input impedance	note 2	-	15	-	kΩ
CLOCHE (pin 7)						
V_{tc}	tuning voltage		2.5	3.5	4.5	V
f_0	resonance frequency	note 3	4.266	4.286	4.306	MHz
B	bandwidth		241	268	295	kHz
Demodulator						
V_{td}	tuning voltage; pin 8		3.5	-	4.8	V
$V_{O(p-p)}$	output voltage amplitude (peak-to-peak value); pin 9	100/75 colour bar	0.97	1.05	1.13	V
$V_{O(p-p)}$	output voltage amplitude (peak-to-peak value); pin 10	100/75 colour bar	1.23	1.33	1.43	V
NLE	non-linearity error	100/75 colour bar; note 4	-	-	3	%
-(B-Y)/-(R-Y)	ratio of -(B-Y) and -(R-Y)		1.23	1.27	1.32	
$f_{be-(R-Y)}$	black-level error -(R-Y)	note 5	-	-	5	kHz
$f_{be-(B-Y)}$	black-level error -(B-Y)	note 5	-	-	7	kHz
V_O	output voltage level during blanking		-	2.8	-	V
B_O	output bandwidth		-	1.3	-	MHz
S/N	signal-to-noise ratio	note 6	40	-	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_p	pole-frequency LF de-emphasis		77	85	93	kHz
f_p/f_0	ratio of pole and zero frequency		-	3	-	
$V_{rh(p-p)}$	residual harmonic voltage (peak-to-peak value)		-	-	10	mV
$Z_{O(e)}$	output impedance SECAM enabled	pin 1 HIGH	-	-	600	Ω
$Z_{O(d)}$	output impedance SECAM disabled	pin 1 LOW	1	-	-	MΩ
Sandcastle pulse						
V_{bl}	blanking detection level		1.0	1.25	1.5	V
V_{bg}	burst gate detection level		3.5	3.85	4.2	V
t_f	falling edge of burst gate to start sync		8.5	9.0	9.5	µs
Reference/communication						
f_{ref}	reference frequency	note 7	-	4.4336	-	MHz
$V_{ref(p-p)}$	reference voltage amplitude (peak-to-peak value)		0.20	-	0.50	V
V_{ed}	SECAM enable detection level; pin 1		-	2.8	3.3	V
V_{dd}	SECAM disabled detection level; pin 1	note 8	1.5	2.0	-	V
I_s	sink current at SECAM identification; pin 1	note 9	-	150	-	µA
Identification						
t_i	identification time		-	4	-	frames
H	colour on/off hysteresis		3	-	-	dB

Notes to the characteristics

1. If measured in the burst-period of a blue line.
2. The video input is AC-coupled.
3. During scan.
4. Measured as 100% x ($|V_u| - |V_i|$) / ($|V_u| + |V_i|$); see Fig. 3.
5. Converted to input frequency error.
6. Defined as the ratio between the peak-to-peak value of the B-Y component of the demodulated 100/75 colour bar and the peak-to-peak value of the noise.
7. The reference should be stable during frame blanking.
8. The SECAM enable and disable timing should preferrably be at the end of the frame blanking.
9. The externally supplied voltage should exceed 0.5 V.

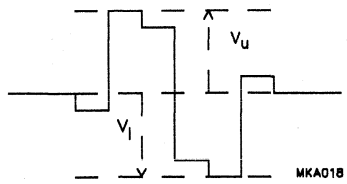


Fig.3 Non-linearity definition.

TIMING

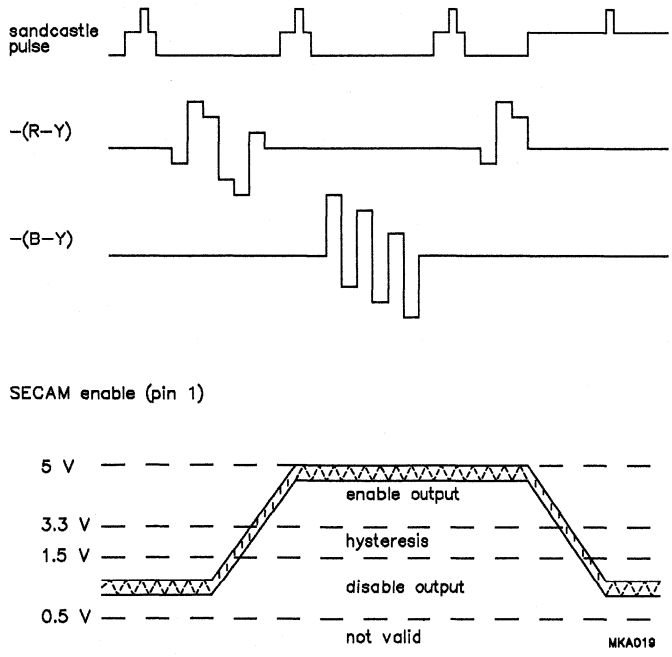


Fig.4 Timing waveforms.

APPLICATION INFORMATION

The leakage current at pin 8 should be well below 20 nA to meet the specification of the black levels (C8 = 220 nF). The leakage current at pin 7 should be well below 60 nA to meet the specification of the Cloche resonance frequency (C7 = 100 nF).

The capacitors C7 and C8 should be connected to the ground pin as close as possible to the package. If not, this can result in a black level error for both channels.

TEST INFORMATION

The performance of the Cloche filter can be measured at pin 2. The use of a FET-probe is advised for low capacitive loading.

TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH INTEGRATED FILTERS AND I²C-BUS CONTROL

GENERAL DESCRIPTION

The TDA8415 is a processor of stereo/dual language signals (B/G-standard) for stereo sound television receivers and VTRs, using the switched-capacitor technique. The AF signals at the TDA8415 inputs must be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The carrier frequency of the second channel is also modulated by an identification signal (stereo or dual sound). The device is controlled by a microcomputer via the two-line, bidirectional I²C-bus.

Features

- Use of the switched-capacitor technique for signal processing
- Small amount of peripheral components
- Integrated anti-aliasing filters
- Low distortion AF signal handling
- Integrated de-emphasis with a time constant of 50 μs
- Function and software are compatible with the TDA8405
- Two general purpose output ports
- Full ESD protection

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage (pin 15)		V_P	–	12	–	V
Supply current (pin 15)		I_P	–	10	–	mA
AF output signal (RMS value) (pins 11 to 14)		V_o	–	2	–	V
Weighted signal-to-noise ratio of the AF output signals (CCIR 468/3)		(S+W)/W	70	–	–	dB
Crosstalk attenuation stereo mode at	f = 1 kHz	α_S	40	–	–	dB
dual sound mode at	f = 40 Hz to 12.5 kHz	α_{DS}	70	–	–	dB
Pilot signal input sensitivity		V_i	–	2.5	–	mV
Total harmonic distortion		THD	–	0.1	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

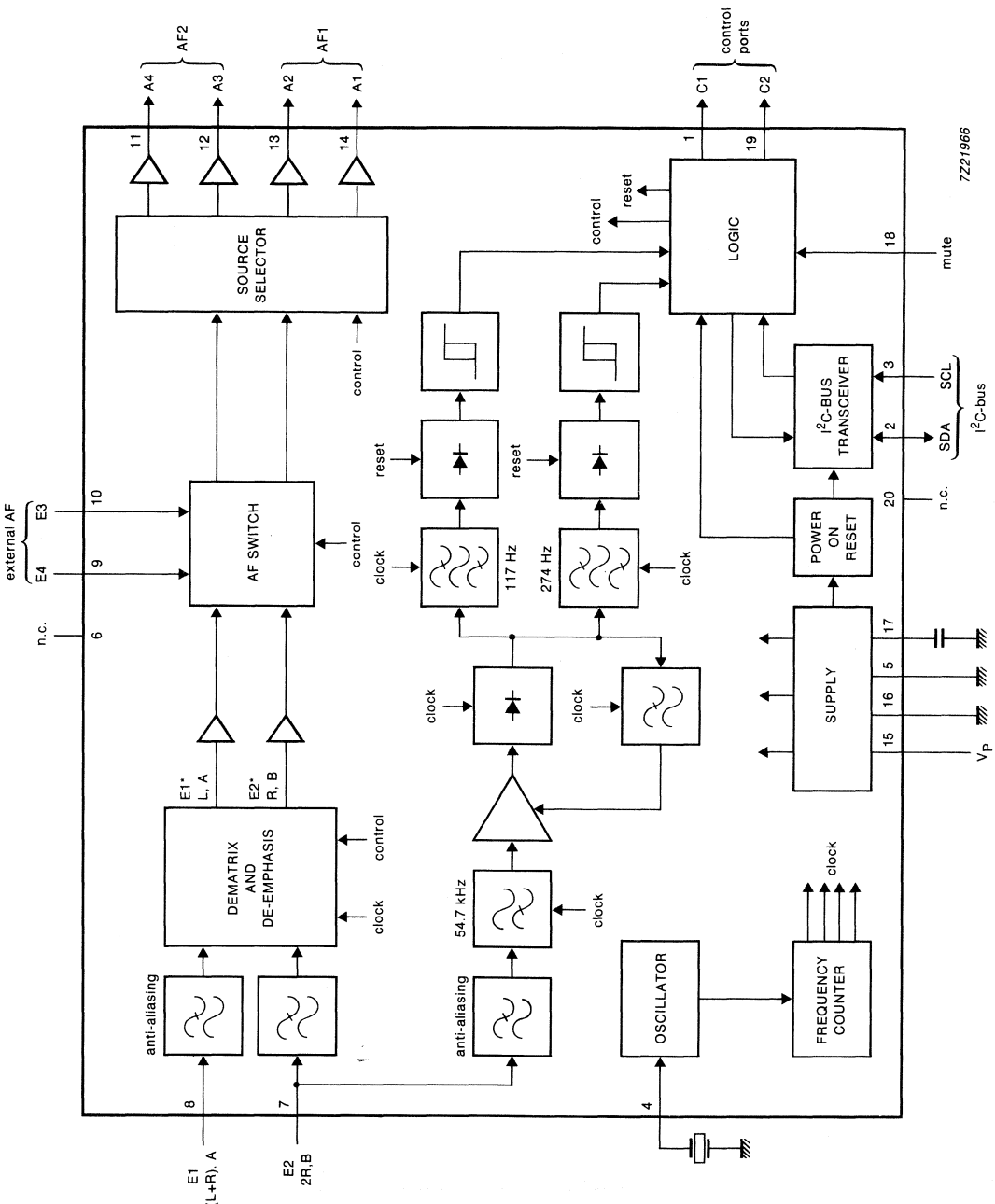


Fig.1 Block diagram.

DEVELOPMENT DATA

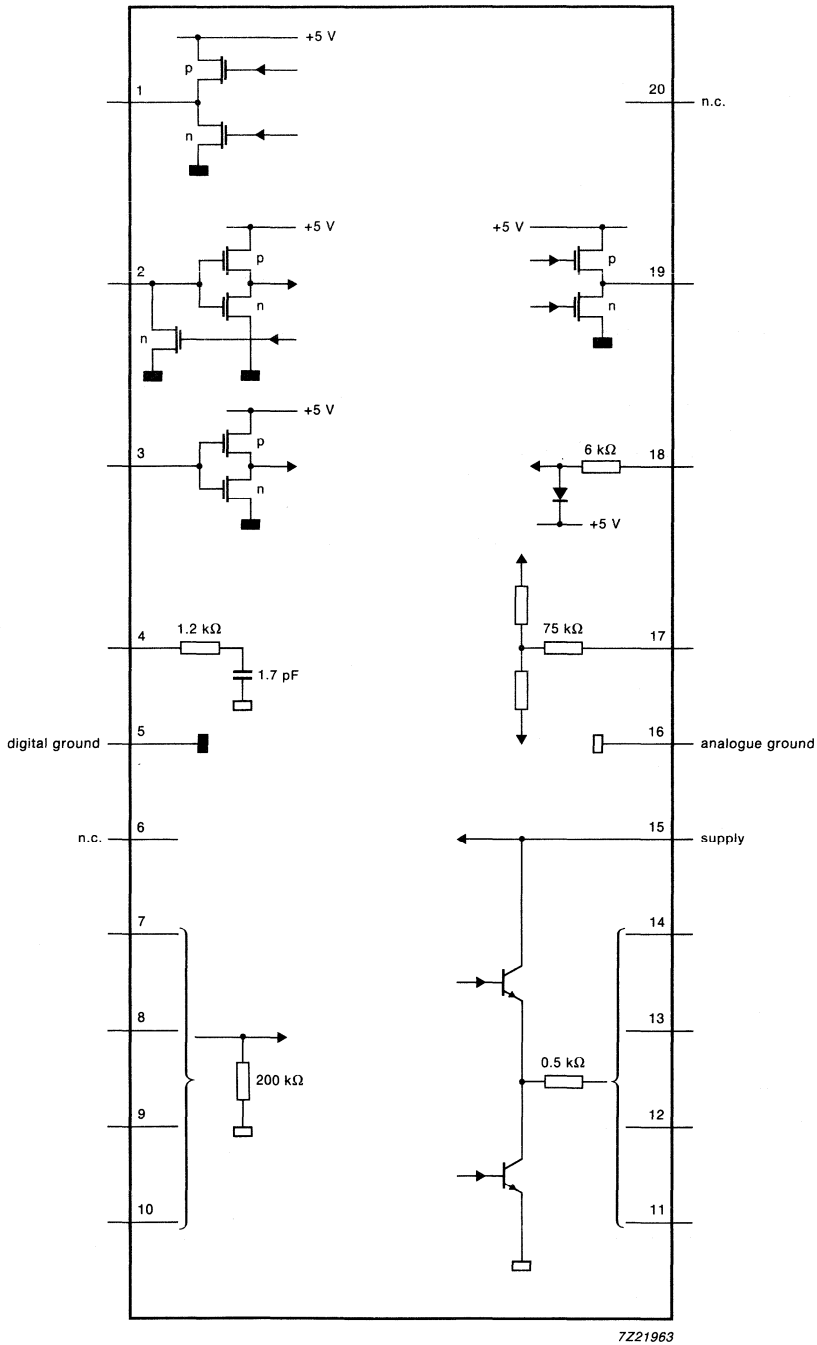


Fig.2 Input and output loading diagram.

PINNING

1	Control port C1	11	Output A4 AF 2 output
2	SDA, serial data line (I^2C-bus)	12	Output A3 AF 2 output
3	SCL, serial clock line (I^2C-bus)	13	Output A2 AF 1 output
4	Oscillator input (or quartz)	13	Output A1 AF 1 output
5	Digital ground (0 V)	15	Supply voltage V_P
6	Not connected, but reserved	16	Analogue ground (0 V)
7	Sound channel input AF2 (E2)	17	Ripple rejection improvement
8	Sound channel input AF1 (E1)	18	Mute input
9	External AF input (E4)	19	Control port C2
10	External AF input (E3)	20	Not connected, but reserved

FUNCTIONAL DESCRIPTION

Anti-aliasing filters

Frequency band limitation is performed by a second order Sallen and Key low-pass filter inserted in the AF signal path and the identification circuit. This limitation is necessary because of the time-discrete signal processing needed to meet the Nyquist criterium.

Identification

To enable the identification of the transmitted AF signal (mono, stereo or dual sound), the carrier frequency of the second channel (E2) is also modulated by an identification signal. The identification signal is a 54.6875 kHz pilot carrier signal which is 50% amplitude modulated by either a 117.4 Hz signal for stereo transmission or by a 274.1 Hz signal for dual sound transmission.

The identification section of the circuit consists of a 54 kHz high-pass filter followed by a gain controlled amplifier with an AM demodulator. The total gain of the high-pass filter and the amplifier is approximately 56 dB. The demodulated identification signal is filtered by the identification band-pass filters, (117.4 Hz for stereo transmission, 274.1 Hz for dual sound transmission). The output from either filter is converted to a DC signal by a peak detector and the necessary hysteresis is performed by a Schmitt-trigger. The resultant DC output signals indicate the status of the transmitter (mono, stereo or dual sound).

De-matrix and de-emphasis

Depending on the results of the identification circuit (mono, stereo or dual sound) the AF signals at the inputs E1 and E2 are converted to the signals at E1* and E2* as listed in Table 1.

Table 1 Transmitter status

transmitter status	E1	E2	E1*	E2*
mono	0.7(L+R)	–	2(L+R)	–
stereo	0.7(L+R)	2R	4L	4R
dual sound	0.7A	B	2A	2B

Where L = left channel signal; R = right channel signal; A = first sound channel signal and B = second sound channel signal.

This section of the circuit also performs the de-emphasis (50 μs time constant) with a high degree of accuracy.

AF switch

The AF switch is used to switch to either the internal sound sources (E1* or E1* and E2*) or, to the external sound source (E3 and E4) and is controlled via the I²C-bus.

Source selector

The source selector is used to connect the outputs from the AF switch to the outputs A1 to A4 as illustrated by Table 5. The selector is controlled via the I²C-bus.

Muting

In this mode the AF outputs A1 to A4 are muted, and the identification circuit is deactivated (mono). The muting is active after power-on reset or as a result of user control (via the mute input and bit CR3 of the control byte of the mute and port control register; see Table 4).

Sound mute

If the switch register is set to (00) hex, (sound mute) only the AF outputs are muted, the identification circuit is still active and can be read (status register) via the I²C-bus.

Power-on reset

The following actions are carried out by the internal power-on reset when it is active:

- The AF outputs are muted
- The identification circuit is deactivated (mono)
- The control ports (C1 and C2) are set LOW
- The I²C-bus transceiver is initialized

When the power-on reset becomes passive the following occurs:

- The AF outputs are kept in the mute state until the contents of the switch register are changed from (00) hex via the I²C-bus
- The identification circuit is activated
- The control ports are LOW until the mute and control port register is changed (CR bits 10, 11, 20 and 21)
- The I²C-bus transceiver is activated

DEVELOPMENT DATA

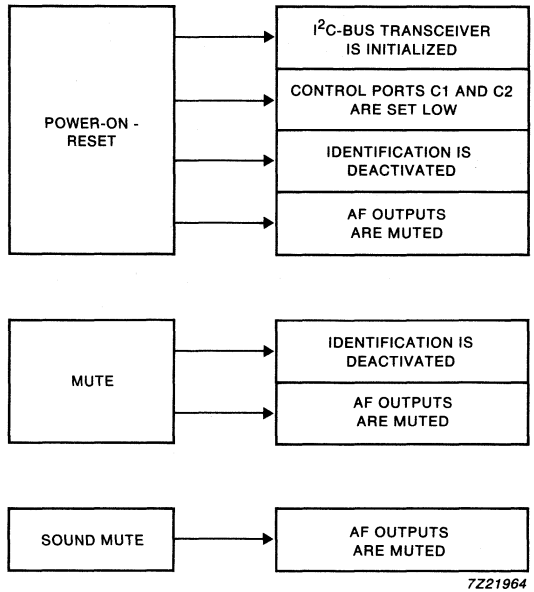


Fig.3 Mute modes.

Control ports

The general purpose control ports C1 and C2 can be set to LOW, HIGH or high impedance via the I²C-bus.

I²C-bus receiver and data handling

Bus specification

The TDA8415 is controlled, via the bidirectional 2-line I²C-bus, by a microcomputer. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

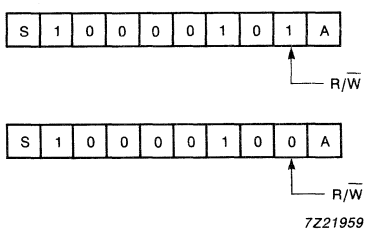
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in the CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as the stop condition (P). The bus receiver will be reset on the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

The I²C-BUS PROTOCOL OF THE TDA8415

The TDA8415 is controlled by a microcomputer and can be written to or read from via the I²C-bus.

The first byte is the address and determines whether the TDA8415 is to be read from (status register) or written to (switch register or mute and port control register).



Read from (TDA8415 is a slave transmitter)

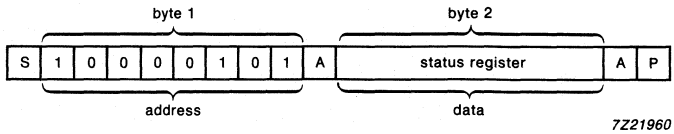
Write to (TDA8415 is a slave receiver)

Where S = start bit and A = acknowledge bit

Fig.4 Address byte.

Reading the TDA8415

Reading the TDA8415 means reading the status register and the data stream will have the format as illustrated in Fig.5 below.



Where S = start bit; A = acknowledge bit and P = stop bit

Fig.5 Read format.

The second byte, the contents of the status register, is defined by Table 2.

Table 2 Status register

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	ST	DS	0	0	0	0	0

PONRES = power on reset
1 = power on reset active after switching on or power breakdown
0 = after reading the status register
ST = stereo transmission
DS = dual sound transmission

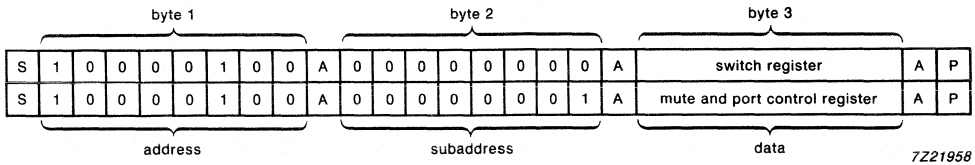
The truth table for the ST and DS bits is provided by Table 3.

Table 3 Truth table for ST and DS bits

ST	DS	definition
0	0	mono transmission
0	1	dual sound transmission
1	0	stereo transmission
1	1	not possible

Writing to the TDA8415

Writing to the TDA8415 means, writing to either the switch register or the mute and port control register. Which one is to be addressed is defined by the subaddress (the second byte) as illustrated by Fig.6 below. The third byte contains the information to be stored in the specified register.



Where S = start bit; A = acknowledge bit and P = stop bit

Fig.6 Write format.

Table 4 defines the contents of the mute and port control register.

DEVELOPMENT DATA

Table 4 Mute and port control register

D7	D6	D5	D4 CR3	D3 CR21	D2 CR20	D1 CR11	D0 CR10	definition
X	X	X				0	0	control port C1 = LOW
X	X	X				0	1	control port C1 = HIGH
X	X	X				1	X	control port C1 = high impedance
X	X	X		0	0			control port C2 = LOW
X	X	X		0	1			control port C2 = HIGH
X	X	X		1	X			control port C2 = high impedance
X	X	X	0					mute is active when pin 18 is LOW (default)
X	X	X	1					mute is active when pin 18 is HIGH

Where: X = don't care.

Table 5 defines the contents of the switch register.

Table 5 Switch register

switch register		input E1	E2	E3	E4	output A1	A2	A3	A4	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
sound mute	–	–	–	–	–	no signal				0	0	0	0	0	0	0	0	(00)
mono	M	M	M	–	–	M	M	M	M	0	0	0	1	0	0	0	0	(10)
	St	L*	R	–	–	L*	L*	L*	L*	0	0	0	1	0	0	0	0	(10)
stereo	St	L*	R	–	–	L	R	L	R	0	0	1	0	1	0	1	0	(2A)
sound A	DS	A	B	–	–	A	A	A	A	0	0	0	1	0	0	0	0	(10)
sound B	DS	A	B	–	–	B	B	B	B	0	0	0	1	1	1	1	1	(1F)
dual sound	DS	A	B	–	–	A	A	B	B	0	0	0	1	1	1	0	0	(1C)
	DS	A	B	–	–	B	B	A	A	0	0	0	1	0	0	1	1	(13)
dual sound	DS	A	B	–	–	A	B	A	A	0	0	0	1	0	0	1	0	(12)
mix	DS	A	B	–	–	A	A	A	B	0	0	0	1	1	0	0	0	(18)
	DS	A	B	–	–	A	B	A	B	0	0	0	1	1	0	1	0	(1A)
	DS	A	B	–	–	B	B	A	B	0	0	0	1	1	0	1	1	(1B)
	DS	A	B	–	–	A	B	B	B	0	0	0	1	1	1	1	0	(1E)
external	–	–	–	E3	E4	E3	E3	E3	E3	0	1	1	1	0	0	0	0	(70)
	–	–	–	E3	E4	E4	E4	E4	E4	0	1	1	1	1	1	1	1	(7F)
	–	–	–	E3	E4	E3	E4	E3	E4	0	1	1	1	1	0	1	0	(7A)
	–	–	–	E3	E4	E4	E4	E3	E3	0	1	1	1	0	0	1	1	(73)
	–	–	–	E3	E4	E3	E3	E4	E4	0	1	1	1	1	1	0	0	(7C)
	–	–	–	E3	E4	E3	E4	E3	E3	0	1	1	1	0	0	1	0	(72)
	–	–	–	E3	E4	E3	E3	E3	E4	0	1	1	1	1	0	0	0	(78)
	–	–	–	E3	E4	E4	E4	E3	E4	0	1	1	1	1	0	1	1	(7B)
	–	–	–	E3	E4	E3	E4	E4	E4	0	1	1	1	1	1	1	0	(7E)

Where: M = mono; St = stereo. DS = dual sound; R = right; L = left; L* = (L+R)/2; A = sound A; B = sound B.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage*	$V_P = V_{15-16}$	–	–	13.2	V
Output current					
pins 11, 12, 13, 14	I_O	–	–	10	mA
pins 1 and 19 (sink)	I_O	–	–	7	mA
(source)	$-I_O$	–	–	3	mA
Input voltage (not pin 18)	V_I	0	–	V_P	V
Input voltage pin 18	$V_I = V_{18-16}$	–	–	7	V
Output voltage	V_O	0	–	V_P	V
Total power dissipation	P_{tot}	–	–	1	W
ESD protection (each pin) (0 Ω/200 pF)		500	–	–	V
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Storage temperature range	T_{stg}	–40	–	+ 150	°C

DEVELOPMENT DATA

* Supply voltage may be applied only when both pins 5 and 15 are connected to ground.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C. Measurement conditions (see Fig.7): reference level is 1 V (RMS); test frequency = 3.183 kHz; noise measurement in accordance with DIN 45405, CCIR 468-3; oscillator frequency = 10 MHz; pre-emphasis time constant = 50 μs.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage		$V_P = V_{15-16}$	10.8	12	13.2	V
Supply current		$I_P = I_{15}$	–	10	–	mA
DC levels						
pins 7 - 14 and 17		V_{n-16}	–	3.25	–	V
pin 4		V_{4-5}	–	2	–	V
Bus transceiver						
Clock frequency (I^2C-bus)	note 1	f_{CLK}	0.7	–	100	kHz
Clock SCL (pin 3)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Timing LOW period		t_{LOW}	4.7	–	–	μs
Timing HIGH period		t_{HIGH}	4	–	–	μs
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Data SDA (pin 2)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	0.25	–	–	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Output current LOW		I_{OL}	3	–	–	mA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Mute port (pin 18)						
Input voltage LOW	note 2	V_{IL}	−0.3	–	1.5	V
Input voltage HIGH	note 2	V_{IH}	3	–	5	V
Control ports (pins 1 and 19)						
Output voltage LOW	note 3	V_{OL}	–	–	0.5	V
Output voltage HIGH	note 3	V_{OH}	4.5	–	5	V
Output impedance	3-state	Z_o	1	–	–	MΩ
Output current LOW		I_{OL}	1	–	–	mA
Output current HIGH		$-I_{OH}$	1	–	–	mA
AF stages and identification (pins 7 to 14)						
Input impedance (pins 7 to 10)		Z_i	150	200	–	kΩ
Input voltage E1		V_I	–	–	0.7	V
Input voltage E2		V_I	–	–	1	V
Input voltage E2 for identification active (RMS value)	note 4	V_i	2.5	–	–	mV
Voltage gain 7-15/output	note 5	G_v	5.9	6	6.1	dB
Voltage gain 8-15/output	note 5	G_v	8.9	9	9.1	dB
Voltage gain 9, 10-15/output		G_v	−0.1	0	0.1	dB
Crosstalk attenuation	notes 6 to 8					
dual mode		α_{ds}	70	75	–	dB
stereo mode		α_s	30	50	–	dB

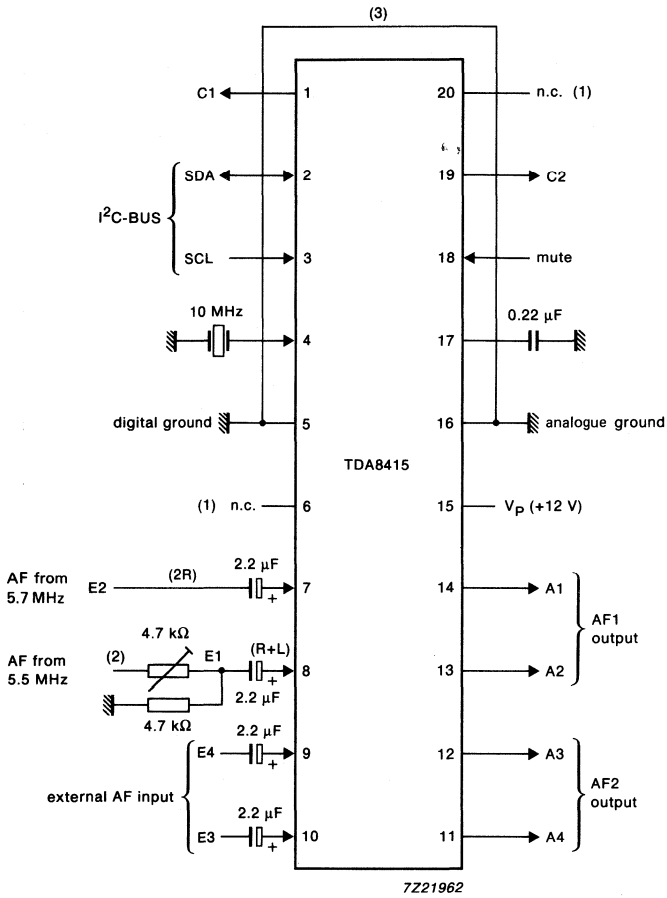
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AF stages and identification (continued)						
Output impedance (pins 11 to 14)		Z_o	400	500	600	Ω
De-emphasis time constant	note 9		49.5	50	50.5	μs
Frequency response	note 6	Δf	−1	–	1	dB
Total harmonic distortion	note 10	THD	–	–	0.2	%
Capacitive load (pins 11 to 14)		C_L	–	–	1.5	nF
Output signal (RMS value) (pins 11 to 14)	THD ⩽ 0.2%	V_o	–	–	2	V
Ripple rejection	note 11	RR	50	66	–	dB
Noise from I^2C-bus		NR	–	–	−80	dB
Signal-to-noise ratio		(S+W)/W	70	–	–	dBV CCIR
Signal suppression during mute	note 6	SS	70	75	–	dB
Change of output DC voltage level between any two modes			–	–	30	mV
Oscillator						
Oscillator frequency		f_{OSC}	–	10	–	MHz
External oscillator signal (RMS value)		V_{4-5}	1.7	–	–	V
Quartz series resistor		R1	–	–	100	Ω
Impedance		Z_i	–	−1.2 + j9.3	–	kΩ
Capacitance		C_{OSC}	–	1.7	–	pF

Notes to the characteristics

1. Full specification of I²C-bus will be supplied on request.
2. Programmable mute state. If the CR3 bit of the mute and port control register is LOW, the mute is active LOW; if it is HIGH, the mute input is active HIGH.
3. Output current $I_O \approx 1$ mA.
4. Unmodulated.
5. f = 400 Hz; R_L = 1 MΩ.
6. 40 Hz $\leqslant$ f $\leqslant$ 15 kHz.
7. In dual mode: A(B)-signal into B(A)-channel.
   In stereo mode: R-signal into left, L-signal = 0, reference is 1 V RMS.
8. Source impedance $|Z_S| < 1$ kΩ.
9. Equivalent to an output level of −3 dB at f = 3.183 kHz.
10. V_o = 1 V RMS; f = 1 kHz.
11. Test circuit see Fig.7.

DEVELOPMENT DATA

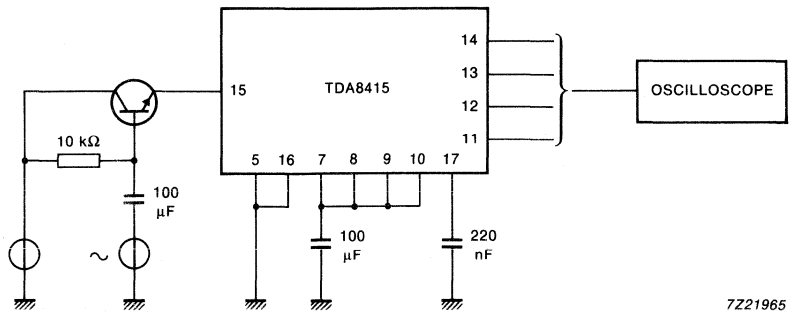


(1) These pins are not connected internally and should not be connected on the printed circuit board in order to maintain compatibility with future devices.

(2) This potentiometer has to be adjusted to achieve the best stereo separation.

(3) Direct connection between pins 5 and 16 is needed.

Fig.7 Application and test circuit.



Voltage input = supply voltage + pulse voltage at 70 Hz = 12 V ± 50 mV (p-p).

Fig.8 Ripple rejection test circuit.

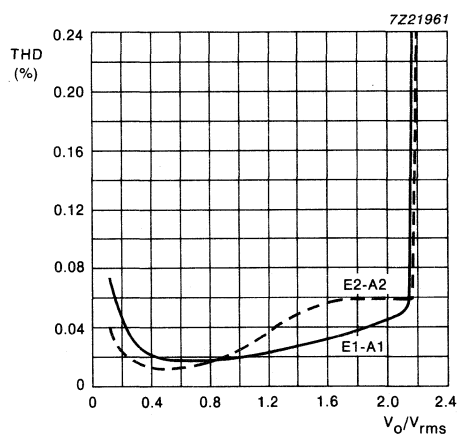


Fig.9 Total harmonic distortion diagram (stereo mode).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH INTEGRATED FILTERS AND I²C-BUS CONTROL

GENERAL DESCRIPTION

The TDA8416 is a processor of stereo/dual language signals (B/G-standard) for stereo sound television receivers and VTRs, using the switched-capacitor technique. The AF signals at the TDA8416 inputs must be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The carrier frequency of the second channel is also modulated by an identification signal (stereo or dual sound). The device is controlled by a microcomputer via the two-line, bidirectional I²C-bus.

Features

- Use of the switched-capacitor technique for signal processing
- Small amount of peripheral components
- Integrated anti-aliasing filters
- Low distortion AF signal handling
- Integrated de-emphasis with a time constant of 50 μs
- Two general purpose output ports
- Full ESD protection

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage (pin 15)		V_P	–	12	–	V
Supply current (pin 15)		I_P	–	10	–	mA
AF output signal (RMS value) (pins 11 to 14)		V_o	–	2	–	V
Weighted signal-to-noise ratio of the AF output signals (CCIR 468/3)		(S+W)/W	70	–	–	dB
Crosstalk attenuation stereo mode at	f = 1 kHz	α_S	40	–	–	dB
dual sound mode at	f = 40 Hz to 12.5 kHz	α_{DS}	70	–	–	dB
Pilot signal input sensitivity		V_i	–	2.5	–	mV
Total harmonic distortion		THD	–	0.1	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

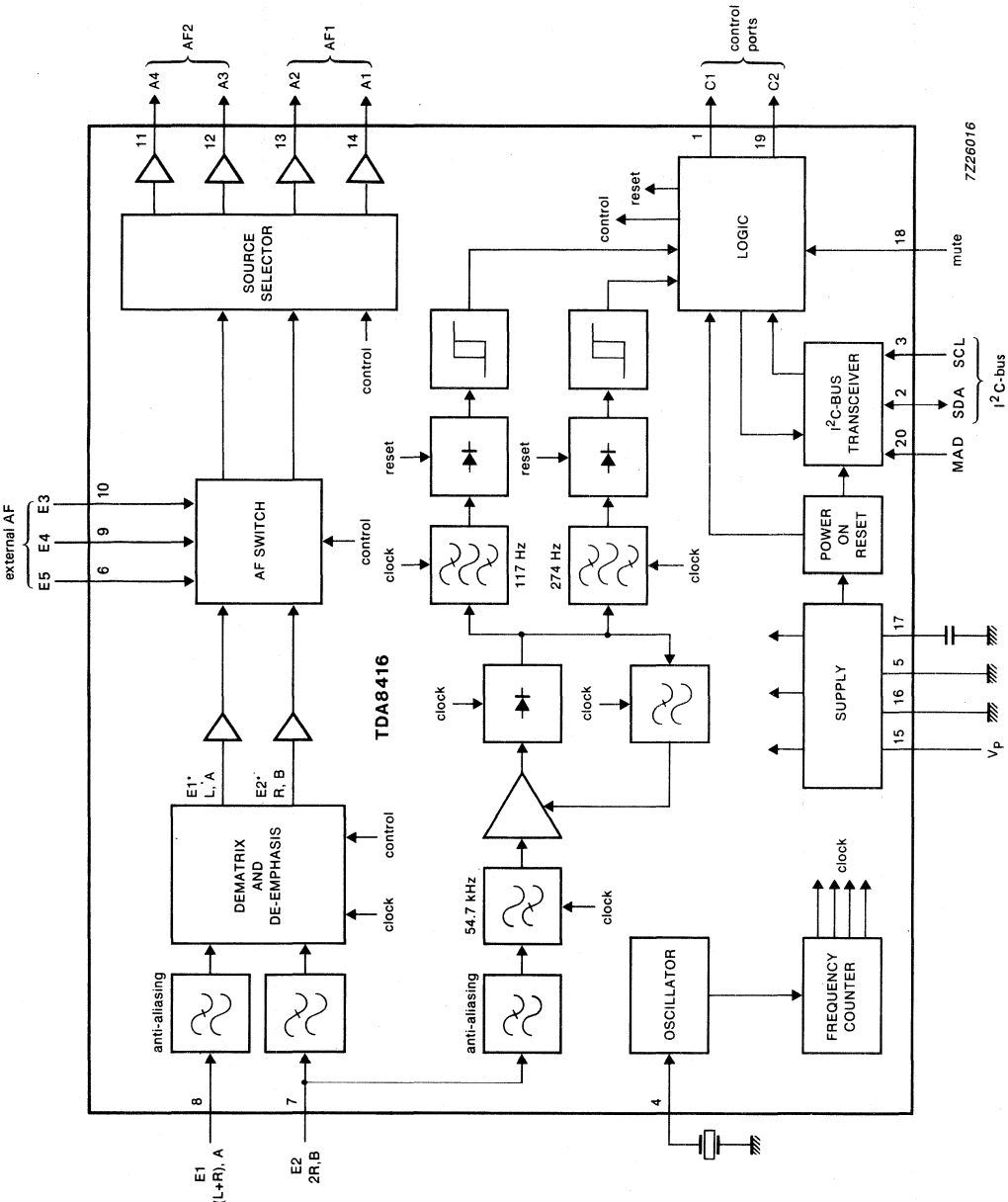


Fig.1 Block diagram.

DEVELOPMENT DATA

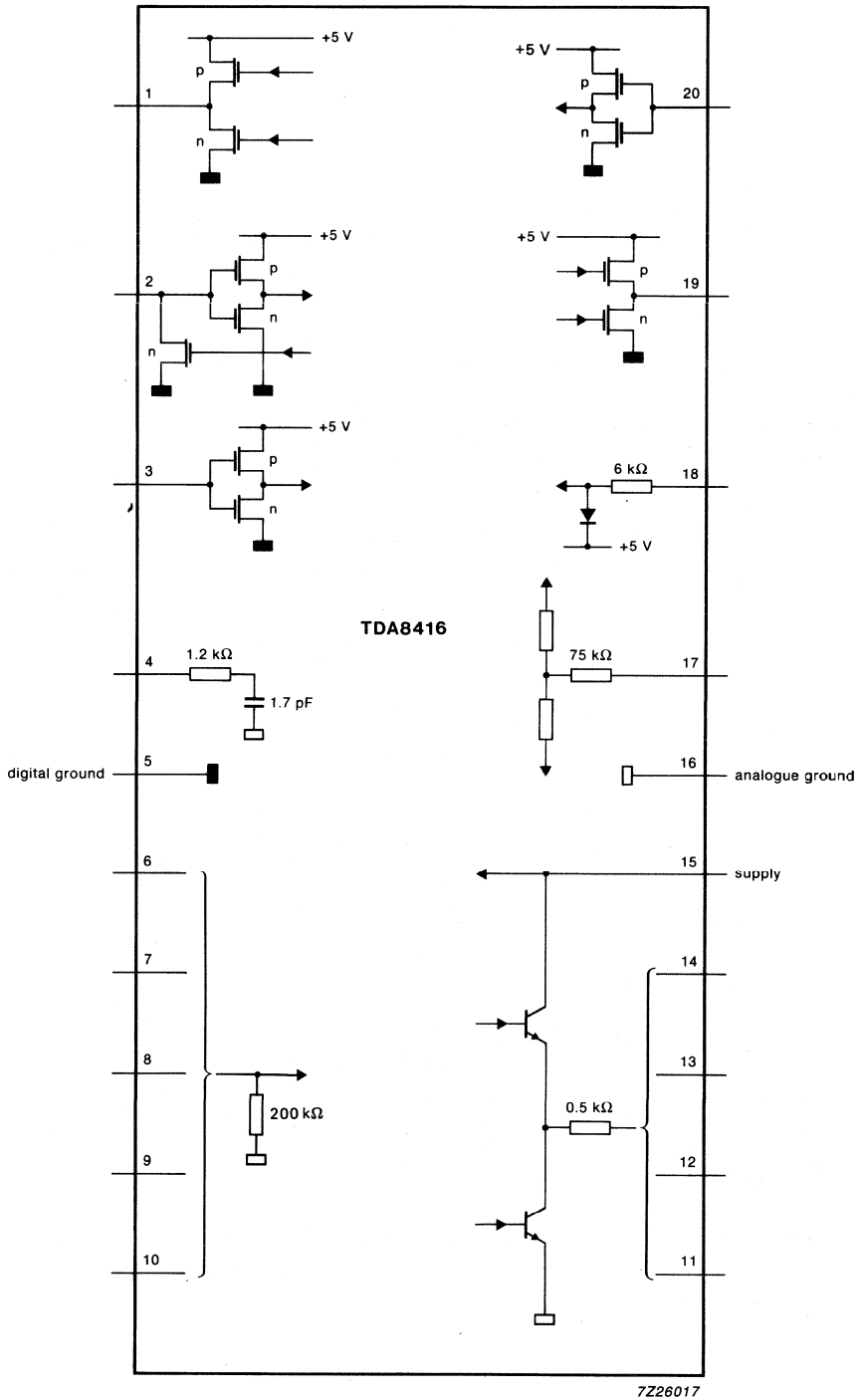


Fig.2 Input and output loading diagram.

PINNING

1 Control port C1
2 SDA, serial data line (I^2C-bus)
3 SCL, serial clock line (I^2C-bus)
4 Oscillator input (or quartz)
5 Digital ground (0 V)
6 External AF input (E5)
7 Sound channel input AF2 (E2)
8 Sound channel input AF1 (E1)
9 External AF input (E4)
10 External AF input (E3)
11 Output A4 AF 2 output
12 Output A3 AF 2 output
13 Output A2 AF 1 output
13 Output A1 AF 1 output
15 Supply voltage V_P
16 Analogue ground (0 V)
17 Ripple rejection improvement
18 Mute input
19 Control port C2
20 Module address (MAD)

FUNCTIONAL DESCRIPTION

Anti-aliasing filters

Frequency band limitation is performed by a second order Sallen and Key low-pass filter inserted in the AF signal path and the identification circuit. This limitation is necessary because of the time-discrete signal processing needed to meet the Nyquist criterium.

Identification

To enable the identification of the transmitted AF signal (mono, stereo or dual sound), the carrier frequency of the second channel (E2) is also modulated by an identification signal. The identification signal is a 54.6875 kHz pilot carrier signal which is 50% amplitude modulated by either a 117.4 Hz signal for stereo transmission or by a 274.1 Hz signal for dual sound transmission.

The identification section of the circuit consists of a 54 kHz high-pass filter followed by a gain controlled amplifier with an AM demodulator. The total gain of the high-pass filter and the amplifier is approximately 56 dB. The demodulated identification signal is filtered by the identification band-pass filters, (117.4 Hz for stereo transmission, 274.1 Hz for dual sound transmission). The output from either filter is converted to a DC signal by a peak detector and the necessary hysteresis is performed by a Schmitt-trigger. The resultant DC output signals indicate the status of the transmitter (mono, stereo or dual sound).

De-matrix and de-emphasis

Depending on the results of the identification circuit (mono, stereo or dual sound) the AF signals at the inputs E1 and E2 are converted to the signals at E1* and E2* as listed in Table 1.

Table 1 Transmitter status

transmitter status	E1	E2	E1*	E2*
mono	0.7(L+R)	–	2(L+R)	–
stereo	0.7(L+R)	2R	4L	4R
dual sound	0.7A	B	2A	2B

Where:

L = left channel signal
R = right channel signal
A = first sound channel signal
B = second sound channel signal

This section of the circuit also performs the de-emphasis (50 μs time constant) with a high degree of accuracy.

AF switch

The AF switch is used to switch to either the internal sound sources (E1* or E1* and E2*) or, to the external sound source (E3 and E4) and is controlled via the I²C-bus.

Source selector

The source selector is used to connect the outputs from the AF switch to the outputs A1 to A4 as illustrated by Table 5. The selector is controlled via the I²C-bus.

Muting

In this mode the AF outputs A1 to A4 are muted, and the identification circuit is deactivated (mono). The muting is active after power-on reset or as a result of user control (via the mute input and bit CR3 of the control byte of the mute and port control register; see Table 4).

Sound mute

If the switch register is set to (00) hex, (sound mute) only the AF outputs are muted, the identification circuit is still active and can be read (status register) via the I²C-bus.

Power-on reset

The following actions are carried out by the internal power-on reset when it is active:

- The AF outputs are muted
- The identification circuit is deactivated (mono)
- The control ports (C1 and C2) are set LOW
- The I²C-bus transceiver is initialized

When the power-on reset becomes passive the following occurs:

- The AF outputs are kept in the mute state until the contents of the switch register are changed from (00) hex via the I²C-bus
- The identification circuit is activated
- The control ports are LOW until the mute and control port register is changed (CR bits 10, 11, 20 and 21)
- The I²C-bus transceiver is activated

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

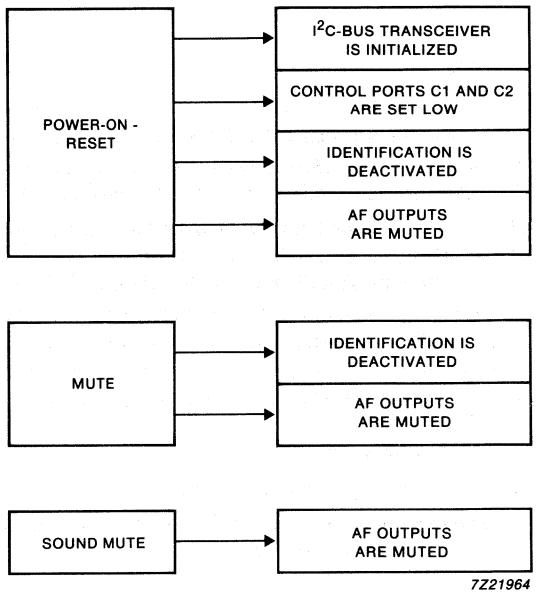


Fig.3 Mute modes.

Control ports

The general purpose control ports C1 and C2 can be set to LOW, HIGH or high impedance via the I²C-bus.

I²C-bus receiver and data handling

Bus specification

The TDA8416 is controlled, via the bidirectional 2-line I²C-bus, by a microcomputer. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

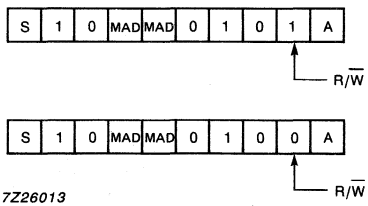
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in the CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as the start condition (S).
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as the stop condition (P). The bus receiver will be reset on the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

The I²C-BUS PROTOCOL OF THE TDA8416

The TDA8416 is controlled by a microcomputer and can be written to or read from via the I²C-bus.

The first byte is the address and determines whether the TDA8416 is to be read from (status register) or written to (switch register or mute and port control register).



Read from (TDA8416 is a slave transmitter)

Write to (TDA8416 is a slave receiver)

Where:

S = start bit
A = acknowledge bit
MAD = module address bit

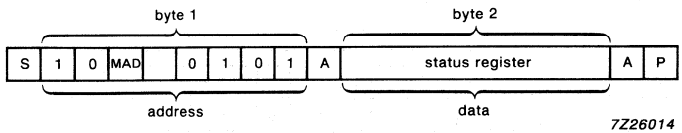
The MAD input (pin 20) allows the TDA8416 to operate from two different addresses:

MAD = LOW => A3 = A4 = 0 -> slave address = 1000 010
MAD = HIGH => A3 = A4 = 1 -> slave address = 1011 010

Fig.4 Address byte.

Reading the TDA8416

Reading the TDA8416 means reading the status register and the data stream will have the format as illustrated in Fig.5.



Where:

S = start bit
A = acknowledge bit
P = stop bit
MAD = module address

Fig.5 Read format.

The second byte, the contents of the status register, is defined by Table 2.

Table 2 Status register

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	ST	DS	0	0	0	0	0

Where:

PONRES = power on reset
1 = power on reset active after switching on or power breakdown
0 = after reading the status register
ST = stereo transmission
DS = dual sound transmission

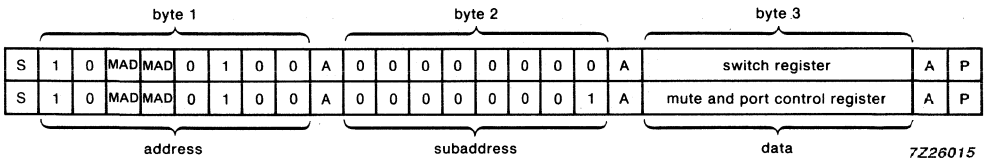
The truth table for the ST and DS bits is provided by Table 3.

Table 3 Truth table for ST and DS bits

ST	DS	definition
0	0	mono transmission
0	1	dual sound transmission
1	0	stereo transmission

Writing to the TDA8416

Writing to the TDA8416 means, writing to either the switch register or the mute and port control register. Which one is to be addressed is defined by the subaddress (the second byte) as illustrated by Fig.6. The third byte contains the information to be stored in the specified register.



Where:

S = start bit
A = acknowledge bit
P = stop bit
MAD = module address

Fig.6 Write format.

Table 4 defines the contents of the mute and port control register.

Table 4 Mute and port control register

D7	D6	D5	D4 CR3	D3 CR21	D2 CR20	D1 CR11	D0 CR10	definition
X	X	X				0	0	control port C1 = LOW
X	X	X				0	1	control port C1 = HIGH
X	X	X				1	X	control port C1 = high impedance
X	X	X		0	0			control port C2 = LOW
X	X	X		0	1			control port C2 = HIGH
X	X	X		1	X			control port C2 = high impedance
X	X	X	0					mute is active when pin 18 is LOW (default)
X	X	X	1					mute is active when pin 18 is HIGH

Where:

X = don't care

DEVELOPMENT DATA

Table 5 defines the contents of the switch register.

Table 5 Switch register

switch register		input E1	E2	E3	E4	E5	output A1	A2	A3	A4	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
sound mute	–	–	–	–	–	–	no signal				0	0	0	0	0	0	0	0	(00)
mono	M	M	M	–	–	–	M	M	M	M	0	0	0	1	0	0	0	0	(10)
	St	L*	R	–	–	–	L*	L*	L*	L*	0	0	0	1	0	0	0	0	(10)
stereo	St	L*	R	–	–	–	L	R	L	R	0	0	1	0	1	0	1	0	(2A)
sound A	DS	A	B	–	–	–	A	A	A	A	0	0	0	1	0	0	0	0	(10)
sound B	DS	A	B	–	–	–	B	B	B	B	0	0	0	1	1	1	1	1	(1F)
dual sound	DS	A	B	–	–	–	A	A	B	B	0	0	0	1	1	1	0	0	(1C)
	DS	A	B	–	–	–	B	B	A	A	0	0	0	1	0	0	1	1	(13)
dual sound	DS	A	B	–	–	–	A	B	A	A	0	0	0	1	0	0	1	0	(12)
mix	DS	A	B	–	–	–	A	A	A	B	0	0	0	1	1	0	0	0	(18)
	DS	A	B	–	–	–	A	B	A	B	0	0	0	1	1	0	1	0	(1A)
	DS	A	B	–	–	–	B	B	A	B	0	0	0	1	1	0	1	1	(1B)
	DS	A	B	–	–	–	A	B	B	B	0	0	0	1	1	1	1	0	(1E)
external	–	–	–	E3	E4	–	E3	E3	E3	E3	0	1	1	1	0	0	0	0	(70)
	–	–	–	E3	E4	–	E4	E4	E4	E4	0	1	1	1	1	1	1	1	(7F)
	–	–	–	E3	E4	–	E3	E4	E3	E4	0	1	1	1	1	0	1	0	(7A)
	–	–	–	E3	E4	–	E4	E4	E3	E3	0	1	1	1	0	0	1	1	(73)
	–	–	–	E3	E4	–	E3	E3	E4	E4	0	1	1	1	1	1	0	0	(7C)
	–	–	–	E3	E4	–	E3	E4	E3	E3	0	1	1	1	0	0	1	0	(72)
	–	–	–	E3	E4	–	E3	E3	E3	E4	0	1	1	1	1	0	0	0	(78)
	–	–	–	E3	E4	–	E4	E4	E3	E4	0	1	1	1	1	0	1	1	(7B)
	–	–	–	E3	E4	–	E3	E4	E4	E4	0	1	1	1	1	1	1	0	(7E)
	–	–	–	–	–	E5	E5	E5	E5	E5	1	0	0	0	0	0	0	0	(80)

Where:

M = mono
St = stereo
DS = dual sound
R = right
L = left
L* = (L + R)/2
A = sound A
B = sound B

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage*	$V_P = V_{15-16}$	–	–	13.2	V
Output current					
pins 11, 12, 13, 14	I_O	–	–	10	mA
pins 1 and 19 (sink)	I_O	–	–	7	mA
(source)	$-I_O$	–	–	3	mA
Input voltage (not pin 18)	V_I	0	–	V_P	V
Input voltage pin 18	$V_I = V_{18-16}$	–	–	7	V
Output voltage	V_O	0	–	V_P	V
Total power dissipation	P_{tot}	–	–	1	W
ESD protection (each pin) (0 Ω/200 pF)	V_{es}	500	–	–	V
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Storage temperature range	T_{stg}	–40	–	+ 150	°C

DEVELOPMENT DATA

* Supply voltage may be applied only when both pins 5 and 15 are connected to ground.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C. Measurement conditions (see Fig.7): reference level is 1 V (RMS); test frequency = 3.183 kHz; noise measurement in accordance with DIN 45405, CCIR 468-3; oscillator frequency = 10 MHz; pre-emphasis time constant = 50 μs.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage		$V_P = V_{15-16}$	10.8	12	13.2	V
Supply current		$I_P = I_{15}$	–	10	–	mA
DC levels						
pins 6 - 14 and 17		V_{n-16}	–	3.25	–	V
pin 4		V_{4-5}	–	2	–	V
Bus transceiver						
Clock frequency (I^2C-bus)	note 1	f_{CLK}	0.7	–	100	kHz
Clock SCL (pin 3)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Timing LOW period		t_{LOW}	4.7	–	–	μs
Timing HIGH period		t_{HIGH}	4	–	–	μs
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Data SDA (pin 2)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	0.25	–	–	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Output current LOW		I_{OL}	3	–	–	mA
MAD (pin 20)						
Input voltage LOW		V_{20-5}	–	–	2.0	V
Input voltage HIGH		V_{20-5}	3.0	–	–	V

parameter	conditions	symbol	min.	typ.	max.	unit
Mute port (pin 18)						
Input voltage LOW	note 2	V_{IL}	−0.3	–	1.5	V
Input voltage HIGH	note 2	V_{IH}	3	–	5	V
Control ports (pins 1 and 19)						
Output voltage LOW	note 3	V_{OL}	–	–	0.5	V
Output voltage HIGH	note 3	V_{OH}	4.5	–	5	V
Output impedance	3-state	Z_o	1	–	–	MΩ
Output current LOW		I_{OL}	1	–	–	mA
Output current HIGH		$-I_{OH}$	1	–	–	mA
AF stages and identification (pins 7 to 14)						
Input impedance (pins 7 to 10)		Z_i	150	200	–	kΩ
Input voltage E1		V_I	–	–	0.7	V
Input voltage E2		V_I	–	–	1	V
Input voltage E2 for identification active (RMS value)	note 4	V_i	2.5	–	–	mV
Voltage gain 7-15/output	note 5	G_v	5.9	6	6.1	dB
Voltage gain 8-15/output	note 5	G_v	8.9	9	9.1	dB
Voltage gain 6, 9, 10-15/output		G_v	−0.1	0	0.1	dB
Crosstalk attenuation	notes 6 to 8					
dual mode		α_{ds}	70	75	–	dB
stereo mode		α_s	30	50	–	dB

DEVELOPMENT DATA

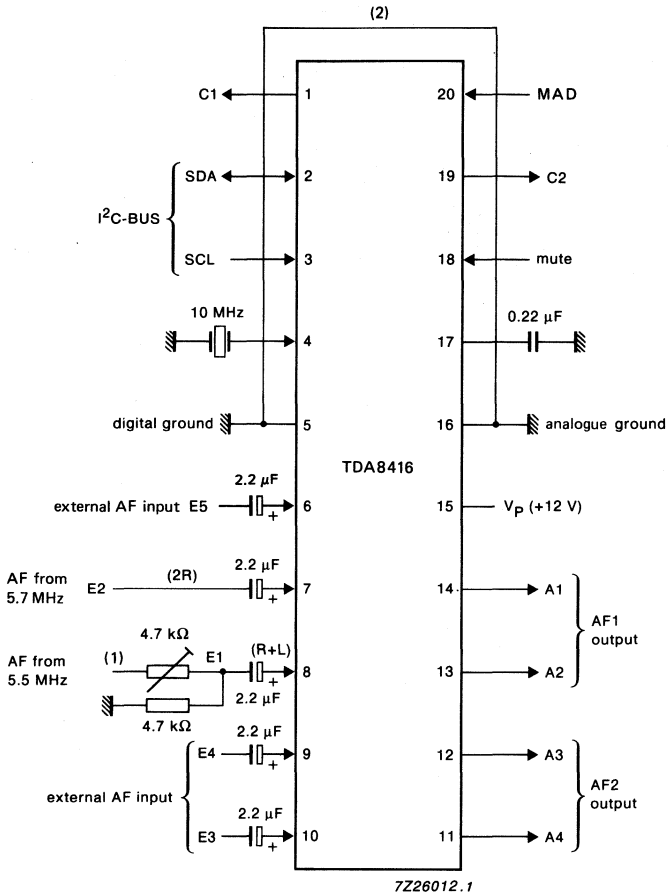
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AF stages and identification (continued)						
Output impedance (pins 11 to 14)		Z_o	400	500	600	Ω
De-emphasis time constant	note 9		49.5	50	50.5	μs
Frequency response	note 6	Δf	−1	–	1	dB
Total harmonic distortion	note 10	THD	–	–	0.2	%
Capacitive load (pins 11 to 14)		C_L	–	–	1.5	nF
Output signal (RMS value) (pins 11 to 14)	THD ⩽ 0.2%	V_o	–	–	2	V
Ripple rejection	note 11	RR	50	66	–	dB
Noise from I^2C-bus		NR	–	–	−80	dB
Signal-to-noise ratio		(S+W)/W	70	–	–	dBV CCIR
Signal suppression during mute	note 6	SS	70	75	–	dB
Change of output DC voltage level between any two modes			–	–	30	mV
Oscillator						
Oscillator frequency		f_{OSC}	–	10	–	MHz
External oscillator signal (RMS value)		V_{4-5}	1.7	–	–	V
Quartz series resistor		R1	–	–	100	Ω
Impedance		Z_i	–	−1.2 + j9.3	–	kΩ
Capacitance		C_{OSC}	–	1.7	–	pF

Notes to the characteristics

1. Full specification of I²C-bus will be supplied on request.
2. Programmable mute state. If the CR3 bit of the mute and port control register is LOW, the mute is active LOW; if it is HIGH, the mute input is active HIGH.
3. Output current $I_O \approx 1$ mA.
4. Unmodulated.
5. f = 400 Hz; R_L = 1 MΩ.
6. 40 Hz $\leqslant$ f $\leqslant$ 15 kHz.
7. In dual mode: A(B)-signal into B(A)-channel.
   In stereo mode: R-signal into left, L-signal = 0, reference is 1 V RMS.
8. Source impedance $|Z_S| < 1$ kΩ.
9. Equivalent to an output level of −3 dB at f = 3.183 kHz.
10. V_O = 1 V RMS; f = 1 kHz.
11. Test circuit see Fig.7.

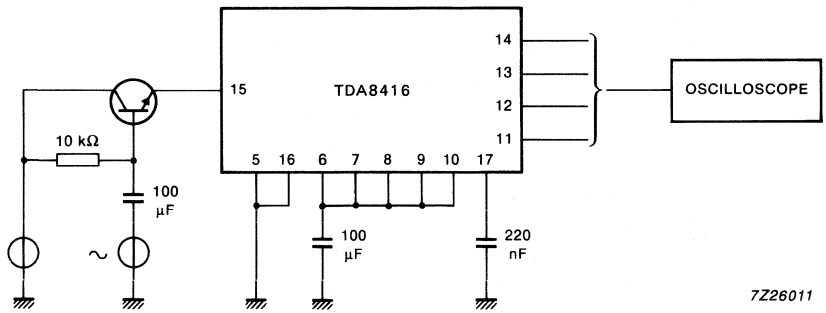
DEVELOPMENT DATA



(1) This potentiometer has to be adjusted to achieve the best stereo separation.

(2) Direct connection between pins 5 and 16 is needed.

Fig.7 Application and test circuit.



Voltage input = supply voltage + pulse voltage at 70 Hz = 12 V ± 50 mV (p-p).

Fig.8 Ripple rejection test circuit.

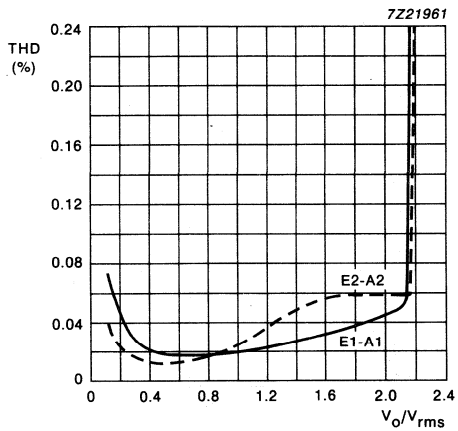


Fig.9 Total harmonic distortion diagram (stereo mode).

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH INTEGRATED FILTERS AND I²C-BUS CONTROL

GENERAL DESCRIPTION

The TDA8417 is a processor of stereo/dual language signals (B/G-standard) for stereo sound television receivers and VTRs, using the switched-capacitor technique. The AF signals at the TDA8417 inputs must be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The carrier frequency of the second channel is also modulated by an identification signal (stereo or dual sound). The device is controlled by a microcomputer via the two-line, bidirectional I²C-bus.

Features

- Use of the switched-capacitor technique for signal processing
- Small amount of peripheral components
- Integrated anti-aliasing filters
- Low distortion AF signal handling
- Integrated de-emphasis with a time constant of 50 μs
- Two general purpose output ports
- Full ESD protection

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage (pin 15)		V_P	–	12	–	V
Supply current (pin 15)		I_P	–	10	–	mA
AF output signal (RMS value) (pins 11 to 14)		V_o	–	2	–	V
Weighted signal-to-noise ratio of the AF output signals (CCIR 468/3)		(S+W)/W	70	–	–	dB
Crosstalk attenuation						
stereo mode at	f = 1 kHz	α_S	40	–	–	dB
dual sound mode at	f = 40 Hz to 12.5 kHz	α_{DS}	70	–	–	dB
Pilot signal input sensitivity		V_i	–	2.5	–	mV
Total harmonic distortion		THD	–	0.1	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

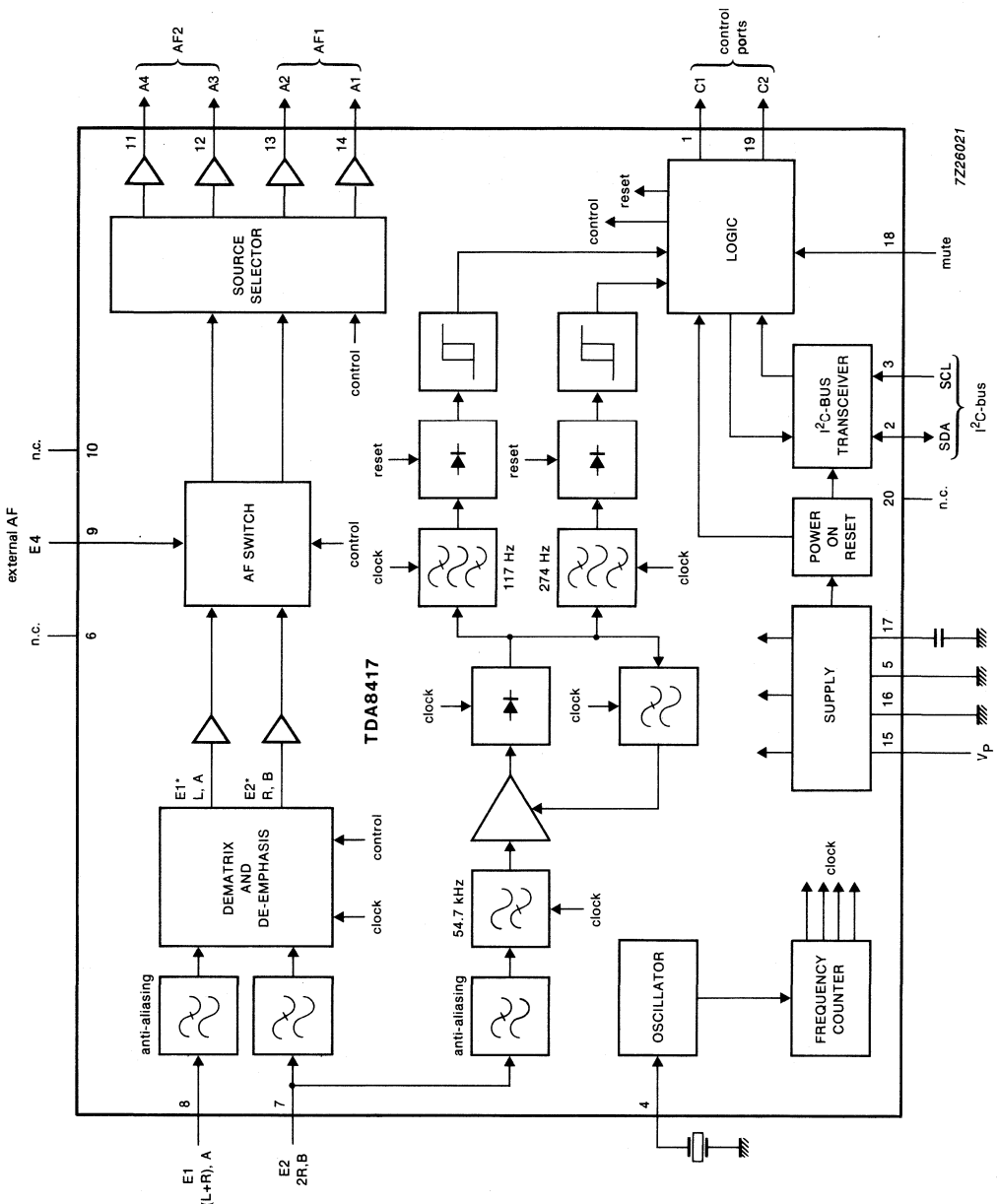


Fig.1 Block diagram.

DEVELOPMENT DATA

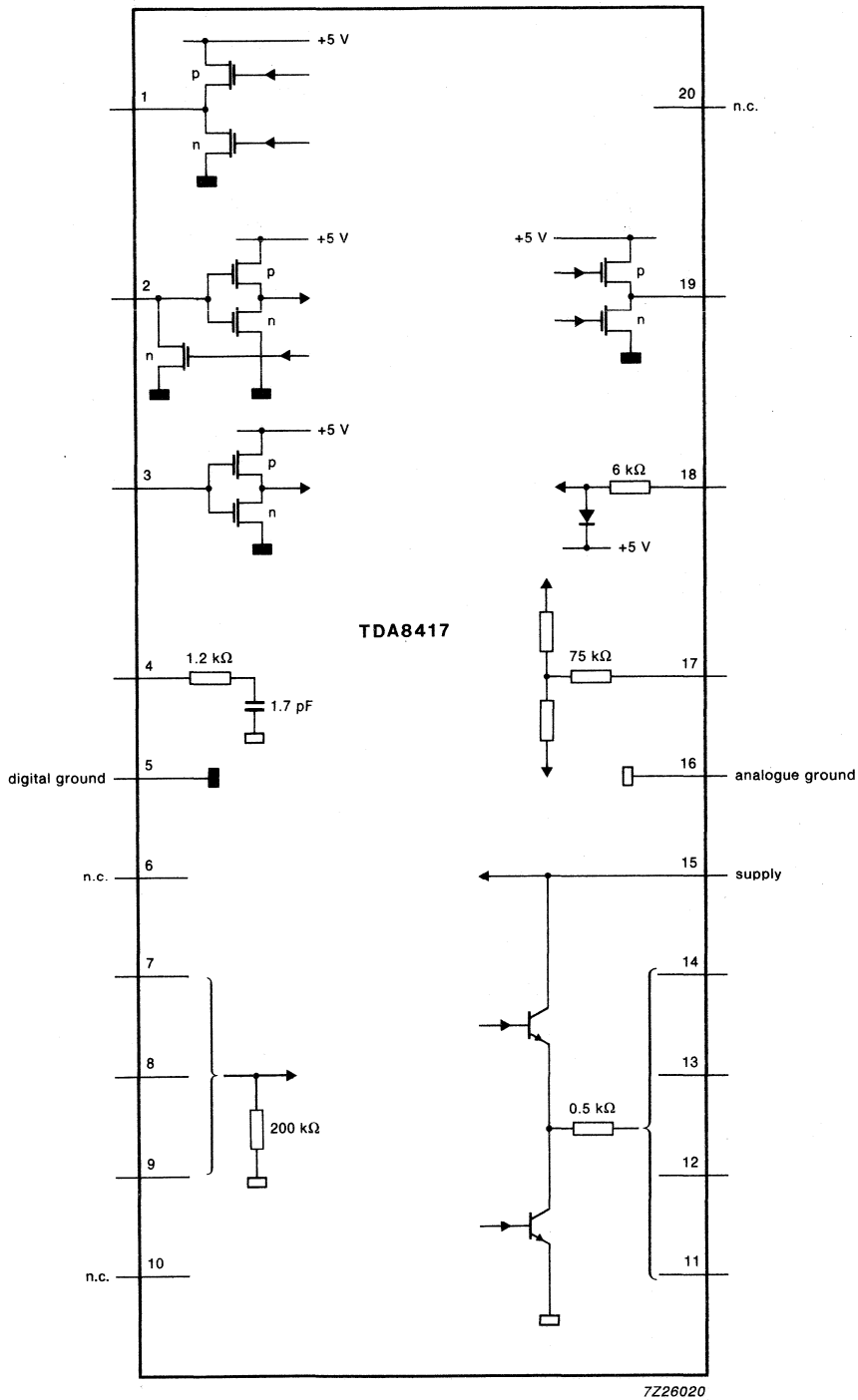


Fig.2 Input and output loading diagram.

PINNING

1	Control port C1	11	Output A4 AF 2 output
2	SDA, serial data line (I^2C-bus)	12	Output A3 AF 2 output
3	SCL, serial clock line (I^2C-bus)	13	Output A2 AF 1 output
4	Oscillator input (or quartz)	13	Output A1 AF 1 output
5	Digital ground (0 V)	15	Supply voltage V_P
6	Not connected, but reserved	16	Analogue ground (0 V)
7	Sound channel input AF2 (E2)	17	Ripple rejection improvement
8	Sound channel input AF1 (E1)	18	Mute input
9	External AF input (E4)	19	Control port C2
10	Not connected, but reserved	20	Not connected, but reserved

FUNCTIONAL DESCRIPTION

Anti-aliasing filters

Frequency band limitation is performed by a second order Sallen and Key low-pass filter inserted in the AF signal path and the identification circuit. This limitation is necessary because of the time-discrete signal processing needed to meet the Nyquist criterium.

Identification

To enable the identification of the transmitted AF signal (mono, stereo or dual sound), the carrier frequency of the second channel (E2) is also modulated by an identification signal. The identification signal is a 54.6875 kHz pilot carrier signal which is 50% amplitude modulated by either a 117.4 Hz signal for stereo transmission or by a 274.1 Hz signal for dual sound transmission.

The identification section of the circuit consists of a 54 kHz high-pass filter followed by a gain controlled amplifier with an AM demodulator. The total gain of the high-pass filter and the amplifier is approximately 56 dB. The demodulated identification signal is filtered by the identification band-pass filters, (117.4 Hz for stereo transmission, 274.1 Hz for dual sound transmission). The output from either filter is converted to a DC signal by a peak detector and the necessary hysteresis is performed by a Schmitt-trigger. The resultant DC output signals indicate the status of the transmitter (mono, stereo or dual sound).

De-matrix and de-emphasis

Depending on the results of the identification circuit (mono, stereo or dual sound) the AF signals at the inputs E1 and E2 are converted to the signals at E1* and E2* as listed in Table 1.

Table 1 Transmitter status

transmitter status	E1	E2	E1*	E2*
mono	0.7(L+R)	–	2(L+R)	–
stereo	0.7(L+R)	2R	4L	4R
dual sound	0.7A	B	2A	2B

Where:

L = left channel signal
R = right channel signal
A = first sound channel signal
B = second sound channel signal

This section of the circuit also performs the de-emphasis (50 μs time constant) with a high degree of accuracy.

AF switch

The AF switch is used to switch to either the internal sound sources (E1* or E1* and E2*) or, to the external sound source (E3 and E4) and is controlled via the I²C-bus.

Source selector

The source selector is used to connect the outputs from the AF switch to the outputs A1 to A4 as illustrated by Table 5. The selector is controlled via the I²C-bus.

Muting

In this mode the AF outputs A1 to A4 are muted, and the identification circuit is deactivated (mono). The muting is active after power-on reset or as a result of user control (via the mute input and bit CR3 of the control byte of the mute and port control register; see Table 4).

Sound mute

If the switch register is set to (00) hex, (sound mute) only the AF outputs are muted, the identification circuit is still active and can be read (status register) via the I²C-bus.

Power-on reset

The following actions are carried out by the internal power-on reset when it is active:

- The AF outputs are muted
- The identification circuit is deactivated (mono)
- The control ports (C1 and C2) are set LOW
- The I²C-bus transceiver is initialized

When the power-on reset becomes passive the following occurs:

- The AF outputs are kept in the mute state until the contents of the switch register are changed from (00) hex via the I²C-bus
- The identification circuit is activated
- The control ports are LOW until the mute and control port register is changed (CR bits 10, 11, 20 and 21)
- The I²C-bus transceiver is activated

FUNCTIONAL DESCRIPTION (continued)

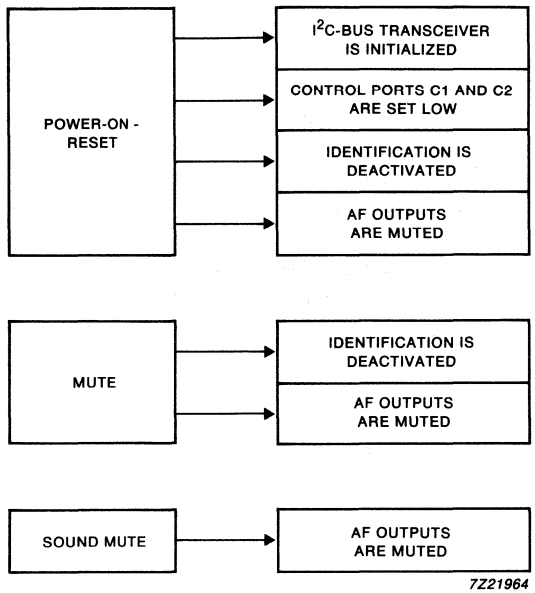


Fig.3 Mute modes.

Control ports

The general purpose control ports C1 and C2 can be set to LOW, HIGH or high impedance via the I²C-bus.

I²C-bus receiver and data handling

Bus specification

The TDA8417 is controlled, via the bidirectional 2-line I²C-bus, by a microcomputer. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

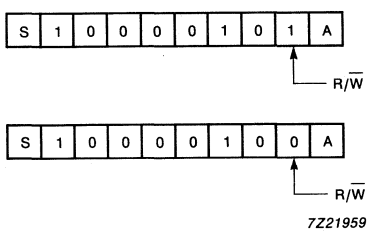
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in the CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as the stop condition (P). The bus receiver will be reset on the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

The I²C-BUS PROTOCOL OF THE TDA8417

The TDA8417 is controlled by a microcomputer and can be written to or read from via the I²C-bus.

The first byte is the address and determines whether the TDA8417 is to be read from (status register) or written to (switch register or mute and port control register).



Read from (TDA8417 is a slave transmitter)

Write to (TDA8417 is a slave receiver)

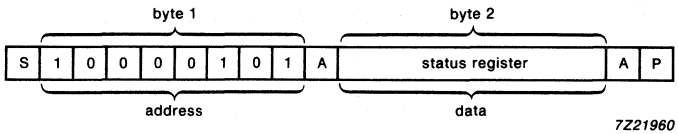
Where:

S = start bit
A = acknowledge bit

Fig.4 Address byte.

Reading the TDA8417

Reading the TDA8417 means reading the status register and the data stream will have the format as illustrated in Fig.5 below.



Where:

S = start bit
A = acknowledge bit
P = stop bit

Fig.5 Read format.

The second byte, the contents of the status register, is defined by Table 2.

Table 2 Status register

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	ST	DS	0	0	0	0	0

Where:

PONRES = power on reset
1 = power on reset active after switching on or power breakdown
0 = after reading the status register
ST = stereo transmission
DS = dual sound transmission

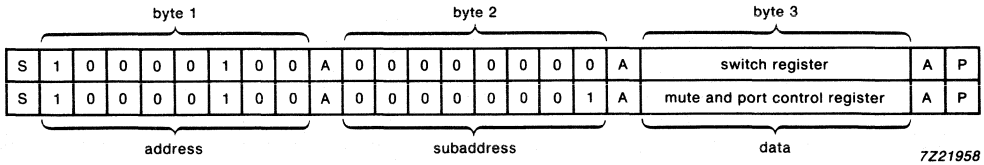
The truth table for the ST and DS bits is provided by Table 3.

Table 3 Truth table for ST and DS bits

ST	DS	definition
0	0	mono transmission
0	1	dual sound transmission
1	0	stereo transmission

Writing to the TDA8417

Writing to the TDA8417 means, writing to either the switch register or the mute and port control register. Which one is to be addressed is defined by the subaddress (the second byte) as illustrated by Fig.6 below. The third byte contains the information to be stored in the specified register.



Where:

S = start bit
A = acknowledge bit
P = stop bit

Fig.6 Write format.

Table 4 defines the contents of the mute and port control register.

Table 4 Mute and port control register

D7	D6	D5	D4 CR3	D3 CR21	D2 CR20	D1 CR11	D0 CR10	definition
X	X	X				0	0	control port C1 = LOW
X	X	X				0	1	control port C1 = HIGH
X	X	X				1	X	control port C1 = high impedance
X	X	X		0	0			control port C2 = LOW
X	X	X		0	1			control port C2 = HIGH
X	X	X		1	X			control port C2 = high impedance
X	X	X	0					mute is active when pin 18 is LOW (default)
X	X	X	1					mute is active when pin 18 is HIGH

Where:

X = don't care

DEVELOPMENT DATA

Table 5 defines the contents of the switch register.

Table 5 Switch register

switch register		input E1	E2	E4	output A1	A2	A3	A4	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
sound mute	–	–	–	–	no signal				0	0	0	0	0	0	0	0	(00)
mono	M	M	M	–	M	M	M	M	0	0	0	1	0	0	0	0	(10)
	St	L*	R	–	L*	L*	L*	L*	0	0	0	1	0	0	0	0	(10)
stereo	St	L*	R	–	L	R	L	R	0	0	1	0	1	0	1	0	(2A)
sound A	DS	A	B	–	A	A	A	A	0	0	0	1	0	0	0	0	(10)
sound B	DS	A	B	–	B	B	B	B	0	0	0	1	1	1	1	1	(1F)
dual sound	DS	A	B	–	A	A	B	B	0	0	0	1	1	1	0	0	(1C)
	DS	A	B	–	B	B	A	A	0	0	0	1	0	0	1	1	(13)
dual sound	DS	A	B	–	A	B	A	A	0	0	0	1	0	0	1	0	(12)
mix	DS	A	B	–	A	A	A	B	0	0	0	1	1	0	0	0	(18)
	DS	A	B	–	A	B	A	B	0	0	0	1	1	0	1	0	(1A)
	DS	A	B	–	B	B	A	B	0	0	0	1	1	0	1	1	(1B)
	DS	A	B	–	A	B	B	B	0	0	0	1	1	1	1	0	(1E)
external	–	–	–	E4	E4	E4	E4	E4	0	1	1	1	1	1	1	1	(7F)

Where:

M = mono
St = stereo
DS = dual sound
R = right
L = left
L* = (L + R)/2
A = sound A
B = sound B

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage*	$V_P = V_{15-16}$	–	–	13.2	V
Output current					
pins 11, 12, 13, 14	I_O	–	–	10	mA
pins 1 and 19 (sink)	I_O	–	–	7	mA
(source)	$-I_O$	–	–	3	mA
Input voltage (not pin 18)	V_I	0	–	V_P	V
Input voltage pin 18	$V_I = V_{18-16}$	–	–	7	V
Output voltage	V_O	0	–	V_P	V
Total power dissipation	P_{tot}	–	–	1	W
ESD protection (each pin) (0 Ω/200 pF)	V_{es}	500	–	–	V
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Storage temperature range	T_{stg}	–40	–	+ 150	°C

DEVELOPMENT DATA

* Supply voltage may be applied only when both pins 5 and 15 are connected to ground.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C. Measurement conditions (see Fig.7): reference level is 1 V (RMS); test frequency = 3.183 kHz; noise measurement in accordance with DIN 45405, CCIR 468-3; oscillator frequency = 10 MHz; pre-emphasis time constant = 50 μs.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage		$V_P = V_{15-16}$	10.8	12	13.2	V
Supply current		$I_P = I_{15}$	–	10	–	mA
DC levels						
pins 7 - 14 and 17		V_{n-16}	–	3.25	–	V
pin 4		V_{4-5}	–	2	–	V
Bus transceiver						
Clock frequency (I^2C-bus)	note 1	f_{CLK}	0.7	–	100	kHz
Clock SCL (pin 3)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Timing LOW period		t_{LOW}	4.7	–	–	μs
Timing HIGH period		t_{HIGH}	4	–	–	μs
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Data SDA (pin 2)						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3	–	5	V
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	0.25	–	–	μs
Input current LOW		$-I_{IL}$	–	–	10	μA
Input current HIGH		I_{IH}	–	–	10	μA
Output current LOW		I_{OL}	3	–	–	mA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Mute port (pin 18)						
Input voltage LOW	note 2	V_{IL}	−0.3	–	1.5	V
Input voltage HIGH	note 2	V_{IH}	3	–	5	V
Control ports (pins 1 and 19)						
Output voltage LOW	note 3	V_{OL}	–	–	0.5	V
Output voltage HIGH	note 3	V_{OH}	4.5	–	5	V
Output impedance	3-state	Z_o	1	–	–	MΩ
Output current LOW		I_{OL}	1	–	–	mA
Output current HIGH		$-I_{OH}$	1	–	–	mA
AF stages and identification (pins 7 to 14)						
Input impedance (pins 7 to 9)		Z_i	150	200	–	kΩ
Input voltage E1		V_I	–	–	0.7	V
Input voltage E2		V_I	–	–	1	V
Input voltage E2 for identification active (RMS value)	note 4	V_i	2.5	–	–	mV
Voltage gain 7-15/output	note 5	G_v	5.9	6	6.1	dB
Voltage gain 8-15/output	note 5	G_v	8.9	9	9.1	dB
Voltage gain 9-15/output		G_v	−0.1	0	0.1	dB
Crosstalk attenuation	notes 6 to 8					
dual mode		α_{ds}	70	75	–	dB
stereo mode		α_s	30	50	–	dB

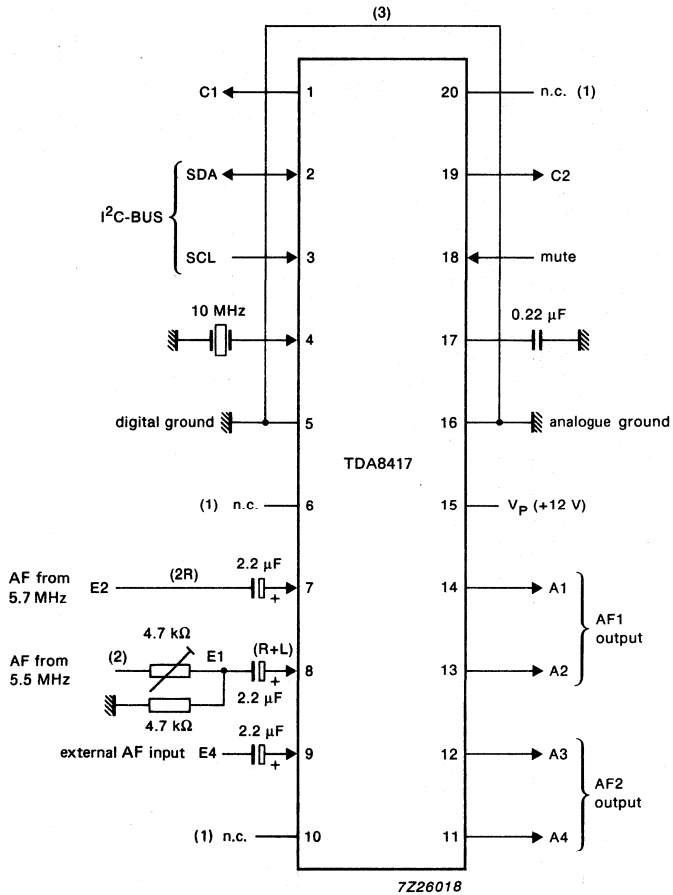
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AF stages and identification (continued)						
Output impedance (pins 11 to 14)		Z_o	400	500	600	Ω
De-emphasis time constant	note 9		49.5	50	50.5	μs
Frequency response	note 6	Δf	−1	–	1	dB
Total harmonic distortion	note 10	THD	–	–	0.2	%
Capacitive load (pins 11 to 14)		C_L	–	–	1.5	nF
Output signal (RMS value) (pins 11 to 14)	THD ⩽ 0.2%	V_o	–	–	2	V
Ripple rejection	note 11	RR	50	66	–	dB
Noise from I^2C-bus		NR	–	–	−80	dB
Signal-to-noise ratio		(S+W)/W	70	–	–	dBV CCIR
Signal suppression during mute	note 6	SS	70	75	–	dB
Change of output DC voltage level between any two modes			–	–	30	mV
Oscillator						
Oscillator frequency		f_{OSC}	–	10	–	MHz
External oscillator signal (RMS value)		V_{4-5}	1.7	–	–	V
Quartz series resistor		R1	–	–	100	Ω
Impedance		Z_i	–	−1.2 + j9.3	–	kΩ
Capacitance		C_{OSC}	–	1.7	–	pF

Notes to the characteristics

1. Full specification of I²C-bus will be supplied on request.
2. Programmable mute state. If the CR3 bit of the mute and port control register is LOW, the mute is active LOW; if it is HIGH, the mute input is active HIGH.
3. Output current $I_O \approx 1$ mA.
4. Unmodulated.
5. f = 400 Hz; R_L = 1 MΩ.
6. 40 Hz ⩽ f ⩽ 15 kHz.
7. In dual mode: A(B)-signal into B(A)-channel.
   In stereo mode: R-signal into left, L-signal = 0, reference is 1 V RMS.
8. Source impedance $|Z_S| < 1$ kΩ.
9. Equivalent to an output level of −3 dB at f = 3.183 kHz.
10. V_o = 1 V RMS; f = 1 kHz.
11. Test circuit see Fig.7.

DEVELOPMENT DATA

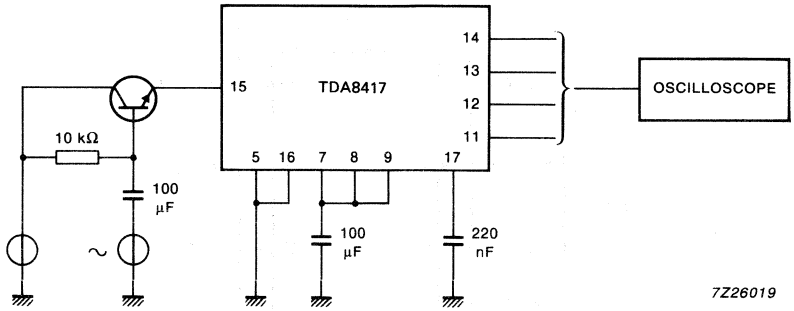


(1) These pins are not connected internally and should not be connected on the printed-circuit board in order to maintain compatibility with future devices.

(2) This potentiometer has to be adjusted to achieve the best stereo separation.

(3) Direct connection between pins 5 and 16 is needed.

Fig.7 Application and test circuit.



Voltage input = supply voltage + pulse voltage at 70 Hz = 12 V ± 50 mV (p-p).

Fig.8 Ripple rejection test circuit.

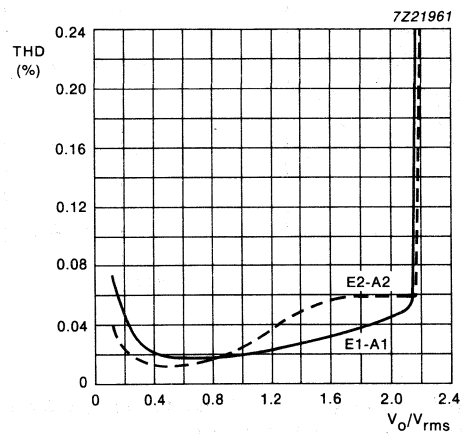


Fig.9 Total harmonic distortion diagram (stereo mode).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

HI-FI STEREO AUDIO PROCESSOR; I²C BUS

GENERAL DESCRIPTION

The TDA8421 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel (CH1) and a headphone channel (CH2), digital controlled via the I²C bus, for application in hi-fi audio and television sound.

Features

- Input selector
- Mode selector
- Loudspeaker channel (CH1) } with volume control, balance control and mute
- Headphone channel (CH2) }
- Pseudo stereo and spatial function
- Bass and treble control
- Electrostatic discharge protection diodes

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	200	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	90	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Channel separation	α	–	75	–	dB
Volume control range CH1	G	−62	–	16	dB
Treble control range	G	−12	–	12	dB
Bass control range	G	−12	–	15	dB
Volume control range CH2	G	−62	–	0	dB

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

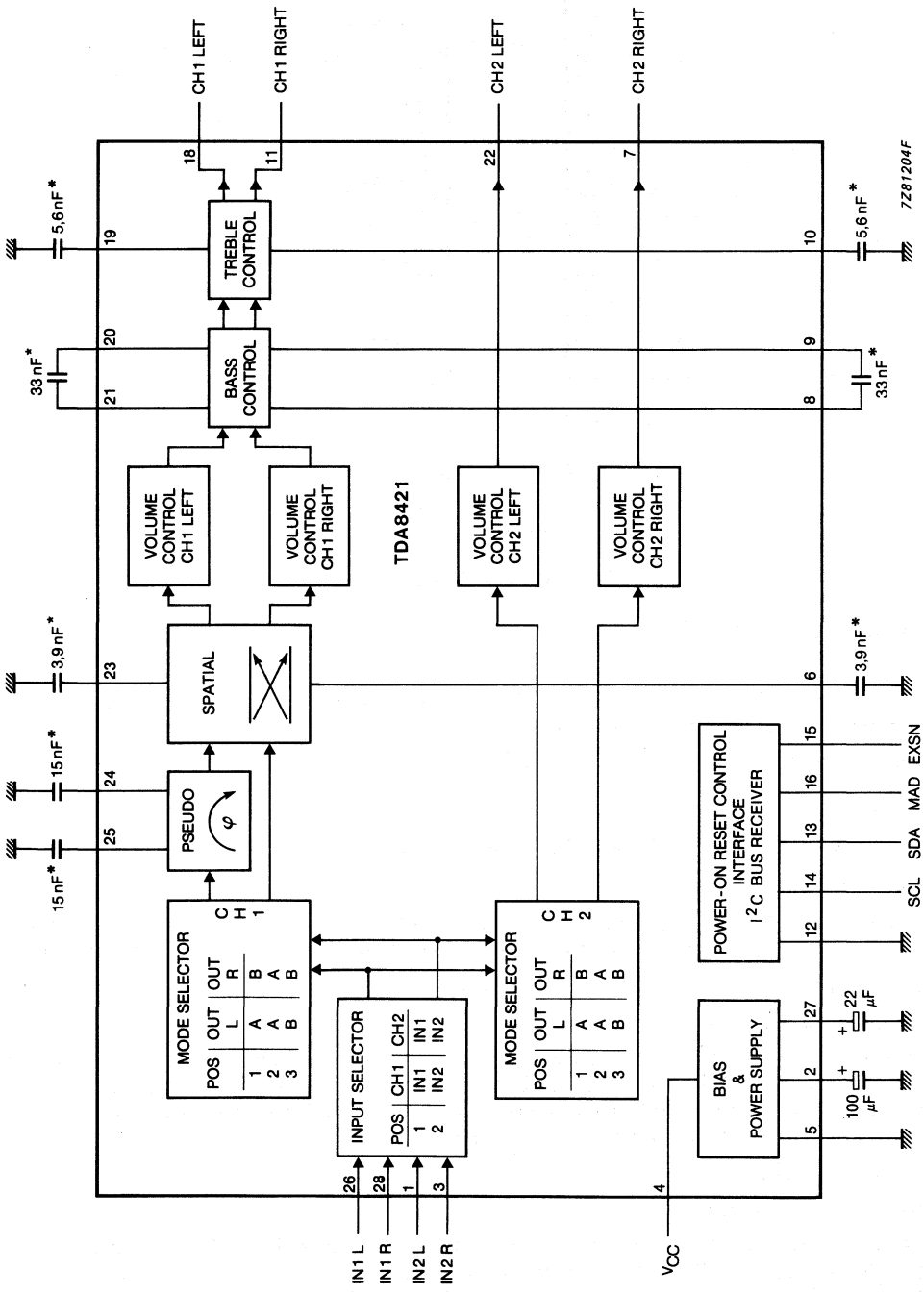


Fig. 1 Block diagram.

* These values are dependent on the required frequency response and effect.

PINNING

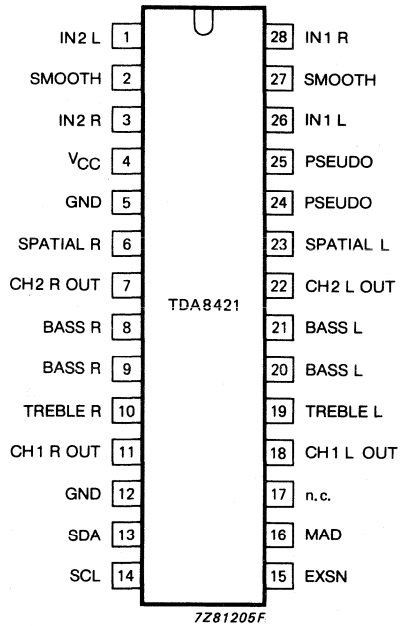


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the input selector. The selection is made from the following AF input signals:

- IN1 L (pin 26); IN1 R (pin 28)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Where IN1 is an internal input signal and IN2 an external input signal.

Mode selector

For each channel (CH1 and CH2) there is a mode selector which selects between stereo, sound A and sound B in the event of bilingual transmission. Both mode selectors can be controlled independently.

Headphone channel (CH2)

Volume control and balance

The stages for volume control for CH2 consist of two parts for left and right. In each part the gain can be adjusted between 0 and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Loudspeaker channel (CH1)

Volume control and balance

The loudspeaker channel (CH1) also consists of two parts for volume control (left and right). In each part the gain can be adjusted between + 16 dB and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Stereo/pseudo stereo/spatial stereo mode

It is possible to select three modes. Stereo, pseudo or spatial stereo. The pseudo stereo mode receives mono transmissions and the stereo and spatial stereo mode receives stereo transmissions.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8421 includes a bias and power supply stage, which generates a voltage of ½ V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both the loudspeaker channel (CH1) and the headphone channel (CH2). The muting can be switched by transmission of the mute bit.

I^2C bus receiver and data handling

Bus specification

The TDA8421 is controlled via the 2-wire I^2C bus by a microcomputer. The two wires (SDA — serial data, SCL — serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8421 starts with the module address MAD.

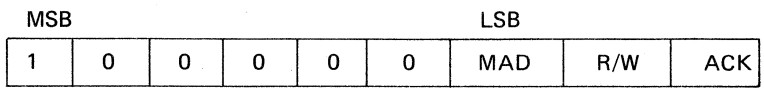


Fig. 3 TDA8421 module address.

The module address is determined by pin 16. When connected to ground MAD = 0; when connected to V_{CC} MAD = 1. Thus two TDA8421s can be selected within a system.

Subaddress

After the module address byte a second byte is used to select the functions for both channels:

- CH1 – Volume left, volume right, bass, treble and switch functions
- CH2 – Volume left, volume right and switch functions

The subaddress SAD is stored within the TDA8421. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

		128	64	32	16	8	4	2	1
	function	MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	0	0	0	0	0	0	0	0
	volume right	0	0	0	0	0	0	0	1
	bass	0	0	0	0	0	0	1	0
	treble	0	0	0	0	0	0	1	1
	switch functions	0	0	0	0	1	0	0	0
CH2	volume left	0	0	0	0	0	1	0	0
	volume right	0	0	0	0	0	1	0	1
	switch functions	0	0	0	0	1	1	0	0
						subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8421. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

	function		MSB 7	6	5	4	3	2	1	LSB 0
	volume left	VL1	1	1	V05	V04	V03	V02	V01	V00
	volume right	VR1	1	1	V15	V14	V13	V12	V11	V10
CH1	bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
	treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
	switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS
	volume left	VL2	1	1	V25	V24	V23	V22	V21	V20
CH2	volume right	VR2	1	1	V35	V34	V33	V32	V31	V30
	switch functions	S2	1	1	1	1	EXS	MH1	MH0	1

Truth tables

Truth tables for the switch functions

Table 3 Input selector

function	IS
IN1	0
IN2	1

Table 4 Mode selectors

	CH1		CH2	
mode	ML0	ML1	MH0	MH1
stereo	1	1	1	1
sound A	1	0	1	0
sound B	0	1	0	1
----------	0	0	0	0

Table 5 Stereo/pseudo stereo/spatial stereo

choice	STL	EFL
spatial	1	1
stereo	1	0
pseudo	0	1
----------	0	0

Table 6 Mute

mute	MU
active; automatic after POR*	1
not active	0

Where: POR = Power-On Reset.

Table 7 Output for external switch

EXSN	EXS
ground	1
open collector	0

Truth tables for the volume base and treble controls.

Table 8 Volume control

CH1	CH2	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
16	0	1	1	1	1	1	1
14	−2	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
−46	−62	1	0	0	0	0	0
−48	⩽−90	0	1	1	1	1	1
.	.	.	.	.	.	.	.
−62	⩽−90	0	1	1	0	0	0
⩽−90	⩽−90	0	1	0	1	1	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
⩽−90	⩽−90	0	0	0	0	0	0

Where: The values of CH1 and CH2 are in 2 dB/step measured in dBs.

* Attenuation ⩾ 90 dB

Table 9 Bass control

3dB/step (dB)	BA3	BA2	BA1	BA0
15	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
15	1	0	1	1
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Table 10 Treble control

3dB/step (dB)	TR3	TR2	TR1	TR0
12	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all eight functions have to be adjusted with eight data transmissions. It is recommended that data information for switch functions in CH1 are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 5. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

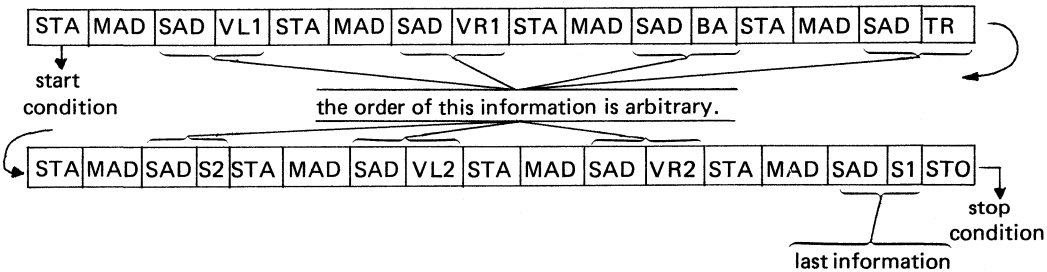


Fig. 4 Data transmission after a power-on reset.

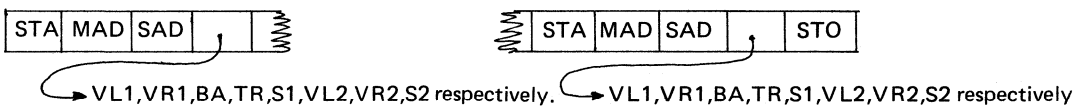


Fig. 5 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range at pins for external capacitors				
pins 2, 6, 8 to 10, 19 to 21, 23 to 25, 27	V_{cap}	0	V_{CC}	V
pin 13	V_{SDA}	0	V_{CC}	V
pin 14	V_{SCL}	0	V_{CC}	V
pin 15	V_{EXSN}	0	V_{CC}	V
pin 16	V_{MAD}	0	V_{CC}	V
Voltage range at pins 1, 3, 7, 11, 18, 22, 26, 28	V_I, V_O	0	V_{CC}	V
Output current at pins 7, 11, 18, 22	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70$ °C	P_{tot}	–	1350	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	–25	150	°C
Electrostatic handling *	$\pm V_{ESD}$	–	2000	V

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ resistor.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Supply current at V_{CC} = 12 V	I_{CC}	–	42	55	mA
Internal input voltage IN1 L,R (pins 26,28) IN2 L,R (pins 1,3) DC voltage internally generated; capacitive coupling recommended	V_I	5,4	6,0	6,6	V
MAD (pin 16)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	0	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
SDA; SCL (pins 13 and 14)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
Output voltage at CH1 (pins 11 and 18); CH2 (pins 7 and 22)	V_O	5,4	½ V_{CC}	6,6	V
pins with external capacitors					
pins 6 to 10; 19 to 21; 23 to 25	$V_{cap.n}$	–	½ V_{CC}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0,1	–	V
External switch (pin 15) at I_{EXSN} = 1 mA					
Output voltage HIGH	V_{EXSNH}	–	–	16	V
Output voltage LOW	V_{EXSNL}	–	–	0,3	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 100\ pF$; T_{amb} = 25 °C unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 6)					
SDA, SCL (pin 13 and 14)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0,3	μs
Set-up time for start condition	$t_{SU;STA}$	4,7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Input signals					
IN1 L (pin 26) IN1 R (pin 28) IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (r.m.s. value) at V_u = –4 dB; THD ≤ 0,5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_{n-5}	35	50	–	kΩ
Frequency response (–0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
LOUDSPEAKER CHANNEL OUTPUTS					
CH1 LEFT (pin 18); CH1 RIGHT (pin 11)					
Output voltage range (r.m.s. value) at THD $\leqslant$ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level weighted according to CCIR468-2					
gain = 16 dB	V_n	–	90	–	μV
gain = 0 dB	V_n	–	20	40	μV
gain = $\leqslant$ –90 dB	V_n	–	15	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz) for $V_{i(rms)}$ = 0,5 V; gain = + 16 dB to –30 dB	THD	–	0,05	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = + 2 dB to –30 dB	THD	–	0,07	0,2	%
for $V_{i(rms)}$ = 2,0 V; gain = –4 dB to –30 dB	THD	–	0,1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
VOLUME CONTROL					
For truth table see Table 8					

parameter	symbol	min.	typ.	max.	unit
Loudspeaker channel (CH1)					
Control range at f = 1 kHz					
maximum voltage gain (16 dB step)	G_{max}	15	–	–	dB
minimum voltage gain (–62 dB step)	G_{min}	–60	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 16 dB to –30 dB	ΔG	–	–	0,5	dB
gain from –30 dB to –62 dB	ΔG	–	–	1	dB
TREBLE CONTROL (CH1)					
For truth table see Table 10					
Control range for C_{10-5}; C_{19-5} = 5,6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
BASS CONTROL					
For truth table see Table 9					
Control range for C_{8-9}; C_{20-21} = 33 nF					
Maximum emphasis at 40 kHz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial:					
Antiphase crosstalk	α	–	50	–	%
Pseudo:					
Phase shift (see Fig. 15)					

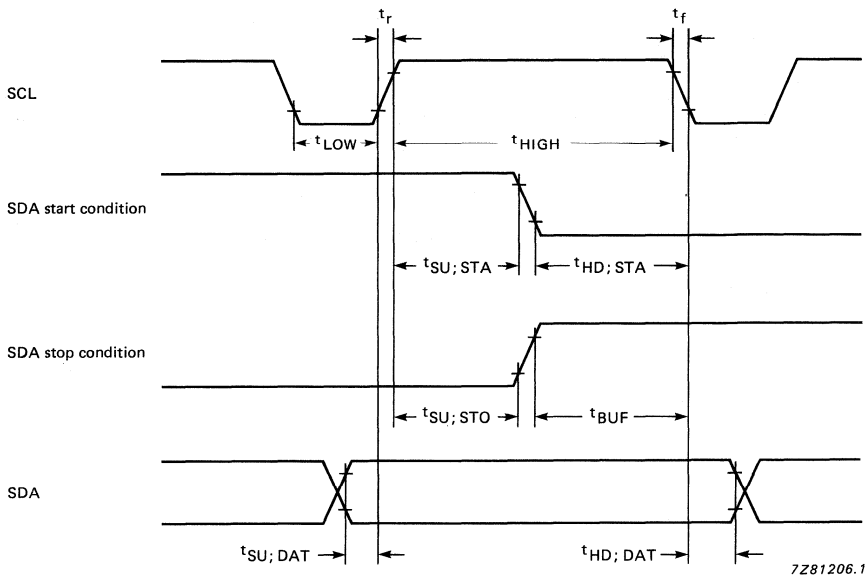
AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
HEADPHONE CHANNEL OUTPUTS					
CH2 LEFT (pin 22); CH2 RIGHT (pin 7)					
Output voltage range (r.m.s. value) at THD ⩽ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level (weighted according to CCIR468-2)					
gain = 0 dB	V_n	–	15	–	μV
gain = 16 dB	V_n	–	12	25	μV
gain = ⩽ –90 dB	V_n	–	10	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz) for $V_{i(rms)}$ = 0,2 V; gain = 0 dB to –30 dB	THD	–	0,01	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = 0 dB to –30 dB	THD	–	0,1	–	%
for $V_{i(rms)}$ = 2,0 V gain = –4 dB to –30 dB	THD	–	0,3	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
Crosstalk between any input/output f = 100 Hz to 12,5 kHz	α	65	70	–	dB
Crosstalk IN1/IN2 gain = 0 dB; R_G = 0	α	95	100	–	dB

parameter	symbol	min.	typ.	max.	unit
Headphone channel (CH2)					
Control range					
maximum voltage gain (0 dB step)	G_{max}	−1	–	–	dB
minimum voltage gain (−62 dB step)	G_{min}	−57	–	–	dB
last position	G_{off}	−80	−85	–	dB
mute position	G_{mute}	−85	−90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 0 dB to −40 dB	ΔG	–	–	0,5	dB
gain from −40 dB to −62 dB	ΔG	–	–	2	dB

Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels.



$t_{SU;STA}$ = start code set-up time
$t_{HD;STA}$ = start code hold time
$t_{SU;STO}$ = stop code set-up time
t_{BUF} = BUS free time
$t_{SU;DAT}$ = data set-up time
$t_{HD;DAT}$ = DATA hold time

Fig. 6 Timing requirements for I²C bus.

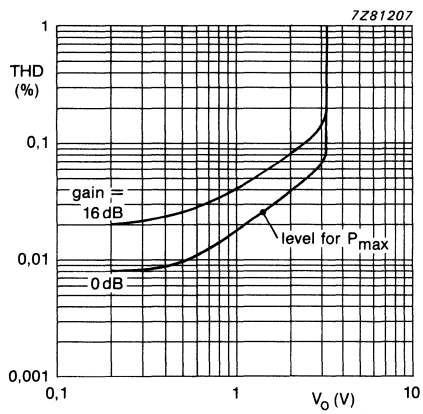


Fig. 7 Distortion loudspeaker channel CH1 as a function of the output voltage with gain as parameter.

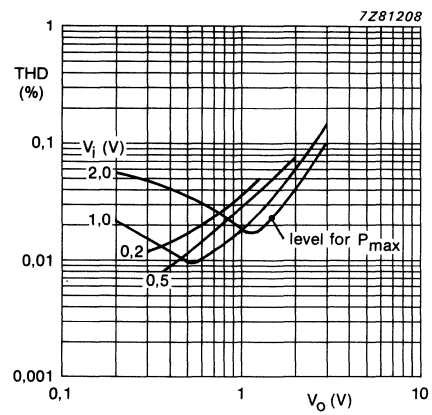


Fig. 8 Distortion loudspeaker channel CH1 as a function of the output voltage with input voltage as parameter.

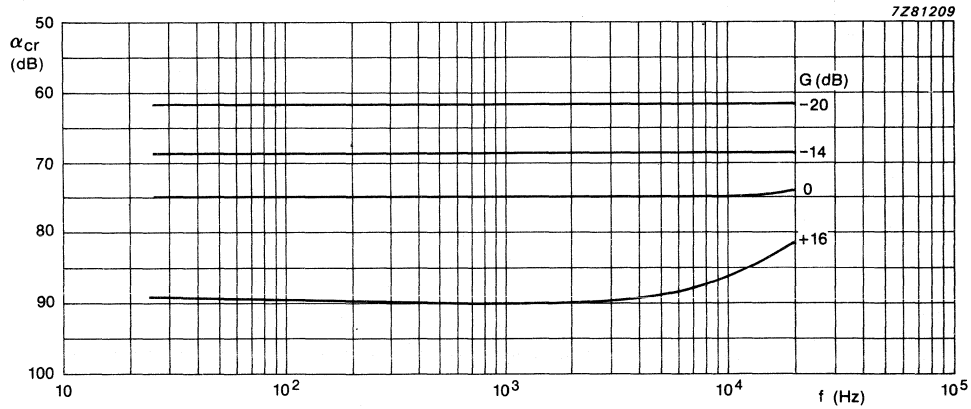


Fig. 9 Channel separation loudspeaker channel CH1 as a function of frequency.

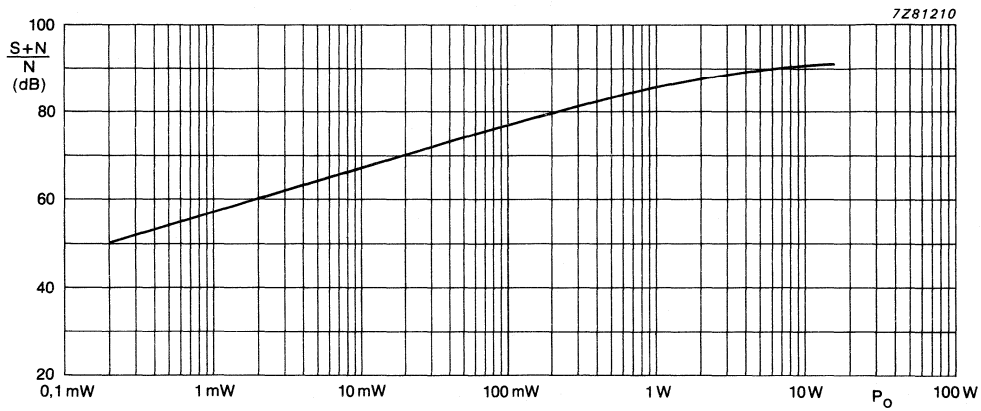


Fig. 10 Signal-to-noise ratio as a function of output power.
Input voltage V_i = 0,5 V; according to CCIR; quasi peak; P_o = 15 W.

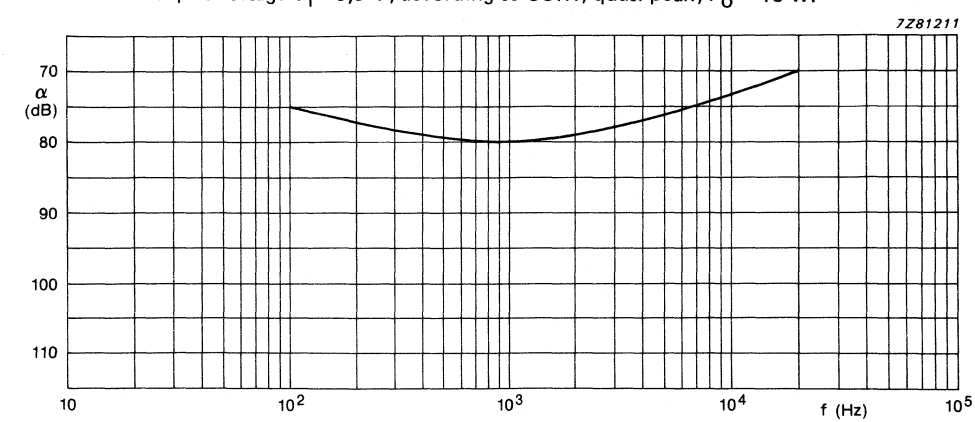


Fig. 11 Crosstalk 2-tone mode as a function of frequency.
CH1: mode AA, Gain + 16 dB; CH2: mode BB, Gain 0 dB. Signal input RIGHT; input LEFT to ground, measured at output CH1.

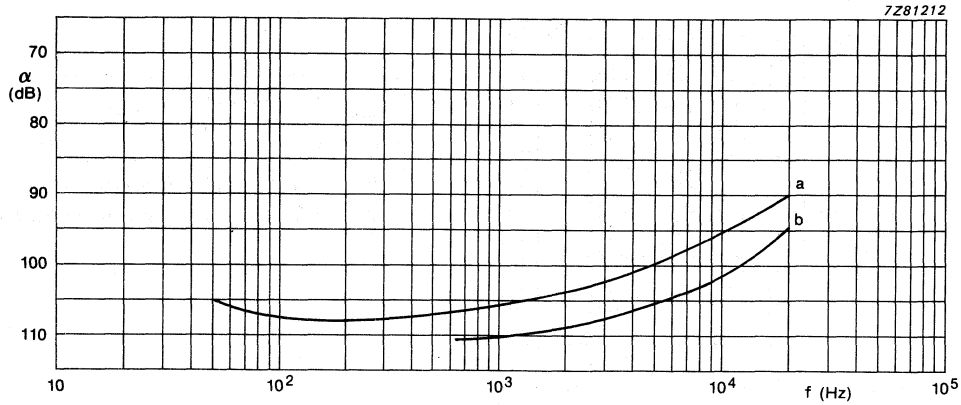


Fig. 12 Crosstalk between IN1 and IN2 as a function of frequency; measured at output CH1, $R_G = 0$.
a) Gain = + 16 dB; V_i = 200 mV. b) Gain = 0 dB; V_i = 1 V.

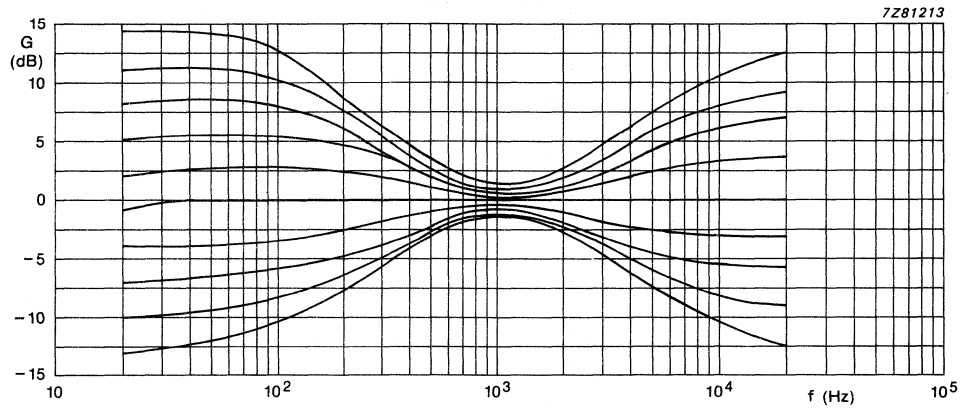


Fig. 13 Bass and treble tone control. C_{bass} = 33 nF, C_{treble} = 5,6 nF.

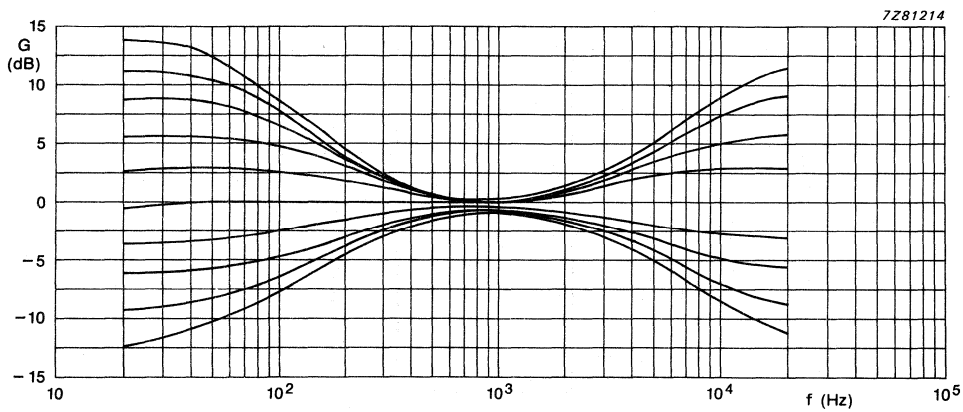
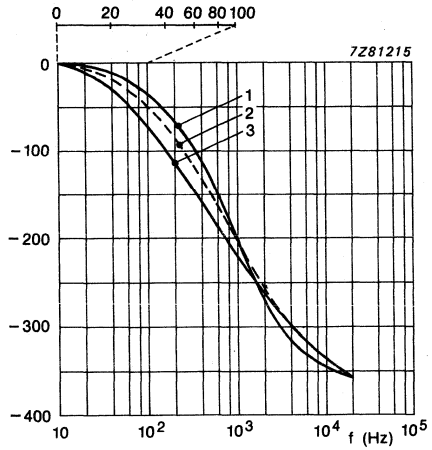


Fig. 14 Bass and treble tone control. C_{bass} = 68 nF, C_{treble} = 3,9 nF.



curve	pin 24 (nF)	pin .. (nF)	effect
1	15	15	normal
2	5,6	47	intensified
3	5,6	68	more intensified

Fig. 15 Pseudo (phase) as a function of frequency CH1 left.

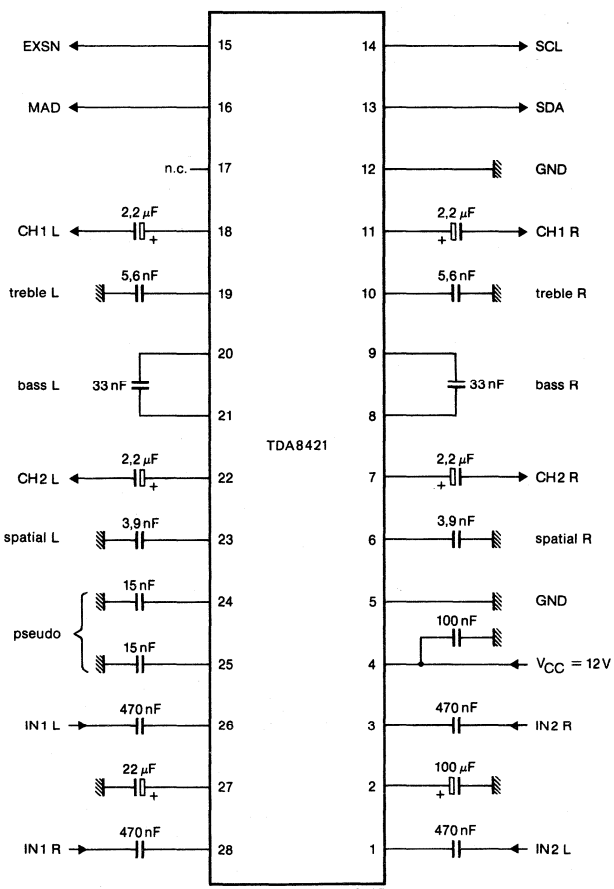
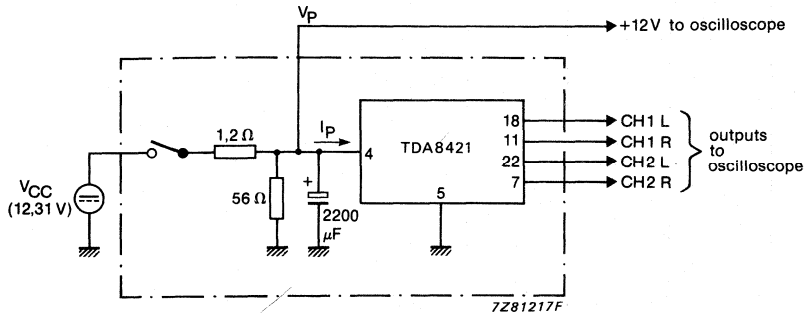


Fig. 16 Test and application circuit diagram.



I_{CC} = 45 mA;
I_{load} = 259 mA;
t_{on} = 2,64 ms;
t_{off} = 102 ms.

Fig. 17 Turn-on/off power supply circuit diagram.

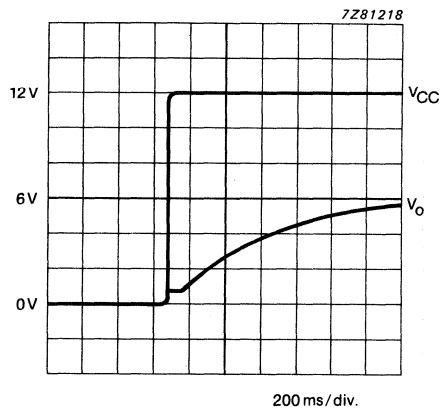


Fig. 18 Turn-on behaviour;
C = 2,2 μF; R_L = 10 kΩ.

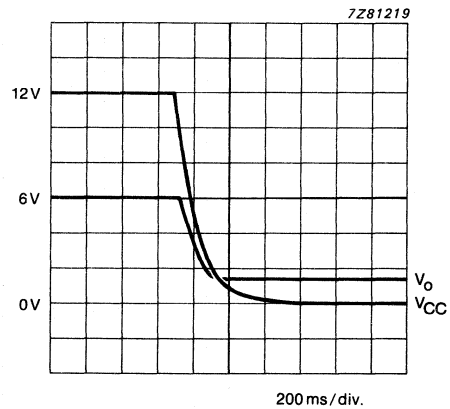


Fig. 19 Turn-off behaviour;
without modulation.

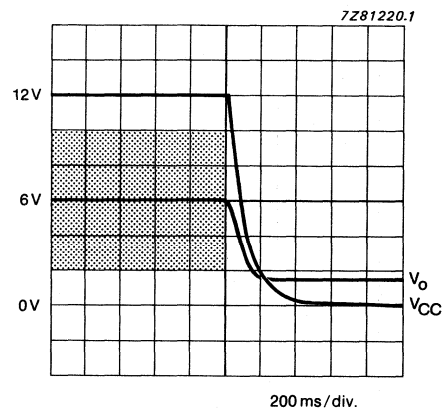


Fig. 20 Turn-off behaviour; with modulation (shaded area).

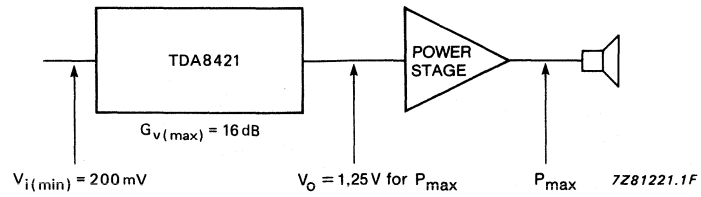


Fig. 21 Level diagram loudspeaker channel CH1 with $V_{i(min)}$ = 200 mV; V_o = 1,25 for P_{max}.

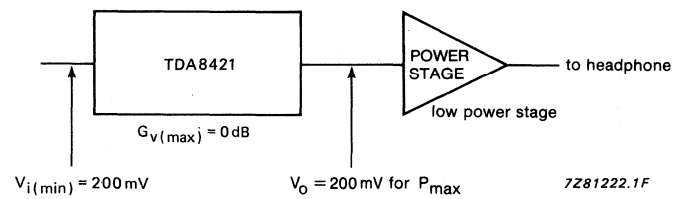


Fig. 22 Level diagram headphone channel CH2 with V_i = 200 mV; V_o = 200 mV for P_{max}.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

HI-FI STEREO AUDIO PROCESSOR; I²C-BUS

GENERAL DESCRIPTION

The TDA8425 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel facility, digitally controlled via the I²C-bus for application in hi-fi audio and television sound.

Features

- Source and mode selector for two stereo channels
- Pseudo stereo, spatial stereo, linear stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	10.8	12.0	13.2	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	300	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	86	–	dB
Total harmonic distortion	THD	–	0.05	–	%
Channel separation	α	–	80	–	dB
Volume control range	G	−64	–	6	dB
Treble control range	G	−12	–	12	dB
Bass control range	G	−12	–	15	dB

PACKAGE OUTLINE

20-lead dual in-line; plastic (SOT146).

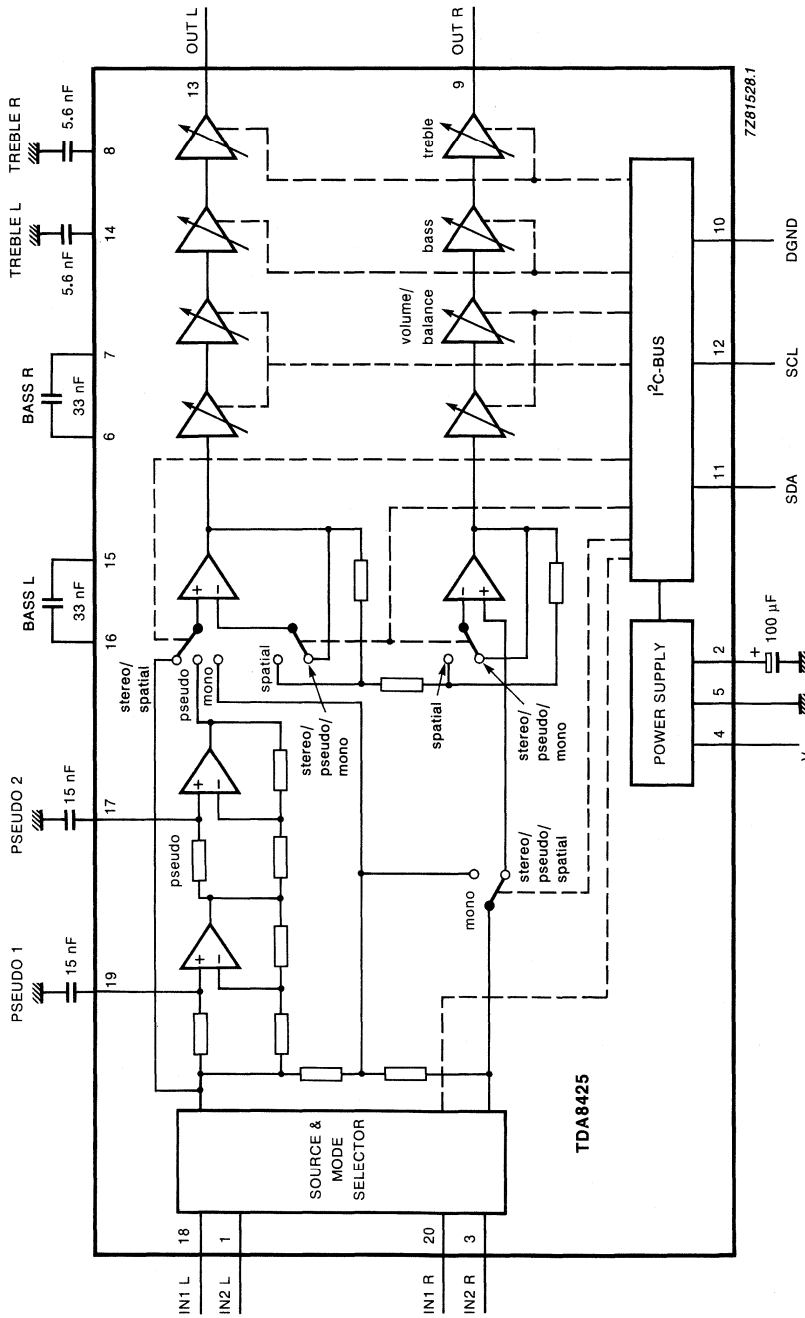


Fig. 1 Block diagram.

PINNING

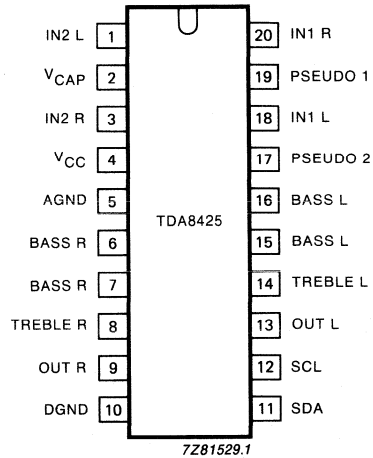


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Source selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the source selector. The selection is made from the following AF input signals:

- IN1 L (pin 18); IN1 R (pin 20)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Mode selector

The mode selector selects between stereo, sound A and sound B (in the event of bilingual transmission) for OUT R and OUT L.

Volume control and balance

The volume control consists of two stages (left and right). In each part the gain can be adjusted between +6 dB and −64 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 80 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right output channels.

Linear stereo, pseudo stereo, spatial stereo and forced mono mode*

It is possible to select four modes: linear stereo, pseudo stereo, spatial stereo or forced mono. The pseudo stereo mode handles mono transmissions, the spatial stereo mode handles stereo transmissions and the forced mono can be used in the event of stereo signals.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

* During forced mono mode the pseudo stereo mode cannot be used.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8425 includes a bias and power supply stage, which generates a voltage of $0.5 \times V_{CC}$ with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both parts of the treble amplifier. The muting can be switched by transmission of the mute bit.

I²C-bus receiver and data handling

Bus specification

The TDA8425 is controlled via the 2-wire I²C-bus by a microcomputer.
The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH.
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition.
The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8425 starts with the module address MAD.

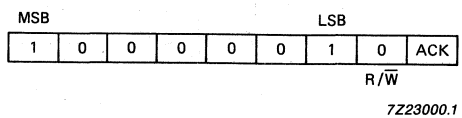


Fig. 3 TDA8425 module address.

Subaddress

After the module address byte a second byte is used to select the following functions:

- Volume left, volume right, bass, treble and switch functions

The subaddress SAD is stored within the TDA8425. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

	128	64	32	16	8	4	2	1
	MSB							LSB
function	7	6	5	4	3	2	1	0
volume left	0	0	0	0	0	0	0	0
volume right	0	0	0	0	0	0	0	1
bass	0	0	0	0	0	0	1	0
treble	0	0	0	0	0	0	1	1
switch functions	0	0	0	0	1	0	0	0
					subaddress SAD			

The automatic increment feature of the slave address enables a quick slave receiver initialization, within one transmission, by the I²C-bus controller (see Fig. 5).

Definition of 3rd byte

A third byte is used to transmit data to the TDA8425. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

function		MSB 7	6	5	4	3	2	1	LSB 0
volume left	VL	1	1	V05	V04	V03	V02	V01	V00
volume right	VR	1	1	V15	V14	V13	V12	V11	V10
bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS

Truth tables

Truth tables for the switch functions

Table 3 Source selector

function	ML1	ML0	IS	channel
stereo	1	1	0	1
stereo	1	1	1	2
sound A	0	1	0	1
sound B	1	0	0	1
sound A	0	1	1	2
sound B	1	0	1	2

Table 4 Pseudo stereo/spatial stereo/linear stereo/forced mono

choice	STL	EFL
spatial stereo	1	1
linear stereo	1	0
pseudo stereo	0	1
forced mono*	0	0

Table 5 Mute

mute	MU
active; automatic after POR	1
not active	0

Where: POR = Power-ON Reset.

Truth tables for the volume, bass and treble controls

Table 6 Volume control

2 dB/step (dB)	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
6	1	1	1	1	1	1
4	1	1	1	1	1	0
−62	0	1	1	1	0	1
−64	0	1	1	1	0	0
⩽ −80	0	1	1	0	1	1
⩽ −80	0	0	0	0	0	0

* Pseudo stereo function is not possible in this mode.

Table 7 Bass control

3 dB/step (dB)	BA3	BA2	BA2	BA0
15	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
15	1	0	1	1
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Table 8 Treble control

3 dB/step (dB)	TR3	TR2	TR2	TR0
12	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all five functions have to be adjusted with five data transmissions. It is recommended that data information for switch functions are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 6. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

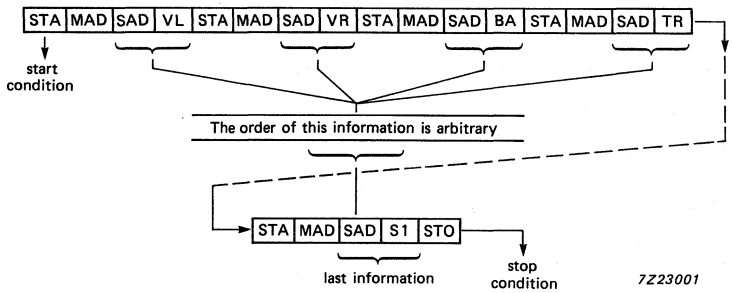


Fig. 4 Data transmission after a power-on reset.

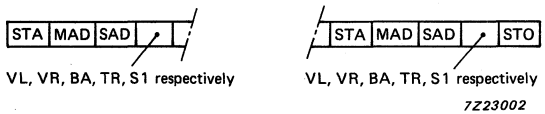


Fig. 5 Data transmission after a power-on reset with auto increment.

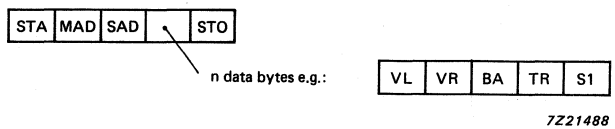


Fig. 6 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for pins with external capacitors	V_{cap}	0	V_{CC}	V
Voltage range for pins 11 and 12	$V_{SDA, SCL}$	0	V_{CC}	V
Voltage range at pins 1, 3, 9, 11, 12, 13, 18 and 20	$V_{I/O}$	0	V_{CC}	V
Output current at pins 9 and 13	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70\ ^oC$	P_{tot}	–	450	mW
Operating ambient temperature range	T_{amb}	0	70	^oC
Storage temperature range	T_{stg}	–25	+ 150	^oC
Electrostatic handling, classification A*				

* Human body model: C = 100 pF, R = 1.5 kΩ and V ⩾ 4 kV; charge device model: C = 200 pF, R = 0 Ω and V ⩾ 500 V.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	10.8	12.0	13.2	V
Supply current					
at V_{CC} = 12 V	I_{CC}	–	26	35	mA
Internal reference voltage	V_{ref}	5.4	0.5 x V_{CC}	6.6	V
Internal voltage at pins 1, 3, 18 and 20 DC voltage internally generated; capacitive coupling recommended	V_I	–	V_{REF}	–	V
Internal voltage at pins 9 and 13	V_O	–	V_{REF}	–	V
SDA; SCL (pins 11 and 12)					
input voltage HIGH	V_{IH}	3.0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0.3	–	1.5	V
input current HIGH	I_{IH}	–	–	+ 10	μA
input current LOW	I_{IL}	−10	–	–	μA
Output voltage at pins with external capacitors					
pins 6 to 8, 14 to 17, 19	$V_{cap.n}$	–	V_{REF}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0.3	–	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 1000\ pF$; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 7)					
SDA, SCL (pin 11 and 12)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4.7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0.3	μs
Set-up time for start condition	$t_{SU;STA}$	4.7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4.7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4.7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
INPUTS					
IN1 L (pin 18) IN1 R (pin 20); IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (RMS value) at V_u = −12 dB; THD ⩽ 0.5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_i	20	30	40	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz
OUTPUTS					
OUT R (pin 9); OUT L (pin 13)					
Output voltage range (rms value) at THD ⩽ 0.7%; $V_{i(max)}$ ⩽ 2 V	$V_{o(rms)}$	0.6	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Signal plus noise-to-noise ratio (weighted according to CCIR 468-2); V_o = 600 mV					
gain = 6 dB	(S+N)/N	–	78	–	dB
gain = 0 dB	(S+N)/N	–	86	–	dB
gain = ⩽ −20 dB	(S+N)/N	–	68	–	dB

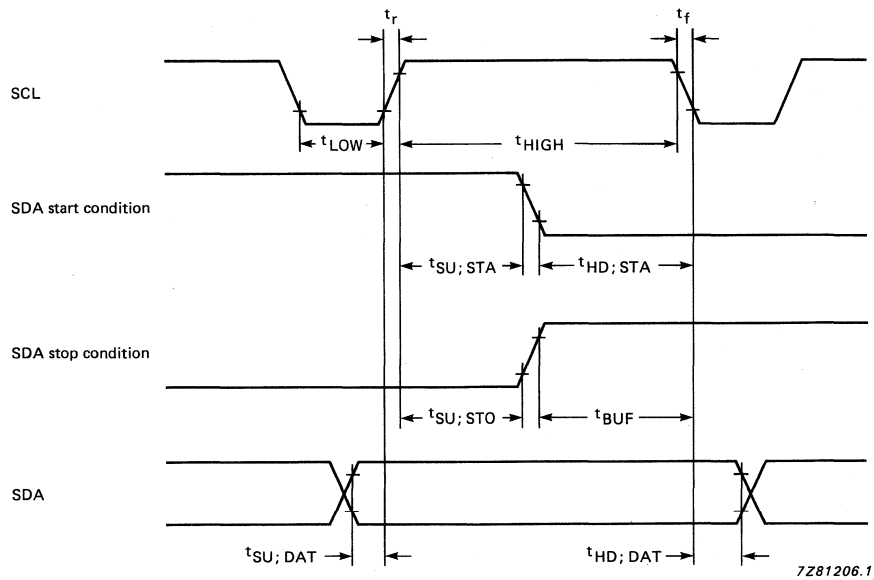
AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS (continued)					
Crosstalk between inputs at gain = 0 dB; 1 kHz; opposite inputs grounded (50 Ω); IN1L (pin 18) to IN2L (pin 1) or IN1R (pin 20) to IN2R (pin 3)	α_{cr}	–	100	–	dB
Total harmonic distortion (f = 20 Hz to 12.5 kHz)					
for $V_{i(rms)}$ = 0.3 V; gain = + 6 dB to –40 dB	THD	–	0.05	–	%
for $V_{i(rms)}$ = 0.6 V; gain = 0 dB to –40 dB	THD	–	0.07	0.4	%
for $V_{i(rms)}$ = 2.0 V; gain = –12 dB to –40 dB	THD	–	0.1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cs}	–	80	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	100	–	dB
VOLUME CONTROL					
For truth table see Table 6					
Control range at f = 1 kHz (36 steps)					
maximum voltage gain (6 dB step)	G_{max}	5	6	–	dB
minimum voltage gain (–64 dB step)	G_{min}	–63	–64	–	dB
mute position	G_{mute}	–80	–90	–	dB
Gain tracking error; balance in mid-position	G	–	–	2	dB
Step resolution					
gain from 6 dB to –40 dB	G_{step}	1.5	2.0	2.5	dB/step
gain from –42 dB to –64 dB	G_{step}	1.0	2.0	3.0	dB/step
TREBLE CONTROL					
For truth table see Table 8					
Control range for $C_{8\text{-}5}$; $C_{14\text{-}5}$ = 5.6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step

parameter	symbol	min.	typ.	max.	unit
BASS CONTROL					
For truth table see Table 7					
Control range for C_{6-7}; C_{15-16} = 33 nF					
Maximum emphasis at 40 Hz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 Hz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	52	–	%
Pseudo: Phase shift (see Fig. 8)					

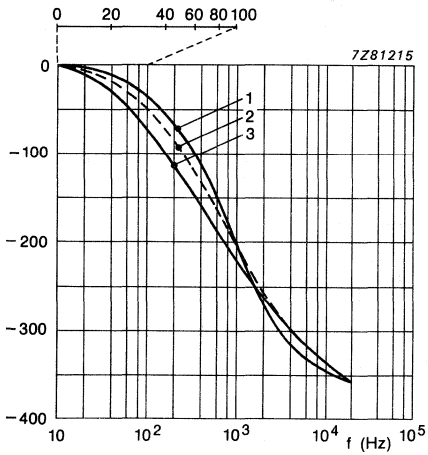
Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels (left and right).



$t_{SU;STA}$ = start code set-up time.
$t_{HD;STA}$ = start code hold time.
$t_{SU;STO}$ = stop code set-up time.
t_{BUF} = bus free time.
$t_{SU;DAT}$ = data set-up time.
$t_{HD;DAT}$ = data hold time.

Fig. 7 Timing requirements for I²C-bus.



curve	pin 17 (nF)	pin 19 (nF)	effect
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified

Fig. 8 Pseudo (phase in degrees) as a function of frequency (left output).

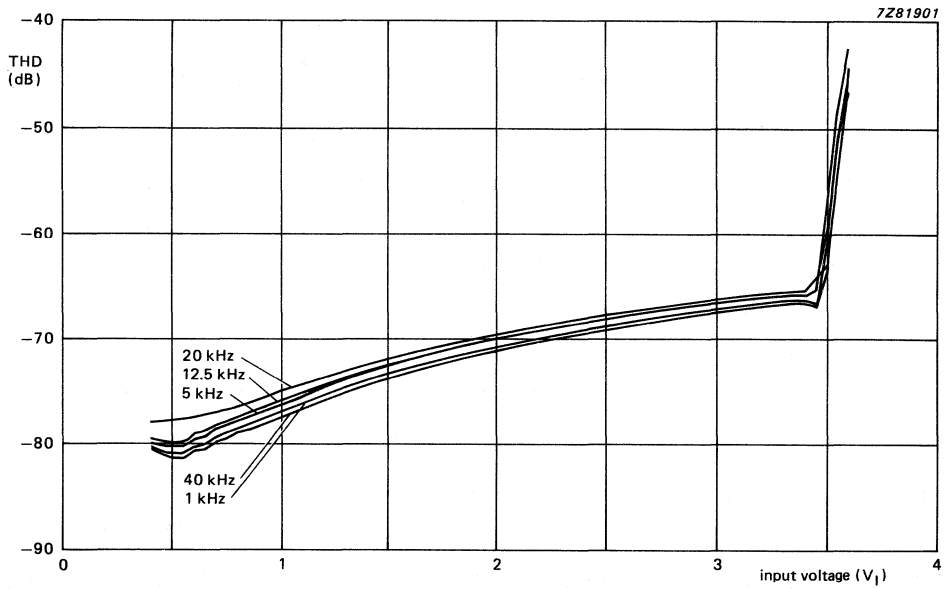


Fig. 9 Input signal handling capability; gain = −10 dB; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

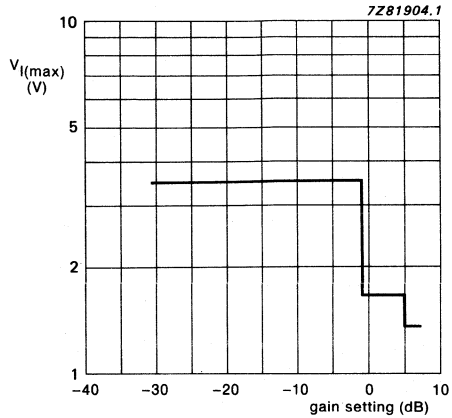


Fig. 10 Input signal handling capacility plotted against gain setting; THD = −60 dB; f = 1 kHz; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

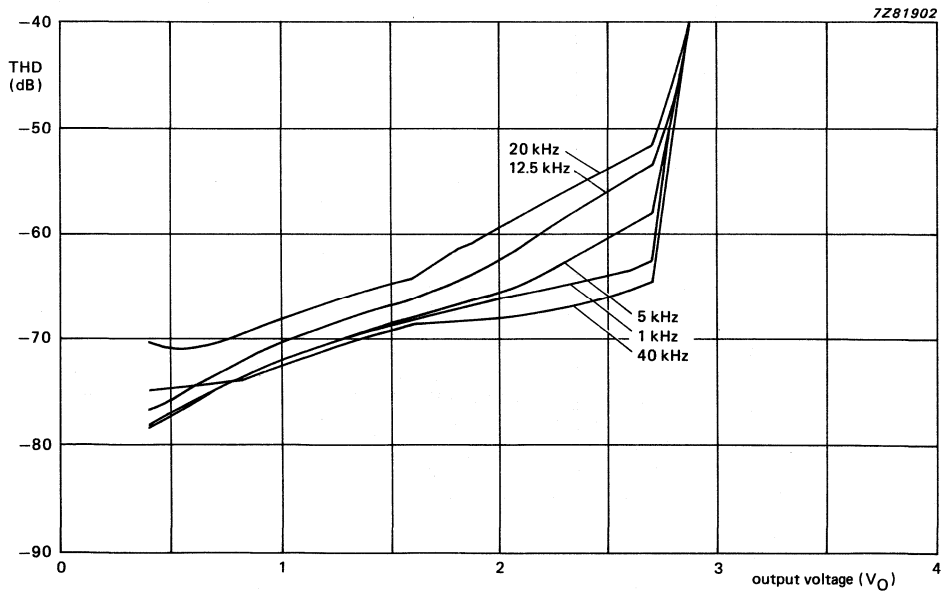


Fig. 11 Output signal handling capability; gain = 6 dB; R_S = 600 Ω; R_L = 10 kΩ, bass/trebble = 0 dB, V_{CC} = 12 V.

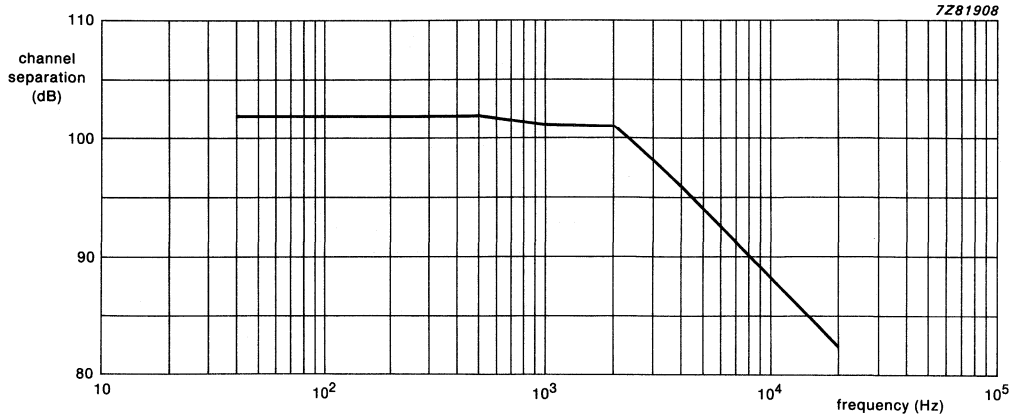
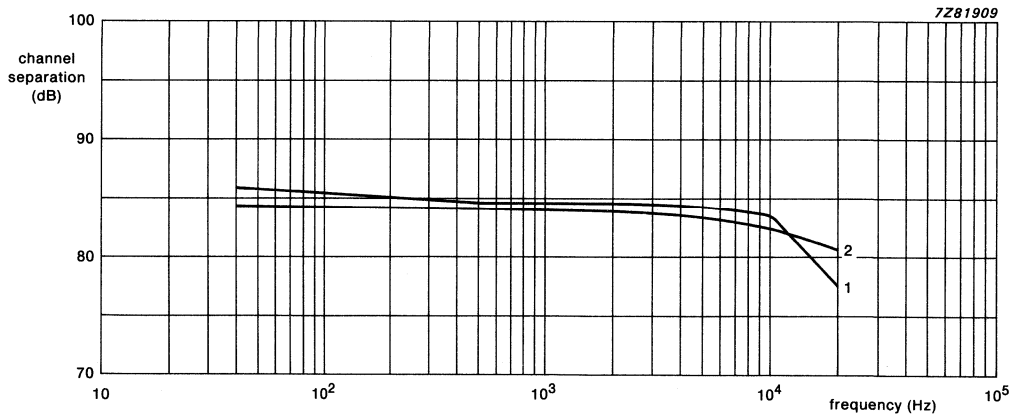


Fig. 12 Source selector separation (channel 2 and channel 1); gain = 0 dB; V_{i1} = 0 V; V_{i2} = 1 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.



(1) gain = 0 dB; V_i = 1.0 V.
(2) gain = 6 dB; V_i = 0.5 V.

Fig. 13 Stereo channel separation as a function of frequency; R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

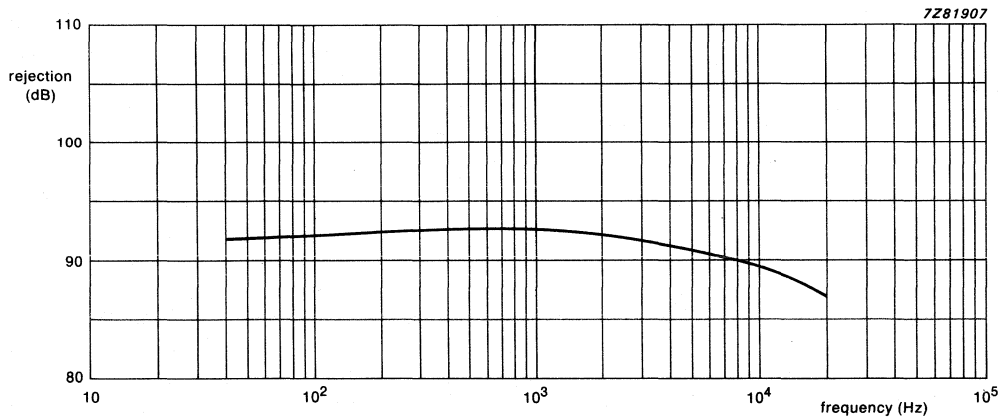


Fig. 14 Mute signal rejection as a function of frequency; gain = 0 dB; V_i = 1.0 V; R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

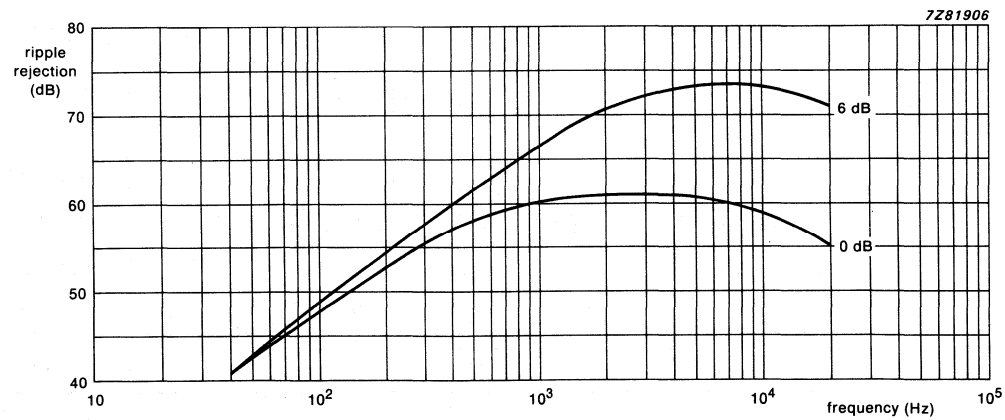


Fig. 15 Ripple rejection as a function of frequency; voltage ripple = 0.3 V (rms); R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

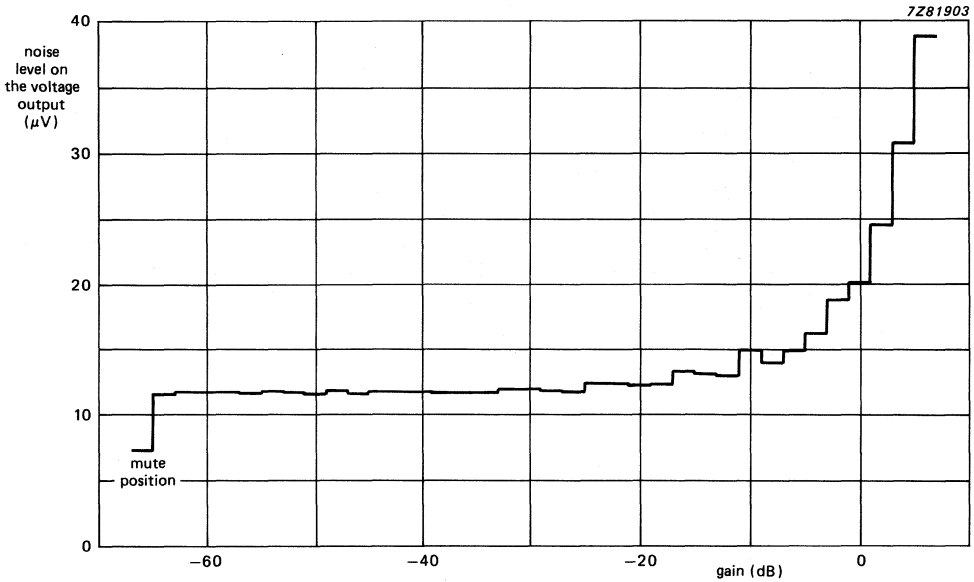


Fig. 16 Noise output voltage as a function of gain; weighted CCIR468 quasi peak gain, + 6 dB to −64 dB; V_i = 0 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

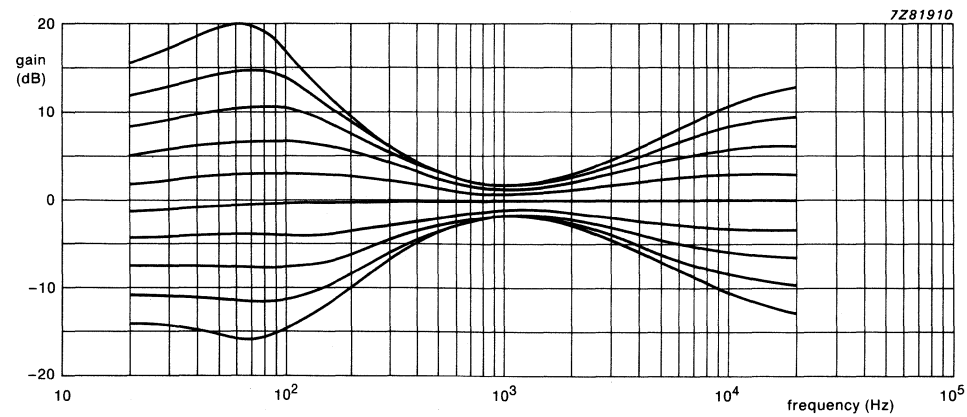


Fig. 17 Frequency response of bass and trebble control; bass and trebble gain settings = −12 to + 15 dB; gain is 0 dB; V_i = 0.1 V; R_{S9} = 600 Ω; R_L = 10 kΩ; V_{CC} = 12 V.

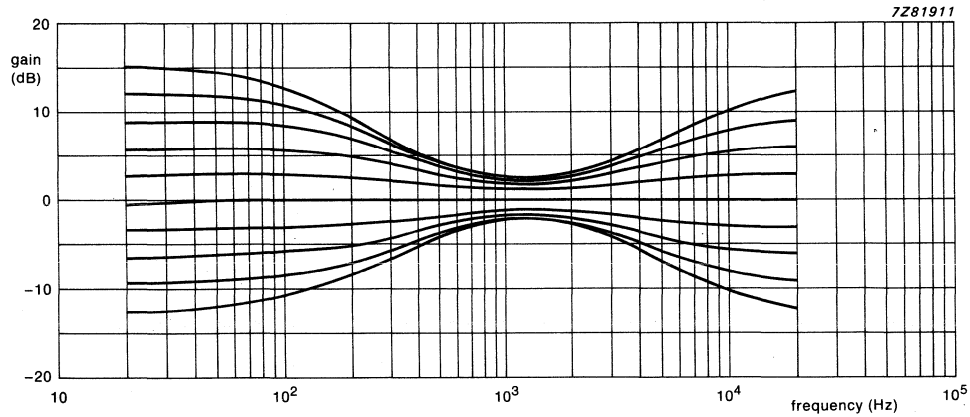


Fig. 18 Tone control with T-filter.

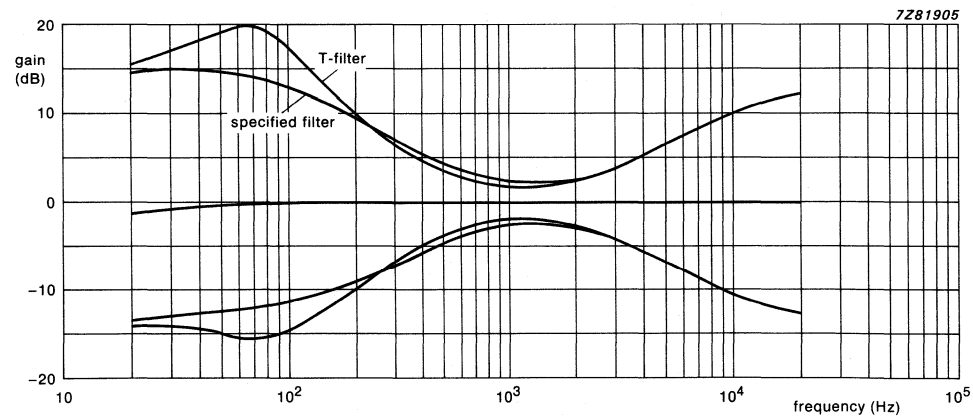


Fig. 19 Tone control.

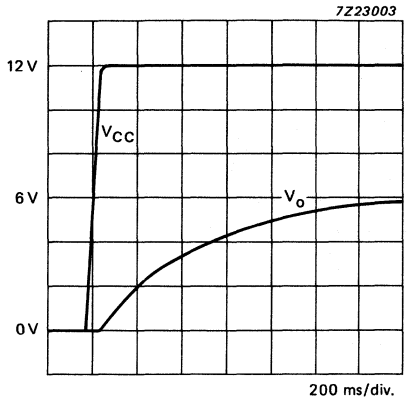


Fig. 20 Turn-on behaviour;
$C = 2.2\ \mu F$; $R_L = 10\ k\Omega$.

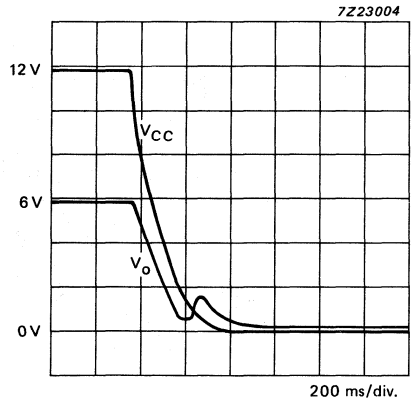


Fig. 21 Turn-off behaviour;
without modulation.

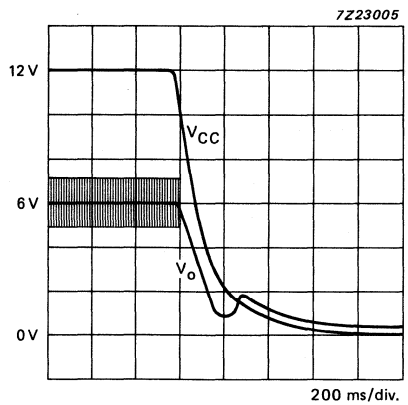
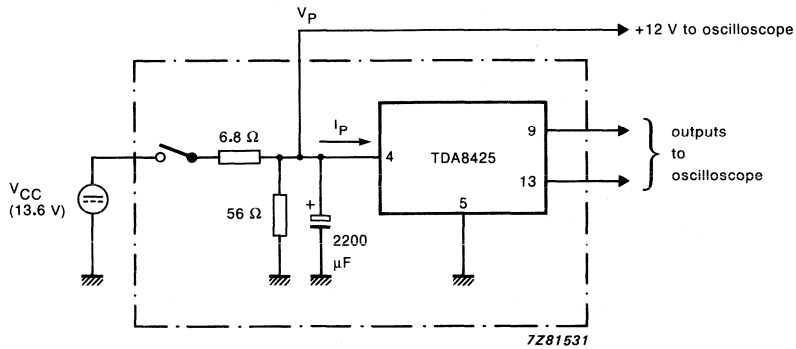


Fig. 22 Turn-off behaviour; with modulation (shaded area).



I_{CC} = 25 mA
I_{load} = 239 mA
t_{on} = 15 ms
t_{off} = 110 ms

Fig. 23 Turn-on/off power supply circuit diagram.

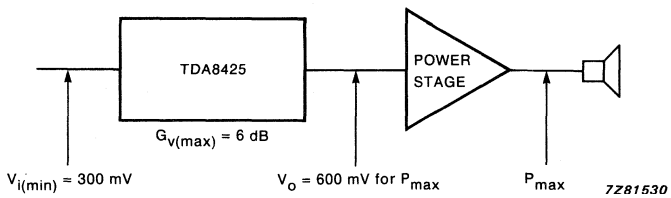


Fig. 24 Level diagram.

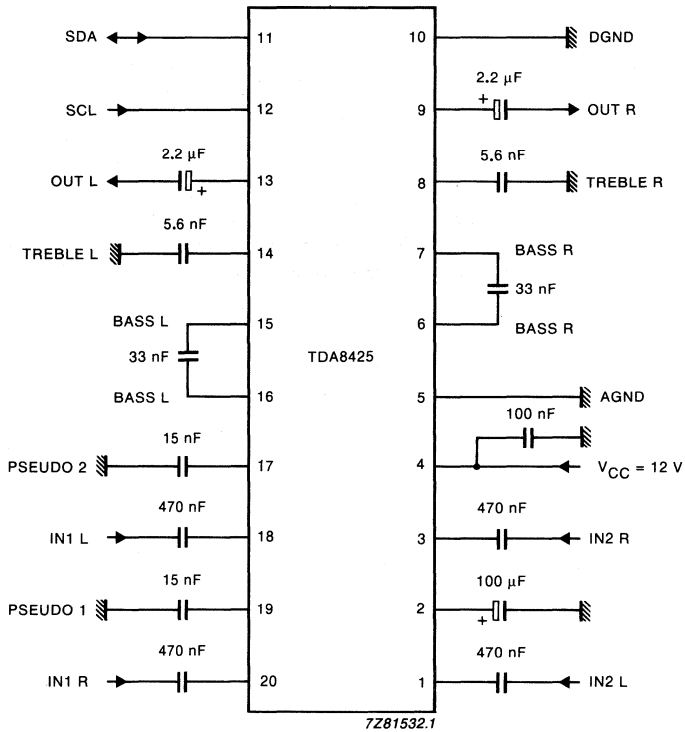


Fig. 25 Test and application circuit diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

HI-FI STEREO AUDIO PROCESSOR; I²C-BUS

GENERAL DESCRIPTION

The TDA8426 is a stereo sound circuit with a loudspeaker channel facility, digital controlled via the I²C-bus, for application in hi-fi audio and television sound. Reduced spatial antiphase crosstalk (30%) makes the device especially suitable for application in projection television receivers.

Features

- Source and mode selector for two stereo channels
- Pseudo stereo, spatial stereo, linear stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	10.8	12.0	13.2	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	300	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	86	–	dB
Total harmonic distortion	THD	–	0.05	–	%
Channel separation	α	–	80	–	dB
Volume control range	G	–64	–	6	dB
Treble control range	G	–12	–	12	dB
Bass control range	G	–12	–	15	dB

PACKAGE OUTLINE

20-lead dual in-line; plastic (SOT146).

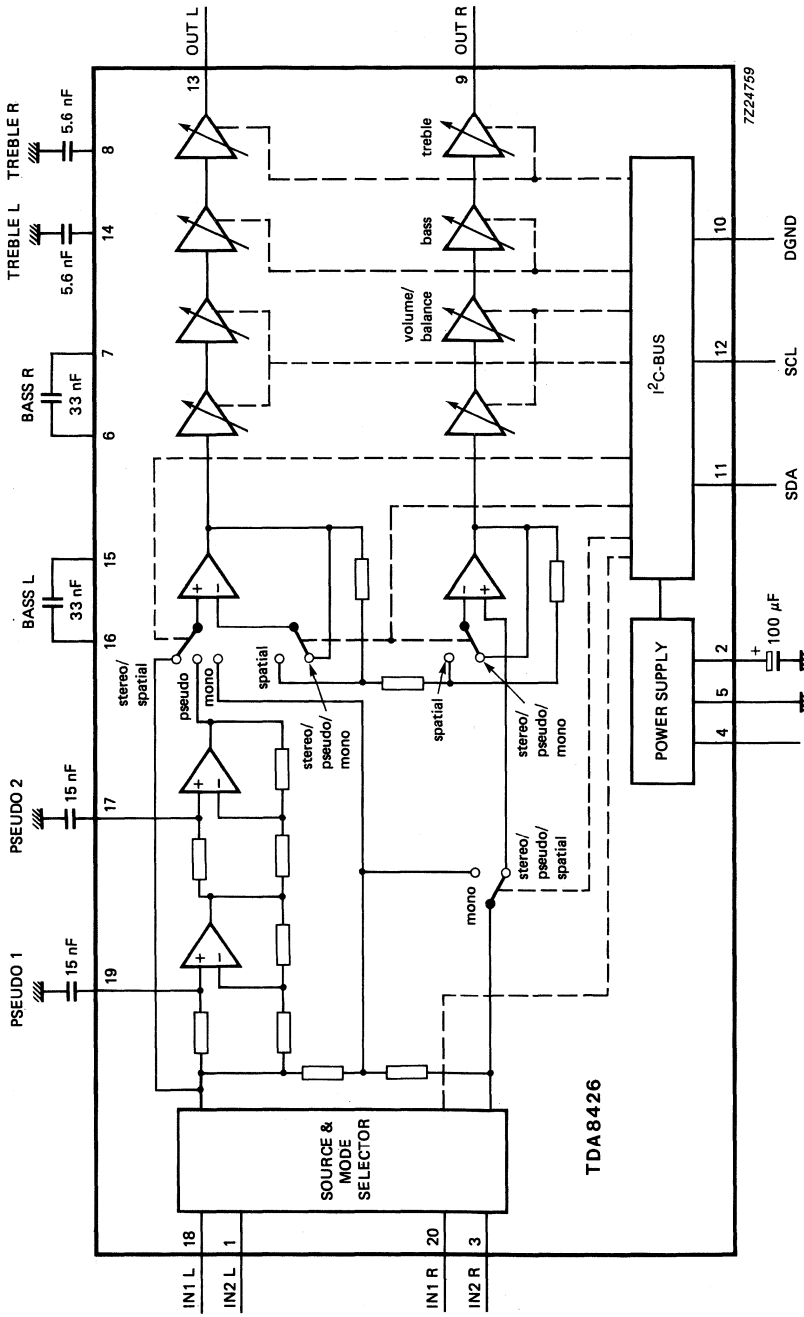


Fig.1 Block diagram.

PINNING

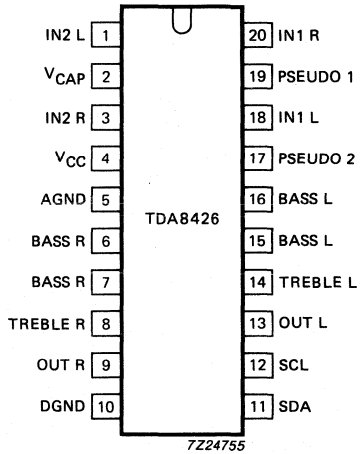


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Source selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the source selector. The selection is made from the following AF input signals:

- IN1 L (pin 18); IN1 R (pin 20)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Mode selector

The mode selector selects between stereo, sound A and sound B (in the event of bilingual transmission) for OUT R and OUT L.

Volume control and balance

The volume control consists of two stages (left and right). In each part the gain can be adjusted between +6 dB and −64 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 80 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right output channels.

Linear stereo, pseudo stereo, spatial stereo and forced mono mode*

It is possible to select four modes: linear stereo, pseudo stereo, spatial stereo or forced mono. The pseudo stereo mode handles mono transmissions, the spatial stereo mode handles stereo transmissions and the forced mono can be used in the event of stereo signals.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

* During forced mono mode the pseudo stereo mode cannot be used.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8426 includes a bias and power supply stage, which generates a voltage of $0.5 \times V_{CC}$ with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both parts of the treble amplifier. The muting can be switched by transmission of the mute bit.

I^2C-bus receiver and data handling

Bus specification

The TDA8426 is controlled via the 2-wire I^2C-bus by a microcomputer.
The two wires (SDA — serial data, SCL — serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH.
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition.
The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8426 starts with the module address MAD.

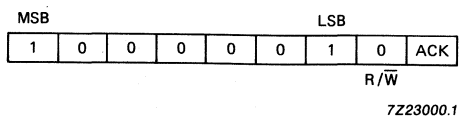


Fig. 3 TDA8426 module address.

Subaddress

After the module address byte a second byte is used to select the following functions:

- Volume left, volume right, bass, treble and switch functions

The subaddress SAD is stored within the TDA8426. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

	128	64	32	16	8	4	2	1
	MSB							LSB
function	7	6	5	4	3	2	1	0
volume left	0	0	0	0	0	0	0	0
volume right	0	0	0	0	0	0	0	1
bass	0	0	0	0	0	0	1	0
treble	0	0	0	0	0	0	1	1
switch functions	0	0	0	0	1	0	0	0
					subaddress SAD			

The automatic increment feature of the slave address enables a quick slave receiver initialization, within one transmission, by the I²C-bus controller (see Fig. 5).

Definition of 3rd byte

A third byte is used to transmit data to the TDA8426. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

function		MSB 7	6	5	4	3	2	1	LSB 0
volume left	VL	1	1	V05	V04	V03	V02	V01	V00
volume right	VR	1	1	V15	V14	V13	V12	V11	V10
bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS

Truth tables

Truth tables for the switch functions

Table 3 Source selector

function	ML1	ML0	IS	channel
stereo	1	1	0	1
stereo	1	1	1	2
sound A	0	1	0	1
sound B	1	0	0	1
sound A	0	1	1	2
sound B	1	0	1	2

Table 4 Pseudo stereo/spatial stereo/linear stereo/forced mono

choice	STL	EFL
spatial stereo	1	1
linear stereo	1	0
pseudo stereo	0	1
forced mono*	0	0

Table 5 Mute

mute	MU
active; automatic after POR	1
not active	0

Where: POR = Power-ON Reset.

Truth tables for the volume, bass and treble controls

Table 6 Volume control

2 dB/step (dB)	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
6	1	1	1	1	1	1
4	1	1	1	1	1	0
–62	0	1	1	1	0	1
–64	0	1	1	1	0	0
⩽ –80	0	1	1	0	1	1
⩽ –80	0	0	0	0	0	0

* Pseudo stereo function is not possible in this mode.

Table 7 Bass control

3 dB/step (dB)	BA3	BA2	BA2	BA0
15	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
15	1	0	1	1
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Table 8 Treble control

3 dB/step (dB)	TR3	TR2	TR2	TR0
12	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all five functions have to be adjusted with five data transmissions. It is recommended that data information for switch functions are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 6. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

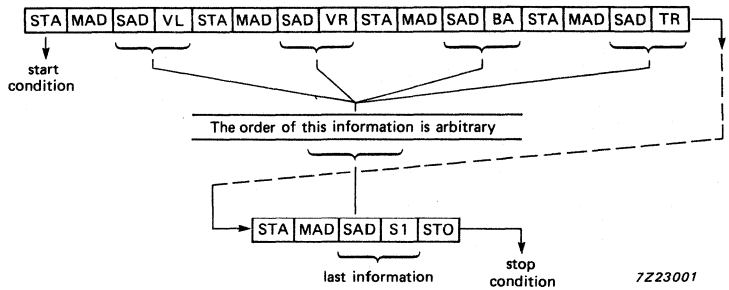


Fig. 4 Data transmission after a power-on reset.

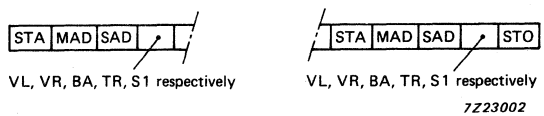


Fig. 5 Data transmission after a power-on reset with auto increment.

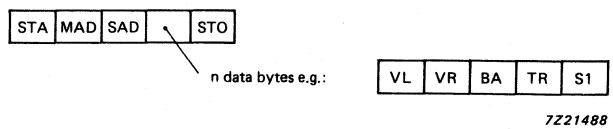


Fig. 6 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for pins with external capacitors	V_{cap}	0	V_{CC}	V
Voltage range for pins 11 and 12	$V_{SDA, SCL}$	0	V_{CC}	V
Voltage range at pins 1, 3, 9, 11, 12, 13, 18 and 20	$V_{I/O}$	0	V_{CC}	V
Output current at pins 9 and 13	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70$ °C	P_{tot}	–	450	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	–25	+ 150	°C
Electrostatic handling, classification A*				

* Human body model: C = 100 pF, R = 1.5 kΩ and V ⩾ 4 kV; charge device model: C = 200 pF, R = 0 Ω and V ⩾ 500 V.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	10.8	12.0	13.2	V
Supply current					
at V_{CC} = 12 V	I_{CC}	–	26	35	mA
Internal reference voltage	V_{ref}	5.4	0.5 x V_{CC}	6.6	V
Internal voltage at pins 1, 3, 18 and 20 DC voltage internally generated; capacitive coupling recommended	V_I	–	V_{ref}	–	V
Internal voltage at pins 9 and 13	V_O	–	V_{ref}	–	V
SDA; SCL (pins 11 and 12)					
input voltage HIGH	V_{IH}	3.0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0.3	–	1.5	V
input current HIGH	I_{IH}	–	–	+ 10	μA
input current LOW	I_{IL}	−10	–	–	μA
Output voltage at pins with external capacitors					
pins 6 to 8, 14 to 17, 19	$V_{cap.n}$	–	V_{ref}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0.3	–	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 1000\ pF$; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C-bus timing (see Fig. 7)					
SDA, SCL (pin 11 and 12)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4.7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0.3	μs
Set-up time for start condition	$t_{SU;STA}$	4.7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4.7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4.7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
INPUTS					
IN1 L (pin 18) IN1 R (pin 20); IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (RMS value) at V_u = −12 dB; THD ≤ 0.5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_i	20	30	40	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz
OUTPUTS					
OUT R (pin 9); OUT L (pin 13)					
Output voltage range (rms value) at THD ≤ 0.7%; $V_{i(max)} \leq 2$ V	$V_{o(rms)}$	0.6	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Signal plus noise-to-noise ratio (weighted according to CCIR 468-2); V_o = 600 mV					
gain = 6 dB	(S+N)/N	–	78	–	dB
gain = 0 dB	(S+N)/N	–	86	–	dB
gain = ≤ −20 dB	(S+N)/N	–	68	–	dB

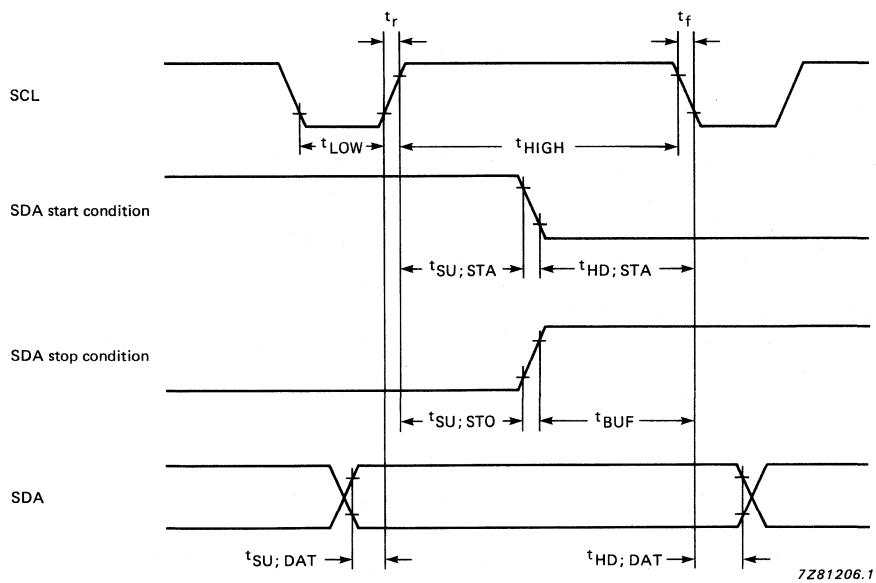
AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS (continued)					
Crosstalk between inputs at gain = 0 dB; 1 kHz; opposite inputs grounded (50 Ω); IN1L (pin 18) to IN2L (pin 1) or IN1R (pin 20) to IN2R (pin 3)	α_{cr}	–	100	–	dB
Total harmonic distortion (f = 20 Hz to 12.5 kHz)					
for $V_{i(rms)}$ = 0.3 V; gain = + 6 dB to –40 dB	THD	–	0.05	–	%
for $V_{i(rms)}$ = 0.6 V; gain = 0 dB to –40 dB	THD	–	0.07	0.4	%
for $V_{i(rms)}$ = 2.0 V; gain = –12 dB to –40 dB	THD	–	0.1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cs}	–	80	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	100	–	dB
VOLUME CONTROL					
For truth table see Table 6					
Control range at f = 1 kHz (36 steps)					
maximum voltage gain (6 dB step)	G_{max}	5	6	–	dB
minimum voltage gain (–64 dB step)	G_{min}	–63	–64	–	dB
mute position	G_{mute}	–80	–90	–	dB
Gain tracking error; balance in mid-position	G	–	–	2	dB
Step resolution					
gain from 6 dB to –40 dB	G_{step}	1.5	2.0	2.5	dB/step
gain from –42 dB to –64 dB	G_{step}	1.0	2.0	3.0	dB/step
TREBLE CONTROL					
For truth table see Table 8					
Control range for $C_{8\text{-}5}$; $C_{14\text{-}5}$ = 5.6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step

parameter	symbol	min.	typ.	max.	unit
BASS CONTROL					
For truth table see Table 7					
Control range for C_{6-7}; C_{15-16} = 33 nF					
Maximum emphasis at 40 Hz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 Hz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	30	–	%
Pseudo: Phase shift (see Fig. 8)					

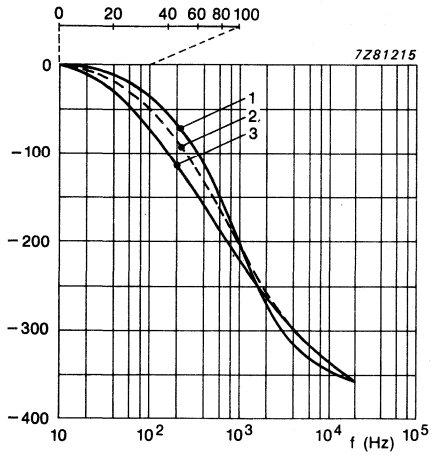
Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels (left and right).



$t_{SU;STA}$ = start code set-up time.
$t_{HD;STA}$ = start code hold time.
$t_{SU;STO}$ = stop code set-up time.
t_{BUF} = bus free time.
$t_{SU;DAT}$ = data set-up time.
$t_{HD;DAT}$ = data hold time.

Fig. 7 Timing requirements for I²C-bus.



curve	pin 17 (nF)	pin 19 (nF)	effect
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified

Fig. 8 Pseudo (phase in degrees) as a function of frequency (left output).

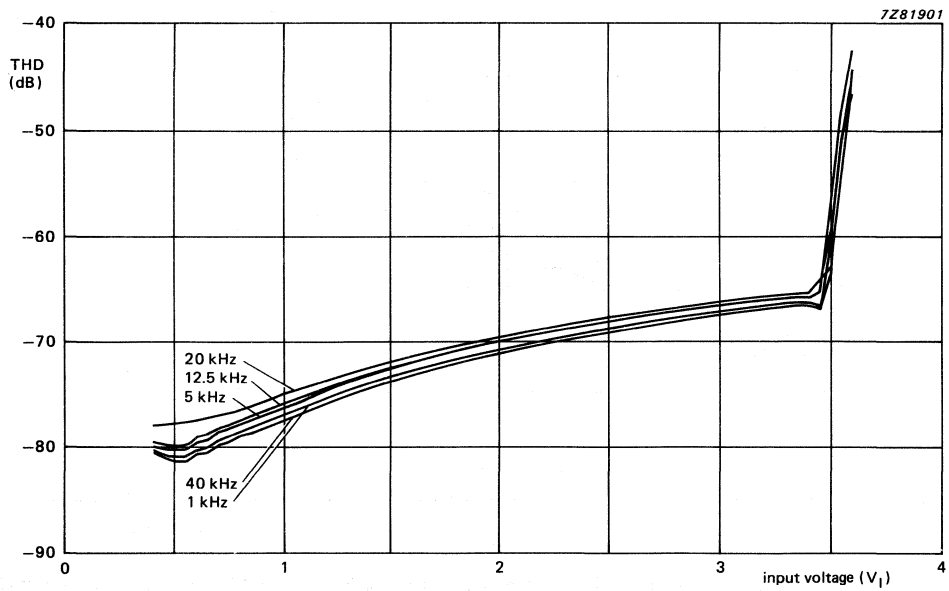


Fig. 9 Input signal handling capability; gain = −10 dB; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

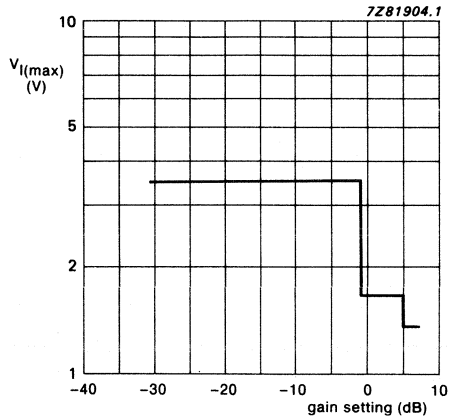


Fig. 10 Input signal handling capacility plotted against gain setting; THD = −60 dB; f = 1 kHz; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

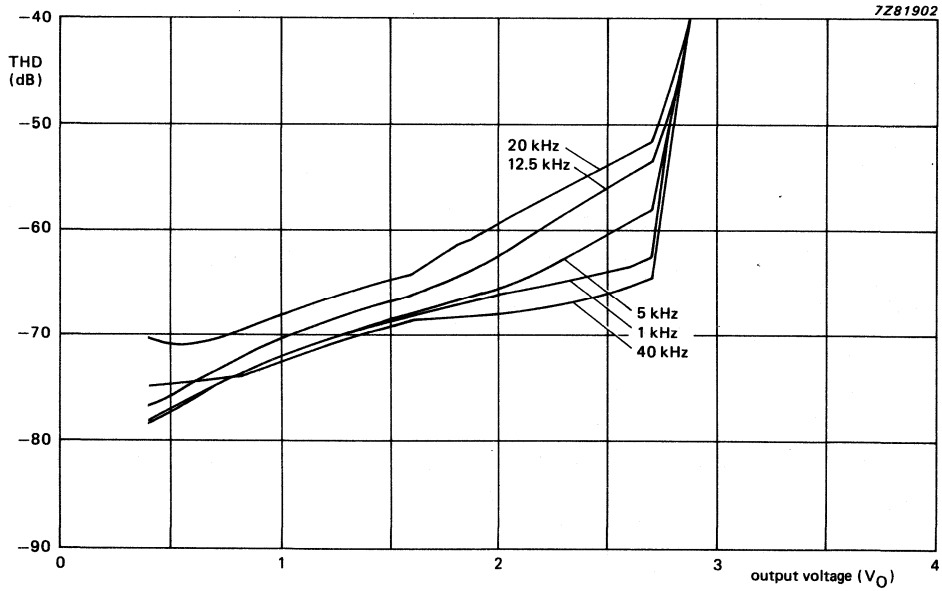


Fig. 11 Output signal handling capability; gain = 6 dB; R_S = 600 Ω; R_L = 10 kΩ, bass/trebble = 0 dB, V_{CC} = 12 V.

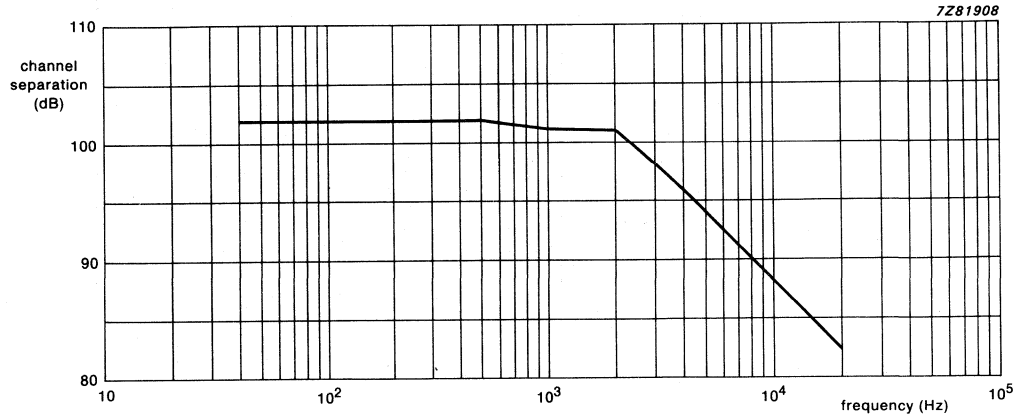
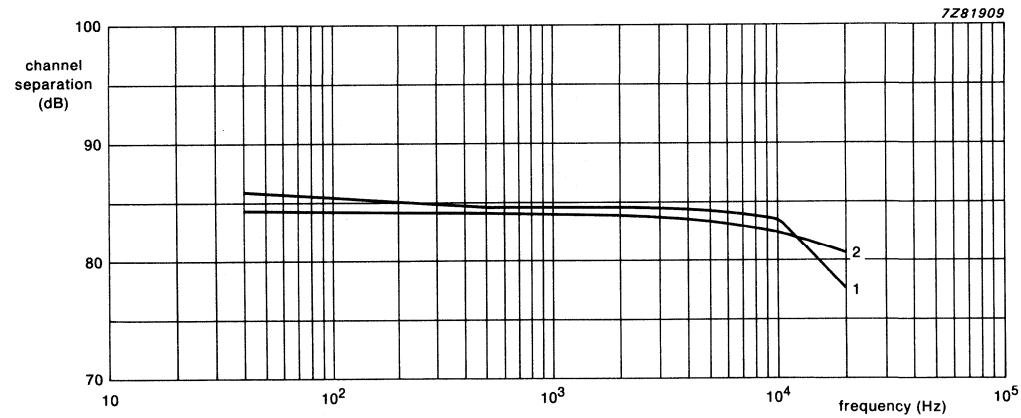


Fig. 12 Source selector separation (channel 2 and channel 1); gain = 0 dB; V_{i1} = 0 V; V_{i2} = 1 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.



(1) gain = 0 dB; V_i = 1.0 V.
(2) gain = 6 dB; V_i = 0.5 V.

Fig. 13 Stereo channel separation as a function of frequency; R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

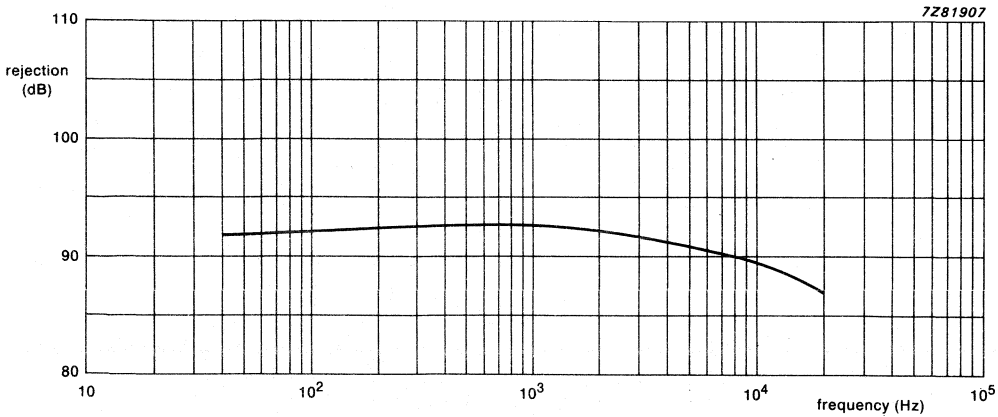


Fig. 14 Mute signal rejection as a function of frequency; gain = 0 dB; V_i = 1.0 V; R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

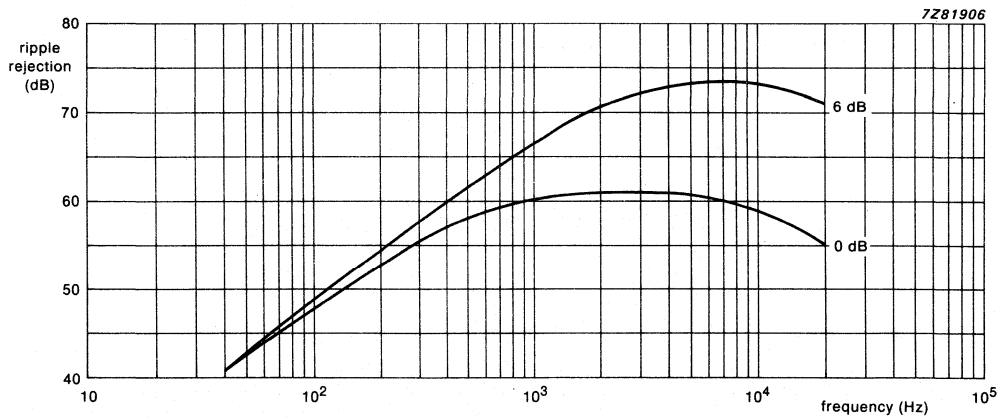


Fig. 15 Ripple rejection as a function of frequency; voltage ripple = 0.3 V (rms); R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

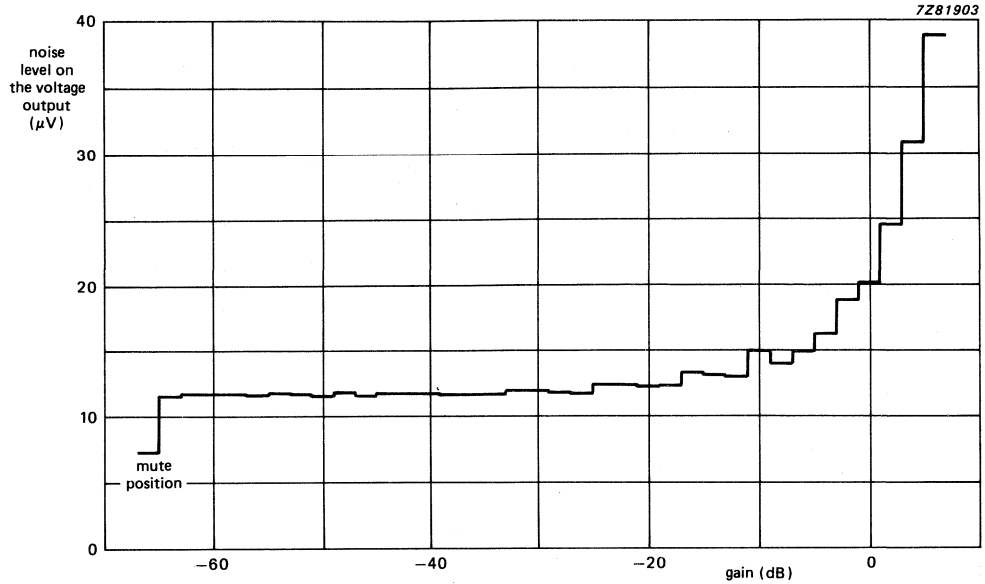


Fig. 16 Noise output voltage as a function of gain; weighted CCIR468 quasi peak gain, + 6 dB to −64 dB; V_i = 0 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

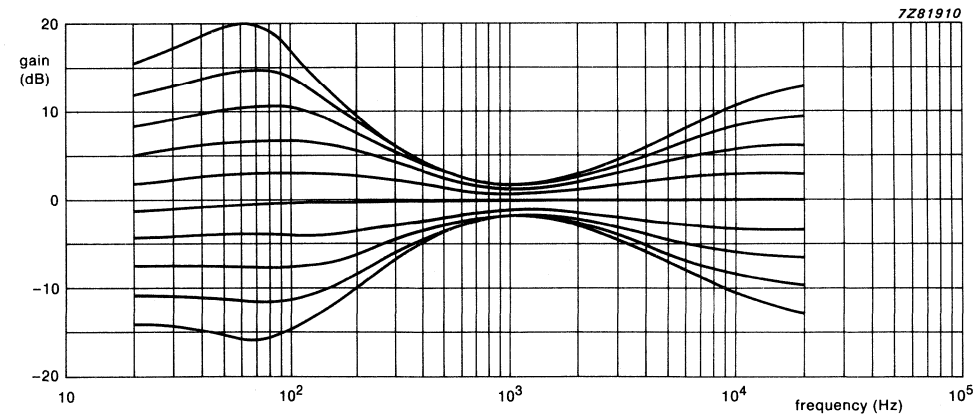


Fig. 17 Frequency response of bass and trebble control; bass and trebble gain settings = −12 to + 15 dB; gain is 0 dB; V_i = 0.1 V; R_{SG} = 600 Ω; R_L = 10 kΩ; V_{CC} = 12 V.

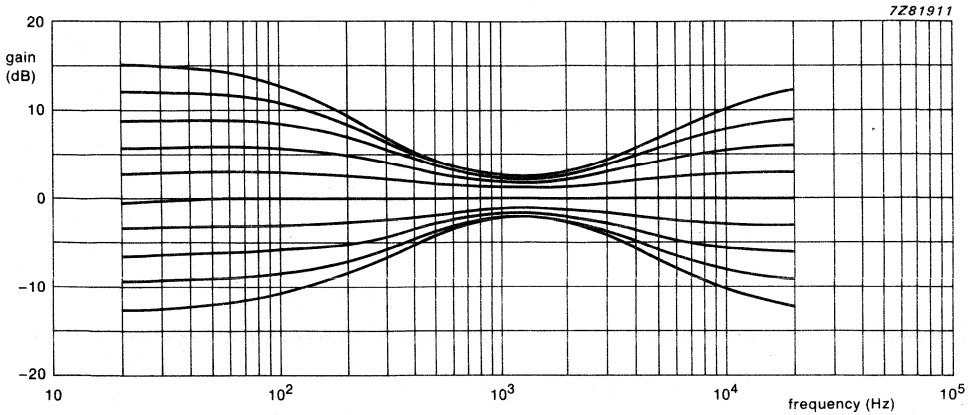


Fig. 18 Tone control with T-filter.

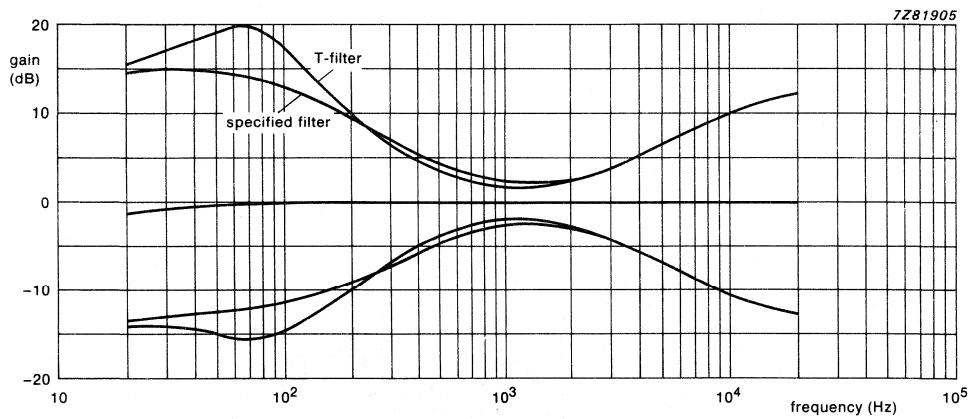


Fig. 19 Tone control.

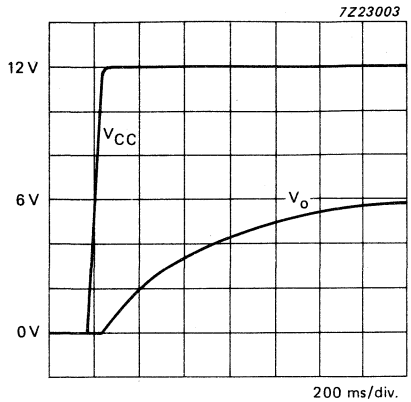


Fig. 20 Turn-on behaviour;
$C = 2.2\ \mu F$; $R_L = 10\ k\Omega$.

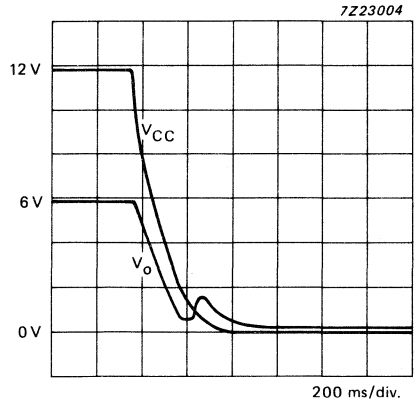


Fig. 21 Turn-off behaviour;
without modulation.

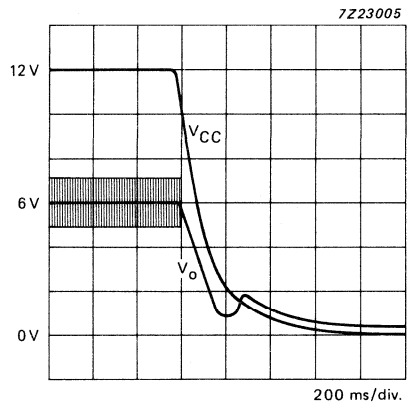
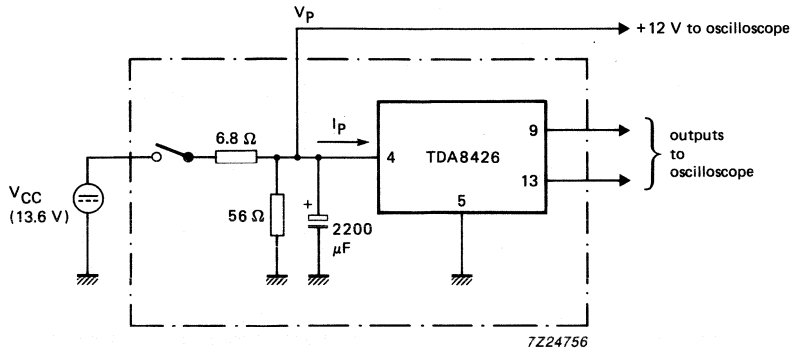


Fig. 22 Turn-off behaviour; with modulation (shaded area).



I_{CC} = 25 mA
I_{load} = 239 mA
t_{on} = 15 ms
t_{off} = 110 ms

Fig.23 Turn-on/off power supply circuit diagram.

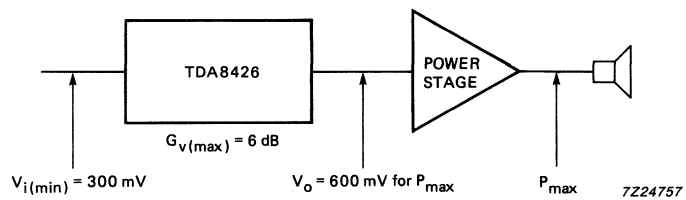


Fig.24 Level diagram.

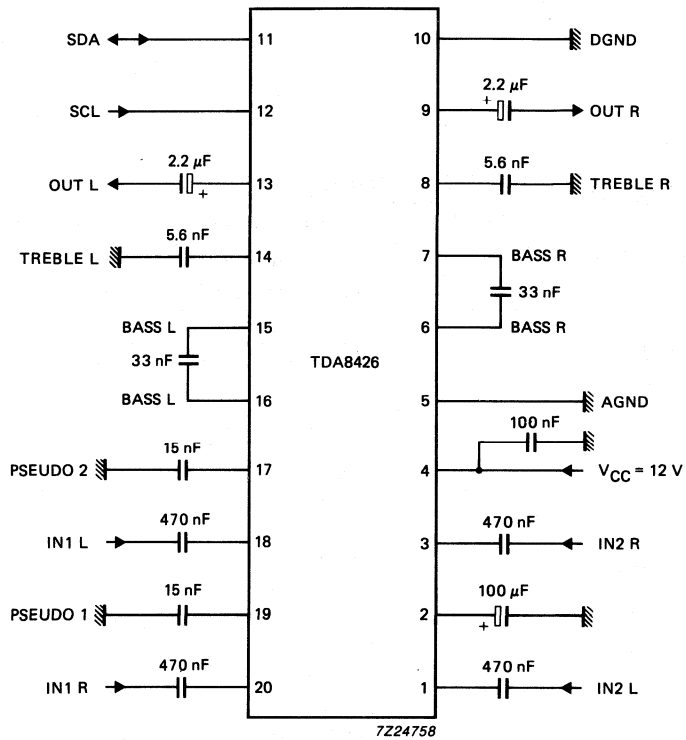


Fig.25 Test and application circuit diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Deflection processor for computer controlled TV receivers

TDA8433

FEATURES

- I²C-bus interface
- Input for vertical sync
- Sawtooth generator with amplitude independent of frequency
- Vertical deflection output stage driver
- East-west raster correction drive output
- EHT modulation input
- Changes picture width and height without affecting geometry.

GENERAL DESCRIPTION

The TDA8433 is an I²C-bus controlled deflection processor which, together with a sync processor (e.g. TDA2579A, see Fig.6), contains the control and drive functions of the deflection part in a computer controlled TV receiver. The TDA8433 replaces all picture geometry settings which were previously set manually during manufacture.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage (pin 12)	10.8	12.0	13.2	V
I_{CC}	supply current (pin 12)	12	20	27	mA
V_2	vertical sync trigger level	–	3	–	V
V_{21}	vertical feedback (note 1) DC level AC level	 –1.7 1.65	 1.85 1.8	 2.05 1.95	 V V_P
V_{24}	EHT compensation operating range	1.7	–	6	V
V_{11-13}	inputs for control register data: not locked to video at 50 Hz status at 60 Hz status	 – 0.8 V_{CC} –	 0.7 – –	 1 – 0.7 V_{CC}	 V V V
V_{10-13}	HCENT comparator switching level	–	V_{17}	–	V
V_{14-13}	SDA I²C-bus switching level data input	–	3.5	–	V
V_{15}	SCL I²C-bus switching level clock input	–	3.5	–	V
V_1	device selection where: Ao = '1' Ao = '0'	 9.0 0	 – –	 V_{CC} 2.0	 V V

Note to the quick reference data

1. VR_{in} = 0; V-S-corr = 0; V_{shift} = 20 H; V_{ampl} = 20 H.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8433	24	DIL	plastic	SOT101

Deflection processor for computer controlled TV receivers

TDA8433

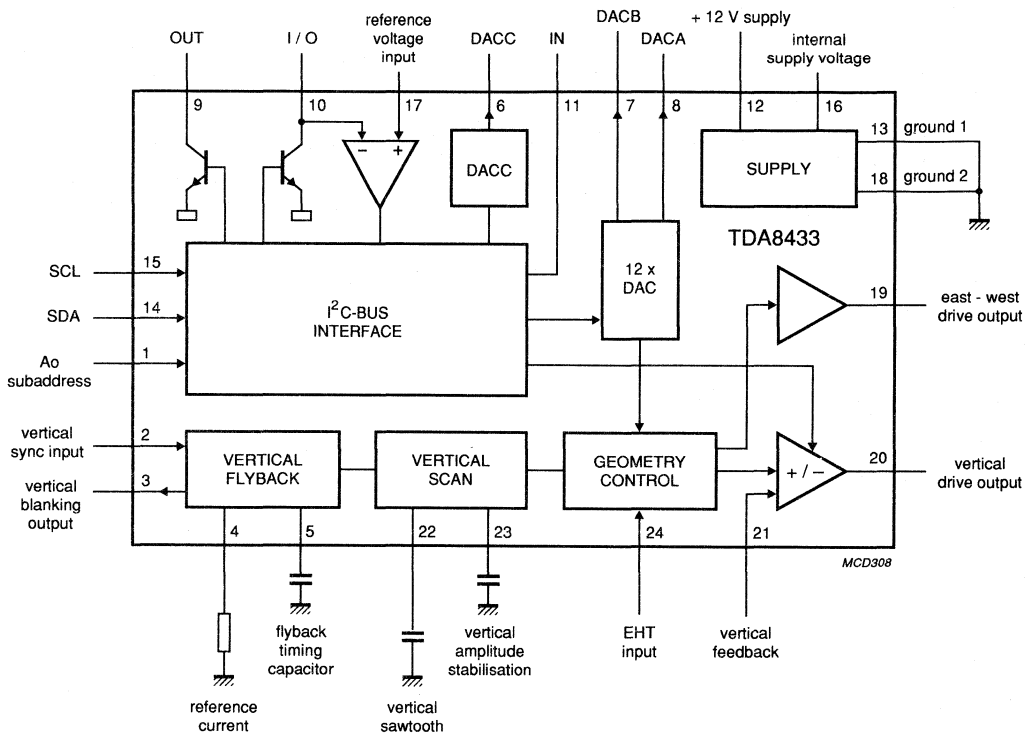


Fig.1 Block diagram.

Deflection processor for computer controlled TV receivers

TDA8433

PINNING

PIN	DESCRIPTION
1	Ao subaddress
2	vertical sync input
3	vertical blanking output
4	I_{ref} resistor
5	vertical blanking/flyback timing capacitor
6	DACC (tau switching)
7	DACB (horizontal phase)
8	DACA (horizontal frequency)
9	OUT (video switch)
10	I/O (f_o adjustment)
11	IN (HLOCKN –50/60 Hz)
12	positive supply +12 V
13	ground 1
14	serial data input
15	serial clock input
16	internal supply voltage
17	voltage reference for I/O
18	ground 2 (waveform)
19	east-west drive output
20	vertical drive output
21	vertical feedback
22	vertical sawtooth capacitor
23	vertical amplitude capacitor
24	EHT input

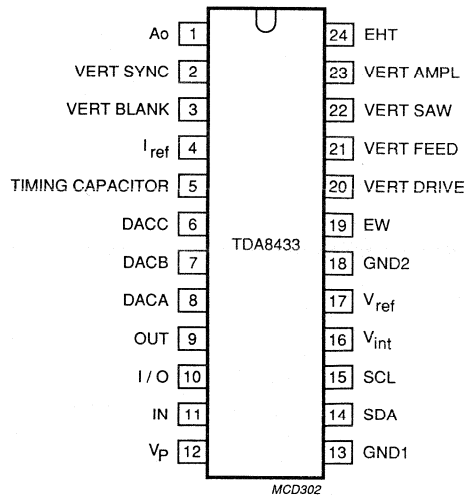


Fig.2 Pinning diagram.

PIN FUNCTIONS

Pin 1 - Ao subaddress

The Ao bit is the least significant bit of the bus-address. It enables two TDA8433s, with different addresses, to be connected to the same bus.

Pin 2 - Vertical sync input

Positive trigger pulses of > 3 V are sufficient to exceed the internal threshold of the ramp generator. Flyback and blanking will then start and, during the blanking period, the circuit will be inhibited for further input pulses (see Fig.3). It should be noted that the TDA8433 has no vertical oscillator therefore, the sync processor, which is used in this combination, has to provide trigger pulses as well when the video input is absent.

Pin 3 - Vertical blanking

The positive going blanking pulse is fed from a current source. The blanking period is fixed by the capacitor connected to pin 5 and the resistor connected to pin 4 (see Fig.3).

Pins 4 and 5 - Reference/flyback timing

The external resistor connected between pin 4 and ground provides a reference current for the triangle generator circuit. This circuit generates the triangle waveform at pin 5. The width of the blanking pulse is set by the external capacitor connected to pin 5.

Pin 6 - DACC (tau switching)

The output voltage, which depends on the VTRA and VTRC bits in the I²C-bus control register, is connected to the coincidence detector of the sync processor. In this way the time constants of the horizontal PLL (in the sync processor) can be set. If the TDA2579 is used (see Fig.6) the effect will be as listed in Table 1.

Table 1 Sync processor time constants

VTRA	VTRC	OUTPUT	TIME CONSTANT
'0'	'0'	12 V	automatic operation
'0'	'1'	5.3 V	medium
'1'	'0'	1.5 V	fast (video recorder)
'1'	'1'	0.2 V	not to be used

Pin 7 - DACB (horizontal phase)

The voltage at pin 7 is fed to the horizontal pulse modulator in the sync processor. This voltage, together with the signal produced by the phase 2 detector during horizontal flyback, sets the phase of the horizontal output with respect to the flyback pulse in the horizontal output stage. The voltage range is variable between 0.05 V and 10 V.

Pin 8 - DACA (horizontal frequency)

The frequency of the horizontal oscillator in the external sync processor is adjusted by the voltage level at pin 8. The voltage is variable in 63 steps from 0.05 V to 10 V (i.e. 0.158 V per step).

Pin 9 - OUT (video switch)

The output at pin 9 is controlled by the CVBS bit from the control register where

CVBS = logic 0; the output is HIGH (open collector)

CVBS = logic 1; the output is LOW (saturation voltage)

An external video selector can be controlled by means of this switching function.

Pins 10 and 17 - I/O and Voltage reference

Pin 10 is connected to the output of the phase 1 detector in the sync processor. Whether the pin is used as an input or an output is dependent on the PHI1 bit of the horizontal frequency (HFREQ) register. When PHI = logic 0 (output transistor open) pin 10 is used as an input. The DC information at this pin is compared with the reference voltage at pin 17 and is reflected in the HCENT of the status register.

HCENT = logic 0; input > V_{ref} at V_{17}
HCENT = logic 1; input < V_{ref} at V_{17}

In this way the free running frequency can be adjusted by computer while the oscillator is locked. Alternatively, when PHI1 = logic 1, pin 10 is switched to ground. The free running frequency of the oscillator can the be adjusted while watching the screen provided that pin 10 is connected to the video input of the sync processor.

Pin 11 -IN (HLOCKN and 50/60 Hz)

This pin is connected to the combined MUTE and 50/60 Hz pin of the sync processor. The various DC levels define the state of the HLOCKN and 50/60 Hz bits in the status register (see Table 2.)

Table 2 Status register bits

STATE OF SYNC PROCESSOR (TDA2579)	TYPICAL VOLTAGE AT PIN 11	STATE OF	
		HLOCKN	50/60 Hz
Not locked to computer video	< 0.7 V(min.)	'1'	'0'
60 Hz transmitter found	0.7 to 0.75 V_{CC}	'0'	'0'
50 Hz transmitter found	> 0.75 V_{CC} to V_{CC}	'0'	'1'

Pin 12 - Positive supply (12 V)

The nominal supply voltage at pin 12 is 12 V which should remain within the defined limits. The nominal current consumption is 20 mA.

Pins 13 and 18 - Ground (1 and 2)

Ground 1 (pin 13) is for the bus transceiver section
Ground 2 (pin 18) is for the sawtooth and picture geometry control section.

Pins 14 and 15 - SDA and SCL (serial data and serial clock)

Input serial data is applied to pin 14. The serial clock input from the I²C-bus is applied to pin 15.

Pin 16 - Internal supply voltage (+5 V)

In some applications it may be necessary to connect a capacitor to this pin to avoid interference.

Pin 19 - East-west drive output

The output drive for the East-west correction circuit has a nominal range from 1.6 to 11.7 V and contains 5 programmable parameters (see Fig.5). The parameters are:

- Picture width
- East-west raster correction
- East-west trapezium correction
- East-west corner correction
- Compensation for EHT variations

Pins 20 and 21 - Vertical drive output and vertical feedback input

The vertical comparator and drive output stage is designed so that the feedback signal applied to pin 21 can be inverted in the comparator by the V-out control bit. This enables the use of two different vertical output stages.
One output stage is without an internal comparator (e.g. TDA3654). The feedback signal at pin 21 has a negative slope during scan. During power-up the IC is adapted (preset) for this type of output stage.
The other output stage contains a comparator. The drive for this output stage is obtained by interconnecting pins 20 and 21 and switching the V-out polarity. The V-out bit will then be set to logic 1.
In both cases the drive signal available at pin 20 contains 5 parameters which can be set via the I²C-bus control;

- Picture hight
- Vertical linearity
- Vertical S-correction
- Vertical shift
- Extent of compensation for EHT variations (see Fig.4.)

Pins 22 and 23 - Vertical sawtooth/vertical amplitude capacitor

The 100 nF capacitor connected to pin 22 is charged and discharged by two current sources in the vertical ramp generator. In order to obtain an equal amplitude, at different frequencies, an amplitude comparator has been incorporated. The circuit, together with the 330 nF capacitor connected to pin 23, keeps the sawtooth amplitude at reference voltage level (7.1 V). The external load of the amplitude stabilization loop of pin 23 should be as low as possible. The recommended value is ≥ 500 MΩ.

Pin 24 - EHT input (Modulation)

A voltage between 1.7 and 6 V (depending on the EHT variations) applied to pin 24 will modulate the amplitude of the vertical drive sawtooth and the East-west drive output. In this way the effect of beam current variations can be virtually eliminated.

I²C-BUS CONTROL

The addresses for the I²C-bus are 100011Ao0 (write) and 100011Ao1 (read). The inclusion of the Ao bit makes it possible to control two different deflection processors. After receiving the address byte the I²C-bus transmits its status byte in which the status of the control bits is contained.

PONRES - Power-on-reset

After switch-on, or a power dip below 6.7 V, the PONRES bit is set to logic 1. After a status read operation PONRES is reset to logic 0.

HLOCKN - Horizontal lock

This bit indicates whether the horizontal oscillator in the sync processor is locked to the video signal. When the oscillator is locked HLOCKN is set to logic 0 (V_{11} > 0.7 V). When the oscillator is not locked HLOCKN is set to logic 1 (V_{11} < 0.7 V).

HCENT - Horizontal centre

This bit is set to logic 0 when the horizontal oscillator frequency is too high ($V_{10} > V_{ref}$). The bit is set to logic 1 when the frequency is too low $V_{10} < V_{ref}$).

IN - 50/60 Hz

The voltage at pin 11 also contains the 50/60 Hz information where:

logic 0 = ≤ V_{11} 0.75 V_{CC} (60 Hz or no transmitter)
logic 1 = ≥ V_{11} 0.75 V_{CC} (50 Hz)

The sequence of data in the status byte is: PONRES, HLOCKN, 50/60 Hz, 0 0 0 0.

A write operation starts with address byte 100011Ao0. The device is then ready to receive the subaddress byte e.g. trapezium (HEXOA) 00001010 followed by the data byte e.g. HEX20. The DAC will then set the trapezium correction signal into the selected position (see Fig.5). If more data bytes follow within one transmission then, by means of an auto-increment, the next highest subaddress will be selected. Wrap-around occurs after HEXOF.

Table 3 Registers

FUNCTION	SUB ADDR HEX	DATA BITS	PRESET VALUE HEX	SETT HEX	MIN.	TYP.	MAX.	UNIT
H-frequency	00	PHI-X-6	01	00 3F	– 9.5	0.05 10	0.2 11	V V
H-phase	01	6	01	00 3F	– 9.5	0.05 10	0.2 11	V V
Picture height $V_{21/20}$	02	6	01	00 3F	– +15	–19 +19	–22 –	% %
V-linearity	03	6	01	00 3F	0 13	– 17	1 21	% %
V-S correction	04	6	01	00 3F	0 15	– 19	1 –	% %
V-shift	05	6	01	00 3F	+17 –17	+19 –19	+22 +22	% %
V-compensation V_{24} = 1.7 V	06	5	01	00 1F	tbf –8	0 –10	– –12	– %
Picture width	07	6	01	00 3F	– 6.0	1.6 6.6	2.4 7.2	V V
E-W parabola (Reg: 07 = 0)	08	6	01	00 3F	– 7.0	0.07 7.5	0.1 8.5	V V
E-W corner (Reg: 08 = 3F)	09	6	01	00 3F	– 1.7	0 2.2	tbf 2.8	V V
Trapezium Reg: 07 = 00; 08 = 20H	0A	6	01	00 3F	0.75 1.0	1.25 1.9	– –	V V
H-compensation Reg. 07 = 00; 08 = 0; 09 = 00 V_{24} = 1.7 V	0B	5	01	00 1F	0 –	tbf 10	– –	% %

FUNCTION	SUB ADDR HEX	DATA BITS	PRESET VALUE HEX	SETT HEX	MIN.	TYP.	MAX.	UNIT
Not used	0C/0E	–	–		–	–	–	–
Control	0F	X-VOUT	–	40	11.5	11.9	V_{CC}	V
		VTRA–VTRC	–	50	5.0	5.3	5.6	V
		CVBS–X–X–X	–	60	1.2	1.5	1.8	V
				70	0	0.2	0.5	V
				40	5.5	7.5	9.5	kΩ
				50	2.4	3.3	4.2	kΩ
				60	0.7	1.0	1.35	kΩ
				70	–	50	–	Ω
				00	–	–	(VBS)	V
				08	–	–	0.4 (1 mA)	V
PHI1 bit	00	1	–	80	–	–	0.4 (–2 mA)	V
				00	–	–	V_{CC}	V
Not used	10–EF							
Test functions	F0–FF							

Note to Table 3

tbf = value to be fixed.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	10.8	13.2	V
I_{CC}	supply current	12	27	mA
P_{tot}	total power dissipation	–	360	mW
T_{amb}	operating ambient temperature range	–25	+75	°C
T_{stg}	storage temperature range	–55	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	–	35	K/W

CHARACTERISTICS

V_{CC} = 12 V; V_{24} = 1/2 x V_{CC}; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	supply voltage (pin 12)		10.8	12.0	13.2	V
I_{CC}	supply current (pin 12)		12	20	27	mA
Ao subaddresses (pin 1)						
V_1	switching level allowed voltage for Ao = '0' for Ao = '1'	note 1	– – 9	2.3 – –	– 2 V_{CC}	V V V
I_1	input current		–	–	+10	µA
V_1	not allowed voltage range		2.0	–	8.9	V
Vertical sync input (pin 2)						
V_2	switching level		2.5	3.0	3.5	V
I_2	current during non-active state	V_2 = 0 V	–	3	10	µA
Vertical blanking output (pin 3)						
$V_{3(p-p)}$	pulse amplitude (peak-to-peak value)	1 mA load	–	–	V_{CC}–2	V
V_3	output voltage	1 mA load	10.0	10.5	–	V
I_O	output source current		1	–	–	mA
t_W	pulse width	R_4 = 75 kΩ C_5 = 8.2 nF	–	1.13	–	ms
Reference (pin 4)						
V_4	reference voltage		6.8	7.15	7.5	V
I_4	current range		90	–	150	µA
Vertical blanking timing (pin 5)						
$V_{5(p-p)}$	amplitude of triangular pulse (peak-to-peak value)	R_4 = 75 kΩ C_5 = 8.2 nF	7.5	7.9	8.3	V
t_W	width of triangular pulse		–	1.3	–	ms
I_5	sink current	V_5 = 3.5 V; I_4 = 100 µA	85	105	125	µA
I_5	source current	V_5 = 3.5 V; I_4 = 100 µA	80	100	120	µA
DACC output (pin 6)						
V_6	voltages at VTR(A) and VTR(C) where: (A) = '0'; (C) = '0' (A) = '0'; (C) = '1' (A) = '1" (C) = '0' (A) = '1'; (C) = '1'		 11.5 5.0 1.2 0	 11.9 5.3 1.5 0.2	 – 5.6 1.8 0.5	 V V V V

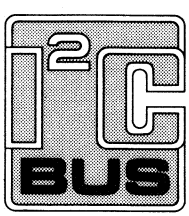
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DACC output (pin 6)						
Z_6	output impedance at VTR(A) and VTR(C) where: (A) = '0'; (C) = '0' (A) = '0'; (C) = '1' (A) = '1'; (C) = '0' (A) = '1'; (C) = '1'		 5.5 2.4 0.7 –	 7.5 3.3 1.0 50	 9.5 4.2 1.35 –	 kΩ kΩ kΩ Ω
DACB horizontal phase (pin 7)						
V_7	output voltage at HEX00 at HEX3F		 – 9.4	 0.05 10.0	 0.2 11.0	 V V
ΔV_7	variable DC output voltage for setting horizontal frequency		0.05	–	10	V
R_7	internal resistance		–	0.3	1.0	kΩ
	step size	note 3	10	–	190	%
RR	ripple rejection		26	–	–	dB
DACA horizontal frequency (pin 8)						
V_8	output voltage at HEX00 at HEX3F		 – 9.5	 0.05 10.0	 0.2 11.0	 V V
ΔV_8	variable DC output voltage for setting horizontal frequency		0.05	–	10	V
R_8	internal resistance		–	0.3	1.0	kΩ
	step size	note 3	10	–	190	%
RR	ripple rejection		26	–	–	dB
OUT video switch (pin 9)						
FOR EXTERNAL CVBS SWITCH WHEN CVBS BIT = 1						
V_9	saturation voltage	I_{sink} = 1 mA	–	–	0.4	V
I_L	leakage current		–	–	2	μA
I/O combined input/output (pin 10)						
V_{10}	when used as an output (open collector) where PHI1 = '0' where PHI1 = '1'		 – –	 – –	 V_{CC} 0.4	 V V
I_{sink}	sink current		–	–	2	mA
V_{10}	when used as an input (switching point HCENT is '0' to '1')	PHI1 = '0'	V_{17} – 35 mV	V_{17}	V_{17} + 35 mV	V
I_{10}	input current		–	–	2	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IN HLOCKN and 50/60 Hz (pin 11)						
V_{11}	HLOCKN switching level		–	0.7	–	V
V_{11}	switching level where: HLOCKN = '0' HLOCKN = '1'		 1.0 –	 – –	 – 0.4	 V V
V_{11}	switching level where: 50/60 Hz = '0' 50/60 Hz = '1'	 state 50 Hz	 – 0.8 V_{CC}	 – –	 0.7 V_{CC} –	 V V
I_{11}	source current		10	25	35	µA
SDA serial data input (pin 14)						
V_{14}	switching level where: SDA = '0' SDA = '1'		 – 3.0	 – –	 1.5 –	 V V
I_{14}	sink current		–	0.5	10	µA
SCL serial clock input (pin 15)						
V_{15}	switching level where: SDA = '0' SDA = '1'		 – 3.0	 – –	 1.5 –	 V V
I_{15}	sink current		–	0.5	10	µA
Internal supply voltage						
V_{16}	maximum allowed load	1 mA load	4.5	5.0	5.5	V
V_{17}	voltage reference for pin 10 (pin 17)		1.0	–	V_{CC} – 1.5	V
I_{17}	input load current		–	–	2.0	µA
E-W drive output (pin 19; see application information)						
V_{19}	output voltage	1 mA load	0.5	–	11.5	V
I_{19}	output current		±1.0	–	±2.0	mA
RR	ripple rejection		24	30	–	dB
R_I	internal resistance		–	1	2	kΩ
t_R	response time		–	2	–	µs
Vertical drive output (pin 20; see application information)						
V_{20}	output voltage	1 mA load	0.5	–	10.5	V
I_{20}	output current		±1.5	±2.0	–	mA
RR	ripple rejection	note 2	35	40	–	dB
	DAC stepsize	note 3	10	–	190	%
Vertical feedback (pin 21; see application information: Register 02 = 20H, 03 = 0, 04 = 0, 05 = 20H, 06 = 0)						
V_{21}	DC input voltage		1.7	1.85	2.05	V
$V_{21(p-p)}$	AC output voltage (peak-to-peak value)	note 2	1.65	1.8	1.95	V
I_{21}	input current		–	–	–3	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical sawtooth voltage (pin 22; see application information)						
V_{22}	top level of sawtooth		6.7	7.1	7.4	V
V_{22}	minimum level of sawtooth	I_{sink} = 0.5 mA	–	–	50	mV
I_{22}	discharge sink current	V_{22} = 3.5 V	6.5	9.5	15	mA
I_{22}	charge source current	V_{23} = 5 V; V_{22} = 3.5 V	1	20	35	µA
I_{22}	control range	5 V to 1 V	80	135	190	µA
$\|Z_{22}\|$	AC impedance		–	3	–	MΩ
C_{EXT}	external capacitance		–	100	–	nF
Vertical sawtooth stabilizer (pin 23; see application information)						
I_{23}	discharge sink current	V_{22} = 2 V	200	250	300	µA
I_{23}	charge source current	V_{22} = 9.75 V	185	235	285	µA
C_{EXT}	external capacitance		–	390	–	nF
I_L	leakage current	note 5	–	–	0.015	µA
EHT modulation input (pin 24; see application information)						
V_{24}	voltage operating range		1/7 V_{CC}	–	1/2 V_{CC}	V
I_{24}	input current		–	0.5	2.0	µA

Notes to the characteristics

1. Outside the test mode.
2. Test condition (hex values): register 02 = 3F; 03 = 00; 04 = 00; 05 = 20; 06 = 00; V_{22} = 1/2 V_4; f = 50 Hz to 30 kHz.
3. $\frac{Value\ StepN - Value\ StepN{-}1}{average\ step\ size} \times 100\%$ (63>*N*>1).
4. Applies to both modes.
5. External load of this pin (leakage current capacitor etc.) should be ≥ 500 MΩ.



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

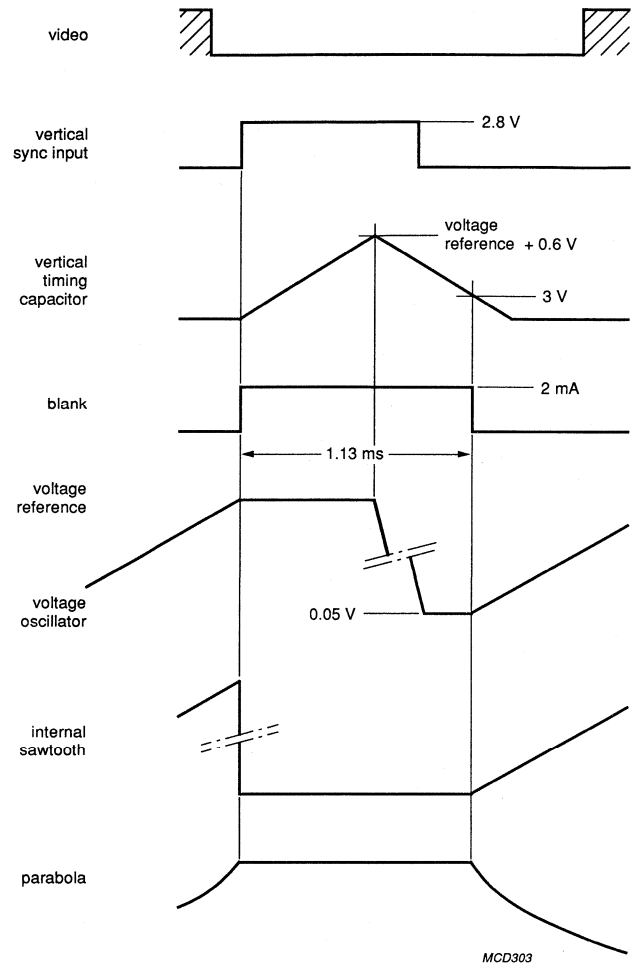


Fig.3 Vertical sawtooth timing.

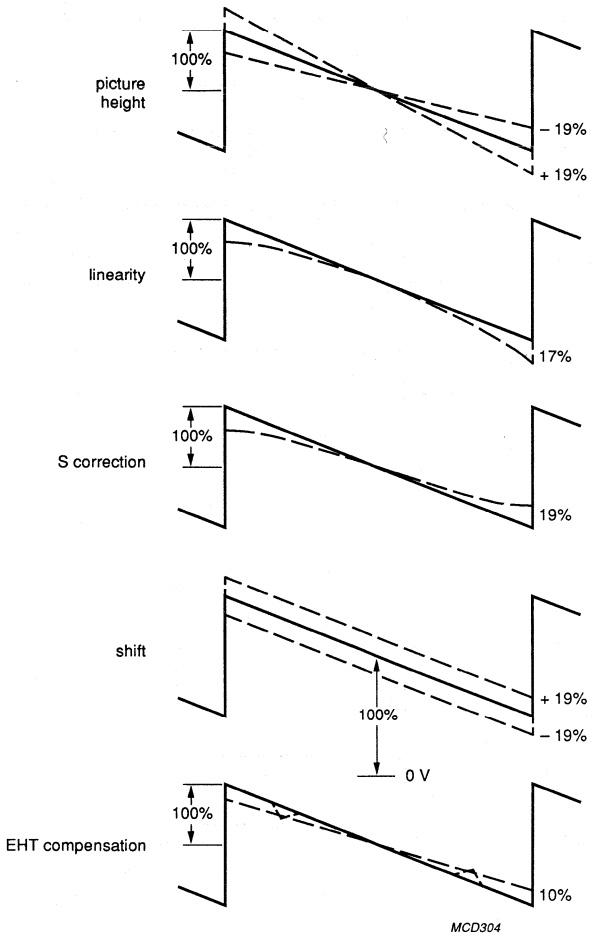


Fig.4 Vertical raster-corrections.

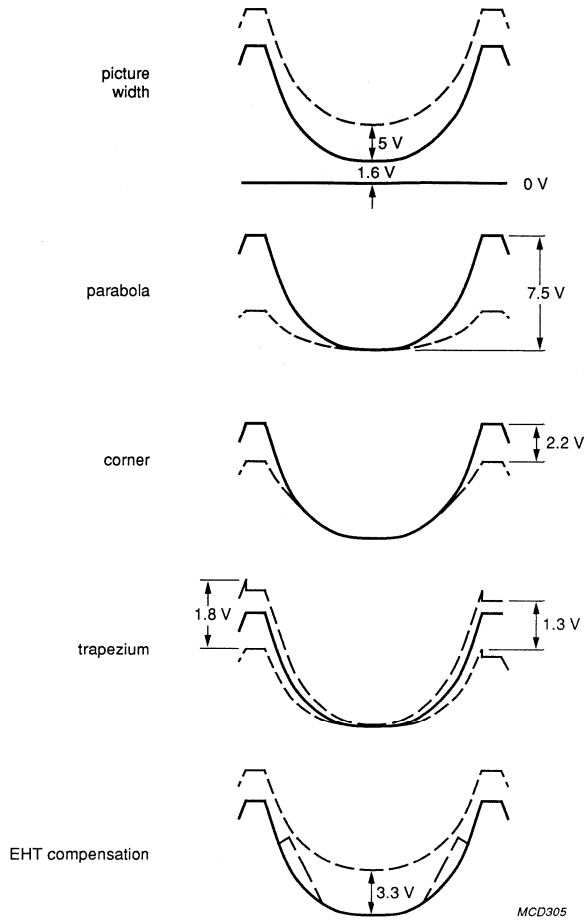


Fig.5 East-west raster-corrections.

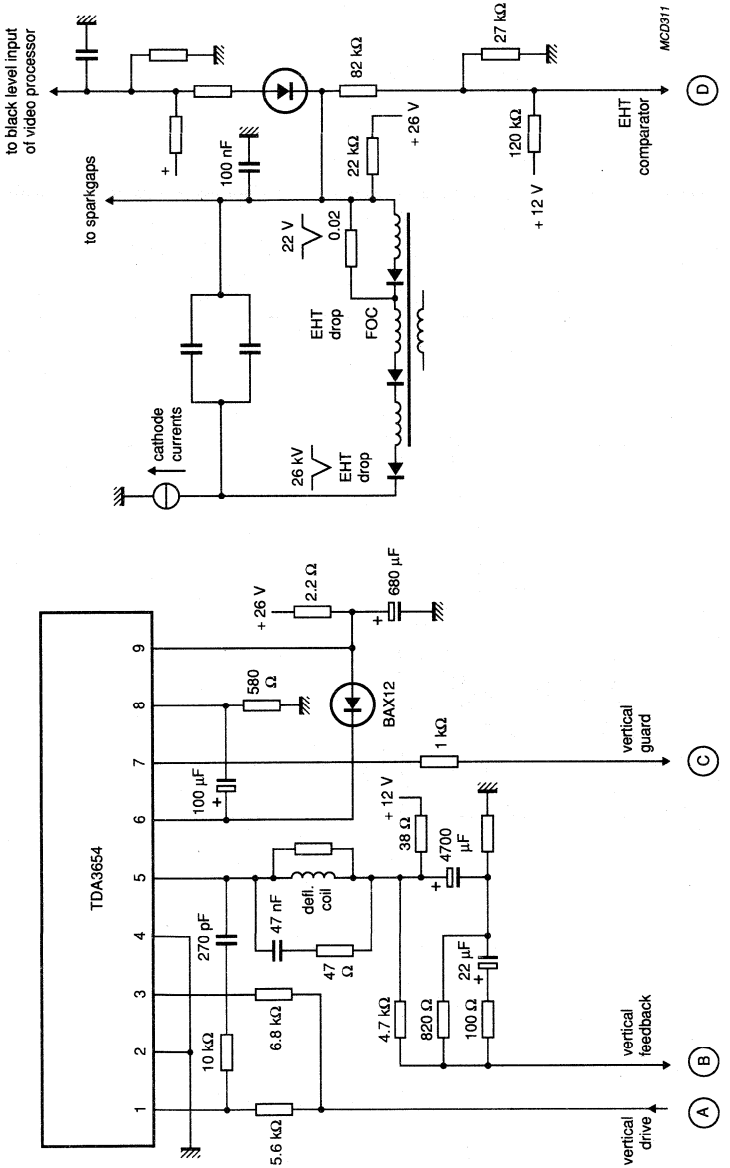


Fig.6 Application diagram (continued in Fig.7).

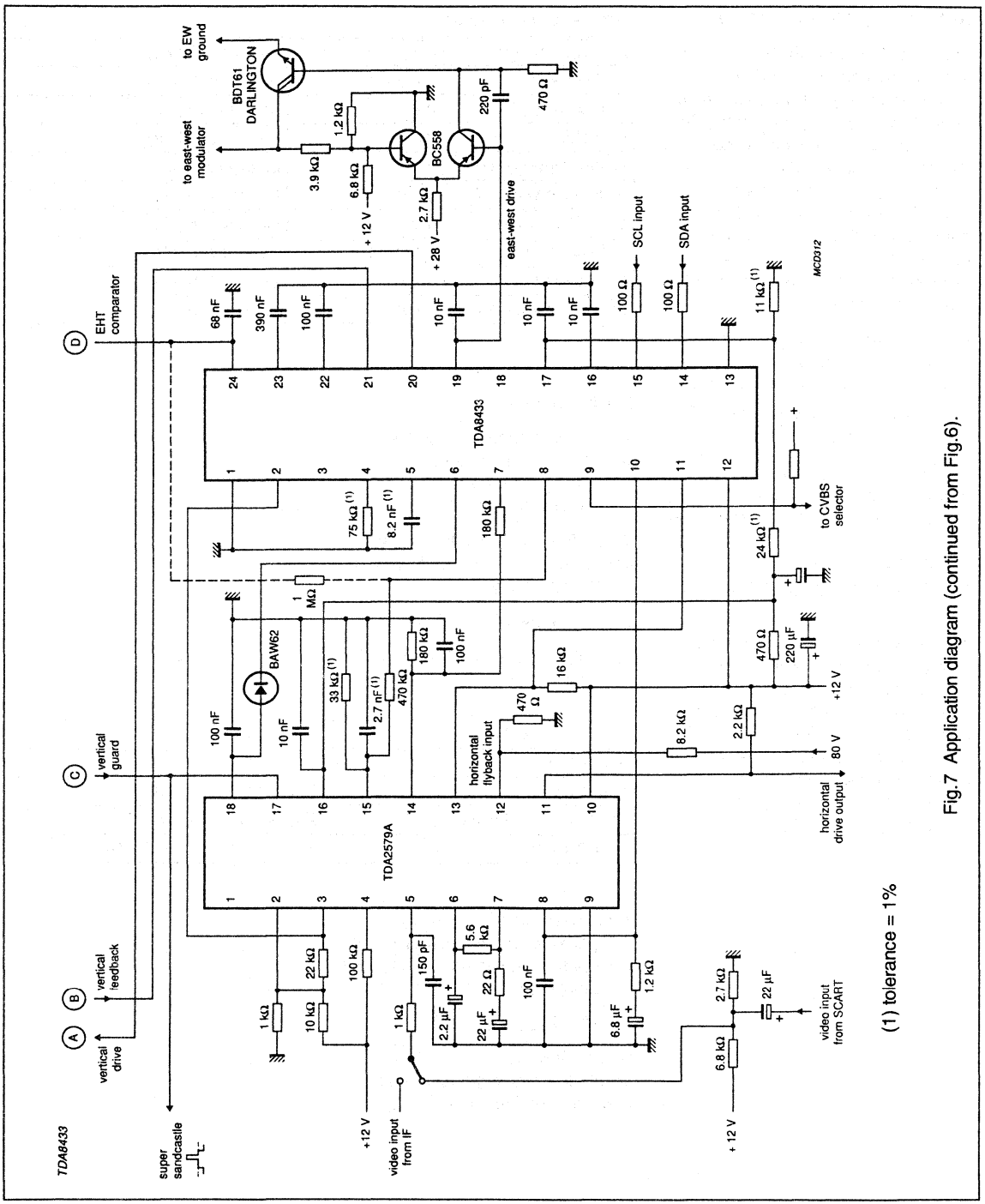


Fig.7 Application diagram (continued from Fig.6).

(1) tolerance = 1%

APPLICATION INFORMATION

The formulae from which the typical vertical drive and typical E-W drive waveforms are generated are given in the following sub-paragraphs. For this purpose a typical application diagram for the vertical drive stage is assumed to be as illustrated in Fig.7. Pin 20 is the vertical drive output which drives an inverting power amplifier. The feedback network, R1 to R4 and C1 and C2, has two functions;

- To transfer the voltage on the feedback pin (pin 21) to a voltage across the feedback resistor R1
- To stabilize the voltage across C1 at a fixed value.

For this typical application the formula for the vertical scan waveform refers to the voltage at pin 21.
The formula for the E-W drive waveform refers to the voltage at pin 19.

All DAC variables that control the vertical and E-W drive waveforms are normalized. Each DAC is defined as having a control range between 0 and 1. The 0 corresponds to a register value of HEX00 and the 1 to a maximum value of HEX1F (for a 5-bit DAC) or HEX3F (for a 6-bit DAC).

Table 4 DAC variables

a: Picture height	$0 < a < 1$	64 steps (6 bits)
y: V-linearity	$0 < y < 1$	64 steps (6 bits)
s: V-S correction	$0 < s < 1$	64 steps (6 bits)
d: V-shift	$0 < d < 1$	64 steps (6 bits)
v: V-compensation	$0 < v < 1$	32 steps (5 bits)
w: Picture width	$0 < w < 1$	64 steps (6 bits)
p: E-W parabola	$0 < p < 1$	64 steps (6 bits)
c: E-W corner	$0 < c < 1$	64 steps (6 bits)
t: Trapezium	$0 < t < 1$	64 steps (6 bits)
h: H-compensation	$0 < h < 1$	32 steps (5 bits)

Further definitions

V_{SAW} = Instantaneous sawtooth voltage (pin 22) normally; $V_{saw} > 0$ $V_{saw} < 7.1$ V; V_{CC} = supply voltage applied to pin 12.

V_{EHT} = EHT compensation voltage applied to pin 1, normally between 1/2 V_{CC} and 1/7 V_{CC}.

V_{OFF} = Internal offset voltage.

V_{int} = Internal reference voltage of 7.1 V (also on pin 4)

$A = 0.80\ (a + 2)/3$	$P = 0.55\ p$
$Y = 0.17\ y$	$C = 0.38\ c$
$S = 0.42\ s$	$T = 0.32\ (1 + 2t)$ volts
$D = 2.4 - 0.7\ d$ volts	$E = (V_{CC} / 2 - V_{EHT}) / 42$
$W = 0.16\ w$	$Z = -1 + 2 \times (V_{saw} - T)\ V_{int}$

If the Trapezium function (T) compensates for the internal offset voltage then the actual formula for Z will simplify to:

$Z = -1 + 2V_{saw}/V_{int}$

Since $0\ V < V_{SAW} < 7.1$ V, this is simply a negative going sawtooth and it follows that: $-1 < Z < 1$.

Vertical drive waveform

The vertical drive waveform has certain interactions between the parameters whereby:

- The S-correction influences the picture height
- The linearity correction can influence the picture shift.

The alignment can be made non-repetitive. Once correct values for the V-S correction and V-linearity are set, the picture height may be changed without affecting the V-S correction and V-linearity on the screen.
The formula for the vertical drive waveform at pin 21 is:

$V_{vert} = D + 1.32\ A\ \{(Z - SA^2\ Z^3)\ (1 - VE) + YZ^2\}$ volts.

Picture height

The amplitude of the sawtooth waveform is controlled by 'A'. It follows therefore that:

$0.53 < A < 0.8$

The nominal value for 'A' is found for a = 0.5, therefore A = 0.67. By programming the picture height, the sawtooth amplitude can be adjusted from –19% to +19%. Without S-correction (S = O) and linearity correction (Y = O), the nominal sawtooth amplitude is (with A = 0.67);

$1.32 \times 0.67 \times 2 = 1.77\ V_{(p\text{-}p)}$

V-linearity

This function is meant to compensate for non-linearity of AC coupled vertical output stages. The linearity correction changes proportionally to the picture height setting. The range for linearity control is typically 17% of the peak-to-peak value of the linear sawtooth (see Fig.7).

V-S correction

The range for the V-S correction (SA^2) is defined as a percentage of the undistorted peak-to-peak sawtooth voltage (see Fig.7). The actual S-correction component (SA^2) is dependent on the the picture height setting where:

At maximum picture height (A = 0.80) : $SA^2 = 0.282$
At nominal picture height (A = 0.62) : $SA^2 = 0.197$
At minimum picture height (A = 0.53) : $SA^2 = 0.125$

Picture shift

The DC level of the output is fixed by 'D'. It can be adjusted within a range of –19% to +19%. In actual application this will be used for shifting the picture vertically.

V-compensation

The vertical deflection can be modulated by the instantaneous value of the signal applied to the EHT compensation input. This external signal should reflect the EHT variations. The amount of deflection reduction is in the range 0 to 10%, if pin 24 is at $(V_{CC} / 2) - 4.3$ V (maximum modulation i.e. 1.7 V typical). Thus for maximum modulation, the V-drive waveform can be reduced to 90% of its value. There is no reduction when the EHT-compensation input is at $V_{CC} / 2$ V (i.e. 6 V typical).

Trapezium

The trapezium function is the only IC-confined adjustment and is intended to compensate for any internal offsets. The function is called Trapezium because of its effect on the picture if an AC-coupled vertical deflection stage is used. The trapezium function can alter the picture shift range by a maximum of 190 mV. If the trapezium function is used for purposes other than eliminating the internal offsets, then the V-linearity can affect the actual picture height. This can affect the symmetry of the S-correction which, in turn, can affect the V-linearity.

E-W drive waveform

In order to obtain independent control of the picture width, parabola function and th H-compensation on a screen each function has been designed to be dependent on the other two. With reference to Fig.8, the voltage across the H-deflection stage is:

$V_{def1} = V_{supply}\ (1 - W)\ (1 - P)\ (1 - E)$

Where:

V_{supply}	=	supply voltage for H-deflection stage
W	=	picture width alignment
P	=	parabola function
E	=	H-compensation

This shows for instance, that the H-compensation is made dependent on the actual value of the parabola function. For a TV set which needs a large parabola compensation and, also, a large EHT-compensation, this function allows an optimal EHT-compensation independent of the parabola function.
All correction voltages are related to the supply voltage. The TDA8433 is designed to accept a supply voltage of 30 V. Normally higher voltages are employed therefore a voltage amplifier, with a gain of $V_{supply}/30$, is used between the TDA8433 and the diode modulator.

The formula for the E-W drive output voltage at pin 19 is:

$$V_{E\text{-}W} = 30 \times \{1 - (1 - W)(1 - PA^2 Z^2 + CA^4 Z^4)(1 - 1.1 \times hE)\} + 1.8 \text{ V}$$

As can be seen from the formula, the picture width, parabola function and H-compensation are influenced by each other. The functions are discussed separately with the other compensations set to zero.

Picture width control (P-C-h-O)

It is possible to change the picture width by adjusting 'W' from 0 to 0.16. Thus the complete range for the picture control width is −10 to +10%. By only changing the picture width control the output voltage at pin 19 can vary between 1.8 and 6.6 V typical.

Parabola function

The parabola function is also dependent on the picture height function. The values given are valid for a nominal height setting (A = 0.67 V). The parabola function consists of two parts:

- A parabola part - E-W parabola is created by squaring a linear sawtooth. The range of this pure parabola varies from 0 to 25% typical i.e. the amplitude of the parabola waveform is programmable from 0 to 7.5 V (typical).
- A fourth order part - E-W corner is created by squaring the parabola. The range of this corner correction varies from 0 to 7% (typical) i.e. the amplitude of the corner correction waveform is programmable from 0 to −2.2 V (typical). A negative output voltage is not possible. The E-W corner correction waveform has to be subtracted from one of the other alignment functions.

The split-up into the E-W parabola and the E-W corner enables each television set to be aligned with straight vertical lines. The trapezium is also related to the parabola function. The main reason for the trapezium correction is to compensate for internal offsets in the geometry control part. Therefore:

- The amount of trapezium correction is fully dependent on the amount of parabola correction and corner correction that is needed. With no parabola and corner correction the trapezium output will be zero.
- The maximum possible trapezium output is 1.6 V (typical - see Fig.7). This is the case where: a = 0.5, c = 0 and p = 1 i.e. no corner correction and the maximum parabola correction at nominal picture height settings.

H-compensation control

The horizontal deflection can be modulated by the instantaneous value of the signal applied to the EHT compensation input. This external signal should reflect the EHT variations. The amount of deflection reduction is in the range 0 to 10% if the input at pin 7 is at $(V_{supply}/2) - 4.3$ V (maximum modulation is 1.7 V typical). With maximum modulation this range corresponds to an output voltage of 0 to 3.3 V. There is no reduction when the EHT-compensation input is at $V_{supply}/2$ V (typical 6 V).

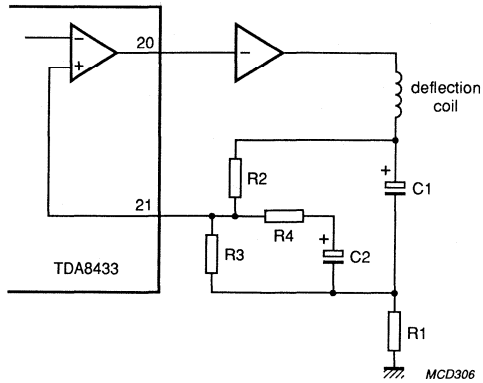


Fig.8 Application diagram of an AC coupled amplifier stage.

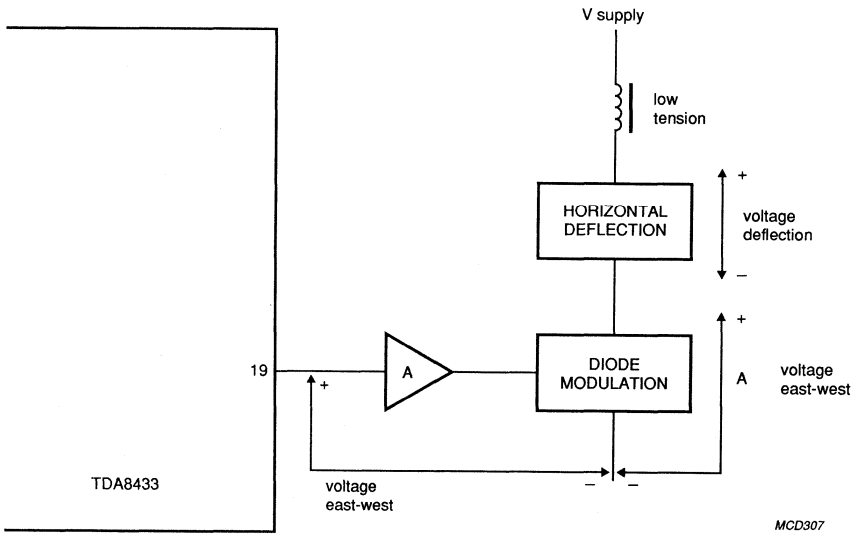


Fig.9 Application diagram for driving the diode modulator.

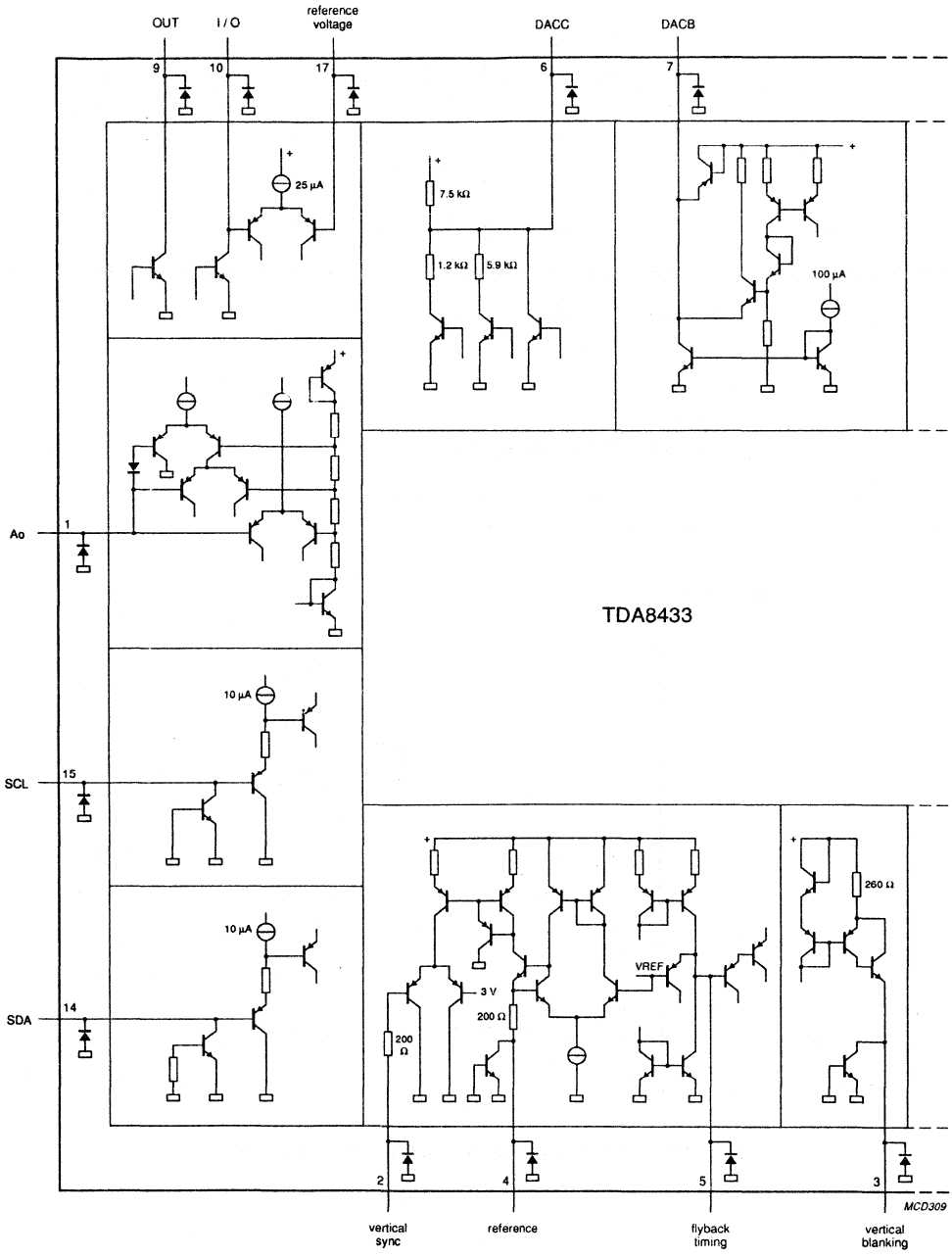


Fig.10 Input/output pin-configuration of TDA8433 (continued in Fig.11).

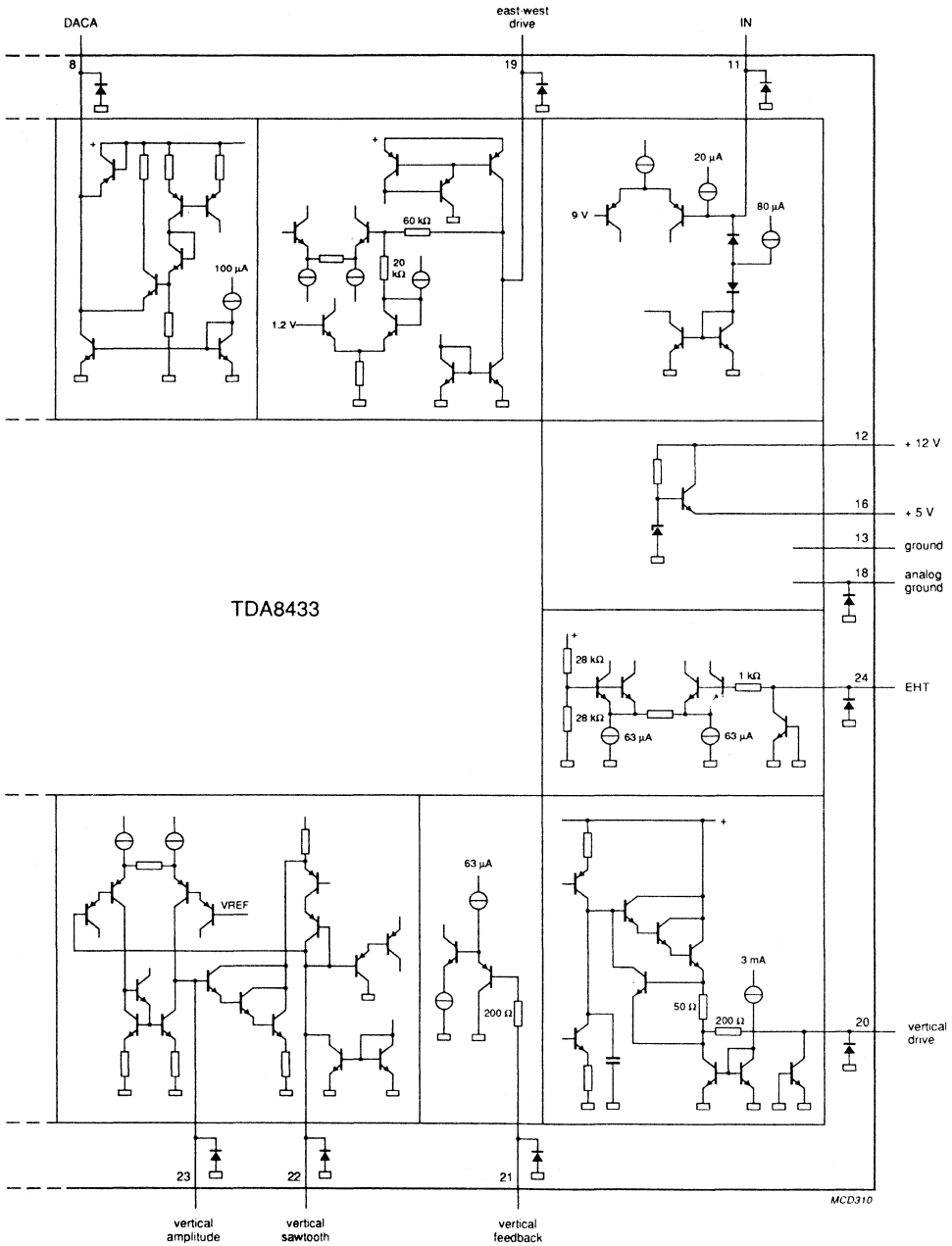


Fig.11 Input/output pin-configuration of TDA8433 (continued from Fig.10).

SWITCH FOR CTV RECEIVERS

GENERAL DESCRIPTION

The TDA8440 is a versatile video/audio switch, intended to be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

It provides two 3-state switches for audio channels and one 3-state switch for the video channel and a video amplifier with selectable gain (times 1 or times 2).

The integrated circuit can be used in conjunction with a microcontroller from the MAB8400 family, and is controlled via a bidirectional I^2C bus. Sufficient sub-addressing is provided for the I^2C bus mode. It can also be controlled directly by d.c. switching signals.

Features

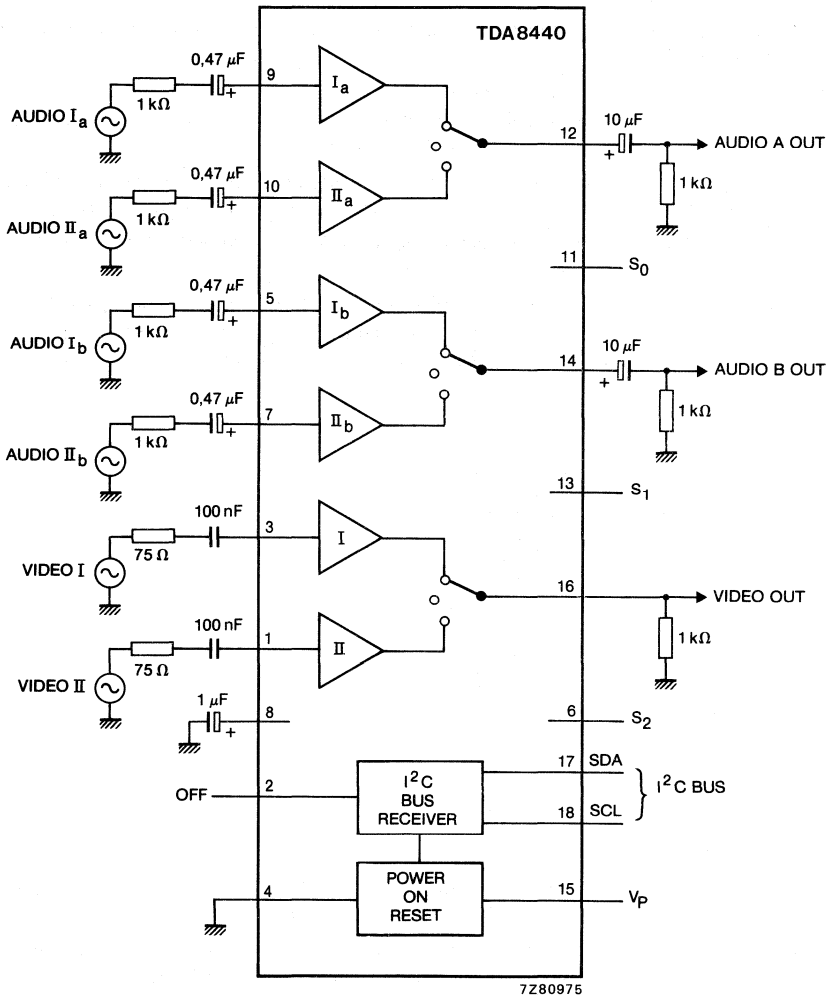
- Combined analogue and digital circuitry gives maximum flexibility in channel switching
- 3-state switches for all channels
- Selectable gain for the video channels
- Sub-addressing facility
- I^2C bus or non-I^2C bus mode (controlled by d.c. voltages)
- Slave receiver in the I^2C bus mode
- External OFF command
- System expansion possible up to 7 devices (14 sources)
- Static short-circuit proof outputs

QUICK REFERENCE DATA

Supply voltage range	V_{15-4}	10 to 13,2	V
Supply current (without load)	I_{15}	typ. 33 max. 50	mA mA
Storage temperature	T_{stg}	max. + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



S0, S1, S2 and OFF (pins 11, 13, 6 and 2) connected to V_P or GND.
If more than 1 device is used, then the outputs and the pins 8 (bias decoupling of the audio inputs) mau may be connected in parallel.

Fig. 1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

The TDA8440 is a monolithic system of switches and can be used in CTV receivers equipped with an AUXILIARY VIDEO/AUDIO plug.

The IC incorporates 3-state switches they comprise:

a) An electronic video switch with selectable gain (times 1 or times 2) for switching between an internal video signal (from the IF amplifier) and an AUXILIARY input signal.

b) Two electronic audio switches, for two sound channels (stereo or dual language), for switching between internal audio sources and signals from the AUXILIARY VIDEO/AUDIO plug.

A selection can be made between two input signals and an OFF-state. The OFF-state is necessary if more than one TDA8440 device is used.

The SDA and SCL pins can be connected to the I^2C bus or to d.c. switching voltages. Inputs S_0 (pin 11), S_1 (pin 13), and S_2 (pin 6) are used for selection of sub-addresses or switching to the non-I^2C mode. Inputs S_0, S_1 and S_2 can be connected to the supply voltage (H) or to ground (L). In this way no peripheral components are required for selection.

Table 1 Sub-addressing

			sub-address		
S_2	S_1	S_0	A_2	A_1	A_0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I^2C addressable		

NON-I^2C BUS CONTROL

If the TDA8440 switching device has to be operated via the AUXILIARY VIDEO/AUDIO plug, inputs S_2, S_1 and S_0 must be connected to the supply line (12 V).

The sources (internal and external) and the gain of the video amplifier can be selected via the SDA and SCL pins with the switching voltage from the AUXILIARY VIDEO/AUDIO plug:

- Sources I are selected if SDA = 12 V (external source)
- Sources II are selected if SDA = 0 V (TV mode)
- Video amplifier gain is 2 x if SCL = 12 V (external source)
- Video amplifier gain is 1 x if SCL = 0 V (TV mode)

If more than one TDA8440 device is used in the non-I^2C bus system, the OFF pin can be used to switch off the desired devices. This can be done via the 12 V switching voltage on the AUXILIARY VIDEO/AUDIO plug.

- All switches are in the OFF position if OFF = H (12 V)
- All switches are in the selected position via SDA and SCL pins if OFF = L (0 V)

I²C BUS CONTROL

Detailed information on the I²C bus is available on request.

Table 2 TDA8440 I²C bus protocol.

STA	A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W	AC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	AC	STO

STA = start condition
A_6 = 1, A_5 = 0, A_4 = 0, A_3 = 1 } Fixed address bits
A_2 = sub-address bit, fixed via S_2 input
A_1 = sub-address bit, fixed via S_1 input
A_0 = sub-address bit, fixed via S_0 input
R/W = read/write bit (has to be 0, only write mode allowed)
AC = acknowledge bit (= 0) generated by the TDA8440
D_7 = 1 audio Ia is selected to audio output a
D_7 = 0 audio Ia is not selected
D_6 = 1 audio IIa is selected to audio output a
D_6 = 0 audio IIa is not selected
D_5 = 1 audio Ib is selected to audio output b
D_5 = 0 audio Ib output is not selected
D_4 = 1 audio IIb is selected to audio output b
D_4 = 0 audio IIb is not selected
D_3 = 1 video I is selected to video output
D_3 = 0 video I is not selected
D_2 = 1 video II is selected to video output
D_2 = 0 video II is not selected
D_1 = 1 video amplifier gain is times 2
D_1 = 0 video amplifier gain is times 1
D_0 = 1 OFF-input inactive
D_0 = 0 OFF-input active
STO = stop condition

OFF FUNCTION

With the OFF input all outputs can be switched off (mode high ohmic), depending on the value of D_0.

D_0/OFF gating

D_0	OFF input	Outputs
0 (off input active)	H	OFF
0	L	in accordance with last defined D_7-D_1 (may be entered while OFF = HIGH)
1 (off input inactive)	H	in accordance with D_7-D_1
1	L	in accordance with D_7-D_1

Power-on reset

The circuit is provided with a power-on reset function.

When the power supply is switched on an internal pulse will be generated that will reset the internal memory S_0, in the initial state all the switches will be in the off position and the OFF input is active (D_7-D_0 = 0) (I^2C mode), position defined via SDA and SCL inputs (non-I^2C mode).

When the power supply decreases below 5 V a pulse will be generated and the internal memory will be reset. The behaviour of the switches will be the same as described above.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		min.	typ.	max.	unit
Supply voltage	pin 15 V_P	–	–	14	V
Input voltage range	pin 17 V_{SDA}	−0,3	–	V_P + 0,3	V
	pin 18 V_{SCL}	−0,3	–	V_P + 0,3	V
	pin 2 V_{OFF}	−0,3	–	V_P + 0,3	V
	pin 11 V_{S0}	−0,3	–	V_P + 0,3	V
	pin 13 V_{S1}	−0,3	–	V_P + 0,3	V
	pin 6 V_{S2}	−0,3	–	V_P + 0,3	V
Video output current	pin 16 $-I_{16}$	–	–	50	mA
Storage temperature range	T_{stg}	–	–	+ 125	°C
Operating ambient temperature range	T_{amb}	0	–	+ 70	°C
Junction temperature	T_j	–	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=		50	K/W

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{15-4}	10	–	13,2	V
Supply current (without load)	I_{15}	–	37	50	mA
Video switch					
Input coupling capacitor	C_1C_3	100	–	–	nF
Voltage gain (times 1; SLC = L)	A_{3-16}	−1	0	+ 1	dB
(times 2; SCL = H)	A_{3-16}	+5	+ 6	+ 7	dB
Voltage gain (times 1; SCL = L)	A_{1-16}	−1	0	+ 1	dB
(times 2; SCL = H)	A_{1-16}	+5	+ 6	+ 7	dB
Input video signal amplitude (gain times 1)	V_{3-4}	–	–	4,5	V
Input video signal amplitude (gain times 1)	V_{1-4}	–	–	4,5	V
Output impedance	Z_{16-4}	–	7	–	Ω
Output impedance in 'OFF' state	Z_{16-4}	100	–	–	kΩ
Isolation (off state) (f_o = 5 MHz)		60	–	–	dB
Signal-to-noise ratio (note 2)	S/S + N	60	–	–	dB
Output top-sync level	V_{16-4}	2,4	2,8	3,2	V
Differential gain	G	–	–	3	%
Minimum crosstalk attenuation (note 1)	V_{16-4}	60	–	–	dB
Supply voltage rejection (note 3)	RR	36	–	–	dB
Bandwidth (1 dB)	B	10	–	–	MHz
Crosstalk attenuation for interference caused by bus signals (source impedance 75 Ω)	α	60	–	–	dB
Audio switch a and b					
Input signal level	$V_{9-4(rms)}$	–	–	2	V
	$V_{10-4(rms)}$	–	–	2	V
	$V_{5-4(rms)}$	–	–	2	V
	$V_{7-4(rms)}$	–	–	2	V
Input impedance	Z_{9-4}	50	100	–	kΩ
	Z_{10-4}	50	100	–	kΩ
	Z_{5-4}	50	100	–	kΩ
	Z_{7-4}	50	100	–	kΩ
Output impedance	Z_{12-4}	–	–	10	Ω
	Z_{14-4}	–	–	10	Ω
Output impedance (off state)	Z_{14-4}	100	–	–	kΩ

parameter	symbol	min.	typ.	max.	unit
Voltage gain	$V_{9\text{-}12}$	−1	0	+ 1	dB
	$V_{10\text{-}12}$	−1	0	+ 1	dB
	$V_{5\text{-}14}$	−1	0	+ 1	dB
	$V_{7\text{-}14}$	−1	0	+ 1	dB
Isolation (off state) (f = 20 kHz)		90	–	–	dB
Signal-to-noise ratio (note 4)	S/S + N	90	–	–	dB
Total harmonic distortion (note 6)	THD	–	–	0,1	%
Crosstalk attenuation for interferences caused by video signals (note 5)					
Weighted	α	80	–	–	dB
Unweighted	α	80	–	–	dB
Crosstalk attenuation for interferences caused by sinusoidal sound signals (note 5)	α	80	–	–	dB
Crosstalk attenuation for interferences caused by the bus signal (weighted) (source impedance = 1 kΩ)		80	–	–	dB
Supply voltage rejection	RR	50	–	–	dB
Bandwidth (−1 dB)	B	50	–	–	kHz
I^2C bus inputs/outputs SDA (pin 17) and SCL (pin 18)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 1,5	V
Input current HIGH*	I_{IH}	–	–	10	μA
Input current LOW*	I_{IL}	–	–	10	μA
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Capacitance of SDA and SDL inputs, pins 17 and 18	C_I	–	–	10	pF
Sub-address inputs S_0 (pin 11), S_1 (pin 13), S_2 (pin 6)					
Input voltage HIGH	V_{IH}	3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	10	μA
Input current LOW	I_{IL}	−50	–	0	μA
OFF input (pin 2)					
Input voltage HIGH	V_{IH}	+3	–	V_P	V
Input voltage LOW	V_{IL}	−0,3	–	+ 0,4	V
Input current HIGH	I_{IH}	–	–	20	μA
Input current LOW	I_{IL}	−10	–	2	μA

* Also if the supply is switched off.

CHARACTERISTICS (continued)

I^2C bus load conditions are as follows:
4 kΩ pull-up resistor to + 5 V; 200 pF to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{s(STA)}$	4	–	–	μs
Start condition hold time	$t_{h(STA)}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL, HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_r	–	–	1	μs
SCL, SDA fall time	t_f	–	–	0,3	μs
Data set-up time (write)	$t_{s(DAT)}$	1	–	–	μs
Data hold time (write)	$t_{h(DAT)}$	1	–	–	μs
Acknowledge (from TDA8440) set-up time	$t_{s(CAC)}$	–	–	2	μs
Acknowledge (from TDA8440) hold time	$t_{h(CAC)}$	0	–	–	μs
Stop condition set-up time	$t_{s(STO)}$	4	–	–	μs

Notes to the characteristics

1. Caused by drive on any other input at maximum level, measured in B = 5 MHz, source impedance for the used input 75 Ω,

   $$\text{crosstalk} = 20 \log \frac{V_{out}}{V_{IN\ max}}.$$

2. $$S/N = 20 \log \frac{V_O \text{ video noise (p-p) (2 V)}}{V_O \text{ noise rms B = 5 MHz}}.$$

3. $$\text{Supply voltage ripple rejection} = 20 \log \frac{V_r \text{ supply}}{V_r \text{ on output}} \text{ at f = max. 100 kHz.}$$

4. $$S/N = 20 \log \frac{V_O \text{ nominal (0,5 V)}}{V_O \text{ noise B = 20 kHz}}.$$

5. Caused by drive of any other input at maximum level, measured in B = 20 kHz, source impedance of the used input = 1 kΩ,

   $$\text{crosstalk} = 20 \log \frac{V_{out}}{V_{in\ max}}$$ according to DIN 45405 (CCIR 468).

6. f = 20 Hz to 20 kHz.
7. All outputs are short-circuit proof (static).
8. The inputs and output (apart from SDA, SCL and OFF) withstand tests of MIL-STD-883 C. It is advisable to connected series resistors to these pins.
9. Timings $t_{S,\ DAT}$ and $t_{H,\ DAT}$ deviate from the I^2C bus specification. After reset has been activated, transmission may only be started after a 50 μs delay.

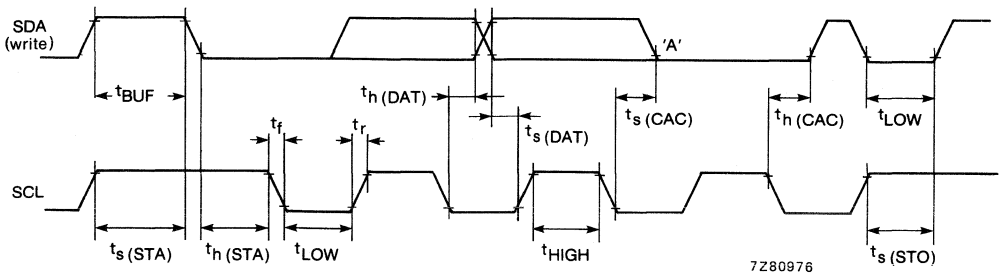


Fig. 2 Timing diagram I^2C bus.

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

I²C-BUS INTERFACE FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8442 provides control of four analogue functions and has one high-current and two switching outputs. Control of the IC is performed via the two-line, bidirectional I²C-bus.

Features

- Four analogue control outputs
- One high-current output port (npn open emitter)
- Two switching output ports (npn collector with internal pull-up resistor)
- I²C-bus slave receiver
- Power-down reset

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current	no outputs loaded	I_P	8	13	18	mA
Total power dissipation	no outputs loaded	P_{tot}	–	–	1	W
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

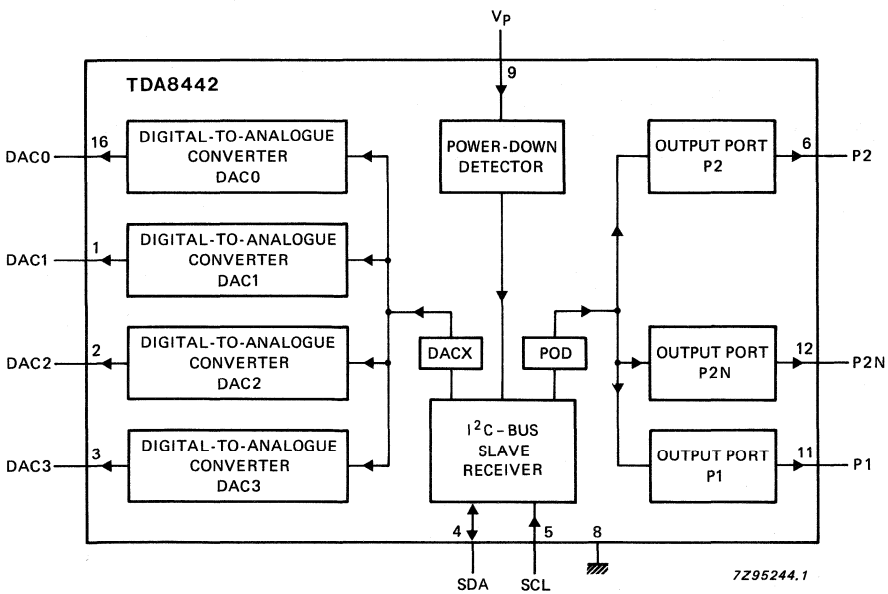


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

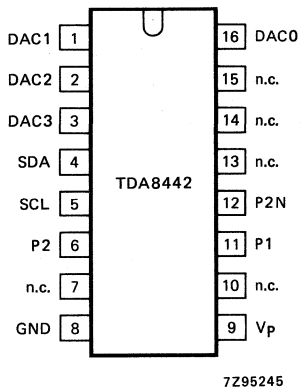


Fig. 2 Pinning diagram

PINNING

1	DAC1	analogue output 1
2	DAC2	analogue output 2
3	DAC3	analogue 3
4	SDA	serial data line } I^2C-bus
5	SCL	serial clock line } I^2C-bus
6	P2	Port 2 npn collector output with internal pull-up resistor
7	n.c.	not connected
8	GND	supply return (ground)
9	V_P	positive supply voltage
10	n.c.	not connected
11	P1	Port 1 open npn emitter output
12	P2N	inverted P2 output
13	n.c.	not connected
14	n.c.	not connected
15	n.c.	not connected
16	DAC0	analogue output 0

FUNCTIONAL DESCRIPTION

Control

Analogue control is facilitated by four 6-bit digital-to-analogue converters (DAC0 to DAC3). The values of the output voltages from the DACs are set via the I^2C-bus.

The high-current output port (P1) is suitable for switching between internal and external RGB signals. It is an open npn emitter output capable of sourcing 14 mA (min.).

The two output ports (P2 and P2N) can be used for NTSC/PAL switching. These are npn collector outputs with internal pull-up resistors of 10 kΩ (typ.). Both outputs are capable of sinking up to 2 mA with a voltage drop of less than 400 mV. If one output is switched on (LOW), the other output is switched off, and vice versa.

Reset

The power-down-reset mode occurs whenever the positive supply voltage falls below 8.5 V (typ.) and resets all registers to a defined state.

OPERATION

Write

The TDA8442 is controlled via the I²C-bus (specifications for the I²C-bus will be supplied on request). Programming of the TDA8442 is performed using the format shown in Fig. 3.

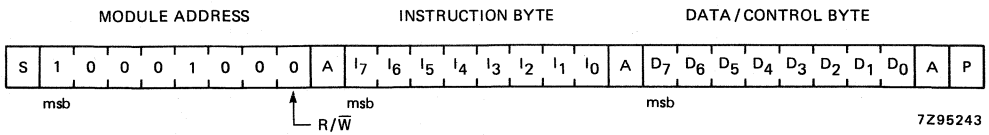


Fig. 3 TDA8442 programming format.

Acknowledge (A) is generated by the TDA8442 only when a valid address is received and the device is not in the power-down-reset mode ($V_P > 8.5$ V (typ.)).

Control

Control is implemented by the instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) together with the corresponding data/control bytes (see Fig. 4).

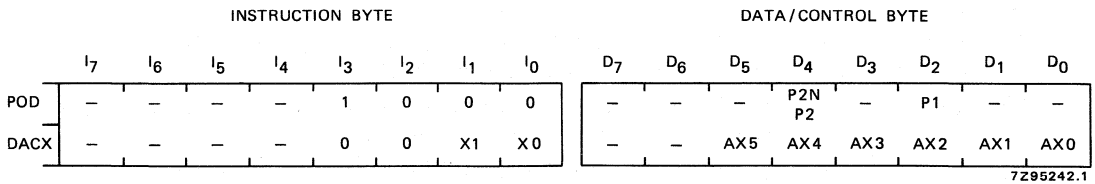


Fig. 4 Control programming.

POD bit P1: If a logic 1 is programmed, the P1 output is switched on. If a logic 0 is programmed or after a power-down-reset, the P1 output is switched off (high-impedance state).

POD bit P2/P2N: If a logic 1 is programmed, the P2 output is switched off and the P2N output is switched on (LOW). If a logic 0 is programmed or after a power-down-reset, the P2 output is switched on (LOW) and the P2N output is switched off.

DAX bits AX5 to AX0: The digital-to-analogue converter selected corresponds to the decimal equivalent of the two bits X1 and X0. The output voltage of the selected DAC is programmed using bits AX5 to AX0, the lowest value being with all data AX5 to AX0 at logic 0 or when power-down-reset has been activated.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 9)	V_P	−0.3	+ 13.2	V
Input/output voltage ranges				
pin 4	V_{SDA}	−0.3	+ 13.2	V
pin 5	V_{SCL}	−0.3	+ 13.2	V
pin 6	V_{P2}	−0.3	V_P*	V
pin 11	V_{P1}	−0.3	V_P*	V
pin 12	V_{P2N}	−0.3	V_P*	V
pins 1 to 3 and pin 16	V_{DAX}	−0.3	V_P*	V
Total power dissipation	P_{tot}	–	1	W
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = + 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current (pin 9)	no outputs loaded	I_P	8	13	18	mA
I²C-bus inputs						
SDA (pin 4); SCL (pin 5)						
Input voltage HIGH	note 1	V_{IH}	3.0	–	V_P−1	V
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input current HIGH	note 1	I_{IH}	–	–	10	μA
Input current LOW	note 1	I_{IL}	–	–	10	μA
I²C-bus output						
SDA (pin 4)	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	3	5	–	mA

* Pin voltage may exceed V_P if the current in that pin is limited to 10 mA.

parameter	conditions	symbol	min.	typ.	max.	unit
Ports P2 and P2N (pins 6 and 12)	npn collector output with pull-up resistor to V_P					
Internal pull-up resistor to V_P		R_O	5	10	15	kΩ
Output voltage switched on (LOW)	I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	2	5	–	mA
Leakage current output switched off		$-I_{leak}$	–	–	25	μA
Port P1 (pin 11)	open npn emitter output					
Output current switched on	V_O = 0 to 5 V	I_O	14	–	–	mA
Leakage current switched off	V_O = 0 to V_P	$\pm I_{leak}$	–	–	100	μA
Digital-to-analogue outputs	note 2					
DAC0 (pin 16)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	3.0	–	4.25	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.15	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	16	–	72	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	45	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC1 (pin 1)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = –2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Digital-to-analogue outputs (continued)						
DAC2 (pin 2)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = −2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC3 (pin 3)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	10.0	–	11.2	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.1	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	70	–	250	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	150	mV
Output impedance	I_O = −2 to + 2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
Power-down reset						
Maximum value of V_P at which power-down reset is active		V_{PD}	6	–	10	V
Rise time of V_P during power-on	V_P rising from 0 V to V_{PD}	t_r	5	–	–	μs

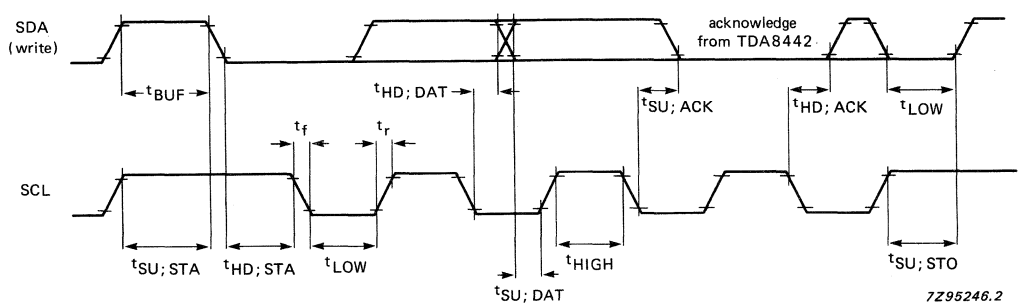
Notes to the characteristics

1. If $V_p < 1$ V, the input current is limited to 10 μA at input voltages up to 13.2 V.
2. Pure capacitive load should be avoided because of possible oscillations.
3. Values are proportional to V_P.

I²C-BUS TIMING

Bus loading conditions: 4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND. All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4.0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
LOW period SCL, SDA	t_{LOW}	4.0	–	–	μs
HIGH period SCL	t_{HIGH}	4.0	–	–	μs
Rise time SCL, SDA	t_r	–	–	1.0	μs
Fall time SCL, SDA	t_f	–	–	0.30	μs
Data set-up time (write)	$t_{SU;DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD;DAT}$	1	–	–	μs
Acknowledge (from TDA8442) set-up time	$t_{SU;ACK}$	–	–	3.5	μs
Acknowledge (from TDA8442) hold time	$t_{HD;ACK}$	0	–	–	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs



Reference levels are 10 and 90%.

Fig. 5 I²C-bus timing; TDA8442.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

I²C-BUS CONTROLLED YUV/RGB SWITCH

GENERAL DESCRIPTION

The TDA8443A is a general purpose two-channel switch for YUV or RGB signals. One channel provides matrixing from RGB to YUV, which can be bypassed.
The IC ic controlled via I²C-bus by seven different addresses or can be used in a non-I²C-bus mode. In the non-I²C-bus mode, control of the circuit is achieved by DC voltages.

Features

- Two RGB/YUV selectable clamped inputs with associated synchronization
- RGB/YUV matrix
- 3-state switching with an OFF-state
- Selectable gain
- I²C-bus or non-I²C-bus mode
- Address selection for 7 devices
- Fast switching

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 18)		$V_P = V_{18-22}$	10.8	12.0	13.2	V
Supply current		I_P	–	65	90	mA
RGB/YUV channels						
Output impedance						
pin 19		$\|Z_{19-22}\|$	–	7	30	Ω
pin 20		$\|Z_{20-22}\|$	–	7	30	Ω
pin 21		$\|Z_{21-22}\|$	–	7	30	Ω
Bandwidth						
–3 dB	mode 0 or 2	B	–	25	–	MHz
+3 dB	mode 0 or 2	B	–	12	–	MHz
+/–3 dB	mode 1	B	–	10	–	MHz
Maximum output amplitude of YUV signals (peak-to-peak)	gain x 1	$V_{O(p-p)}$	2.1	–	–	V
	gain x 2	$V_{O(p-p)}$	4.2	–	–	V
Operating ambient temperature range		T_{amb}	0	–	+70	°C

PACKAGE OUTLINE

24-lead DIL; plastic with internal heat spreader (SOT101B).

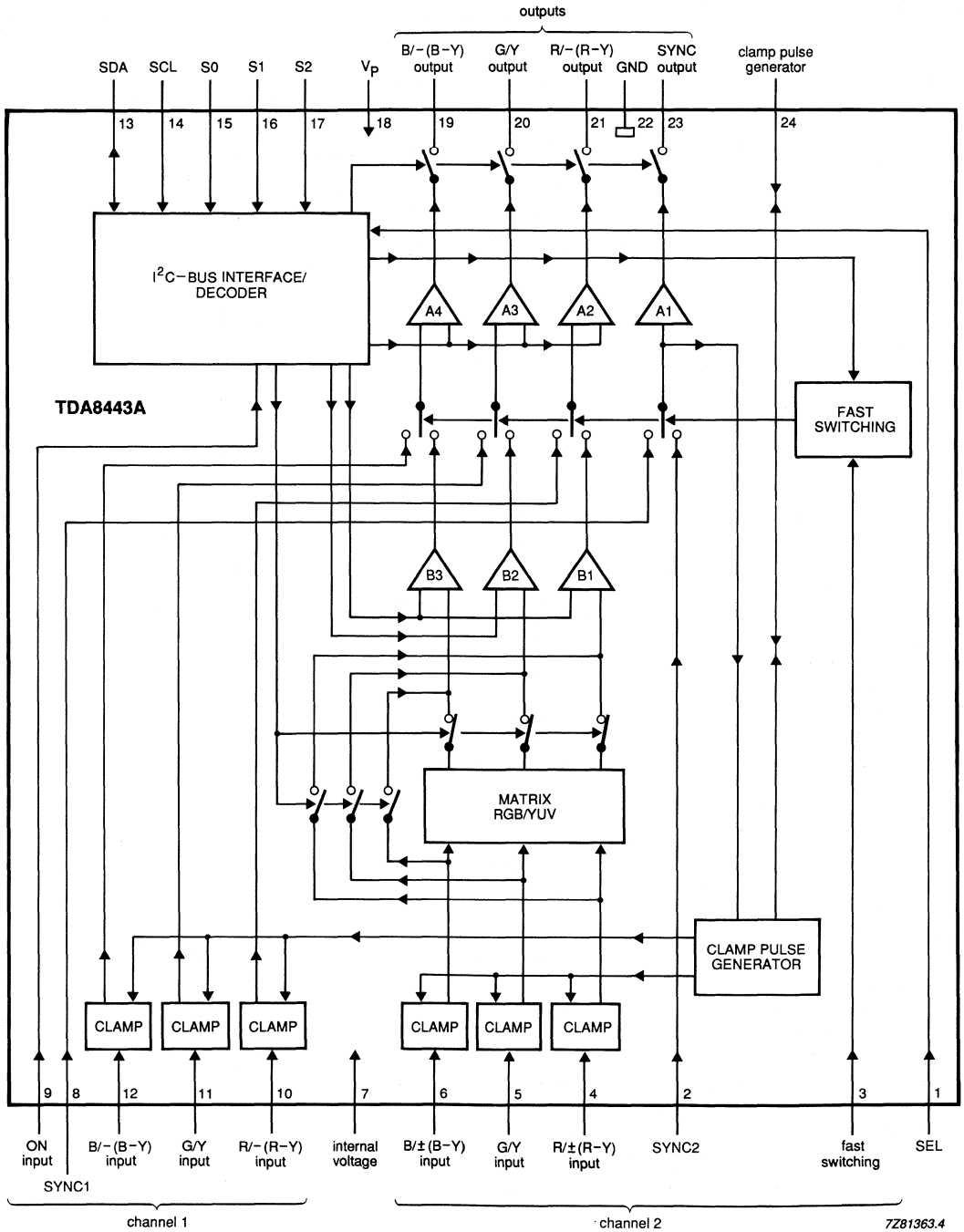


Fig.1 Block diagram.

PINNING

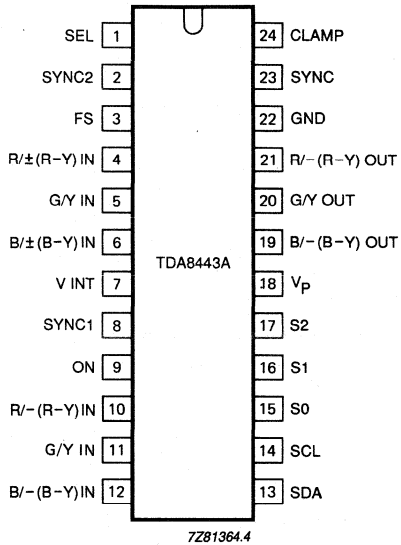


Fig.2 Pinning diagram.

1	SEL	select input (non-I²C-bus mode only)	
2	SYNC2	synchronization input for channel 2	
3	FS	fast switching input	
4	R/± (R-Y) IN	R or (R-Y) signal input	
5	G/Y IN	G or Y signal input	
6	B/± (B-Y) IN	B or (B-Y) signal input	
7	V INT	internal voltage supply	
8	SYNC1	synchronization input for channel 1	
9	ON	ON input	
10	R/–(R-Y) IN	R or –(R-Y) signal input	
11	G/Y IN	G or Y signal input	
12	B/–(B-Y) IN	B or –(B-Y) signal input	
13	SDA	serial data input/output	I²C-bus
14	SCL	serial clock input	I²C-bus
15	S0	address selection inputs	I²C-bus
16	S1	address selection inputs	I²C-bus
17	S2	address selection inputs	I²C-bus
18	V_P	positive supply voltage	
19	B/–(B-Y)	B or –(B-Y) signal output	
20	G/Y OUT	G or Y signal output	
21	R/–(R-Y)	R or –(R-Y) signal output	
22	GND	ground	
23	SYNC	synchronization output	
24	CLAMP	clamping pulse generator input/output	

FUNCTIONAL DESCRIPTION

The circuit contains two sets of inputs (see Fig.1). Both channels can receive RGB or YUV signals. Each set of inputs has its own synchronization input, which internally generates a pulse to clamp the inputs. The internal clamping pulse can also be controlled by a signal (e.g. a sandcastle pulse) applied to pin 24. The pulse will occur during the time that the signal at pin 24 is between 5.5 and 6.5 V. If both a sync signal and a pin 24 signal are used the signal should be applied to pin 24 via a 1 kΩ resistor.

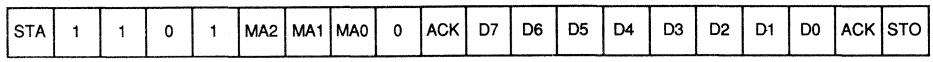
RGB signals of channel 2 can be matrixed to YUV signals.

The outputs can be set in a high impedance OFF state, which allows the use of up to seven devices in parallel (I^2C-bus mode).

The circuit can be controlled by an I^2C-bus compatible microcontroller or directly by DC voltages. The fast switching input can be operated via pin 16 of the peritelevision connector.

I²C-bus mode

The protocol for the devices in I²C-bus mode is shown in Fig.3.



MSA003

Fig.3 I²C-bus protocol.

Where:

STA : start condition
MA2, MA1, MA0 : address selection bits, see Table 1
ACK : acknowledge bit
D7 : channel selection bit, see Table 2
D6 : matrix selection bit, see Table 2
D5, D4, D3 : gain control bits, see Table 3
D2 : fast switching priority bit, see Table 4
D1, D0 : output state control bits, see Table 5
STO : stop condition

Table 1 Address selection

address select pins			address select bits		
S2 pin 17	S1 pin 16	S0 pin 15	MA2	MA1	MA0
L	L	L	*	*	*
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	1	1	1

Where:

L = input voltage LOW
H = input voltage HIGH
* = non-I²C-bus operation

Table 2 Mode control bits D7, D6

mode	D7	D6	function
0	0	0	channel 2 selected, no matrix
1	0	1	channel 2 selected, matrix active
2	1	0	channel 1 selected
–	1	1	not allowed

I²C-bus mode (continued)

Table 3 Gain setting (see also Table 9)

D5	D4	D3	A1	A2, A3, A4	B1, B3	B2
0	0	0	1	1	−1	0.45
0	0	1	1	1	1	1
0	1	0	not allowed			
0	1	1	1	1	−1	0.45
1	0	0	2	2	−1	0.45
1	0	1	2	1	1	1
1	1	0	2	2	1	1
1	1	1	2	1	−1	0.45

Matrix equations

The relationship between output and input signals of the matrix is as follows:

$Y = 0.3\ R + 0.59\ G + 0.11\ B$
$R\text{-}Y = 0.7\ R - 0.59\ G - 0.11\ B$
$B\text{-}Y = -0.3\ R - 0.59\ G + 0.89\ B$

Table 4 Priority/fast switching bit D2

D2	fast switching pin 3	mode
0	X	0 to 2, depending on D7, D6
1	0.4 V	2

Where:
X = don't care

Table 5 Output state control bits

D1	D0	pin 9	function
0	X	X	OFF
1	0	L	OFF
1	0	H	ON
1	1	X	ON

Where:
X = don't care

Power-on reset

If the circuit is switched on in the I²C-bus mode, all bits of D0 to D7 are set to zero.

Timing specifications

I²C-bus load conditions are as follows:
4 kΩ pull-up resistor to + 5 V; 200 pF capacitor to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	max.	unit
Bus free before start	t_{BUF}	4.7	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	μs
SCL and SDA LOW time	t_{LOW}	4.7	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	μs
SCL and SDA rise time	t_r	–	1.0	μs
SCL and SDA fall time	t_f	–	0.3	μs
Data set-up time (write)	$t_{SU;DAT}$	250	–	ns
Data hold time (write)	$t_{HD;DAT}$	1.0	–	μs
Acknowledge set-up time	$t_{SU;ACK}$	–	2	μs
Acknowledge hold time	$t_{HD;ACK}$	0	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4.7	–	μs

Note

Timing $t_{HD;DAT}$ deviates from the I²C-bus specification. After reset has been activated, a delay of 50 μs must occur before transmission may be resumed.

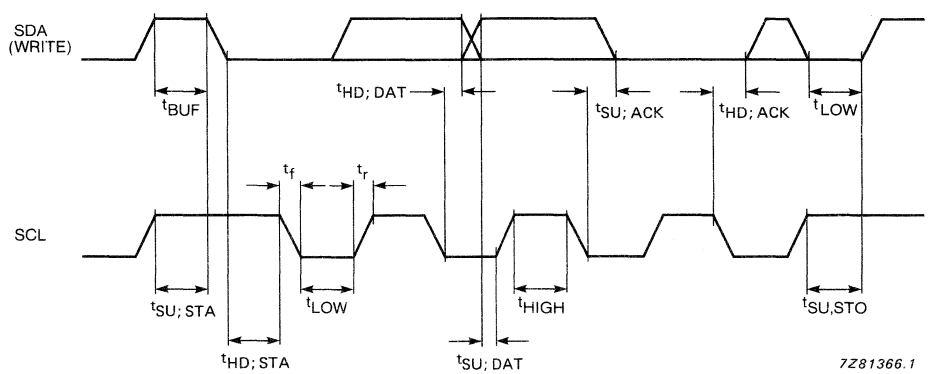


Fig.4 I²C-bus timing diagram.

Non-I²C-bus mode

Table 6 Non-I²C-bus mode (S2 = S1 = S0 = L)

control			mode switched	gain settings			
pin 13	pin 14	pin 1	by FS (pin 3)	A1	A4, A3, A2	B1, B3	B2
L	L	L	2/0	1	1	1	1
L	L	H	2/0	1	2	1	1
L	H	L	2/1	1	1	−1	0.45
L	H	H	2/0	1	1	−1	0.45
H	L	L	2/0	2	1	1	1
H	L	H	2/0	2	2	1	1
H	H	L	2/1	2	1	−1	0.45
H	H	H	2/0	2	1	−1	0.45

Table 7 Fast switching input (pin 3)

FS	mode selected
⩽ 0.4 V	mode 2
1 to 3 V	mode 0 or mode 1 as set by control

Table 8 ON input (pin 9)

ON	function
L	OFF, no output signal, high impedance OFF state
H	function is determined in Table 6

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 18)	V_P	–	14	V
Input voltage range				
SDA (pin 13)	V_I	−0.3	14	V
SCL (pin 14)	V_I	−0.3	14	V
any other pin	V_I	−0.3	V_P + 0.3	V
Maximum output current	I_O	–	20	mA
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 125	°C
Maximum junction temperature	T_j	–	+ 125	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 18)		V_P	10.8	12.0	13.2	V
Supply current		I_P	–	65	90	mA
RGB/YUV channels						
Absolute gain difference (programmed value)			–	0	10	%
Relative gain difference						
between Y output and the (R-Y) and (B-Y) channel inputs			–	0	10	%
between any two other channels			–	0	5	%
Input current		I_I	–	0.5	1.0	μA
Output impedance						
pin 19		$\|Z_{19-22}\|$	–	7	30	Ω
pin 20		$\|Z_{20-22}\|$	–	7	30	Ω
pin 21		$\|Z_{21-22}\|$	–	7	30	Ω
Bandwidth						
–3 dB	mode 0 or 2	B	–	25	–	MHz
+3 dB	mode 0 or 2	B	–	12	–	MHz
±3 dB	mode 1	B	–	10	–	MHz
Mutual time difference at output	all inputs of one source connected together		–	–	25	ns
Maximum output amplitude of YUV signals (peak-to-peak value)	gain x 1	$V_{O(p-p)}$	2.1	–	–	V
	gain x 2	$V_{O(p-p)}$	4.2	–	–	V
Crosstalk between	note 1					
inputs of same source	f = 5 MHz	α	–	–	–30	dB
different sources		α	–	–	–40	dB
Isolation (OFF state)	f = 10 MHz		50	–	–	dB

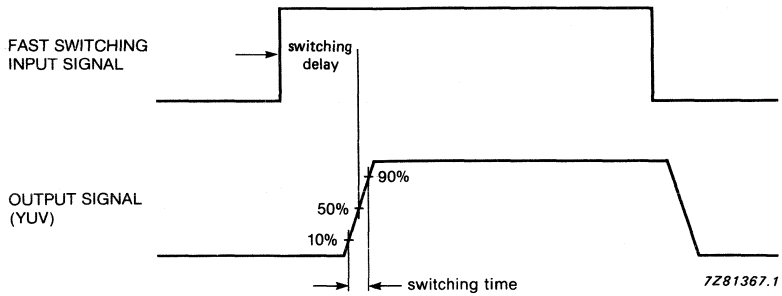
parameter	conditions	symbol	min.	typ.	max.	unit
Differential gain at nominal output signals (peak-to-peak value)	R-Y = 1.05 $V_{(p-p)}$		–	–	10	%
	B-Y = 1.33 $V_{(p-p)}$		–	–	10	%
	Y = 0.34 $V_{(p-p)}$		–	–	10	%
Signal-to-noise ratio nominal input	note 2 B = 5 MHz	S/N	50	–	–	dB
Supply voltage ripple rejection	note 3	RR	30	–	–	dB
DC output levels during clamping		V_O	–	5.3	–	V
Synchronization channels						
Gain difference (programmed value)			–	–	10	%
Bandwidth						
–3 dB		B	–	50	–	MHz
+ 3 dB gain x 1		B	–	20	–	MHz
+ 3 dB gain x 2		B	–	13	–	MHz
Input amplitude of sync signal for correct operation of clamp pulse generator (peak-to-peak value)		$V_{I(p-p)}$	0.2	–	2.5	V
Output impedance (pin 23)		$\lvert Z_{23-22}\rvert$	–	20	30	Ω
Maximum undistorted output amplitude (pin 23) (peak-to-peak value)		$V_{O(p-p)}$	2.5	–	–	V
DC output level on top of sync pulse		V_O	1.5	1.9	2.4	V
I²C-bus inputs						
SDA, SCL						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	–0.3	–	1.5	V
Input current HIGH		I_{IH}	–	–	10	μA
Input current LOW		I_{IL}	–	–	10	μA
I²C-bus output						
SDA (open collector)						
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	–	–	0.4	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Address selection inputs						
S0, S1, S2						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	10	μA
Input current LOW		I_{IL}	−50	−10	0	μA
Fast switching input						
Input voltage HIGH		V_{IH}	1	–	3	V
Input voltage LOW		V_{IL}	−0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	500	μA
Input current LOW		I_{IL}	−100	–	–	μA
Switching time	see Fig.5	t	–	10	–	ns
Switching delay	see Fig.5	t_d	–	20	–	ns
Select input						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0.3	–	0.4	V
Input current HIGH		I_{IH}	–	0	10	μA
Input current LOW		I_{IL}	−50	−10	0	μA
ON input						
Input voltage HIGH		V_{IH}	3	–	V_P	V
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input current HIGH		I_{IH}	–	–	10	μA
Input current LOW		I_{IL}	–	–	10	μA

Notes to the characteristics

1. Crosstalk is defined as the unwanted data transfer from an output, driven at nominal level, to other inputs and outputs on the IC and is expressed as a ratio in dBs.
2. Signal-to-noise ratio = $20 \log \frac{V_{O(p\text{-}p)}}{V_O \text{ noise (RMS) } B = 5 \text{ MHz}}$
3. Supply voltage ripple rejection = $20 \log \frac{V_{RR} \text{ supply}}{V_{RR} \text{ on the output}}$



Input = 0 V (input 1; Mode 2)
Input = 0.75 V (RGB; Mode 1)

Fig.5 Fast switching signal diagram.

APPLICATION INFORMATION

Table 9 Application information

input 1	input 2	output	mode	G2	G1	G0
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.6 V	2	1	1	1
	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V		1	1	1	1
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.68 V U = −2.66 V V = −2.10 V S = 0.6 V	2	1	0	0
	R = 0.75 V G = 0.75 V B = 0.75 V S = 0.3 V		1	1	0	0
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.6 V	2	1	0	1
	Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		0	1	0	1
Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		Y = 0.68 V U = −2.66 V V = −2.10 V S = 0.6 V	2	1	1	0
	Y = 0.34 V U = −1.33 V V = −1.05 V S = 0.3 V		0	1	1	0

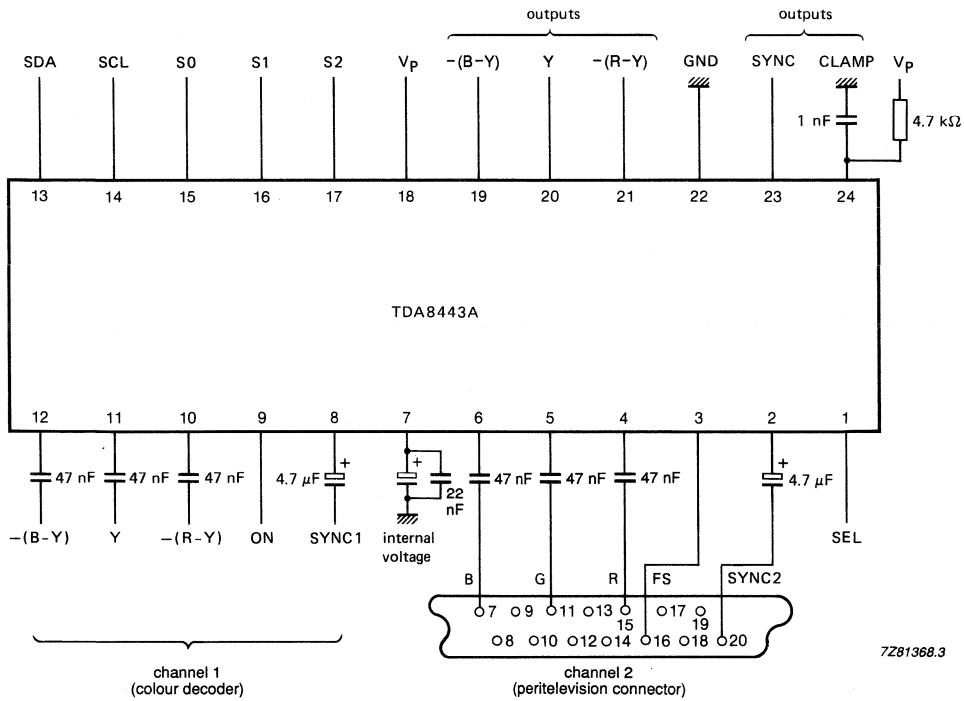


Fig.6 Application diagram (example).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

OCTUPLE 6-BIT DAC WITH I²C-BUS

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

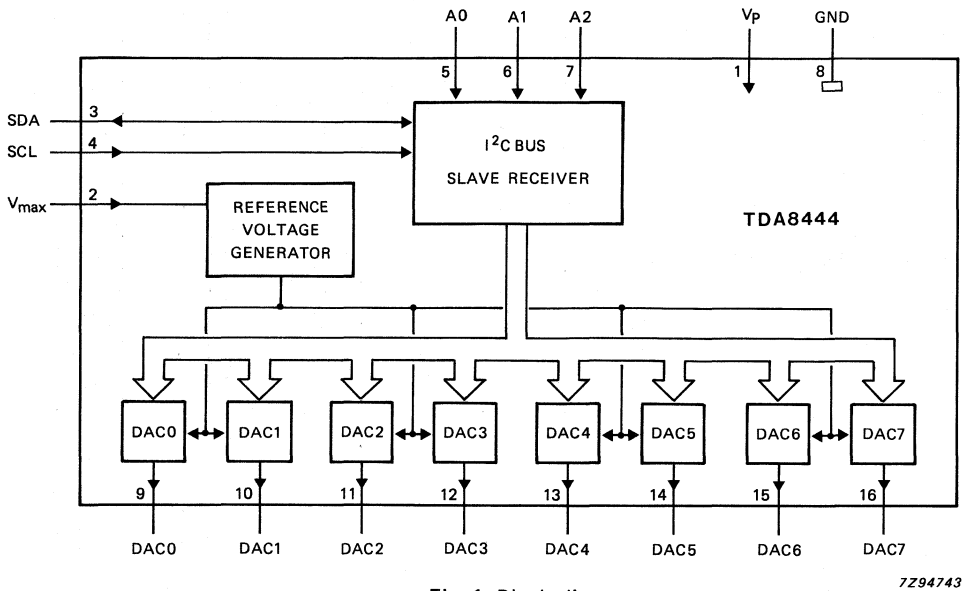


Fig. 1 Block diagram.

PINNING

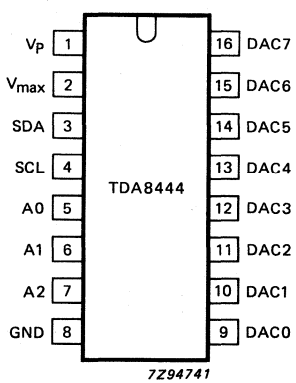


Fig. 2 Pinning diagram.

1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I^2C-bus serial data input/output
4	SCL	I^2C-bus serial data clock
5	A0	programmable address bits for I^2C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I²C-bus interface is a receive-only slave. Data is accepted from the I²C-bus in the following format:

S	0 1 0 0 A2 A1 A0 0	A	I3 I2 I1 I0 SD SC SB SA	A	X X D5 D4 D3 D2 D1 D0	A	P
	← address byte →		← instruction byte →		← first data byte →		

Where:

S	= start condition	A2, A1, A0	= programmable address bits
P	= stop condition	I3, I2, I1, I0	= instruction bits
A	= acknowledge	SD, SC, SB, SA	= subaddress bits
X	= don't care	D5, D4, D3, D2, D1, D0	= data bits

Fig. 3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications.* Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to Vp for An = 1. If the inputs are left floating, An = 1 will result.

FUNCTIONAL DESCRIPTION (continued)

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

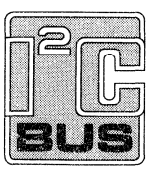
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_1$	−0.5	18	V
Supply current (source)		$I_p = I_1$	−	−10	mA
		$I_P = I_I$	−	40	mA
I^2C-bus line voltage		$V_{3,4}$	−0.5	5.9	V
Input voltage		V_I	−0.5	$V_P + 0.5$	V
Output voltage		V_O	−0.5	$V_P + 0.5$	V
Maximum current on any pin (except pins 1 and 8)		$\pm I_{max}$	−	10	mA
Total power dissipation		P_{tot}	−	500	mW
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−55	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W



Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Voltage level for power-on reset		V_1	1	–	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	–	10.5	V
Pin 2 current	V_2 = 1 V	I_2	–	–	−10	μA
	$V_2 = V_P$	I_2	–	–	10	μA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	–	5.5	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	–	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	–	–	±10	μA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	–	–	0.4	V
Sink current		I_O	3	8	–	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0	–	V_P	V
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2.1	–	–	V
Input current LOW		I_{IL}	–	−7	−12	μA
Input current HIGH		I_{IH}	–	–	1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	V_P–0.5	V
Minimum output voltage	data = 00; I_O = –2 mA	V_{Omin}	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at $V_{max} = V_P$		V_{Omax}	10	10.5	11.5	V
at $1 < V_{max} < 10.5$ V		V_{Omax}		see note		V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; $-2 < I_O < +2$ mA	Z_O	–	4	50	Ω
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = –2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = –2 mA; N = 32		0	–	70	mV

Note to the characteristics

$V_O = 0.95\ V_{max} + V_{Omin}$.

APPLICATION INFORMATION

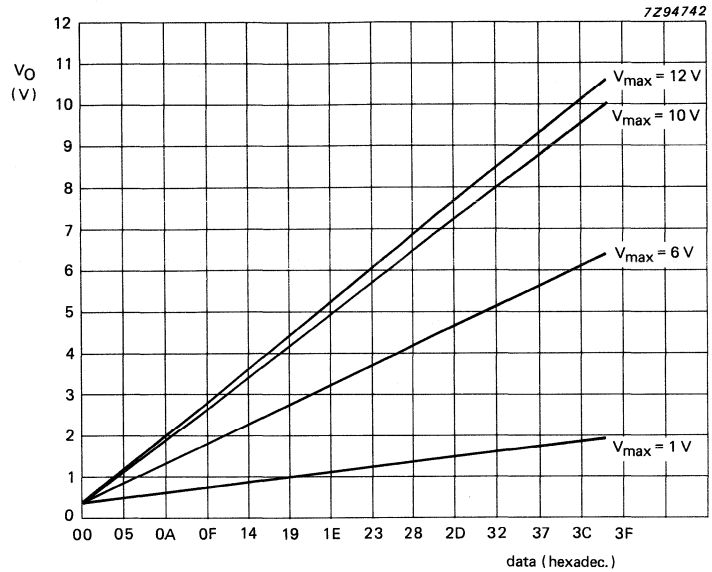


Fig. 4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

Fast RGB/YC switch for digital decoding

TDA8446; TDA8446T

FEATURES

- R, G, B clamped inputs
- Luminance and chrominance difference matrix
- Y-clamped inputs
- Fast switching between internal and external Y
- Chrominance input
- Amplifier with selectable gain
- 3-state switch for chrominance output

APPLICATIONS

- Digital TV systems
- Desktop video architecture

DESCRIPTION

The TDA8446 is a video switch which is designed for use in the DMSD digital video system (DMSD = Digital Multistandard System Decoder). The device is intended for matrixing incoming RGB signals and for switching between luminance signals. It generates SYNC signal and TTL clamping pulses from any video signal with sync pulses.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage range	10.8	–	13.2	V
T_{amb}	operating ambient temperature range	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8446	20	DIL	plastic	SOT146E
TDA8446T	28	SO28L	plastic	SOT136A

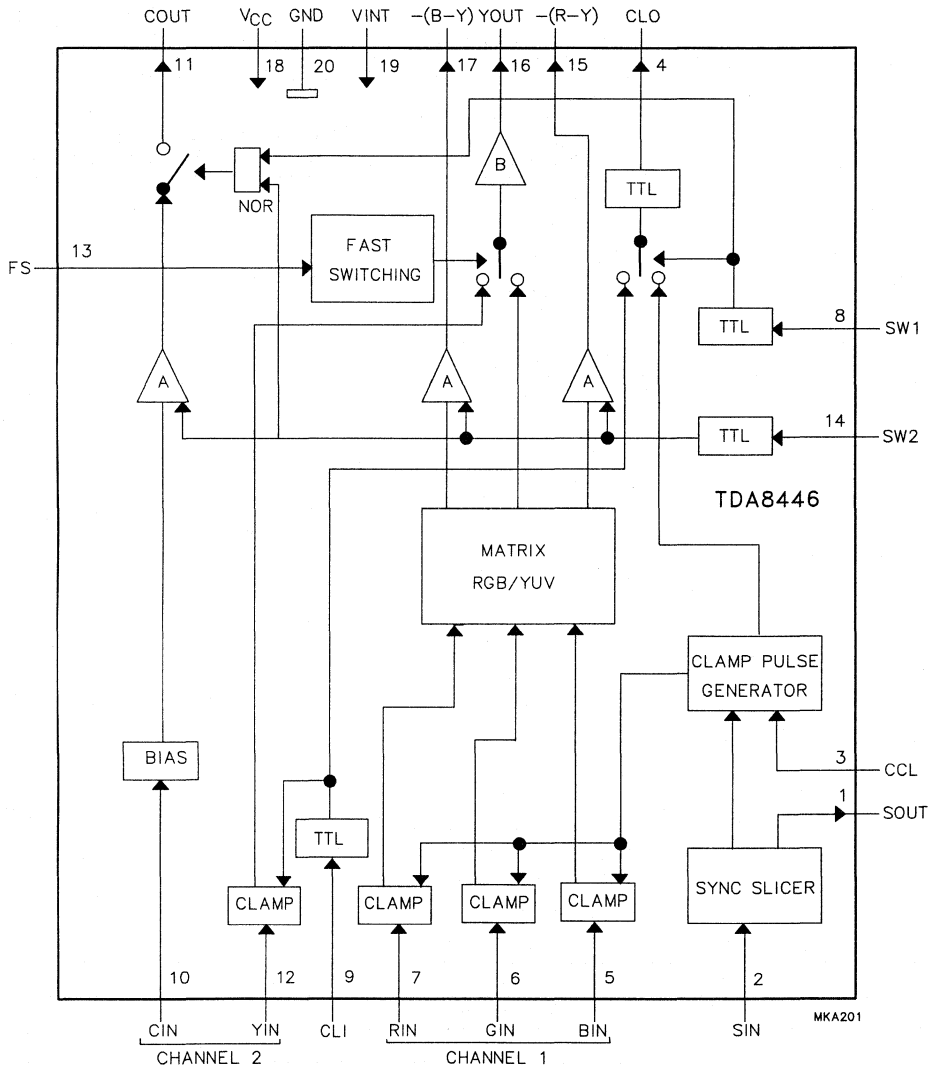


Fig.1 Block diagram (DIL package).

PINNING

SYMBOL	PIN		DESCRIPTION
	DIL	SO	
SOUT	1	1	synchronization signal output; this output provides the synchronization information extracted from the incoming signal at pin 2 (SIN)
SIN	2	2	synchronization signal input; CSYNC or CVBS signal from the video-connector
CCL	3	3	clamping capacitor connection; the clamping pulse is generated by external circuitry connected to this pin; the generated pulse clamps the RGB inputs
n.c.	–	4	not connected
CLO	4	5	clamping pulse output
n.c.	–	6	not connected
BIN	5	7	B-signal input
GIN	6	8	G-signal input
RIN	7	9	R-signal input
SW1	8	10	clamping control signal input; this TTL signal is used to select the clamp signal; a LOW level at this input forces the circuit to output the generated clamping pulse
n.c.	–	11	not connected
CLI	9	12	clamping pulse input; this TTL signal indicates the black level clamping period for the incoming Y signal (active HIGH)
CIN	10	13	chrominance signal input
COUT	11	14	chrominance signal output
YIN	12	15	luminance signal input; this input also accepts the CVBS signal
FS	13	16	fast switching signal input; this signal is used to control fast switching of the luminance signals; a HIGH level at this input forces the circuit to output the internal Y
n.c.	–	17	not connected
n.c.	–	18	not connected
SW2	14	19	gain control signal input; this TTL signal is used to fix the gain of the chrominance amplifiers (A); a LOW level at this input forces the gain A at 6 dB, (HIGH forces 0 dB)
n.c.	–	20	not connected
–(R-Y)	15	21	–(R-Y) signal output
YOUT	16	22	luminance signal output
–(B-Y)	17	23	–(B-Y) signal output
n.c.	–	24	not connected
n.c.	–	25	not connected
V_{CC}	18	26	positive supply voltage (+12 V)
VINT	19	27	internal decoupling
GND	20	28	ground

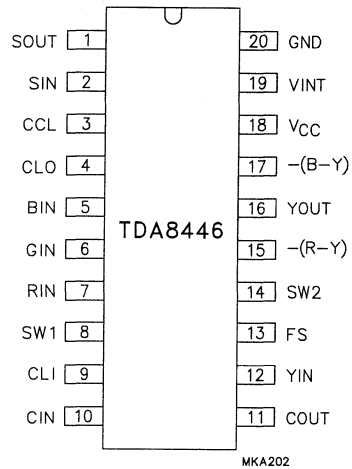


Fig.2 Pin configuration TDA8446 (DIL20).

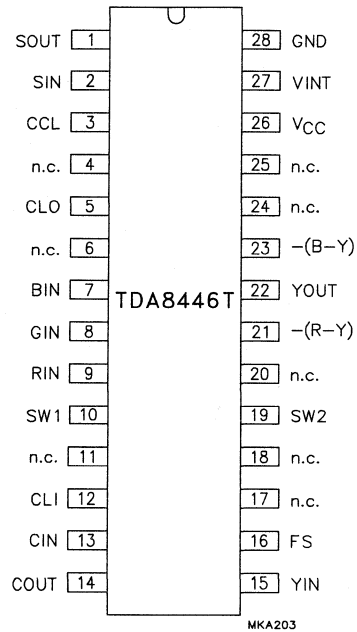


Fig.3 Pin configuration TDA8446T (SO28L).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	positive supply voltage range	−0.3	+14	V
V_I	input voltage	−0.3	+12.3	V
T_{stg}	storage temperature range	−55	+125	°C

HANDLING

Each pin will withstand the ESD test in accordance with MIL-STD-883C class 2 (2000 V to 2999 V). Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses − on each pin as a function of ground.

OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply/temperature					
V_{CC}	positive supply voltage range	10.8	–	13.2	V
T_{amb}	operating ambient temperature range	0	–	+70	°C
TTL inputs (SW1, SW2 and CLI)					
V_{IH}	HIGH level input voltage	2	–	V_{CC}	V
V_{IL}	LOW level input voltage	−0.3	–	+0.8	V
SYNC signal (SIN)					
$V_{S(p-p)}$	sync amplitude	0.2	–	2.5	V
Fast Switching input (FS)					
V_{IH}	HIGH level input voltage	1	–	3	V
V_{IL}	LOW level input voltage	–	–	0.4	V
Video inputs (RIN, GIN, BIN, CIN, YIN)					
$V_{I(p-p)}$	peak-to-peak video amplitude on RIN, GIN and BIN inputs	–	0.7	1	V
C_I	input capacitance	–	100	–	nF
Clamping pulse generator (CCL)					
R_{CP}	clamping resistance	–	4.7	–	kΩ
C_{CP}	clamping capacitance	–	1	–	nF

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{CC}	supply current		–	–	80	mA
RR	supply voltage rejection ratio	note 1	30	–	–	dB
Y and R, G, B channels						
I_{CL}	input clamping current	V_{CC} = 6 V; V_I = 0 V	0.3	–	–	mA
I_I	input current	V_I = 9 V	−1.5	0.5	+1.5	µA
G_A	gain of amplifier A	f = 1 MHz; V_{SW2} = 2.0 V	−1	0	+1	dB
		V_{SW2} = 0.8 V	+5	+6	+7	dB
G_B	gain of amplifier B	f = 1 MHz	−1	0	+1	dB
	RGB matrixed according to the equations: Y = 0.30R + 0.59G + 0.11B R–Y = 0.70R – 0.59G + 0.11B B–Y = –0.30R – 0.59G + 0.89B					
ΔG	relative gain difference	note 2	–	0	10	%
|ΔG|	maximum gain variation	100 kHz < f < 8 MHz	–	3	–	dB
R_O	output resistance		–	15	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Δt	time difference at output	f = 1 MHz; note 3	–	–	25	ns
V_O	DC output level	V_{CCL} = 6 V	–	4.2	–	V
t_{fsd}	fast switching delay	see Fig.4	–	20	–	ns
t_{fs}	fast switching time	see Fig.4	–	10	–	ns
I_{IFS}	input current on fast switching control (pin 13)	V_I = 0.4 V V_I = 1 V	– –	0.7 0.5	– –	µA µA
Chrominance channel (CIN, COUT)						
R_i	internal input resistance		–	50	–	kΩ
V_O	DC output level	I_I = 0	–	5	–	V
G_A	gain of amplifier A	f = 1 MHz $V_{SW1} = V_{SW2}$ = 2.0 V	–1	0	+1	dB
		V_{SW2} = 0.8 V	+5	+6	+7	dB
$\lvert\Delta G\rvert$	maximum gain variation	100 kHz < f < 8 MHz	–	3	–	dB
α_{off}	isolation (off state)	$V_{SW1} = V_{SW2}$ = 0.8 V f = 5 MHz	–	60	–	dB
Z_i	output impedance	$V_{SW1} = V_{SW2}$ = 0.8 V	100	–	–	kΩ
R_o	output resistance		–	7	–	Ω
TTL inputs (SW1, SW2, CLI)						
I_{IH}	HIGH level input current	V_{IH} = 2 V	–	–	10	µA
I_{IL}	LOW level input current	V_{IL} = 0.8 V	–	–	600	µA
Clamp output (CLO)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = 10 µA	2.4	–	–	V
Synchronization channel (SOUT)						
$V_{O(p-p)}$	output amplitude		0.2	–	1.5	V

Notes to the characteristics

1. Supply voltage rejection ratio: 20 log $V_{R(CC)}/V_{R(O)}$.
2. The relative gain difference is measured when only one input signal (R, G, or B) is present.
3. The inputs RIN, GIN and BIN are interconnected; Δt is the maximum time coincidence error between the luminance and chrominance signals.

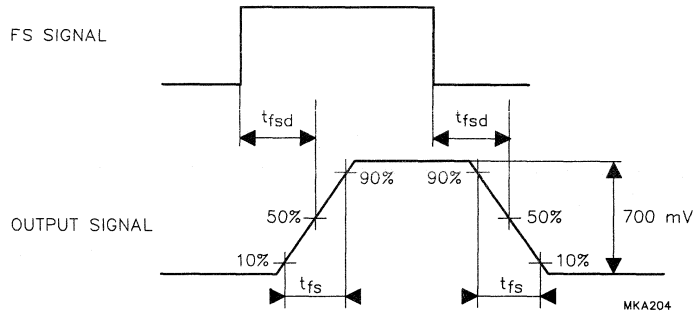


Fig.4 Fast switching times.

APPLICATION INFORMATION

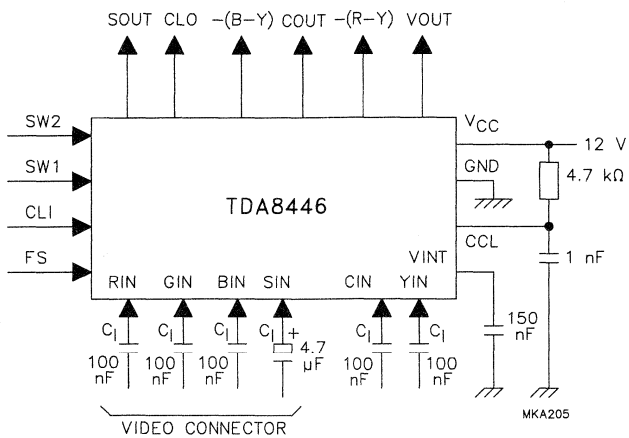


Fig.5 Typical application diagram.

P^2CCD DELAY LINE AND MATRIX

GENERAL DESCRIPTION

The TDA8451A is an integrated P^2CCD (Profiled Peristaltic Charge Coupled Device) delay line and matrix which has been designed to be used in conjunction with various colour decoder ICs (e.g. TDA8466, TDA8391). The device incorporates two delay lines with a delay length of 1 line time for colour difference signals, adding circuits for the delayed and direct signals and clock drivers for the delay lines which are driven from an internal voltage controlled oscillator (VCO) locked to the sandcastle pulse.

The TDA8451A differs from the TDA8451 by the following:

- The VCO is line locked instead of sub-carrier locked
- Adding direct and delayed signals occurs for PAL, SECAM and NTSC

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
analog (pin 3)		$V_{P(a)}$	10.8	12.0	13.2	V
digital (pin 16)		$V_{P(d)}$	10.8	12.0	13.2	V
Supply current						
analog (pin 3)		$I_{P(a)}$	5	10	15	mA
digital (pin 16)		$I_{P(d)}$	10	22	35	mA
Colour difference input signals (peak-to-peak value)	PAL/NTSC mode	$V_{I(p-p)}$	–	–	1.1	V
	SECAM mode	$V_{I(p-p)}$	–	–	2.1	V
Output signals	PAL/NTSC mode 0.8 V(p-p) input	V_O	–	0.8	–	V
	SECAM mode 1.6 V(p-p) input	V_O	–	0.8	–	V
Output resistance		R_O	–	500	–	Ω
Frequency response		Δf	–	1.3	–	MHz
Additional delay		t_d	–	760	–	ns

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38GG2).

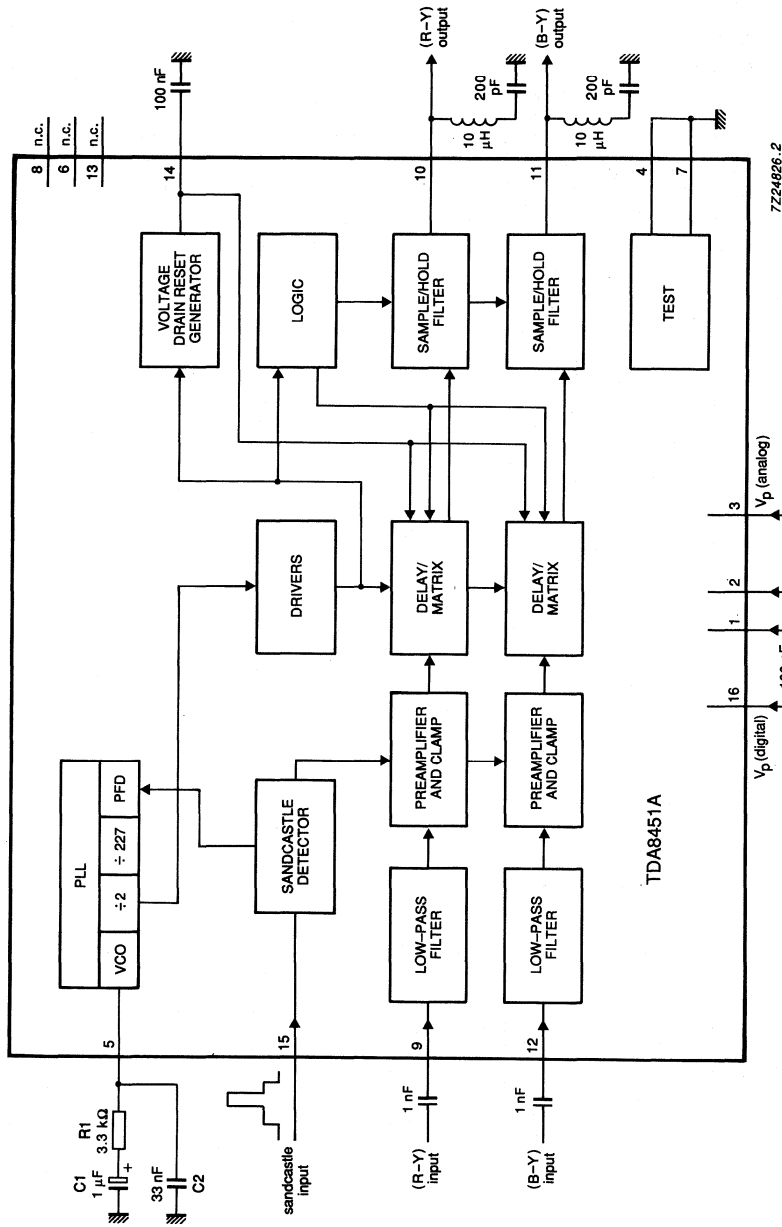


Fig.1 Block diagram.

Notes to Fig.1

1. If the TDA8451A is followed by a TDA4566 (CTI), it is recommended to replace the LC trap (and the usual RC low-pass filter in front of the TDA4566) by an LC low-pass circuit where L = 47 µH and C = 270 pF.
2. For multistandard concepts, including NTSC, the following values are recommended; R1 = 47 kΩ, C1 = 100 nF and C2 = 2.2 nF.

PINNING

1 Ground (digital)
2 Ground (analog)
3 Supply voltage input (analog)
4 Test pin (grounded for normal operation)
5 PLL filter
6 Not connected
7 Test pin (grounded for normal operation)
8 Not connected
9 (R-Y) input
10 (R-Y) output
11 (B-Y) output
12 (B-Y) input
13 Not connected
14 Voltage drain reset generator decoupling
15 Sandcastle input
16 Supply voltage input (digital)

FUNCTIONAL DESCRIPTION

When the (R-Y) and (B-Y) signals have been demodulated in the decoder, the resultant signals are applied to pins 9 and 12. The colour difference signals are then applied via a low-pass filter, preamplifier and clamp circuit to the delay lines. The delayed and direct signals are added in the matrix circuit.

This action occurs for PAL, SECAM and NTSC signals. Consequently, the NTSC colour difference signals are combed.

The frequency generated by the PLL circuit is 454 times the sandcastle frequency. The delay lines are driven by the internal clock drivers at half on the PLL frequency. The outputs from the delay lines are applied to the sample-and-hold low-pass filter output stages which are used to reduce the clock signals.

The P^2CCD delay line and matrix requires a supply voltage of 12 V. The output stages require a higher voltage (approximately 14 V). This voltage is generated internally with a decoupling capacitor connected to pin 14. A circuit for the TDA8451A together with PAL decoder (TDA8391) is illustrated in Fig.2. A circuit for the TDA8451A together with the PAL/NTSC decoder (TDA8466) and the SECAM decoder (TDA8490) is illustrated in Fig.3. The TDA8490 can also be used in combination with the TDA8391.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (analog)		$V_{P(a)}$		13.2	V
Supply voltage (digital)		$V_{P(d)}$		13.2	V
Total power dissipation		P_{tot}	–	1.45	W
Operating ambient temperature range		T_{amb}	−25	+70	°C
Storage temperature range		T_{stg}	−55	+150	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}a}$	55	K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 3) analog		$V_{P(a)}$	10.8	12.0	13.2	V
Supply current (pin 3) analog		$I_{P(a)}$	5	10	15	mA
Supply voltage (pin 3) ripple rejection at 100 mVeff	f = 100 Hz note 1	SVRR	–	10	–	dB
Supply voltage (pin 16) digital		$V_{P(d)}$	10.8	12.0	13.2	V
Supply current (pin 16) digital		$I_{P(d)}$	10	22	35	mA
Supply voltage (pin 16) ripple rejection at 100 mVeff	f = 100 Hz note 1	SVRR	–	25	–	dB
Total power dissipation		P_{tot}	–	0.38	0.66	W
Inputs for demodulated colour difference signals (pins 9 and 12)						
AC coupled and clamped by sandcastle pulse						
Input signal PAL/NTSC mode (peak-to-peak value)		$V_{I(p-p)}$	–	–	1.1	V
Input signal SECAM mode (peak-to-peak value)		$V_{I(p-p)}$	–	–	2.1	V
Input current (outside clamping time)		I_I	–	–	0.1	μA
Input capacitance		C_I	–	10	–	pF
Sandcastle input (pin 15)						
Input resistance		R_{15}	1000	–	–	kΩ
Detection level		V_{15}	6.0	6.8	7.5	V
CD signal output (pins 10 and 11)						
Output signals where input signal is PAL/NTSC at 0.8 V (peak-to-peak value)		$V_{10;\,11(p-p)}$	0.63	0.8	1.01	V
Output signals where input signal is SECAM at 1.6 V (peak-to-peak value)	note 2	$V_{10;\,11(p-p)}$	0.63	0.8	1.01	V

parameter	conditions	symbol	min.	typ.	max.	unit
Output resistance		R_O	300	500	800	Ω
Internal current load of CD outputs		$I_{10;11}$	0.4	–	1.5	mA
DC output level		$V_{10;11}$	4	–	8	V
Rest clock signals (RMS value)	note 3					
at 3.55 MHz		$V_{10\text{-}11(rms)}$	–	–	5	mV
at 7.09 MHz		$V_{10\text{-}11(rms)}$	–	–	6	mV
at 14.19 MHz		$V_{10\text{-}11(rms)}$	–	–	6	mV
Signal-to-noise ratio	note 4	S/N	60	65	–	dB
Linearity of output signals (peak-to-peak value)	note 5					
(R-Y); pin 9 to 10 PAL/NTSC	V_I = 0.85 V	α	0.95	–	–	
(R-Y); pin 9 to 10 SECAM	V_I = 1.60 V	α	0.92	–	–	
(B-Y); pin 12 to 11 PAL/NTSC	V_I = 1.10 V	α	0.95	–	–	
(B-Y); pin 12 to 11 SECAM	V_I = 2.10 V	α	0.92	–	–	
Frequency response	at −3 dB	Δf	1.0	1.3	–	MHz
Difference in amplitude between delayed and undelayed signal			–	–	1.5	%
Difference in amplitude of the two output signals for equal input signals			–	–	5	%
Delay time with a 15625 kHz sandcastle pulse		t_d	–	760	–	ns

Notes to the characteristics

1. The SVRR is measured with a 100 Ω resistor in series with a 1 nF capacitor connected between pin 9 and pin 2 and between pin 12 and pin 2.
2. During SECAM the input signal is available during one of two sequential lines. The output signal is thereby halved in comparison with the PAL signal condition.
   To compensate for this the input signal to the TDA8451A during SECAM is twice that during PAL.
3. The rest clock signals are measured with an FET probe (3.5 pF capacitor in parallel with a 1 MΩ resistor) which is connected directly to pin 1 and pin 10 or pin 1 and pin 11.
4. The signal-to-noise ratio (in the PAL mode) is calculated by:

   $$\frac{V_{O(p\text{-}p)}}{V_{noise(rms)}\ (0\text{-}1\ MHz)}$$ at an input voltage of 0.8 V(p-p), 0 dB gain
5. The linearity is defined as the amplification of the given input voltage swing divided by the amplification when the input voltage swing is decreased to 70%.

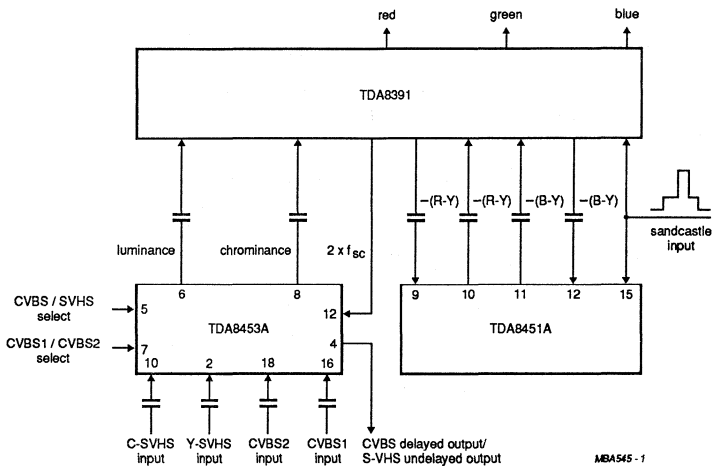


Fig.2 PAL decoder configuration.

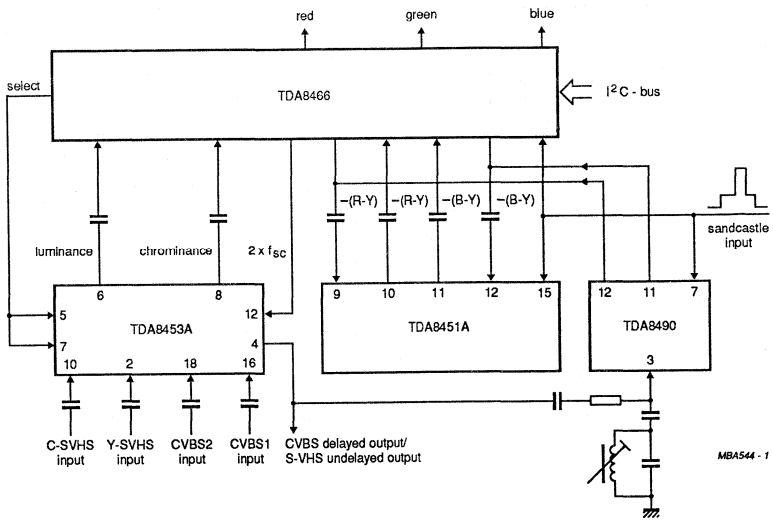


Fig.3 PAL-NTSC-SECAM decoder configuration.

P²CCD FILTER COMBINATION FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8452A is a monolithic integrated P²CCD (Profiled Peristaltic Charge Coupled Device) filter combination which has been designed to be used in conjunction with various colour decoder ICs (e.g. TDA8466, TDA8391). The device incorporates a video input switch, a luminance delay line with different delay lengths for the 3.58 MHz and the 4.43 MHz TV systems, chrominance trap, a chrominance band-pass filter and clock drivers for the filters which are driven from an internal voltage controlled oscillator (VCO) locked to the 2 x f_{sc} signal. The 2 x f_{sc} signal is obtained from the decoder IC.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
analog (pin 2)		$V_{p(a)}$	10.8	12.0	13.2	V
digital (pin 12)		$V_{p(a)}$	10.8	12.0	13.2	V
Supply current						
analog (pin 2)		$I_{p(a)}$	10	20	28	mA
digital (pin 12)		$I_{p(d)}$	20	45	70	mA
CVBS inputs (pins 14 and 16)						
Input signal (peak-to-peak value)		$V_{I(p-p)}$	–	0.7	1.0	V
Luminance output (pin 3)						
output signal (peak-to-peak value)		$V_{3(p-p)}$	–	0.45	–	V
Luminance signal delay						
at 8.87 MHz reference input		t_d	2060	2090	2120	ns
at 7.16 MHz reference input		t_d	2270	2300	2330	ns
Bandwidth	at −3 dB	B	3.7	3.8	–	MHz
Chrominance output (pin 5)						
output signal (peak-to-peak value)		$V_{5(p-p)}$	0.425	0.6	0.85	V
Chrominance filter delay						
at 8.87 MHz reference input		t_d	990	1020	1050	ns
at 7.16 MHz reference input		t_d	1220	1250	1280	ns
Bandwidth (Fig.3)	at −3 dB	B	–	1.15	–	MHz
CVBS output (pin 4)						
output signal (peak-to-peak value)		$V_{4(p-p)}$	–	1.0	–	V
CVBS signal delay						
at 8.87 MHz reference input		t_d	595	625	655	ns
at 7.16 MHz reference input		t_d	730	760	790	ns
Bandwidth (Fig.4)	at −3 dB	B	5.5	6.5	–	MHz
Output resistance		R_O	300	500	800	Ω
Oscillator input signal						
(peak-to-peak value)		$V_{8(p-p)}$	200	–	–	mV

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38GG2).

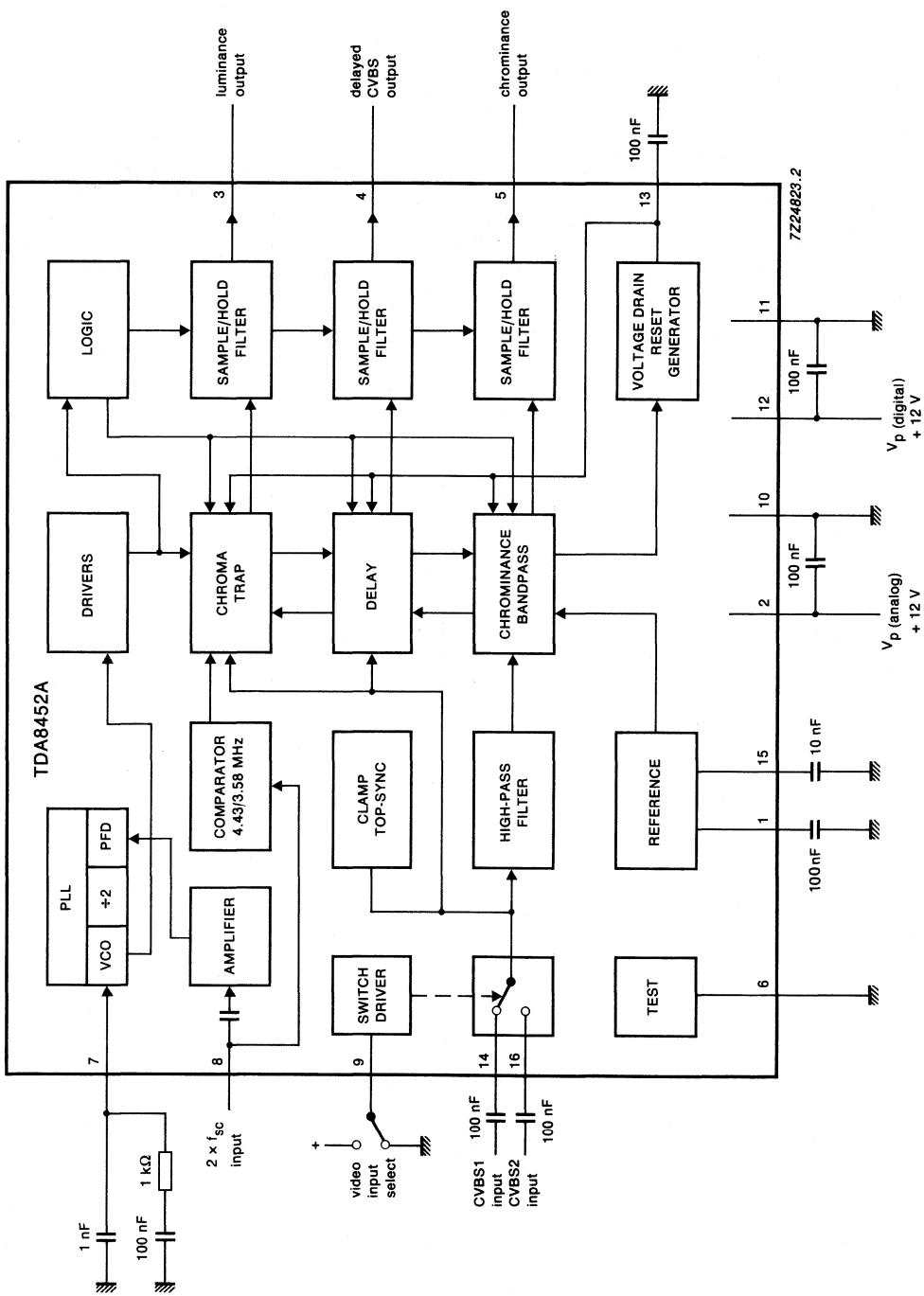


Fig.1 Block diagram.

PINNING

1 Reference decoupling
2 Analog supply voltage input
3 Luminance output
4 Delayed CVBS output
5 Chrominance output
6 Test pin (to be grounded for normal operation)
7 PLL filter
8 2 x f_{sc} input
9 CVBS input select
10 Ground (analog)
11 Ground (digital)
12 Digital supply voltage input
13 Voltage drain reset generator decoupling
14 CVBS1 input
15 Reference decoupling
16 CVBS2 input

FUNCTIONAL DESCRIPTION

The composite video signal (CVBS1 and CVBS2) is applied to pin 14 and/or pin 16. The signal is then routed through three separate paths before being applied to the sample-and-hold filter output stages as follows:

- via a delay line with a delay length of 0.62 μs (for the 4.43 MHz TV system) without filter characteristics. The output signal can be used to drive the sync separation circuit, teletext and SECAM decoders etc.
- via a luminance delay line with chrominance trap with a delay length of 2.09 μs (for the 4.43 MHz TV system). For the 3.58 MHz system the luminance signal will 'skip' part of the delay line so that the total delay of the chrominance signal and the luminance signal are the same (inclusive of the decoder delay and the direct delay of the TDA8451A). The decoder IC, TDA8466, detects whether the subcarrier frequency of the input signal is 3.58 or 4.43 MHz and applies it to the TDA8452A via the DC level of the 2 x f_{sc} reference signal.
- via a chrominance bandpass filter with a delay length of 1.02 μs (for the 4.43 MHz TV system).

The outputs from the delay lines and the bandpass filter are applied to the sample-and-hold low-pass filter output stages which are used to reduce the clock signals.
The reference for the PLL is obtained from the decoder IC which derives the 2 x f_{sc} signal from its reference oscillator (the amplitude of this signal may be small, min. 200 mV(p-p)). The VCO operates at 4 x f_{sc} and the delay lines are 4 phase clocked at $4f_{sc}$.
The P^2CCD filter combination requires a supply voltage of 12 V. The output stages require a higher voltage (approximately 14 V). This voltage is generated internally with a decoupling capacitor connected to pin 13. A circuit for the TDA8452A together with PAL decoder (TDA8391) is illustrated in Fig.5. A circuit for the TDA8452A together with PAL/NTSC decoder (TDA8466) and the SECAM decoder (TDA8490) is illustrated in Fig.6. The TDA8490 can also be used in combination with the TDA8391. Figures 7 and 8 illustrate the luminance and CVBS channel response on T and 2T pulse.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (analog)		$V_p(a)$	–	13.2	V
Supply voltage (digital)		$V_p(d)$	–	13.2	V
Total power dissipation		P_{tot}	–	1.45	W
Operating ambient temperature range		T_{amb}	−25	+70	°C
Storage temperature range		T_{stg}	−55	+150	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}a}$		55	K/W

QUALITY SPECIFICATION

Quality level according to URV-4-2-59/601
(except for pins 14 and 15; 700 V; Human body model)

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C unless otherwise specified (note 1).

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 2) analog		$V_p(a)$	10.8	12.0	13.2	V
Supply current (pin 2) analog		$I_p(a)$	10	20	28	mA
Supply voltage (pin 2) ripple rejection at 100 mVeff	f = 100 Hz	SVRR	–	7	–	dB
Supply voltage (pin 12) digital		$V_p(d)$	10.8	12.0	13.2	V
Supply current (pin 12) digital		$I_p(d)$	20	45	70	mA
Supply voltage (pin 12) ripple rejection at 100 mVeff	f = 100 Hz	SVRR	–	7	–	dB
Total power dissipation		P_{tot}	–	0.78	–	W
Composite video inputs (pins 14 and 16)						
AC coupled and clamped to top sync						
Input signal (peak-to-peak value)		$V_{I(p-p)}$	–	0.7	1.0	V
Input current (non-selected input)		I_I	–	–	0.1	μA
Input current during non-clamping period of selected input		I_I	1.0	3.0	5.0	μA
Input capacitance		C_I	–	5	–	pF
Crosstalk between selected/non-selected channels	R_I = 75 Ω					
at f_{sc} = 1.5 MHz		α	60	65	–	dB
at f_{sc} = 5.0 MHz		α	–	50	–	dB
Video switch control (pin 9)						
Video input (pin 14)		V_9	0	–	1.5	V
Video input (pin 16)		V_9	4	–	V_p	V
Oscillator input signal (pin 8)						
Input signal (peak-to-peak value)	2 x f_{sc}	$V_{8(p-p)}$	200	–	–	mV
Input capacitance		C_I	–	6	–	pF
Input resistance		R_I	–	80	–	kΩ
Input voltage for 3.58 MHz TV system		V_8	6.7	–	V_p	V
4.43 MHz TV system		V_8	0	–	5.3	V

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance signal output (pin 3)						
Output signal (input signal = 0.7 V peak-to-peak value)		$V_{3(p-p)}$	–	0.45	–	V
Black-to-white output signal (CVBS input signal = 0.7 V peak-to-peak value)		$V_{3(p-p)}$	0.23	0.32	0.46	V
Output resistance		R_0	300	500	800	Ω
Output level for top sync		V_3	3.0	–	7.0	V
Luminance output internal load		I_3	0.4	–	1.5	mA
Rest clock signals (RMS value)	note 2					
at 4.43 MHz		$V_{3(rms)}$	–	–	1	mV
at 8.87 MHz		$V_{3(rms)}$	–	–	4	mV
at 17.73 MHz		$V_{3(rms)}$	–	–	12	mV
Signal-to-noise ratio	note 3	S/N	60	65	–	dB
Linearity black-to-white (CVBS input signal = 0.7 V peak-to-peak value)	note 4	$L_{3(p-p)}$	0.95	–	–	
Linearity black-to-white (CVBS input signal = 1.0 V peak-to-peak value)	note 4	$L_{3(p-p)}$	0.94	–	–	
Bandwidth	at −3 dB	B	3.7	3.8	–	MHz
Frequency response with regard to 0 MHz (Fig.2)						
at 2.2 MHz		Δf	−1.0	0.5	2.0	dB
at 3.0 MHz		Δf	−0.5	1.0	2.5	dB
at 3.8 MHz		Δf	−4.0	−2.5	−1.0	dB
at 4.26 MHz		Δf	−19	−16	−10	dB
at 4.43 MHz		Δf	–	−25	−20	dB
at 4.64 MHz		Δf	−19	−12	−10	dB
at 5.5 MHz		Δf	−5.0	−2.5	0	dB
T and 2T response (Fig.7) (CVBS input signal = 0.6 V peak-to-peak value)						
Luminance signal delay						
at 8.87 MHz reference input		t_d	2060	2090	2120	ns
at 7.16 MHz reference input		t_d	2270	2300	2330	ns

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Chrominance signal output (pin 5)						
Output signal (chrominance input signal = 0.465 V peak-to-peak value)		$V_{5(p-p)}$	0.425	0.6	0.85	V
Output resistance		R_0	300	500	800	Ω
DC output level		V_5	3.0	–	7.5	V
Internal load of chrominance output		I_5	0.4	–	1.5	mA
Rest clock signals (RMS value)	note 2					
at 4.43 MHz		$V_{5(rms)}$	–	–	0.2	mV
at 8.87 MHz		$V_{5(rms)}$	–	–	5	mV
at 17.73 MHz		$V_{5(rms)}$	–	–	12	mV
Signal-to-noise ratio	note 3	S/N	60	65	–	dB
Linearity of output signals	note 4					
input = 0.45 V (peak-to-peak value)		$L_{5(p-p)}$	–	0.97	–	
input = 0.65 V (peak-to-peak value)		$L_{5(p-p)}$	–	0.95	–	
Bandwidth (Fig.3)	at −3 dB	B	–	1.15	–	MHz
Frequency response with regard to the top at 4.43 MHz (Fig.3)						
at 0.9 MHz		Δf	–	−22	−17	dB
at 1.9 MHz		Δf	–	−35	−30	dB
at 2.5 MHz		Δf	–	−30	−25	dB
at 3.0 MHz		Δf	–	−20	−16	dB
at 3.8 MHz		Δf	−3.5	−2.5	−1.5	dB
at 4.93 MHz		Δf	−4.0	−3.0	−2.0	dB
at 5.6 MHz		Δf	–	−20	−16	dB
Chrominance filter delay						
at 8.87 MHz reference input		t_d	990	1020	1050	ns
at 7.16 MHz reference input		t_d	1220	1250	1280	ns
Delayed signal output (pin 4)						
Output signal (input signal = 0.7 V peak-to-peak value)		$V_{4(p-p)}$	–	1.0	–	V
Black-to-white output signal (CVBS input signal = 0.7 V peak-to-peak value)		$V_{4(p-p)}$	0.49	0.70	0.98	V
Output resistance		R_0	300	500	800	Ω
Internal load of delayed output		I_4	0.4	–	1.5	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Output sync pulse (input sync pulse = 210 mV peak-to-peak value)		$V_{4(p-p)}$	210	–	–	mV
Output level for top sync		V_4	2.5	–	6.5	V
Rest clock signals (RMS value)	note 2					
at 4.43 MHz		$V_{4(rms)}$	–	–	1	mV
at 8.87 MHz		$V_{4(rms)}$	–	–	5	mV
at 17.73 MHz		$V_{4(rms)}$	–	–	12	mV
Signal-to-noise ratio	note 3	S/N	65	70	–	dB
Linearity black to white (CVBS input signal = 0.7 V peak-to-peak value)	note 4	$L_{4(p-p)}$	0.95	–	–	
Linearity black to white (CVBS input signal = 1.0 V peak-to-peak value)	note 4	$L_{4(p-p)}$	0.94	–	–	
Bandwidth (Fig.4)	at −3 dB	B	5.5	6.5	–	MHz
Frequency response with regard to 2.2 MHz (Fig.4)						
at 0.0 MHz		Δf	−2.5	−1.5	−0.5	dB
at 0.9 MHz		Δf	−2	−1	−0	dB
at at 3.1 MHz		Δf	0	1.0	1.5	dB
at 5.5 MHz		Δf	−3	−1	+0.5	dB
T and 2T response is given in Fig.7 (CVBS input signal = 0.6 V peak-to-peak value)						
CVBS signal delay						
at 8.87 MHz reference input		t_d	595	625	655	ns
at 7.16 MHz reference input		t_d	730	760	790	ns

Notes to the characteristics

1. Unless otherwise specified all figures are related to a CVBS input signal of 0.7 V (peak-to-peak value); 100% contrast; 75% saturation.
   In this condition the input signal is formed by the following components:
   210 mV(p-p) sync pulse
   490 mV(p-p) black-to-white
   465 mV(p-p) chrominance
2. The rest clock signals are measured with an FET probe (3.5 pF capacitor in parallel with a 1 MΩ resistor) connected directly to pins 1 and 3, pins 1 and 4 or pins 1 and 5.
3. The signal-to-noise ratio is specified as: nominal $V_{out(p-p)}/V_{noise(rms)}$ (0-5 MHz) at a CVBS input signal specified in note 1.
4. The linearity is defined as the amplification at the given input voltage swing, divided by the amplification when the input voltage swing is decreased to 70%.

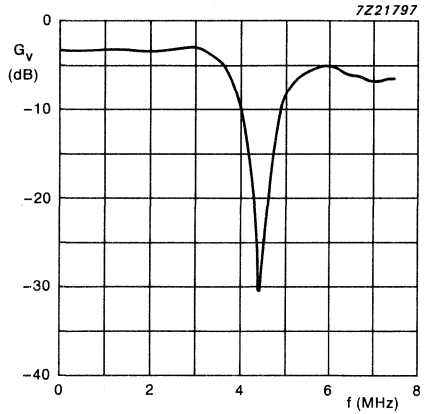


Fig.2 Typical frequency response of luminance signal.

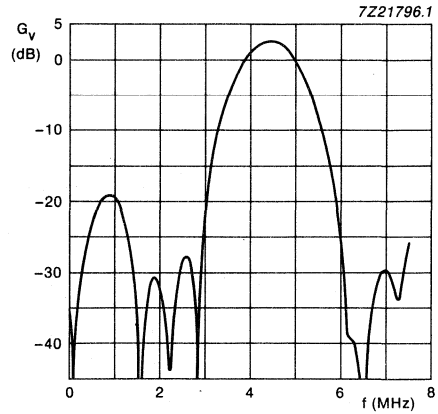


Fig.3 Typical frequency response of chrominance signal.

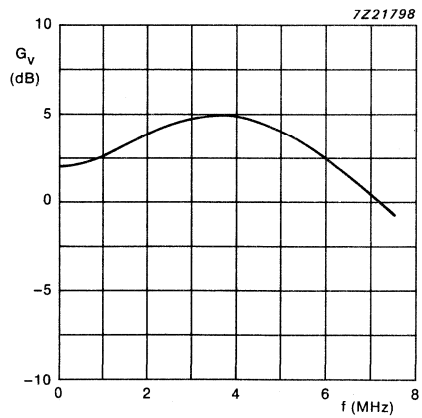


Fig.4 Typical frequency response of delayed signal.

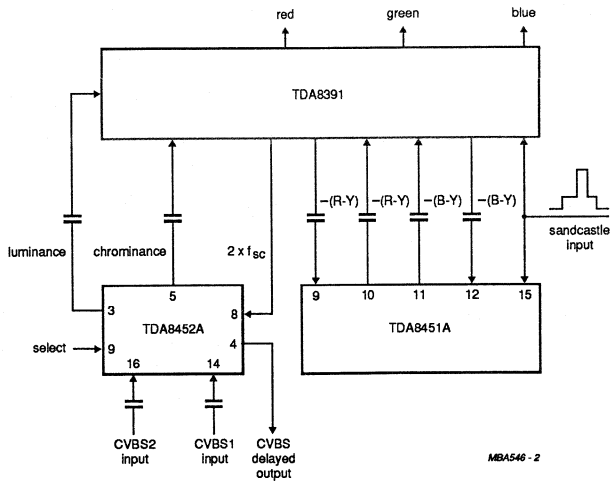


Fig.5 PAL decoder configuration.

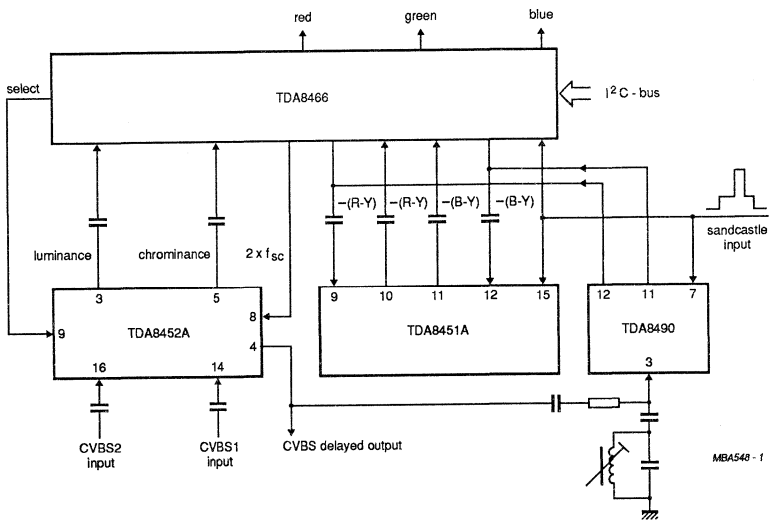


Fig.6 PAL-NTSC-SECAM decoder configuration.

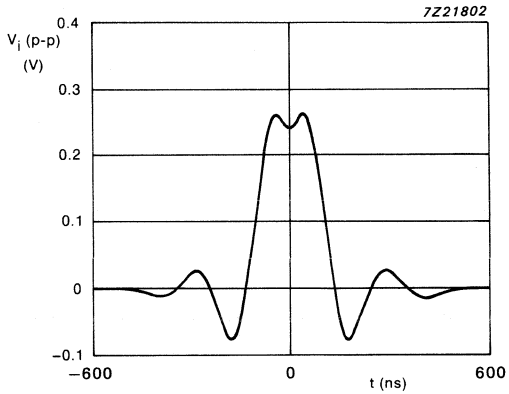


Fig.7(a) Luminance response (T pulse).

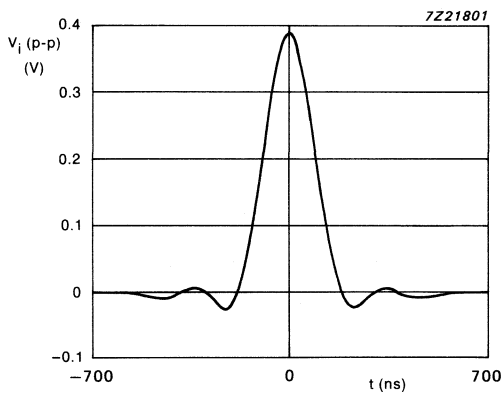


Fig.7(b) Luminance response (2T pulse).

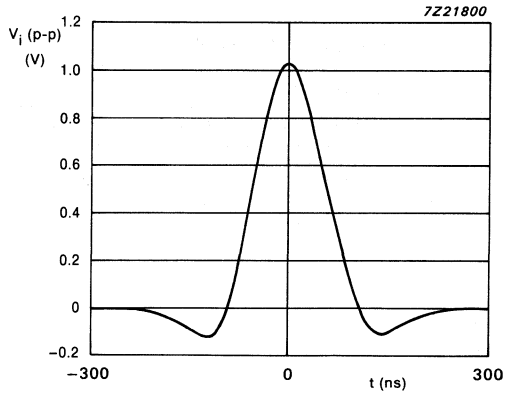


Fig.8(a) CVBS channel response (T pulse).

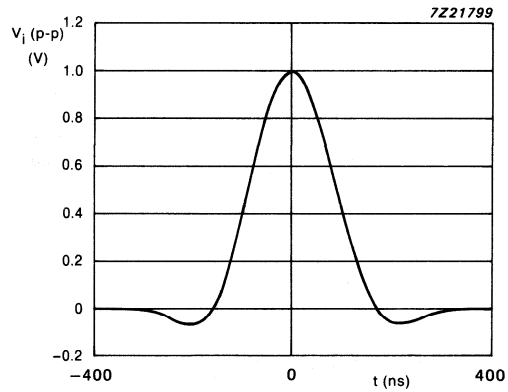


Fig.8(b) CVBS channel response (2T pulse).

P²CCD filter combination for CVBS and S-VHS

TDA8453A

GENERAL DESCRIPTION

The TDA8453A is an integrated P²CCD (Profiled Peristaltic Charge Coupled Device) filter combination which can accommodate CVBS and S-VHS input signals. The device has been designed to be used in conjunction with various colour decoders and incorporates a luminance delay with chrominance trap, a chrominance bandpass filter, a wideband delay line, clock drivers for the filters which are driven from an internal VCO locked to the 2 x f_{sc} signal (obtained from the decoder oscillator), a video switch for three different input signals (2 x CVBS and 1 luminance S-SVHS) and a switch for the chrominance S-VHS. This IC replaces TDA8453.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8453A	18	DIL	plastic	SOT102RG.4

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	supply voltage					
$V_{p(a)}$	analog (pin 3)		10.8	12.0	13.2	V
$V_{p(d)}$	digital (pin 13)		10.8	12.0	13.2	V
	supply current					
$I_{p(a)}$	analog (pin 3)		12	22	30	mA
$I_{p(d)}$	digital (pin 13)		20	50	70	mA
$V_{I(p-p)}$	CVBS input (pins 16 and 18) (peak-to-peak value)		–	0.7	1.0	V
$V_{I(p-p)}$	Y-SVHS input (pin 2) (peak-to-peak value)		–	1.0	1.42	V
$V_{I(p-p)}$	C-SVHS input (pin 10) (peak-to-peak value)		–	660	935	mV
$V_{6(p-p)}$	luminance output for CVBS (pin 6) (peak-to-peak value)		–	0.45	–	V
$V_{6(p-p)}$	luminance output for S-VHS (pin 6) (peak-to-peak value)		–	0.45	–	V
$V_{8(p-p)}$	chrominance output for CVBS (pin 8) (peak-to-peak value)		425	600	850	mV
$V_{8(p-p)}$	chrominance output for S-VHS (pin 8) (peak-to-peak value)		525	594	660	mV
$V_{4(p-p)}$	delayed CVBS output (pin 4) (peak-to-peak value)		–	1.0	–	V
$V_{4(p-p)}$	delayed S-VHS output (pin 4) (peak-to-peak value)		–	0.9	–	V
R_O	output resistance (pins 4, 6 and 8)		300	500	800	Ω
$V_{12(p-p)}$	oscillator input signal (peak-to-peak value)	2 x f_{sc}	200	–	–	mV

P²CCD filter combination for CVBS and S-VHS

TDA8453A

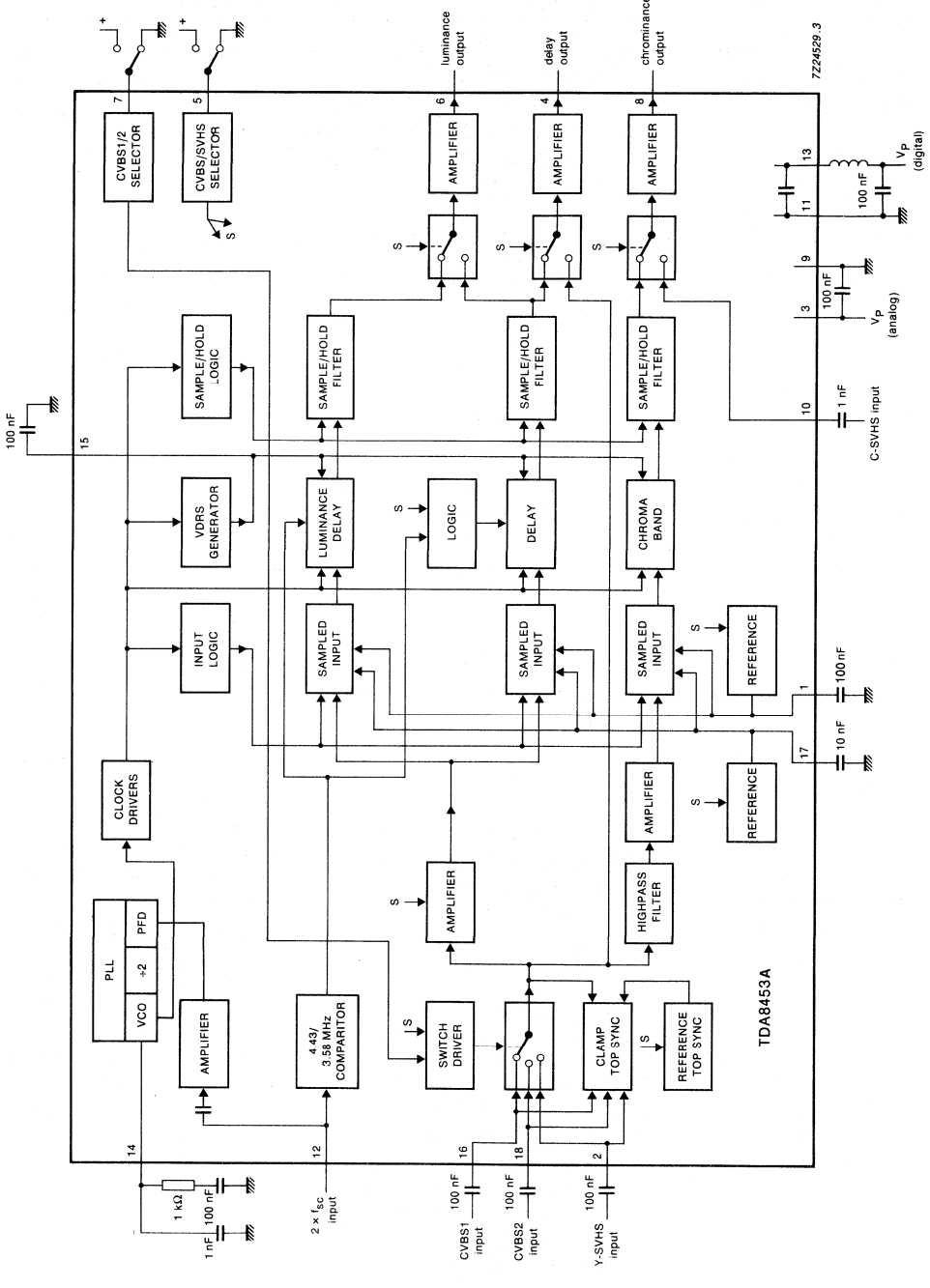


Fig.1 Block diagram.

P²CCD filter combination for CVBS and S-VHS

TDA8453A

FUNCTIONAL DESCRIPTION

The device has four AC-coupled video inputs; CVBS1 (pin 16), CVBS2 (pin 18), luminance S-VHS (Y-SVHS pin 2) and chrominance S-VHS (C-SVHS pin 10).

CVBS1, CVBS2 and S-VHS selectors (pins 5 and 7)

The device can accommodate three different video input signals:

- CVBS1 pins 5 and 7 LOW
- CVBS2 pin 5 LOW, pin 7 HIGH
- S-VHS contains Y-SVHS and C-SVHS; pin 5 HIGH

The slicing level of the CVBS/S-VHS selector and of the CVBS1/CVBS2 selector are different. This means, therefore, that the selectors can be controlled with one signal wire that has three different levels (e.g. by the TDA8466).

CVBS inputs (pins 16 and 18)

When either input is selected by the input switch the signal is routed through three separate paths before being applied to the sample-and-hold filter stages. The paths are via:

- A delay line used to drive the sync separator circuit, teletext and SECAM decoders etc.
- A luminance delay line with chrominance trap
- A chrominance bandpass filter.

The sample-and-hold lowpass filter stages are used to reduce the clock signals. For the 3.58 MHz TV systems the luminance signal will 'skip' part of the delay line to ensure equal delay times in the chrominance and luminance paths.

PINNING

PIN	DESCRIPTION
1	reference decoupling
2	luminance S-VHS input
3	analog supply voltage input
4	delayed CVBS output or undelayed Y-SVHS output
5	CVBS/S-VHS input selector
6	luminance output
7	CVBS1/CVBS2 input selector
8	chrominance output
9	analog ground
10	chrominance S-VHS input
11	digital ground
12	2 x f_{sc} plus 4.43/3.58 MHz selector input
13	digital supply voltage input
14	PLL filter
15	voltage drain reset generator decoupling
16	CVBS1 input
17	reference decoupling
18	CVBS2 input

S-VHS inputs (pins 2 and 10)

If the CVBS/S-VHS selector is in the S-VHS position (pin 5 HIGH), the luminance signal will be routed through two separate paths. The paths are:

- Directly through the input switch to the output switch (pin 4). This signal is used to drive the sync separator circuit
- Via a luminance delay without chrominance trap.

The chrominance S-VHS signal is routed directly to the chrominance output switch (pin 8).
To ensure that the delay of the luminance signal in both the 4.43 MHz and 3.58 MHz TV systems are equal to the total delay of the chrominance S-VHS signal (which is the sum of the delays in the decoder and the delay line IC), the delay line incorporates more stages in the 4.43 MHz TV system than the 3.58 MHz TV system.

Luminance, chrominance and delayed outputs (pins 6, 8 and 4)

The position of the three output switches depends on the selected input (CVBS or S-VHS). The device also incorporates three output amplifiers:

Luminance output (pin 6)

- CVBS luminance delay with chrominance trap
- S-VHS delayed Y-SVHS without chrominance trap

Delay output (pin 4)

- CVBS delayed CVBS signal
- S-VHS undelayed Y-SVHS signal

Chrominance output (pin 8)

- CVBS chrominance bandpass filter with delay
- S-VHS undelayed C-SVHS signal without bandpass filter

Because the amplitude of the CVBS and S-VHS input signals are different, the gain of the input amplifiers and the level of top sync are varied to obtain optimal biasing if S-VHS is selected.

Oscillator (pins 12 and 14)

The reference for the PLL is obtained from the decoder IC which derives the 2 x f_{sc} signal from its reference oscillator (the amplitude of this signal may be small, minimum 200 mV(p-p)). The VCO operates at 4 x f_{sc}, the delay lines and filters are 4 phase clocked at 4 x f_{sc}.
The information whether the incoming signal is 2 x 3.58 MHz or 2 x 4.43 MHz is generated in the decoder IC and fed to the TDA 8453A via the DC level of the 2 x f_{sc} oscillator signal (pin 12). The filter for the PLL is connected to pin 14.

Voltage drain reset generator decoupling (pin 15)

The TDA8453A requires a supply voltage of 12 V. The output stages require a higher voltage (approximately 15 V). This voltage is generated internally with a decoupling capacitor connected to pin 15.

Decoupling reference (pins 1 and 17)

The reference for the sampled inputs of the delay lines and filters are decoupled externally. When S-VHS is selected the reference will vary to give an optimum bias for the sampled input to enable it to adapt to the change in amplification.

A circuit for the TDA8453A together with a PAL decoder (TDA8391) is illustrated in Fig.6. A circuit for the TDA8453A together with a PAL/NTSC decoder (TDA8466) and a SECAM decoder (TDA8490) is illustrated in Fig.7. The TDA8490 can also be used in combination with the TDA8391.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{p(a)}$	analog supply voltage	–	13.2	V
$V_{p(d)}$	digital supply voltage	–	13.2	V
P_{tot}	total power dissipation	–	1.45	W
T_{amb}	operating ambient temperature range	–25	+70	°C
T_{stg}	storage temperature range	–55	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	55	–	K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies (note 1)						
$V_{p(a)}$	analog supply voltage (pin 3)		10.8	12.0	13.2	V
$I_{p(a)}$	analog supply current (pin 3)		12	22	30	mA
SVRR	supply voltage ripple rejection at 100 mVeff (pin 3)	f = 100 Hz	–	7	–	db
$V_{p(d)}$	supply voltage digital (pin 13)		10.8	12.0	13.2	V
$I_{p(d)}$	supply current digital (pin 13)		20	50	70	mA
SVRR	supply voltage ripple rejection at 100 mVeff (pin 13)	f = 100 Hz	–	7	–	dB
P_{tot}	total power dissipation		–	0.86	1.3	W
Composite video inputs (pins 16 and 18)						
AC COUPLED AND CLAMPED ON TOP SYNC (NOTE 2)						
$V_{I(p-p)}$	input signal (peak-to-peak value)		–	0.7	1.0	V
I_I	input current	non-selected input	–	–	0.1	µA
I_I	input current during non-clamping period of selected input		1.0	3.0	5.0	µA
C_I	input capacitance		–	5	–	pF
α	suppression of any other input signal when CVBS1 or CVBS2 is selected (0 to 5 MHz)	R_i = 75 Ω	–	50	–	dB
Y-SVHS input (pin 2)						
AC COUPLED AND CAMPLED ON TOP SYNC; NOTE 3						
$V_{I(p-p)}$	input signal (peak-to-peak value)		–	1.0	1.42	V
I_I	input current	non-selected input	–	–	0.1	µA
I_I	input current during non-clamping period of selected input		1.0	3.0	5.0	µA
C_I	input capacitance		–	5	–	pF
α	suppression of any other input signal when Y-SVHS is selected (0 to 5 MHz)	R_i = 75 Ω	–	50	–	dB
C-SVHS input (pin 10); note 4						
$V_{I(p-p)}$	input signal (peak-to-peak value)		–	660	935	mV
R_I	input resistance		4	6	12	kΩ
C_I	input capacitance		–	4	–	pF
α	suppression of any other input signal when C-SVHS is selected (3.8 to 4.9 MHz)	R_i = 75 Ω	–	50	–	dB
CVBS switch control (pin 7)						
V_7	CVBS1 input (pin 16)	pin 5 LOW	0	–	1.5	V
V_7	CVBS2 input (pin 18)	pin 5 LOW	4	–	V_P	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CVBS/S-VHS switch control (pin 5)						
V_5	CVBS1 or CVBS2 input		0	–	6.8	V
V_5	S-VHS input (pins 2 and 10)		8.2	–	V_P	V
PLL reference input signal (pin 12)						
$V_{12(p-p)}$	input signal (peak-to-peak value)	2 x f_{sc}	200	–	–	mV
C_I	input capacitance		–	6	–	pF
R_I	input resistance		1	–	–	MΩ
V_{12}	DC level for: 4.43 MHz signal 3.58 MHz signal		 0 6.7	 – –	 5.3 V_P	 V V
Luminance signal output (pin 6)						
R_O	output resistance		300	500	800	Ω
V_6	output level for top sync		3	–	7	V
I_6	luminance output internal load		0.4	–	1.5	mA
S/N	signal-to-noise ratio		–	60	–	dB
Luminance signal output for CVBS (pin 5 LOW); note 2						
$V_{6(p-p)}$	output signal (peak-to-peak value)	CVBS input signal = 0.7 V	–	0.45	–	V
$V_{6(p-p)}$	black-to-white output signal (peak-to-peak value)	note 2	225	320	450	mV
$V_{6(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 6	 – – –	 – – –	 1 10 12	 mV mV mV
$L_{6(p-p)}$	linearity black-to-white (peak-to peak-value)	note 7 CVBS input signal = 0.7 V CVBS input signal = 1.0 V	 0.95 0.94	 – –	 – –	
B	bandwidth	at –3 dB	3.7	3.8	–	MHz
Δf	frequency response with regard to 0 MHz (Fig.2) at 2.2 MHz at 3.0 MHz at 3.8 MHz at 4.26 MHz at 4.43 MHz at 4.64 MHz at 5.5 MHz		 –1.0 –0.5 –4.0 –20 – –18 –5.0	 0.5 1.0 –2.5 –15 –25 –12 –2.0	 2.0 2.5 –1.0 –12 –20 –10 1.0	 dB dB dB dB dB dB dB
t_d	luminance signal delay at 8.87 MHz reference input at 7.16 MHz reference input		 2060 2270	 2090 2300	 2120 2330	 ns ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Luminance signal output for S-VHS (pin 5 HIGH); note 3						
$V_{6(p-p)}$	output signal	V_2 = 1 V(p-p)	–	0.45	–	V
$V_{6(p-p)}$	black-to-white output signal (peak-to-peak value)	note 3	225	320	450	mV
$V_{6(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 6	 – – –	 – – –	 1 10 12	 mV mV mV
$L_{6(p-p)}$	linearity black-to-white	note 7 V_2 = 1 V(p-p) V_2 = 1.42 V(p-p)	 0.95 0.94	 – –	 – –	
B	bandwidth	at –3 dB	5.5	6.5	–	MHz
Δf	frequency response with regard to 0 MHz (Fig.3) at 2.2 MHz at 3.0 MHz at 4.43 MHz at 5.5 MHz		 0 0.5 1.0 –1.0	 1.0 1.5 2.0 0.5	 2.5 3.0 3.5 +2.0	 dB dB dB dB
t_d	luminance signal delay at 8.87 MHz reference input at 7.16 MHz		 1045 1010	 1075 1040	 1105 1070	 ns ns
Chrominance signal output (pin 8)						
R_0	output resistance		300	500	800	Ω
V_8	DC output level		3.0	–	7.5	V
I_8	chrominance output internal load		0.4	–	1.5	mA
S/N	signal-to-noise ratio	note 5	–	65	–	dB
Chrominance signal output for CVBS						
$V_{8(p-p)}$	output signal (peak-to-peak value)	$V_{16, 18}$ = 0.465 V(p-p)	425	600	850	mV
$V_{8(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 6	 – – –	 – – –	 0.2 10 12	 mV mV mV
$L_{8(p-p)}$	linearity of output signals	note 7 $V_{16, 18}$ = 0.465 V(p-p) $V_{16, 18}$ = 0.66 V(p-p)	 – –	 0.97 0.95	 – –	
B	bandwidth	at –3 dB	–	1.15	–	MHz
Δf	frequency response with regard to 4.43 MHz (Fig.4) at 0.9 MHz at 1.9 MHz at 2.5 MHz at 3.0 MHz at 3.8 MHz at 4.93 MHz at 5.6 MHz		 – – – – –3.5 –4.0 –	 –20 –35 –30 –20 –2.5 –3.0 –16	 –15 –30 –25 –16 –1.5 –2.0 –14	 dB dB dB dB dB dB dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Chrominance signal output for CVBS						
t_d	chrominance filter delay at 8.87 MHz reference input at 7.16 MHz reference input		 990 1220	 1020 1250	 1050 1280	 ns ns
Chrominance signal output for S-VHS (pin 5 HIGH); note 4						
$V_{8(p-p)}$	output signal (peak-to-peak value)	V_8 = 0.66 V(p-p)	525	594	660	mV
$V_{8(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 6	 – – –	 – – –	 0.2 10 12	 mV mV mV
$L_{8(p-p)}$	linearity of the output signal	note 7 $V_{16, 18}$ = 0.66 V(p-p) $V_{16, 18}$ = 0.935 V(p-p)	 0.97 0.95	 – –	 – –	
B	bandwidth	at –3 dB	6.0	–	–	MHz
Δf	frequency response with regard to 4.43 MHz at 0.9 MHz at 3.0 MHz at 5.6 MHz		 –0.5 –0.5 –1.0	 0 0 0	 +0.5 +0.5 +0.5	 dB dB dB
t_d	chrominance signal delay		–	30	–	ns
Delayed signal output (pin 4)						
R_0	output resistance		300	500	800	Ω
V_4	output level for top sync		2.5	–	7.0	V
I_4	delayed output internal load		0.4	–	1.5	mA
S/N	signal-to-noise ratio	note 5	–	65	–	dB
Delayed signal output for CVBS						
$V_{4(p-p)}$	output signal (peak-to-peak value)	input signal = 0.7 V CVBS(p-p)	–	1.0	–	V
$V_{4(p-p)}$	black-to-white output signal (peak-to-peak value)	note 2	0.49	0.70	0.98	V
$V_{4(p-p)}$	output sync pulse (peak-to-peak value)	input sync pulse = 210 mV(p-p)	210	–	–	mV
$V_{4(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 4	 – – –	 – – –	 1 10 12	 mV mV mV
$L_{4(p-p)}$	linearity black-to-white	note 7 $V_{16, 18}$ = 0.7 V(p-p) $V_{16, 18}$ = 1 V(p-p)	 0.95 0.94	 – –	 – –	
B	bandwidth	at –3 dB	5.5	6.5	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Delayed signal output for CVBS						
Δf	frequency response with regard to 0 MHz (Fig.5)					
	at 0.9 MHz		−0.5	0.5	1.5	dB
	at 2.2 MHz		0	1.0	2.5	dB
	at 3.1 MHz		0	1.5	2.5	dB
	at 5.5 MHz		−3.0	−1.5	0.5	dB
t_d	CVBS signal delay					
	at 8.87 MHzreference input		595	695	655	ns
	at 7.16 MHz reference input		730	760	790	ns
Delayed signal output for S-VHS (pin 5 HIGH); note 3						
$V_{4(p-p)}$	output signal (peak-to-peak value)	V_2 = 1 V(p-p)	–	0.9	–	V
$V_{4(p-p)}$	black-to-white output signal (peak-to-peak value)	note 3	0.55	0.63	0.70	V
$V_{4(p-p)}$	output sync pulse (peak-to-peak value)	input sync pulse = 300 mV(p-p)	210	–	–	mV
$V_{4(rms)}$	rest clock signals (RMS value)	note 4				
	at 4.43 MHz		–	–	1	mV
	at 8.87 MHz		–	–	10	mV
	at 17.73 MHz		–	–	12	mV
$L_{4(p-p)}$	linearity black-to-white	note 7				
		V_2 = 1 V(p-p)	0.95	–	–	
		V_2 = 1.42 V(p-p)	0.94	–	–	
B	bandwidth	at −3 dB	6.0	–	–	MHz
Δf	frequency response with regard to 0 MHz					
	at 2.2 MHz		−0.5	0	0.5	dB
	at 5.5 MHz		−1.0	0	0.5	dB
t_d	Y-SVHS signal delay		–	40	–	ns

Notes to the characteristics

1. To prevent linearities and rest clock signals from deteriorating, it is recommended that the difference between the supply voltages at pins 3 and 13 should be less than 500 mV.
2. Unless otherwise specified all figures are related to a CVBS input signal of 0.7 V(p-p); 100% contrast; 75% saturation.

   In this condition the input signal is formed by the following components:

   210 mV(p-p) sync pulse

   490 mV(p-p) black-to-white

   465 mV(p-p) chrominance
3. The figures are related to a Y-SVHS input signal of 1 V(p-p), 100% contrast. In this condition the input signal is formed by the following components:

   300 mV(p-p) sync pulse

   700 mV(p-p) luminance

Notes to the characteristics

4. The figures are related to a C-SVHS input signal of 660 mV(p-p). This amplitude corresponds to a video signal of 1 V(p-p). 100% contrast and 75% saturation.
5. The signal-to-noise ratio is specified as nominal $V_{out(p-p)}/V_{noise(rms)}$ (0 to 5 MHz).
6. The rest clock signals are measured with an FET probe (3.5 pF in parallel with a 1 MΩ resistor) connected directly to pins 4 and 9, pins 6 and 9 or pins 8 and 9.
7. The linearity is defined as the amplification at the given input voltage swing, divided by the amplification when the input voltage swing is decreased to 70%.

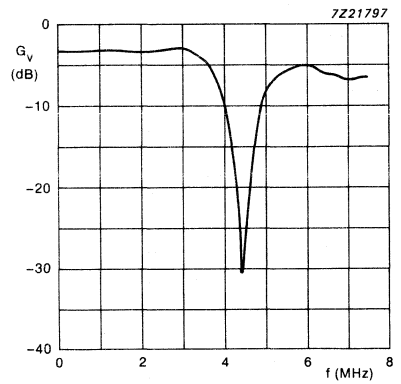


Fig.2 Typical frequency response of luminance signal (CVBS).

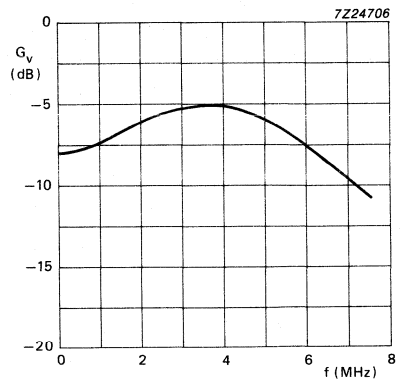


Fig.3 Typical frequency response of luminance signal (S-VHS).

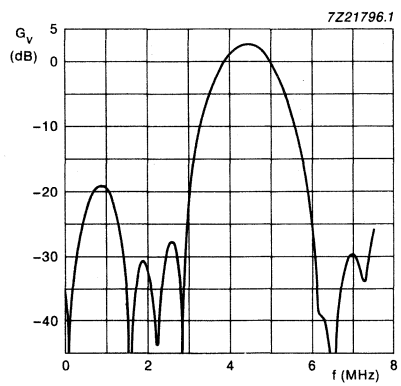


Fig.4 Typical frequency response of chrominance signal (CVBS).

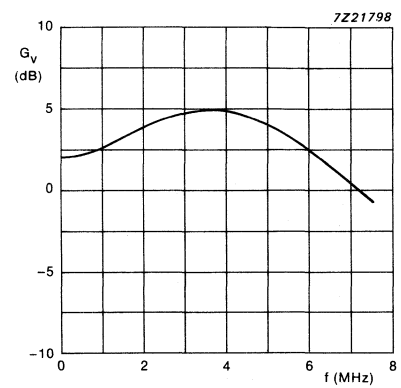


Fig.5 Typical frequency response of delayed signal (CVBS).

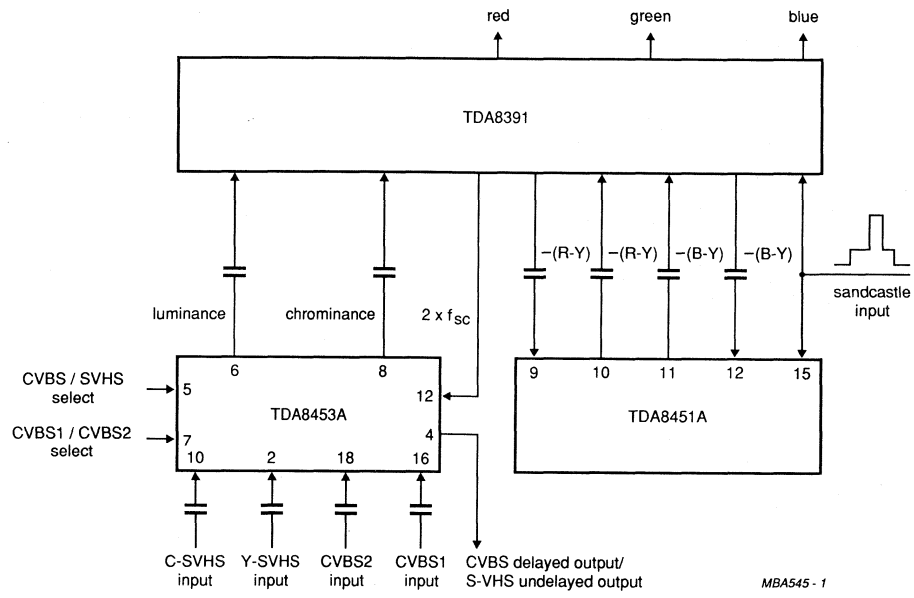


Fig.6 PAL decoder configuration.

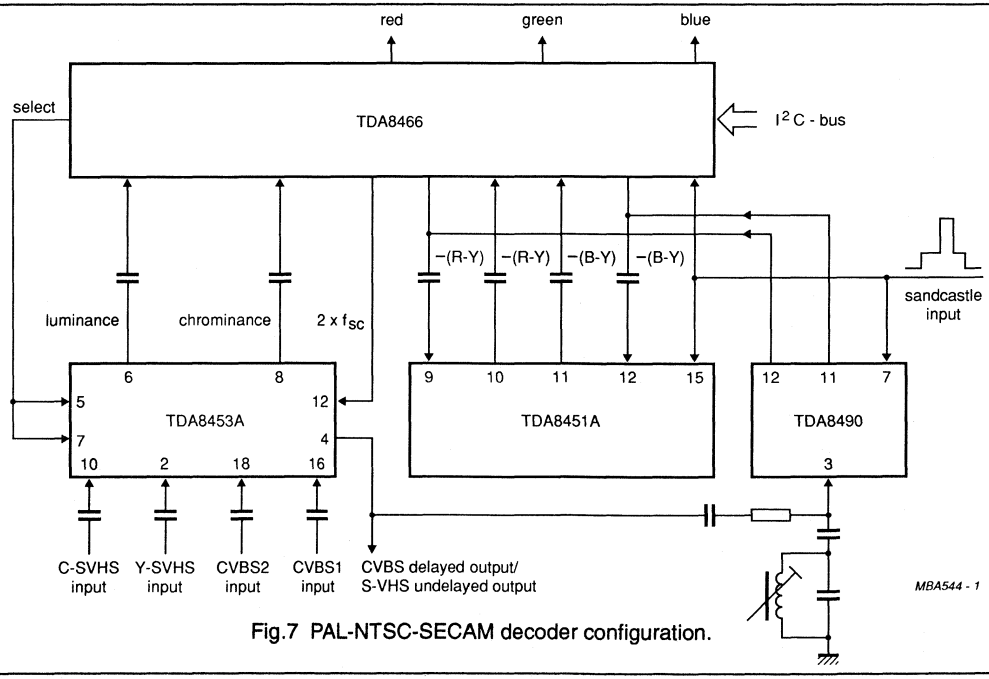


Fig.7 PAL-NTSC-SECAM decoder configuration.

SECAM DECODER

GENERAL DESCRIPTION

The TDA8490 is a monolithic integrated SECAM decoder. This circuit is intended to be used in conjunction with TDA8390 or TDA8461 (PAL decoder), TDA8451 (delay) and TDA8452 (filter). In this application the TDA8490 is placed in parallel with the demodulation circuit of the PAL decoder.

Features

- Limiter input for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Sandcastle pulse detector
- Identification circuit for horizontal and vertical SECAM identification

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_P = V_{9-1}$	10,8	12,0	13,2	V
Supply current		$I_P = I_9$	40	55	70	mA
Chrominance amplifier and demodulator						
Input signal (peak-to-peak value)	SECAM with correct limiting	$V_{3-1(p-p)}$	15	100	300	mV
R-Y and B-Y output						
R-Y output signal amplitude (peak-to-peak value)	pin 12	$V_{12-1(p-p)}$	1,01	1,26	1,51	V
B-Y output signal amplitude (peak-to-peak value)	pin 11	$V_{11-1(p-p)}$	1,28	1,60	1,92	V
Identification						
Input voltage for line identification	pin 4	V_{4-1}	4,1	–	13,2	V
Input voltage for frame identification	pin 4	V_{4-1}	0	–	2,9	V
Switching level for line/frame identification	pin 4	V_{4-1}	3,0	3,5	4,0	V
Sandcastle detector and clamp pulse generator						
Frame blanking detection level		V_{7-1}	1,0	1,5	2,0	V
Line blanking detection level		V_{7-1}	3,0	3,5	4,0	V
Burst gate detection level		V_{7-1}	6,5	7,0	7,5	V

PACKAGE OUTLINE

18-lead DIL; plastic, with internal heat spreader (SOT102).

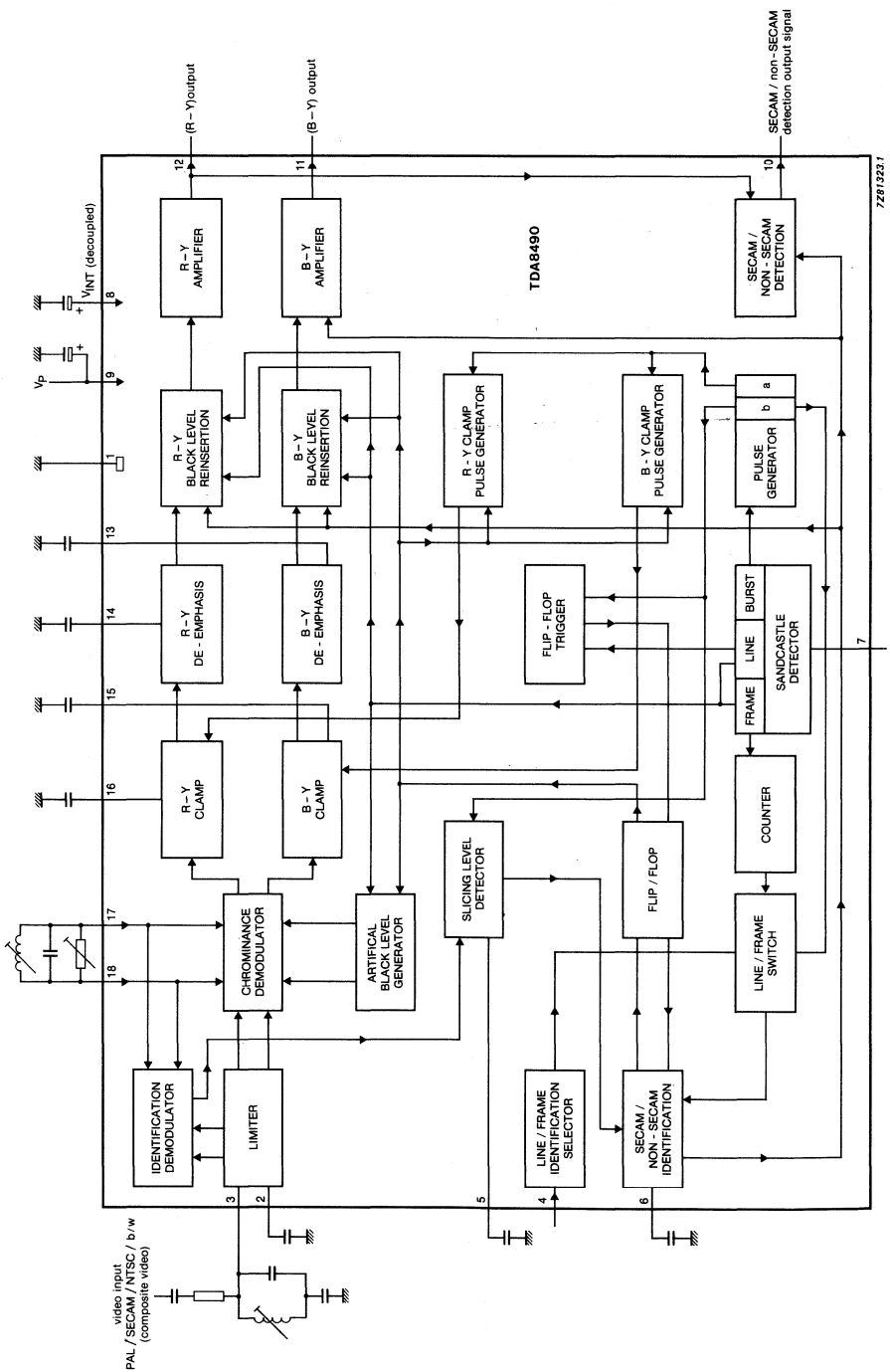


Fig. 1 Block diagram.

PINNING

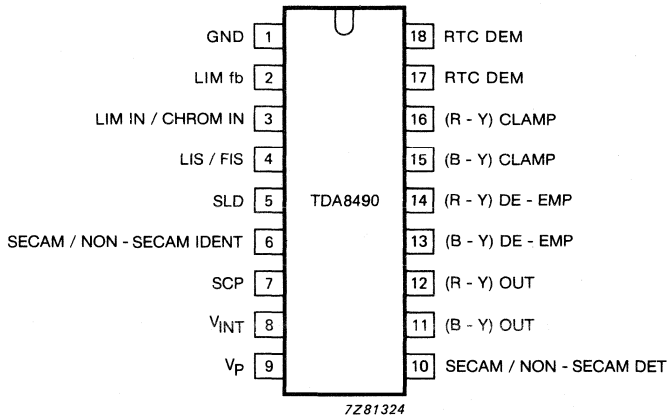


Fig. 2 Pinning diagram.

1	GND	ground	9	V_P	supply voltage
2	LIM fb	limiter feedback	10	SECAM/NON-SECAM DET	SECAM/non-SECAM detection circuit
3	LIM IN/ CHROM IN	limiter input/ chrominance input	11	(B-Y)OUT	(B-Y) signal output
4	LIS/FIS	line identification selector/ frame identification selector	12	(R-Y)OUT	(R-Y) signal output
			13	(B-Y)DE-EMP	(B-Y) de-emphasis circuit
5	SLD	slicing level detector	14	(R-Y)DE-EMP	(R-Y) de-emphasis circuit
6	SECAM/NON-SECAM IDENT	SECAM/non-SECAM identification circuit	15	(B-Y)CLAMP	(B-Y) clamping circuit
			16	(R-Y)CLAMP	(R-Y) clamping circuit
7	SCP	sandcastle pulse input	17	RTC DEM	reference tuned circuit demodulator
8	V_{INT}	internal supply voltage (decoupled)	18	RTC DEM	reference tuned circuit demodulator

FUNCTIONAL DESCRIPTION

Demodulation

The TDA8490 comprises a chrominance and an identification demodulator, both using the same reference tuned circuit. The identification circuit automatically detects whether the incoming signal at pin 3 (applied via a bandpass filter with a bell-shaped response) is SECAM or non-SECAM (NTSC, PAL or black-and-white).

When the SECAM signal is detected, it is applied to a limiter/amplifier after which it is demodulated. The (R-Y) and (B-Y) signals are applied sequentially, therefore, only one demodulator is required. After demodulation the signals are applied to the (R-Y) and (B-Y) clamp circuits, where the black levels are clamped to the same DC level.

Artificial black levels are inserted during line blanking period. The clamp circuits then react upon these levels instead of the demodulated burst signal (necessary in case there are no line burst signals available). The inserted signals may not be identical to the detected black levels, because of circuitry spread. This can be corrected by detuning the demodulator tuned circuit.

R-Y and B-Y output signals

The R-Y and B-Y signals are available every other line. A new black level is reinserted during blanking and timing b (Fig. 5). If a non-SECAM signal is present the R-Y output will generate a DC level of approximately 3,8 V (the same as the black level generated during normal SECAM condition on both outputs). The B-Y output generates a DC level of approximately 0,8 V in this condition.

SECAM or non-SECAM signals may also be identified by the information at pin 10:

- 2,6 V indicates a SECAM signal.
- 0 V indicates a non-SECAM signal.

The SECAM or non-SECAM signals can be identified by using the (B-Y) demodulator output level at pin 11. Depending on the PAL decoder used in conjunction with this device, the information can be passed to the microcomputer via the I^2C bus.

Priority identification

The two chrominance outputs of TDA8490 are connected to the chrominance outputs of the PAL decoder TDA8461 or TDA8390. The output signal of the TDA8490 and PAL decoder alternately determine the priority of the overall system. In the event of a clash on these outputs, caused by a reflected PAL signal being detected as a SECAM signal by TDA8490, the total system will default to PAL priority.

Identification

The identification circuit compares the voltage difference, which is obtained after demodulation, with the state of the flip-flop. For line identification this comparison occurs during the internally generated pulse 'B' (Fig. 3). Only SECAM signals provide voltage difference from line to line during comparison. If the phase relationship between both the signals is incorrect, the flip-flop will receive an extra input pulse.

The identification (as above) occurs when the line identification system is active. When the frame identification system is switched on (pin 4), the system only compares the demodulator output voltage during a 4-line gate pulse, which is present during frame blanking. The 4-line gate pulse starts 10 burst gate pulses after the start of the vertical blanking part of the sandcastle signal. The operation is identical to the line identification. Timing of the 4-line gate pulse is shown in Fig. 4.

Sandcastle detector

The sandcastle pulse detector requires a 3-level sandcastle pulse. It detects the various blanking and gating pulses and generates the correct drive pulses for the clamping circuits (Fig. 3).

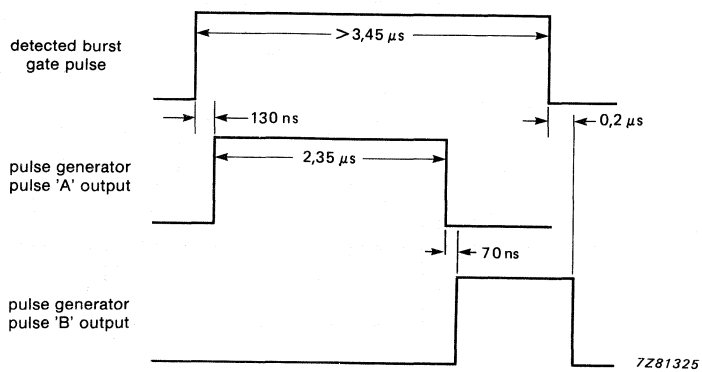


Fig. 3 Burst and derived pulses.

Note

The separated burst pulse is divided into two parts (Fig. 3). Required burst gate pulse: $> 3{,}45\ \mu s$.

Pulse 'A':

- timing R-Y clamp (only present during a red line)
- timing B-Y clamp (only present during a blue line)

Pulse 'B':

- SECAM line identification timing

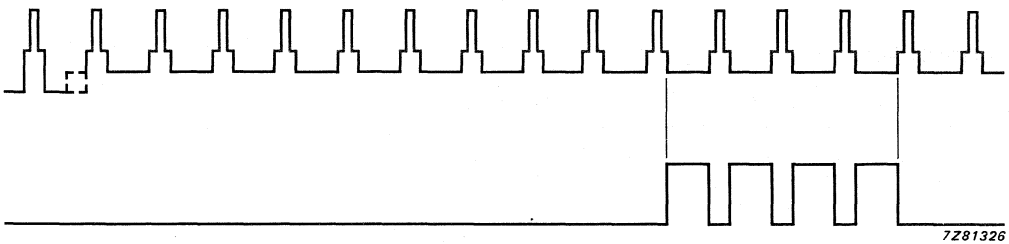


Fig. 4 above: Sandcastle signal during frame period (even and odd).

below: 4-line gate pulse.

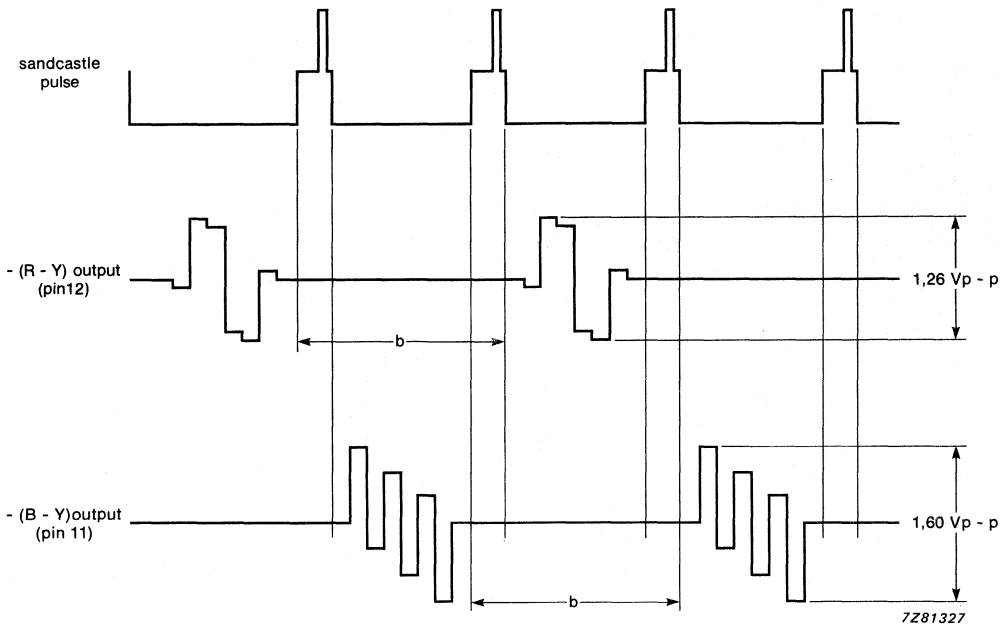


Fig. 5 $-(R\text{-}Y)$ and $-(B\text{-}Y)$ output signals compared to the sandcastle input signal.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 9	V_P	–	13,2	V
Total power dissipation		P_{tot}	–	1,7	W
Storage temperature range		T_{stg}	–25	+ 150	°C
Operating ambient temperature range		T_{amb}	–25	+ 65	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		$V_P = V_{9-1}$	10,8	12,0	13,2	V
Supply voltage	decoupled, pin 8	$V_{INT} = V_{8-1}$	10,6	11,8	13,0	V
Supply current		$I_P = I_9$	40	55	70	mA
Total power dissipation		P_{tot}	–	660	840	mW
Thermal resistance from junction to ambient		$R_{th\ j\text{-}a}$	–	50	–	K/W
External capacitance	pin 8	$C_o = C_{8-1}$	–	–	4,7	μF
Chrominance amplifier and demodulator	note 1					
Input signal (peak-to-peak value)	non-SECAM signal	$V_{3-1(p\text{-}p)}$	–	–	1,1	V
Input signal (peak-to-peak value)	SECAM signal with correct limiting	$V_{3-1(p\text{-}p)}$	15	100	300	mV
Input resistance	pin 3	R_{3-1}	9,5	11,8	14,1	kΩ
Input capacitance	pin 3	C_{3-1}	–	–	5	pF
Input resistance	between pins 17 and 18	R_{17-18}	2,9	3,6	4,3	kΩ
Input capacitance	between pins 17 and 18	C_{17-18}	–	12	–	pF
De-emphasis output resistance	pins 13 and 14	R_{13-1} R_{14-1}	1,45	1,75	2,05	kΩ
Zero point stability of chrominance demodulator	note 2 pins 11 and 12	$f_{11, 12}$	–	5	–	kHz
(B-Y)/(R-Y) gain ratio	note 7		1,38	1,55	1,73	

parameter	conditions	symbol	min.	typ.	max.	unit
R-Y and B-Y output						
R-Y output signal amplitude (peak-to-peak value)	pin 12	$V_{12-1(p-p)}$	1,01	1,26	1,51	V
B-Y output signal amplitude (peak-to-peak value)	pin 11	$V_{11-1(p-p)}$	1,28	1,60	1,92	V
B-Y output signal level	SECAM		3,5	3,8	4,1	V
B-Y output signal level	non-SECAM		–	0,8	1,1	V
R-Y output signal level			3,5	3,8	4,1	V
R-Y signal linearity	note 3		88	95	102	%
B-Y signal linearity	note 4		85	92	99	%
Inserted black levels (demodulated)	function of temperature, note 6		–	0,22	–	kHz/K
Output impedance	pin 12	$\lvert Z_{12-1}\rvert$	–	30	–	Ω
Output impedance	pin 11	$\lvert Z_{11-1}\rvert$	–	30	–	Ω
Identification	SECAM, non-SECAM					
Input voltage for line identification	pin 4	V_{4-1}	4,1	–	13,2	V
Input voltage for frame identification	pin 4	V_{4-1}	0	–	2,9	V
Switching level for line/frame identification	pin 4	V_{4-1}	3,0	3,5	4,0	V
Input current	pin 4	I_4	–	–5	–25	μA
Voltage at pin 6	during non-SECAM	V_{6-1}	–	10,2	–	V
Voltage at pin 6	during SECAM	V_{6-1}	–	7,7	–	V
Identification level at pin 6		V_{6-1}	10,5	10,8	11,0	V
Internal colour 'OFF' (pin 6)	SECAM to non-SECAM	V_{6-1}	9,7	10,0	10,3	V
Internal colour 'ON' (pin 6)	non-SECAM to SECAM	V_{6-1}	8,9	9,2	9,5	V
Colour 'ON' to colour 'OFF' hysteresis	non-SECAM to SECAM	V_{6-1}	0,5	0,8	1,0	V
Voltage at pin 10	during non-SECAM	V_{10-1}	–	1,6	0,5	V
Voltage at pin 10	during SECAM	V_{10-1}	2,1	2,6	3,1	V
Output impedance at pin 10	during SECAM	$\lvert Z_{10-1}\rvert$	1,35	1,60	1,85	kΩ

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle detector and clamp pulse generator	pin 7					
Frame blanking detection level		V_{7-1}	1,0	1,5	2,0	V
Line blanking detection level		V_{7-1}	3,0	3,5	4,0	V
Burst gate detection level		V_{7-1}	6,5	7,0	7,5	V
Input current	V_{7-1} = 0,7 V	I_7	–	–30	–100	μA
Pulse width	see Fig. 3 pulse A		1,85	2,35	2,85	μs
Required pulse width	note 5, see Fig. 3 pulse B		0,6	–	–	μs

Notes to the characteristics

1. For alignment of the reference tuned circuit the input signal on pin 3 must be a SECAM signal at 100 mV(p-p) without deviation during a red and a blue line (black colour information, SECAM). The reference tuned circuit must be aligned to generate a colour output which corresponds to the new reinserted black level information.
2. If the input signal of the limiter is changed from 300 mV(p-p) to 15 mV(p-p), the zero point of the chrominance FM demodulator (f_o is typically 4,33 MHz) will typically shift by 5 kHz.
3. Definition of R-Y linearity = $V_{out\ cyan}/V_{out\ red}$:
   - $f_{nom\ cyan}$ = 4,68 MHz
   - $f_{nom\ red}$ = 4,12 MHz
4. Definition of B-Y linearity = $V_{out\ yellow}/V_{out\ blue}$:
   - $f_{nom\ yellow}$ = 4,02 MHz
   - $f_{nom\ blue}$ = 4,48 MHz
5. The burst gate pulse width must be larger than (2,85 + 0,6)=3,45 μs.
6. Demodulated black level at temperature X = A and at temperature Y = B.
   Artifical black level at temperature X = C and at temperature Y = D.
   Demodulated output signal ($f_o - \Delta f$) at temperature X = E1 and at temperature Y = F1.
   Demodulated output signal ($f_o + \Delta f$) at temperature X = E2 and at temperature Y = F2.

   $$E = \frac{E1 - E2}{2} \text{ and } F = \frac{F1 - F2}{2}$$

   $$\text{specification result} = \frac{(B\text{-}D)/F - (A\text{-}C)/E}{Y\text{-}X} \times \Delta f\ (kHz)/^oC)$$

   for B-Y $f_o = f_{ob}$ = 4,25 MHz and Δf = 230 kHz.
   for R-Y $f_o = f_{or}$ = 4,40625 MHz and Δf = 280 kHz.
7. Due to different deviations (230 or 280 kHz) and correction figures (1,9 or 1,5 x) the total B-Y signal path needs a gain, which is 1,55 x higher than the R-Y path.

APPLICATION INFORMATION

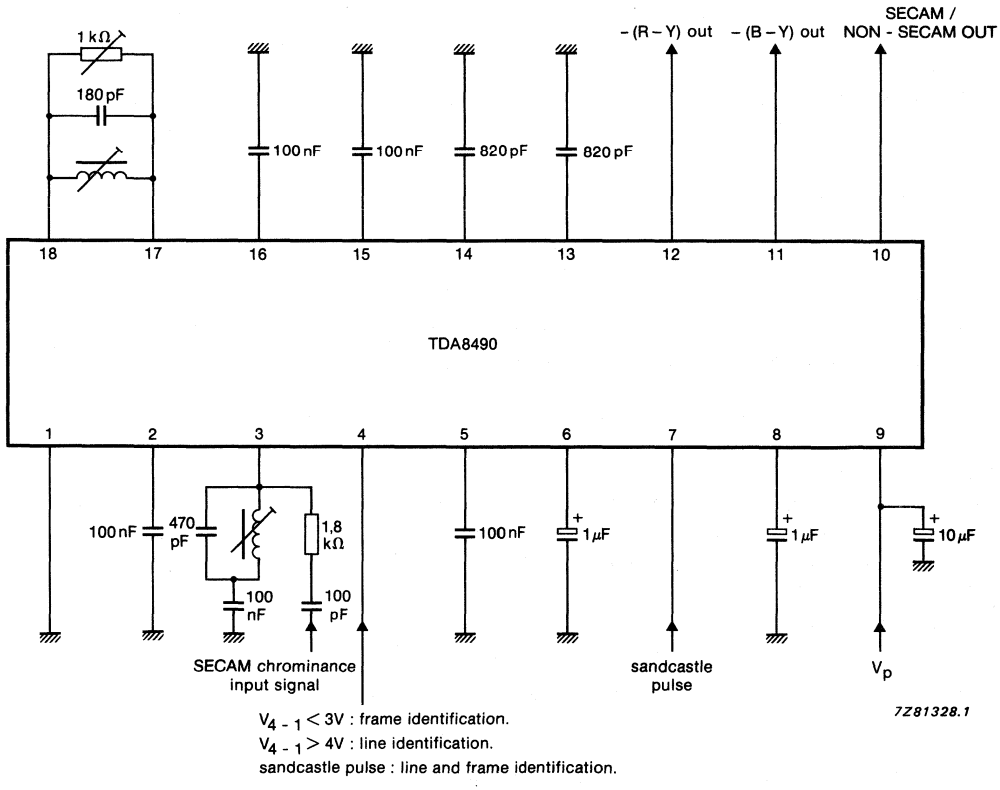


Fig. 6 Application diagram.

4 x 4 video switch matrix TDA8540

GENERAL DESCRIPTION

The TDA8540 is intended for switching between composite video signals, therefore a minimum of four input lines are provided as requested for switching between two S-VHS sources. Each of the four outputs can be set in high impedance state, to enable parallel connection of several devices.

FEATURES

- I²C-bus or the non-I²C-bus mode (controlled by DC voltages)
- S-VHS or CVBS processing
- 3-state switches for all channels
- Selectable gain for the video channels
- Sub-addressing facility
- Slave receiver in the I²C mode
- Auxiliary logic outputs for audio switching
- System expansion possible up to 7 devices (28 sources)
- Static short-circuit proof outputs
- ESD protections

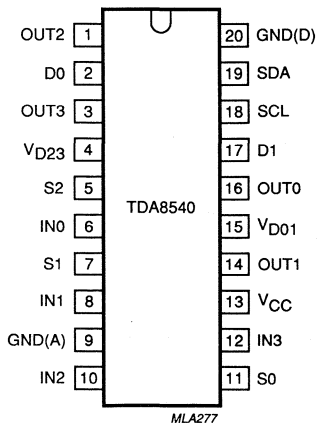


Fig.1 Pinning diagram.

APPLICATIONS

- CTV receivers
- Peritelevision sets
- Satellite receivers

PINNING

SYMBOL	PIN	DESCRIPTION
V_{CC}	13	supply voltage
GND (A)	9	analog ground
GND (D)	20	digital ground
V_{D23}, V_{D01}	4, 15	driver supplies
OUT0 to OUT3	16, 14, 1, 3	video outputs
IN0, IN1	6, 8	video inputs (CVBS or chrominance signal)
IN2, IN3	10, 12	video inputs (CVBS or luminance signal)
S0 to S2	11, 7, 5	sub-addresses inputs
SCL	18	serial clock line input
SDA	19	serial data line input/output
D0, D1	2, 17	control outputs

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.2	-	8.8	V
I_{CC}	supply current		-	20	30	mA
α_{OFF}	isolation "OFF" state	note 1	60	80	-	dB
B	3 dB bandwidth		12	-	-	MHz
α	crosstalk attenuation between channels		+60	+70	-	dB

Note

1. Measured at f = 5 MHz

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8540	20	DIL	plastic	SOT146EE7
TDA8540T	20	SO	plastic	SOT163A

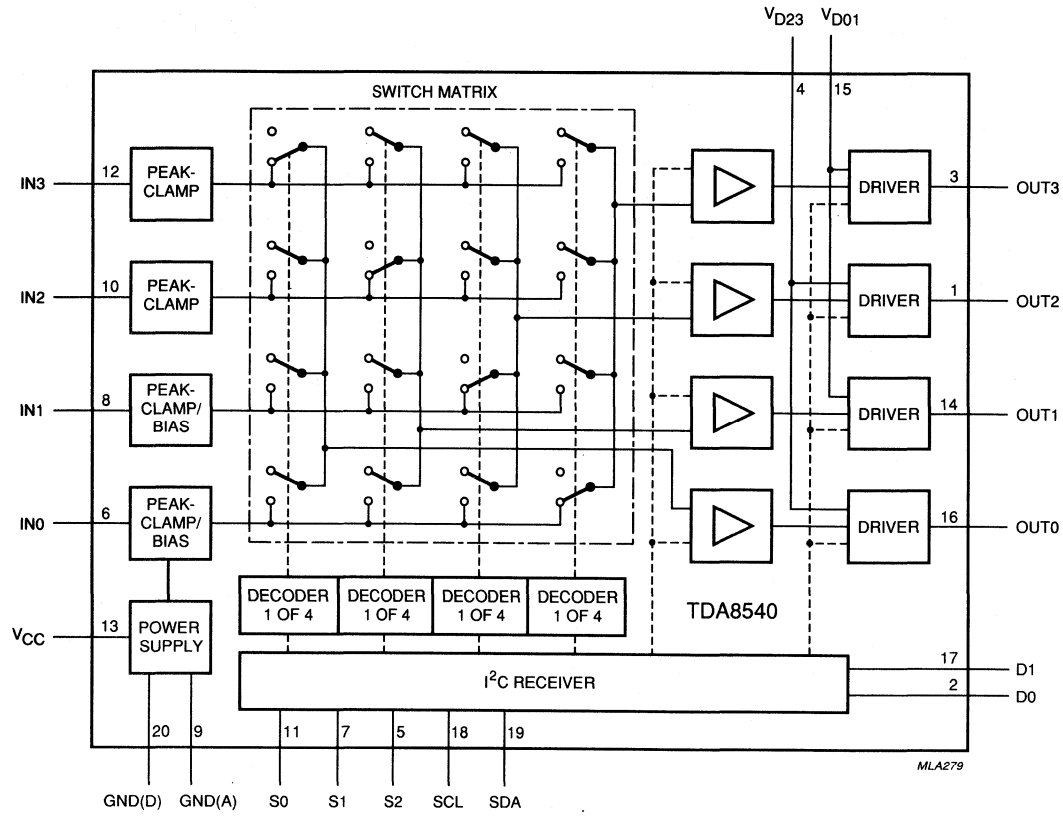


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	9.1	V
P_{tot}	total power dissipation	-	750	mW
T_{stg}	storage temperature range	−55	+125	°C
V_{D01}, V_{D23}	voltage range for the driver supplies	−0.3	13.8	V
IN0 to IN3	voltage range for video inputs	−0.3	7.2	V
OUT0 to OUT3	voltage range for video outputs	−0.3	7.2	V
D0, D1	voltage range for control outputs	−0.3	7.2	V
SDA, SDL	voltage range for I^2C input/output	−0.3	8.8	V
S0 to S2	voltage range for sub-addresses inputs	−0.3	8.8	V

FUNCTIONAL DESCRIPTION

The TDA8540 is controlled via a bidirectional I²C-bus. 3 bits of the I²C address can be selected via sub-address input pins, thus providing a facility for parallel operation of 7 devices.
Control options via the I²C-bus:

- the input signals can be clamped at their negative peak (top sync).
- the gain factor of the outputs can be selected between 1x or 2x.
- each of the four outputs can individually be connected to one of the four inputs.
- each output can individually be set in a high impedance state.
- two binary output data lines can be controlled for switching accompanying sound signals.

The SDA and SCL pins can be connected to the I²C-bus or to DC switching voltage sources.
Address inputs S0 to S2 are used for selection of sub-addresses or to switch the device to the non I²C mode. Inputs S0, S1, S2 can be connected to the supply voltage (H) or the ground (L). In this way no peripheral components are required for selection.

I²C-bus control

After power-up the outputs are switched in the high impedance state, and D0, D1 are at a low level. Detailed information on I²C-bus is available on request.

The slave receiver protocol (see Fig.3)

The TDA8540 behaves like a slave receiver as defined by the I²C-bus specifications.
S : start condition, A : acknowledge bit (generated by TDA8540), P : Stop condition.

Table 1 I²C-bus sub-addressing

S2	S1	S0	SUB-ADDRESS		
			A2	A1	A0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I²C addressable		

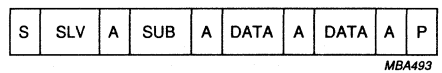


Fig.3 I²C-bus slave receiver protocol.

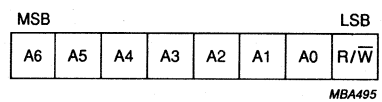


Fig.4 I²C-bus slave address byte SLV.

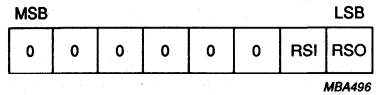


Fig.5 Selection byte SUB.

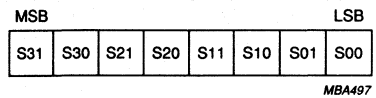


Fig.6 SWI register contents.

For J = 0 to 3

SJI, SJO	00	01	10	11
OUTJ	IN0	IN1	IN2	IN3

MBA494

Fig.7 Selection table for SWI register contents.

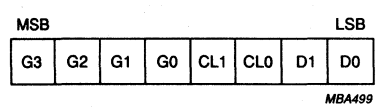


Fig.8 GCO register contents.

The slave address byte (SLV)

The data transmission starts with the slave address SLV, see Fig. 4, A6 = 1, A5 = 0, A4 = 0, A3 = 1. A2, A1, A0 are pin programmable slave address bits, R/$\overline{W}$ = 0 (Write only).

The SUB byte

The SLV address is followed by the SUB byte (see Fig.3, 5) which is needed for the selection of the control functions of the TDA8540.
If SUB = 00H : access to switch control (register SWI, see Fig.7).
If SUB = 01H : access to Gain/Clamp/Data control (register GCO, see Fig.8).
If SUB = 02H : access to Output Enable control (register OEN, see Fig.9).
If more than one data byte is sent, the SUB byte is automatically incremented and if more than 3 data bytes are sent, the interval counter rolls over and the device rewrites the first register.

The data bytes

The data bytes (see Fig.3) are used to determine the setting of the control functions of the TDA8540. The data bytes to be stored in a control register are described in the following sections.

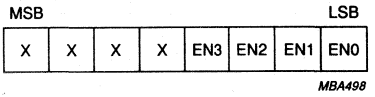


Fig.9 OEN register contents.

SWITCH CONTROL

If SUB = 00H : access to switch control register SWI.
The setting of the switch matrix can be determined by the contents of the SWI register, see Fig.6. Example: if S21 = 0 and S20 = 1 (j = 2), then the OUT2 is connected to IN2, see Fig.7.

GAIN/CLAMP/DATA CONTROL

If SUB = 01H : access to Gain/Clamp/Data control register GCO, see Fig.8.

- Selects the gain of each output; for j = 0 to 3 : if Gj = 0 (respectively 1), then output j has a gain of 2x (respectively 1x)
- Selects clamp action, or mean value on inputs 0 and 1: for CLO (respectively CL1) = 0), input signal on IN0 (respectively IN1) is clamped
- Determines the value of the auxiliary outputs D1 and D0: for j = 0, 1 : if Dj = 0 (respectively 1), TTL Output j is LOW (respectively HIGH)

OEN REGISTER CONTENTS

If SUB = 02H : access to Output Enable control register OEN, see Fig.9.

Table 2

SCL-SDA	0, 0	0, 1	1, 0	1, 1
OUT3	IN3	IN2	IN1	IN0
OUT2	IN2	IN3	IN0	IN1
OUT1	IN1	IN0	IN3	IN2
OUT0	IN0	IN1	IN2	IN3

- Selects the state for each output, active or high impedance: for j = 0 to 3, ENj = 0 (respectively 1) : OUT J in high impedance state (respectively ACTIVE)

After a power-on reset :

- all outputs are switched in the high impedance state
- all outputs are connected to IN01
- the gains are set at 2x
- the inputs IN1 and IN2 are clamped

Note : The device needs reprogramming after a power-on reset due to the four previous mentioned default conditions.

Non I²C-bus control

The device enters the non-I²C mode when S_0, S_1 and S_2 are connected to V_{CC}.

AFTER A POWER-ON RESET

- gain is set at 2x for all outputs
- all inputs are clamped
- all outputs are active
- the matrix position is given by the voltage level of SDA and SCL

SCL AND SDA ARE OPERATING AS NORMAL INPUTS PINS:

- SCL interchanges (OUT3/2) with (OUT1/0)
- SDA interchanges OUT3 with OUT2, and OUT1 with OUT0.

Note :

The clamp action has to be overruled by the external bias command for use with chrominance signals.

OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{amb}	operating ambient temperature range		0	-	70	°C
V_{CC}	supply voltage		7.2	-	8.8	V
Video inputs (pins 6, 8, 10 and 12)						
C_I	external capacitor		-	100	-	nF
V_I	C signal amplitude (peak to peak value)	note 1	-	-	1	V
V_I	CVBS or Y-signal amplitude (peak to peak value)	note 2	-	-	1.5	V
Video drivers (pins 4, 15)						
R_D	external collector resistor	note 3	-	25	-	Ω
C_D	external decoupling capacitor	note 4	-	22	-	µF
Sub-address S0, S1, S2 (pins 5, 7, 11)						
V_{IH}	input voltage HIGH		4	-	V_{CC}	V
V_{IL}	input voltage LOW		0	-	1	V

Notes

1. Only for pins 6, 8 when clamp action is not selected on these pins.
2. On all the video input pins, when the non-I²C bus control mode is selected or when clamp action is selected on pins 6 and 8 (by I²C bus control).
3. Between V_{CC} and pin 4 or pin 15.
4. Between GND (A) and pin 4 or pin 15.

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; gain condition, clamp condition and OFF state are controlled by the I²C bus unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{CC}	supply current		-	20	30	mA
Video inputs : IN0 to IN3 when the clamp is active (note 1)						
I_{LI}	video inputs leakage current	V_I = 3 V	-	0.4	1	µA
V_{clamp}	video input clamp level	I_I = 5 µA	2.1	2.3	2.5	V
I_{clamp}	video inputs clamp current	V_I = 0 V	1.2	-	-	mA
Video inputs : IN0 and IN2 when the clamp is not active (note 1)						
V_{bias}	DC level	I_I = 0	2.6	2.8	3	V
R_I	input resistance		-	10	-	kΩ
Video outputs : OUT0 to OUT3 (note 2)						
Z_O	output impedance in 'OFF' state		100	-	-	kΩ
R_O	output resistance		-	5	-	Ω
α_{OFF}	isolation (OFF state)	f = 5 MHz	60	-	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video outputs : OUT0 to OUT3 (note 2)						
V_{sync}	output top sync level (Y or CVBS)		0.4	0.7	1	V
V_{bias}	output mean value for chrominance signals	G = 2, load = 150 Ω	1.4	1.7	2.0	V
		G = 1, without load	1	1.3	1.6	V
G_1	voltage gain	f = 1 MHz	−1	0	+1	dB
G_2	voltage gain	f = 1 MHz	+5	+6	+7	dB
d_G	differential gain	note 3	-	0.5	3	%
d_φ	differential phase	note 3	-	-	2	deg
DL	non linearity	note 4	-	0.5	2	%
α	crosstalk between channels	note 5	60	70	-	dB
RR	supply voltage rejection	note 6	36	55	-	dB
$\lvert\Delta G\rvert$	bandwidth	100 kHz < f < 5 MHz		0.5		MHz
		100 kHz < f < 8.5 MHz	-	1	-	MHz
		100 kHz < f < 12 MHz		3		MHz
αI^2C	crosstalk attenuation of bus signals		60	-	-	dB
Auxiliary outputs D0, D1 (open collector)						
I_{OH}	input current HIGH	V_{OH} = 5.5 V	-	-	10	μA
V_{OL}	output voltage LOW	I_{OL} = 4 mA	-	-	0.4	V
I²C-bus inputs SCL, SDA						
I_{IH}	input current HIGH	V_{IH} = 3.0 V	-	-	10	μA
I_{IL}	input current LOW	V_{IL} = 1.5 V	−10	-	-	μA
C_I	input capacitance		-	-	10	pF
I²C-bus output SDA						
V_{OL}	output voltage	I_{OL} = 3 mA	-	-	0.4	V
Sub-address S0, S1, S2						
I_{IH}	input current HIGH	$V_{IH} = V_{CC}$	-	-	10	μA
$-I_{IL}$	input current LOW	V_{IL} = 0 V	-	-	20	μA

Notes

1. The simplified circuit is given by Fig. 10 for the IN0 and IN1 inputs and by Fig. 11 for the IN2 and IN3 inputs.
2. Fig. 12 gives a simplified circuit of the output stage of the driver.
3. Gain set at 2x, output loaded with 150 Ω, test signal D2 from CCIR 330.
4. Gain set at 2x, output loaded with 150 Ω, test signal D1 from CCIR 17.
5. Measured from any selected input to output; f = 5 MHz, output loaded with 150 Ω, gain = 2x, $V_{I(p-p)}$ = 1.5 V.
6. Supply ripple rejection is 20 log $\frac{V_{r\,supply)}}{V_{r\,output}}$ measured at f = 1 kHz with $V_{r(supply\ max.)}$ = 100 $mV_{(p-p)}$. The supply voltage rejection ratio is higher than 36 dB at $f_{max.}$ = 100 kHz.

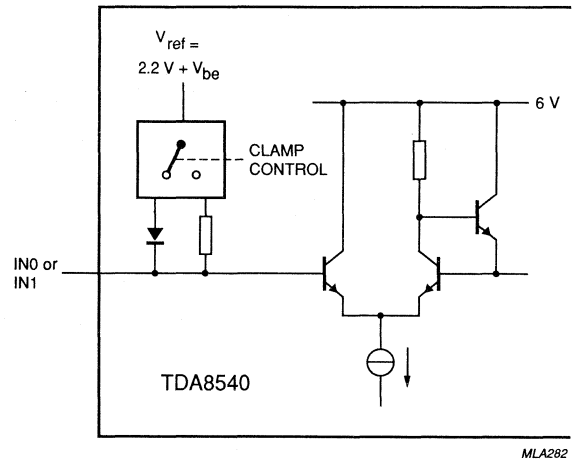


Fig.10 IN0 and IN1 inputs.

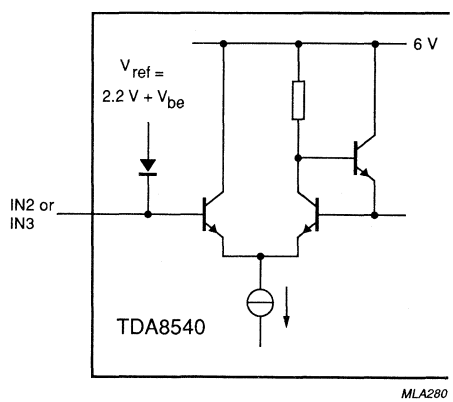


Fig.11 IN2 and IN3 inputs.

APPLICATION DIAGRAM

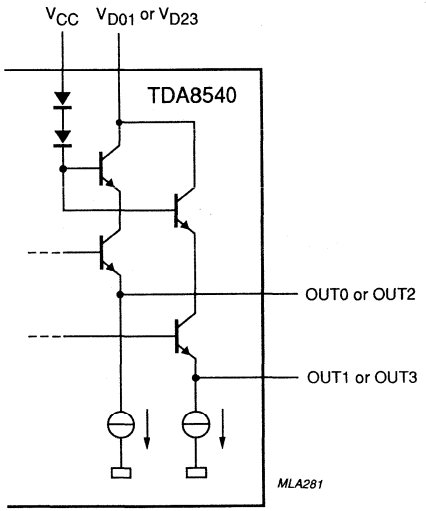


Fig.12 Driver output stage.

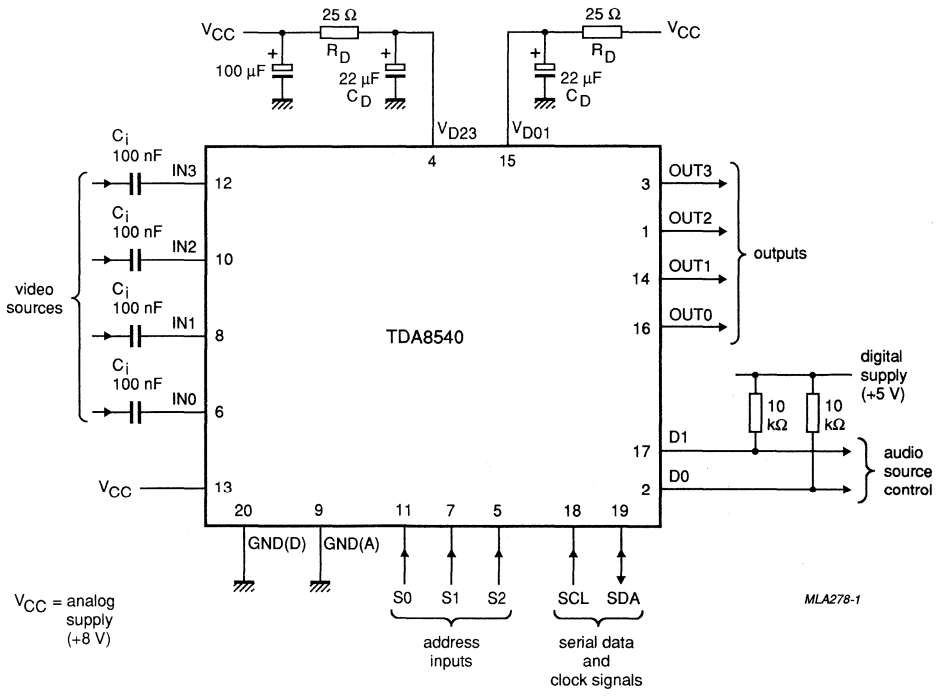


Fig.13 Application diagram.

Philips Semiconductors

Data sheet	
status	Product specification
code	
date of issue	March 1991

TDA8702/TDA8702T

8-bit video digital-to-analog converter

FEATURES

- 8-bit resolution
- Conversion rate up to 30 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Digital TV including:
  - field progressive scan
  - line progressive scan
- Subscriber TV decoders
- Satellite TV decoders
- Digital VCRs.

DESCRIPTION

The TDA8702 is a monolithic bipolar 8-bit digital-to-analog converter (DAC) for video and other applications. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 30 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	-	26	32	mA
I_{CCD}	digital supply current	note 1	-	23	30	mA
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	Z_L = 10 kΩ Z_L = 75 Ω	−1.45 −0.72	−1.60 −0.80	−1.75 −0.88	V V
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
f_{CLK}	maximum conversion rate		30	-	-	MHz
B	−3 dB bandwidth	f_{CLK} = 30 MHz	-	150	-	MHz
P_{tot}	total power dissipation		-	250	340	mW

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8702	16	DIL	plastic	SOT38GE1
TDA8702T	16	SO16	plastic	SOT162A

Notes to the Quick Reference Data

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

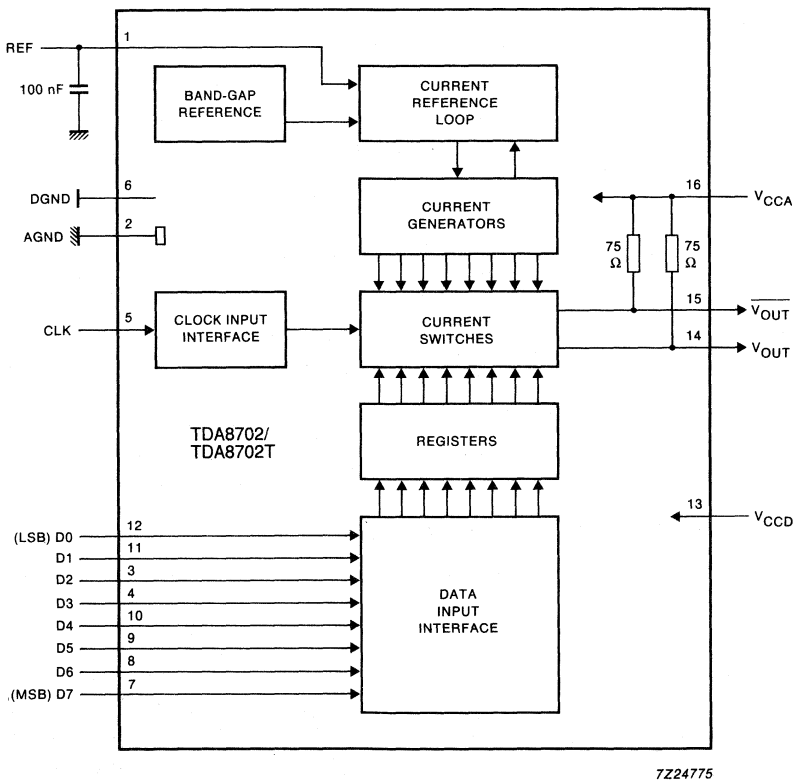


Fig.1 Block diagram.

8-bit video digital-to-analog converter TDA8702/TDA8702T

PIN CONFIGURATION

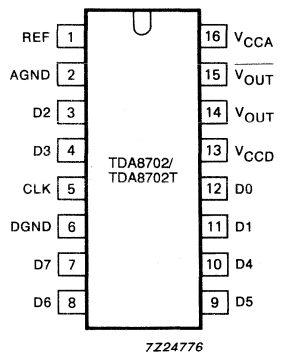


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input, bit 2
D3	4	data input, bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input, bit 7
D6	8	data input, bit 6
D5	9	data input, bit 5
D4	10	data input, bit 4
D1	11	data input, bit 1
D0	12	data input, bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$\overline{V_{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	− 0.3	+ 7.0	V
V_{CCD}	digital supply voltage range	− 0.3	+ 7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differential	− 0.5	+ 0.5	V
AGND – DGND	ground voltage differential	− 0.1	+ 0.1	V
V_I	input voltage range (pins 3 to 5 and 7 to 12)	− 0.3	V_{CCD}	V
I_{14}/I_{15}	total output current range (pins 14 and 15)	− 5	+ 26	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
T_j	junction temperature	-	+125	°C

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT38GE1	+ 85	K/W
$R_{th\ j\text{-}a}$	SOT162A	+110	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2 = 4.5$ V to 5.5 V; $V_{CCD} = V_{13} - V_6 = 4.5$ V to 5.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; V_{REF} decoupled to AGND by a 100 nF capacitor; $T_{amb} = 0$ °C to 70 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	-	26	32	mA
I_{CCD}	digital supply current	note 1	-	23	30	mA
AGND – DGND	ground voltage differential		–0.1	-	+0.1	V
Inputs DIGITAL INPUTS (D7 – D0) AND CLOCK INPUT (CLK)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	-	–0.3	–0.4	mA
I_{IH}	input current HIGH	$V_I = 2.7$ V	-	0.01	20	µA
f_{CLK}	maximum clock frequency		30	-	-	MHz
Outputs (note 2; referenced to V_{CCA})						
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltages	$Z_L = 10$ kΩ	–1.45	–1.61	–1.75	V
	(peak- to-peak value)	$Z_L = 75$ Ω	–0.72	–0.80	–0.88	V
V_{offset}	analog offset output voltage	code = 0	-	–3	–25	mV
ΔV_{OUT}	full-scale analog output voltage temperature coefficient		-	-	200	µV/K
ΔV_{offset}	analog offset output voltage temperature coefficient		-	-	20	µV/k
B	–3 dB bandwidth	note 3; f_{CLK} = 30 MHz	-	150	-	MHz
G_d	differential gain		-	0.6	-	%
ϕd	differential phase		-	1	-	deg
Z_o	output impedance		-	75	-	Ω

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer function (f_{CLK} = 30 MHz)						
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
Switching characteristics (f_{CLK} = 30 MHz; notes 4 and 5; see Figs 3 4 and 5)						
$t_{SU;\,DAT}$	data set-up time		−0.3	-	-	ns
$t_{HD;\,DAT}$	data hold time		2	-	-	ns
t_{PD}	propagation delay time		-	-	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	-	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	-	6.5	8.0	ns
t_d	input to 50% output delay time		-	3.0	5.0	ns
Output transients (glitches; f_{CLK} = 30 MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	-	-	30	ns

Notes to the characteristics

1. D0 to D7 connected to V_{CCD}, CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).
4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $V_{\overline{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data are latched at the rising-edge of the clock. The output voltage remains stable (independent of input data variations) during the high level of the clock (CLK = HIGH). During LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages, see Fig.5).
5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising-edge of the clock and still be recognized. The data hold time ($t_{HD;\,DAT}$) is the minimum period following the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising-edge of the clock and still be recognized.
6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling-edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of offset voltage)

CODE	BINARY INPUT DATA (D7 – D0)	DAC OUTPUT VOLTAGES			
		Z_L = 10 kΩ		Z_L = 75 Ω	
		$V_{\overline{OUT}}$ (V)	V_{OUT} (V)	$V_{\overline{OUT}}$ (V)	V_{OUT} (V)
0	000 00 00	0	–1.6	0	–0.8
1	000 000 01	–0.006	–1.594	–0.003	–0.797
.	. . . . .				
128	100 000 00	–0.8	–0.8	–0.4	–0.4
.	. . . . .				
254	111 111 10	–1.594	–0.006	–0.797	–0.003
255	111 111 11	–1.6	0	–0.8	0

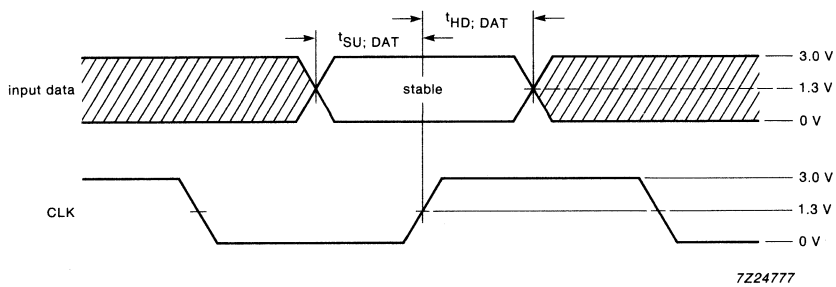


Fig.3 Data set-up and hold times.

Note to Fig.3

The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns, after the first rising-edge of the clock ($t_{SU;\ DAT}$ is negative; –0.3 ns). Data must be held at least 2 ns after the rising-edge ($t_{HD;\ DAT}$ = +2 ns).

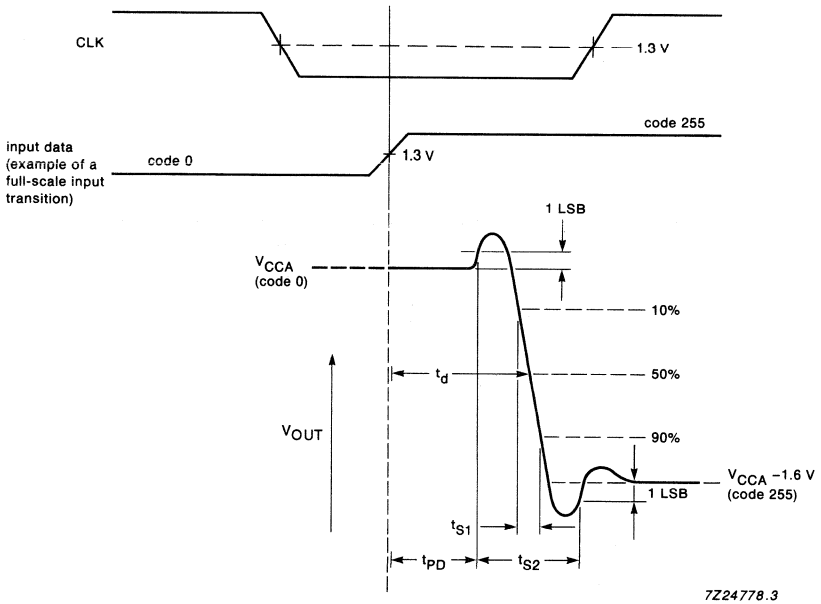


Fig.4 Switching characteristics.

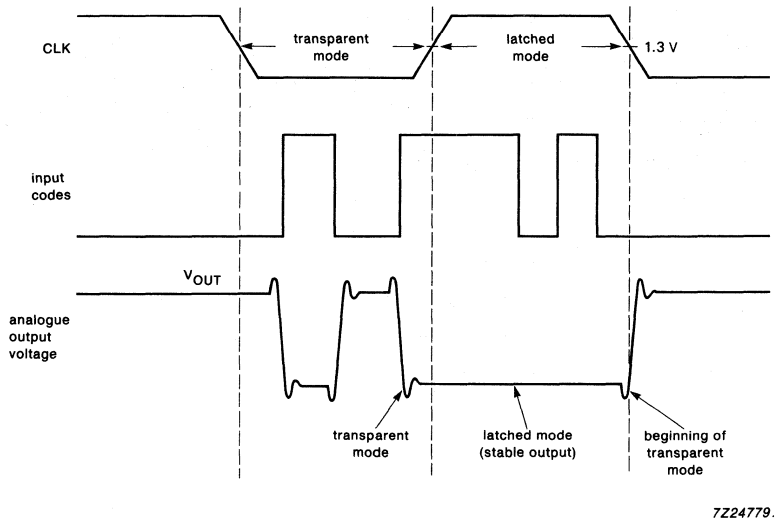


Fig.5 Latched and transparent mode.

Note to Fig.5

During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable, regardless of any changes at the input. A change of input data during the latched mode will be seen on the falling-edge of the clock (beginning of the transparent mode).

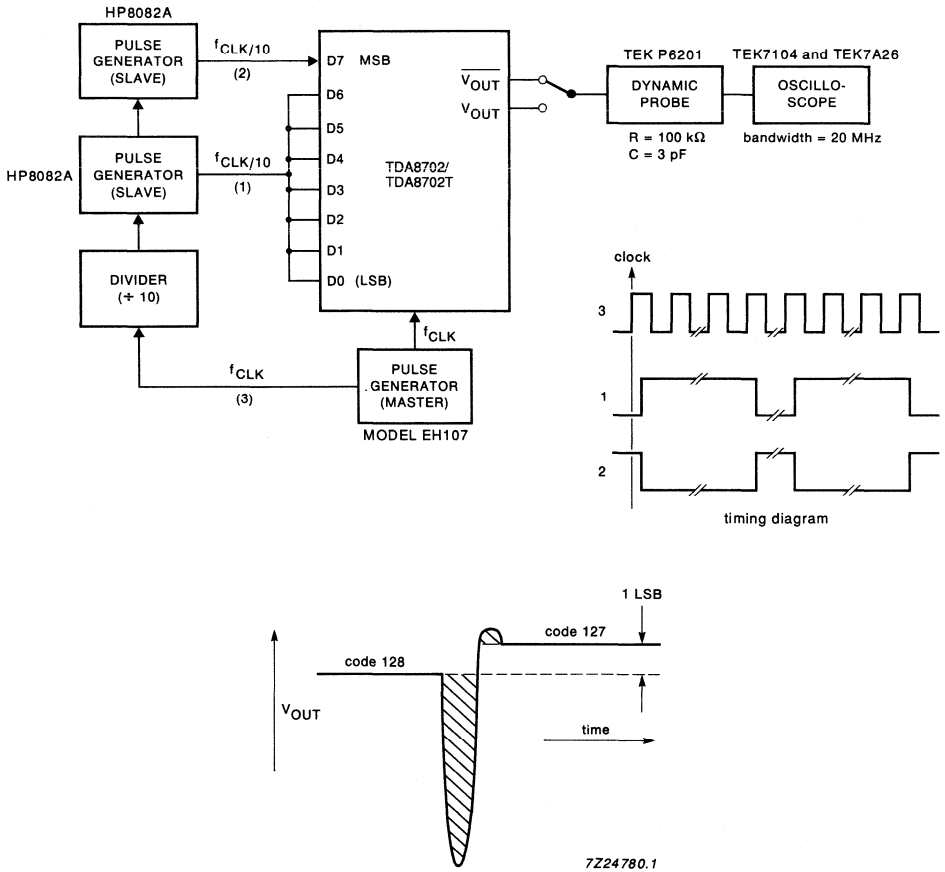


Fig.6 Glitch energy measurement.

Note to Fig.6

The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

INTERNAL PIN CONFIGURATIONS

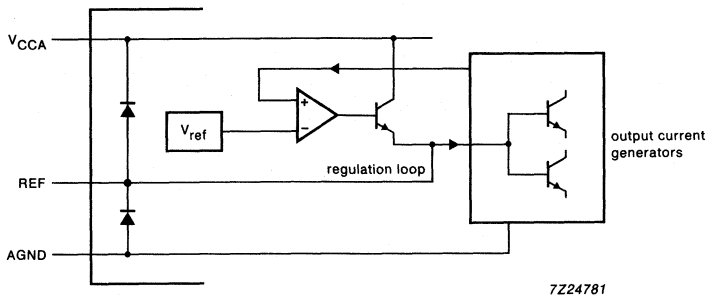


Fig. 7 Reference voltage generator decoupling.

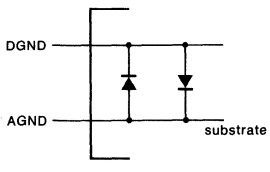


Fig.8 AGND and DGND.

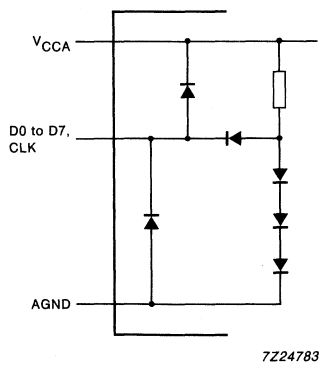


Fig.9 D7 to D0 and CLK.

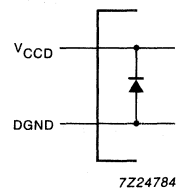


Fig.10 Digital supply.

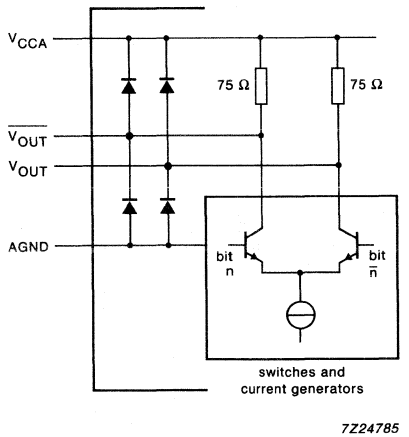


Fig.11 Analog outputs.

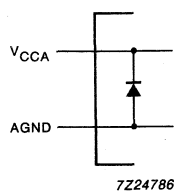


Fig.12 Analog supply.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

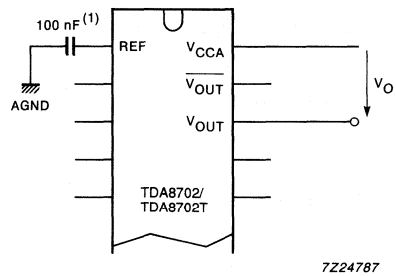


Fig.13 Analog output voltage without external load ($V_O = -V_{\overline{OUT}}$; see Table 1, Z_L = 10 kΩ).

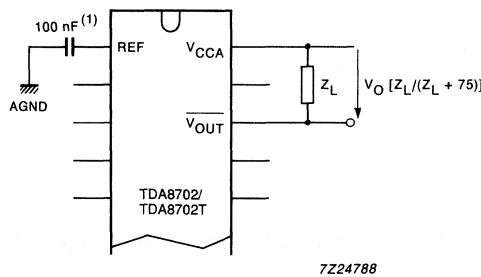


Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).

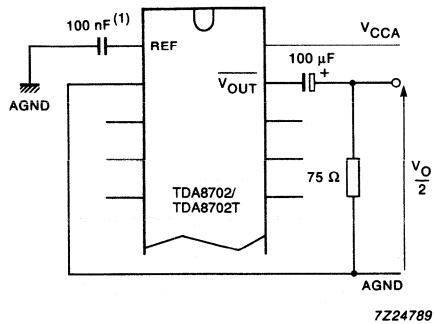


Fig.15 Analog output with AGND as reference.

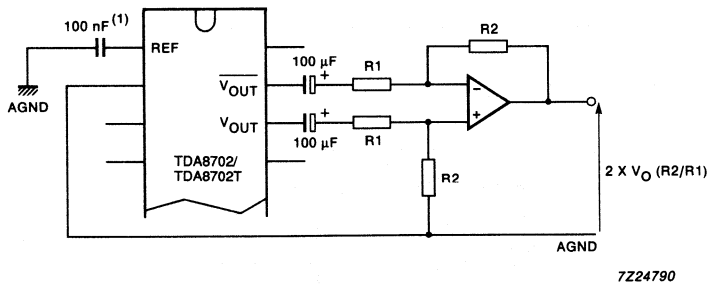


Fig.16 Differential mode (improved supply voltage ripple rejection).

Note to Figs 13, 14,15 and 16

1. This is a recommended value for decoupling pin 1.

8-bit high-speed analog-to-digital converter

TDA8703/8703T

FEATURES

- 8-bit resolution
- Sampling rate up to 40 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.1 effective bits at 4.43 MHz full-scale input)
- Binary or two's complement 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage generator
- Power dissipation only 290 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- General purpose high-speed analog-to-digital conversion
- Digital TV, IDTV
- Subscriber TV decoder
- Satellite TV decoders
- Digital VCR

GENERAL DESCRIPTION

The TDA8703 is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible, although a low-level AC clock input signal is allowed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8703	24	DIL	plastic	SOT101
TDA8703T	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		–	28	36	mA
I_{CCD}	digital supply current		–	19	25	mA
I_{CCO}	output stages supply current		–	11	14	mA
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 1	–	–	±2	LSB
B	–3 dB bandwidth	note 2; f_{CLK} = 40 MHz	–	19.5	–	MHz
$f_{CLK}/f_{\overline{CLK}}$	maximum conversion rate	note 3	40	–	–	MHz
P_{tot}	total power dissipation		–	290	415	mW

Notes to the quick reference data

1. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 27 MHz).
2. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at input).
3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

   If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

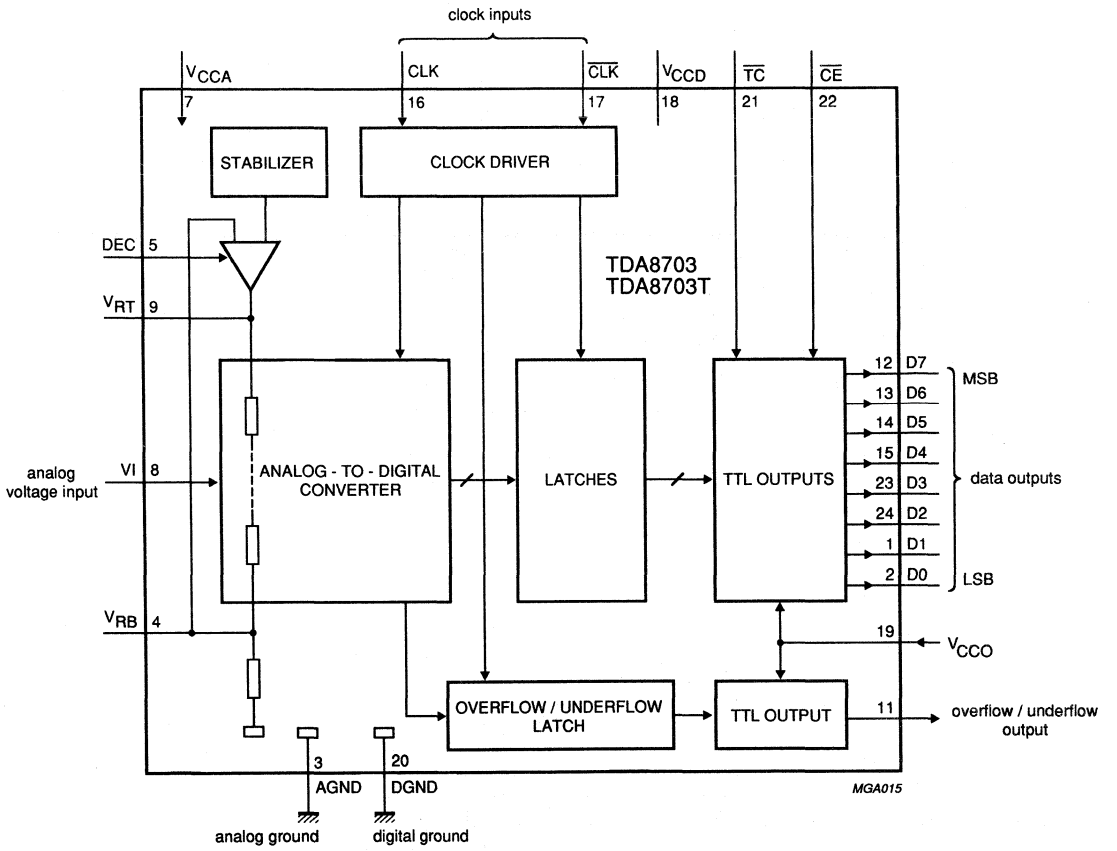


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter

TDA8703/8703T

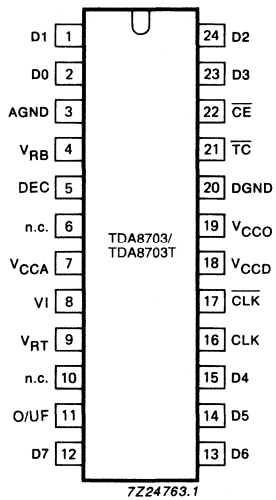


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
AGND	3	analog ground
V_{RB}	4	reference voltage bottom (decoupling)
DEC	5	decoupling input (internal stabilization loop decoupling)
n.c.	6	not connected
V_{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output, bit 7 (MSB)
D6	13	data output, bit 6
D5	14	data output, bit 5
D4	15	data output, bit 4
CLK	16	clock input
$\overline{CLK}$	17	complementary clock input
V_{CCD}	18	positive supply voltage for digital circuits (+5 V)
V_{CCO}	19	positive supply voltage for output stages (+5 V)
DGND	20	digital ground
$\overline{TC}$	21	input for two's complement output (TTL level input, active LOW)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output, bit 3
D2	24	data output, bit 2

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range		−0.3	7.0	V
V_{CCD}	digital supply voltage range		−0.3	7.0	V
V_{CCO}	output stages supply voltage		−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		−1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	−0.3	7.0	V
$V_{CLK(p-p)}/V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)	see note; referenced to DGND	–	2.0	V
I_O	output current		–	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		0	+70	°C
T_j	junction temperature		–	+125	°C

Note to the limiting values

The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:

- TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
- TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
- AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT101)	55 K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT137A)	75 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_3 = 4.5$ V to 5.5 V; $V_{CCD} = V_{18} - V_{20} = 4.5$ V to 5.5 V; $V_{CCO} = V_{19} - V_{20} = 4.5$ V to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $T_{amb} = 0$ °C to +70 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		–	28	36	mA
I_{CCD}	digital supply current		–	19	25	mA
I_{CCO}	output stage supply current	all outputs LOW	–	11	14	mA
Inputs						
CLOCK INPUT $\overline{CLK}$ AND CLK (NOTE 1; REFERENCED TO DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V $V_{CLK}/V_{\overline{CLK}} = V_{CCD}$	– –	– –	100 300	µA µA
Z_i	input impedance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	–	4	–	kΩ
C_i	input capacitance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	–	4.5	–	pF
$V_{CLK(p-p)} - V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)	note 1; DC level = 1.5 V	0.5	–	2.0	V
Inputs $\overline{TC}$ and $\overline{CE}$ (referenced to DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{IH} = 2.7$ V	–	–	20	µA
VI (analog input voltage referenced to AGND)						
$V_{VI(B)}$	input voltage (bottom)		1.33	1.41	1.48	V
$V_{VI(0)}$	input voltage	output code = 0	1.455	1.55	1.635	V
$V_{OS(B)}$	offset voltage (bottom)	$V_{VI(0)} - V_{VI(B)}$	0.125	–	0.155	V
$V_{VI(T)}$	input voltage (top)		3.2	3.36	3.5	V
$V_{VI(255)}$	input voltage	output code = 255	3.115	3.26	3.385	V
$V_{OS(T)}$	offset voltage (top)	$V_{VI(T)} - V_{VI(255)}$	0.085	–	0.115	V
$V_{VI(p-p)}$	input voltage amplitude (peak-to-peak value)		1.66	1.71	1.75	V
I_{IL}	LOW level input current	$V_{VI} = 1.4$ V	–	0	–	µA
I_{IH}	HIGH level input current	$V_{VI} = 3.6$ V	60	120	180	µA

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VI (analog input voltage referenced to AGND)						
Z_i	input impedance	f_i = 1 MHz	–	10	–	kΩ
C_i	input capacitance	f_i = 1 MHz	–	14	–	pF
Reference resistance						
R_{ref}	reference resistance	V_{RT} to V_{RB}	–	220	–	Ω
Outputs						
DIGITAL OUTPUTS (D7 - D0) (REFERENCED TO DGND)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.7	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	µA
Switching characteristics (note 2; see Fig.3)						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		40	–	–	MHz
Analog signal processing (f_{CLK} = 40 MHz)						
B	–3 dB bandwidth	note 3	–	19.5	–	MHz
G_d	differential gain	note 4	–	0.6	–	%
ϕ_d	differential phase	note 4	–	0.8	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz	–	–55	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	–28	–25	dB
SVRR2	supply voltage ripple rejection	note 5	–	1	2.5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 6	–	–	±2	LSB
eff	effective bits	f_i = 4.43 MHz	–	7.1	–	bits
Timing (note 7; see Figs 3 to 6; f_{CLK} = 40 MHz)						
t_{dS}	sampling delay		–	–	2	ns
t_{HD}	output hold time		6	–	–	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	–	8	10	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	–	14	16	ns
t_{dZH}	3-state output delay times	enable-to-HIGH	–	19	25	ns
t_{dZL}	3-state output delay times	enable-to-LOW	–	16	20	ns
t_{dHZ}	3-state output delay times	disable-to-HIGH	–	14	20	ns
t_{dLZ}	3-state output delay times	disable-to-LOW	–	9	12	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

   If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.
2. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 2 ns.
3. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
4. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
5. Supply voltage ripple rejection:
   - SVRR1; variation of the input voltage producing output code 127 for supply voltage variation of 1 V: SVRR1 = 20 log ($\Delta V_{VI(127)}$ / ΔV_{CCA})
   - SVRR2; relative variation of the full-scale range of analog input for a supply voltage variation of 1 V: SVR2 = $\{\Delta(V_{VI(0)} - V_{VI(255)}) / (V_{VI(0)} - V_{VI(255)})\} + \Delta V_{CCA}$.
6. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 27 MHz).
7. Output data acquisition:
   - Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
   - Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; referenced to AGND)

			BINARY OUTPUT BITS								TWO's COMPLEMENT OUTPUT BITS							
STEP	$V_{VI(p-p)}$	O/UF	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow	< 1.55	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1.55	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
254	•	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.26	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow	> 3.26	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{TC}$	$\overline{CE}$	D7 - D0	O/UF
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

Where: X = don't care

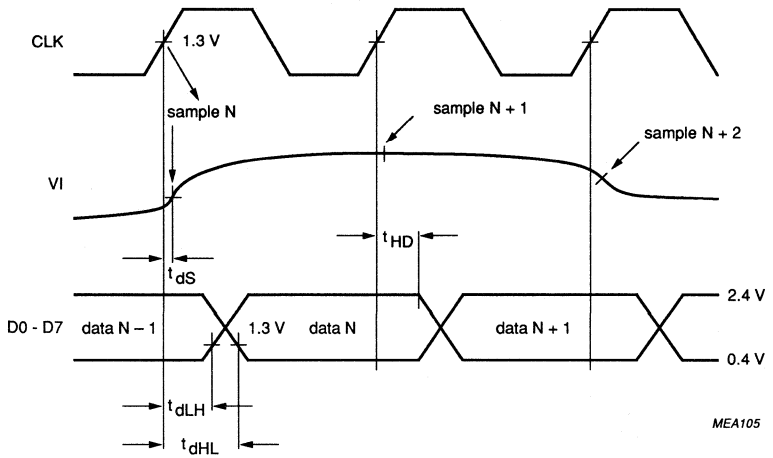


Fig.3 Timing diagram.

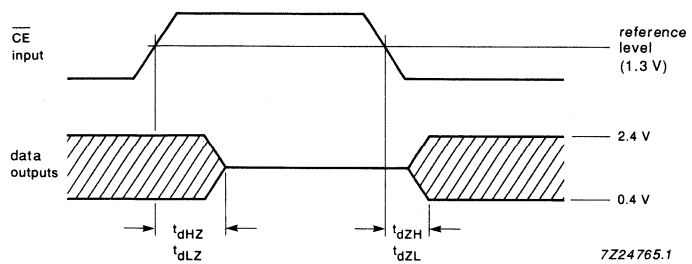


Fig.4 3-state delay timing diagram.

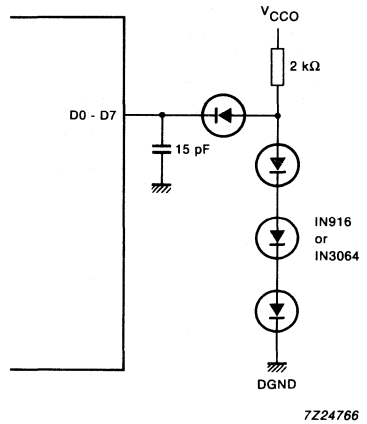


Fig.5 Load circuit for timing measurement; data outputs ($\overline{CE}$ = LOW).

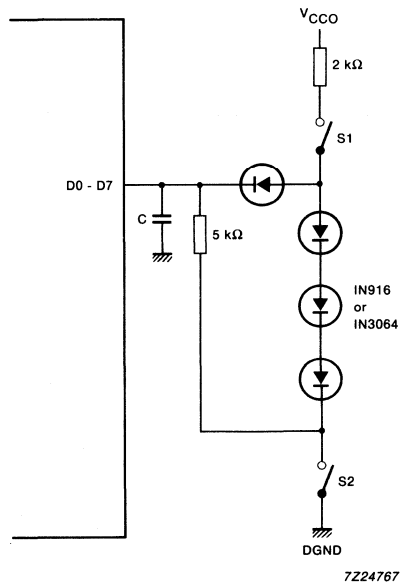


Fig.6 Load circuit for timing measurement; 3-state outputs ($\overline{CE}$: f_i = 1 MHz; V_{VI} = 3 V); see Table 3.

Table 3 Timing measurement for load circuit

TIMING MEASUREMENT	SWITCH S1	SWITCH S2	CAPACITOR
t_{dZH}	open	closed	15 pF
t_{dZL}	closed	open	15 pF
t_{dHZ}	closed	closed	5 pF
t_{dLZ}	closed	closed	5 pF

INTERNAL PIN CONFIGURATIONS

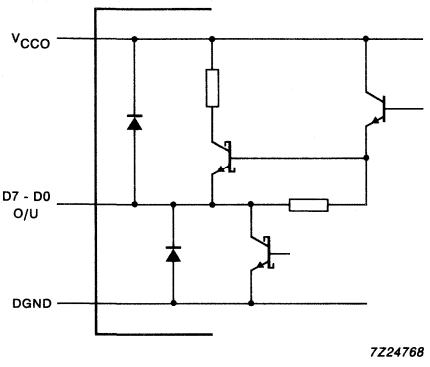


Fig.7 TTL data and overflow/underflow outputs.

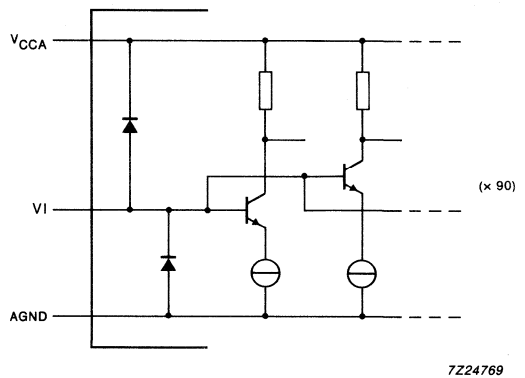


Fig.8 Analog inputs.

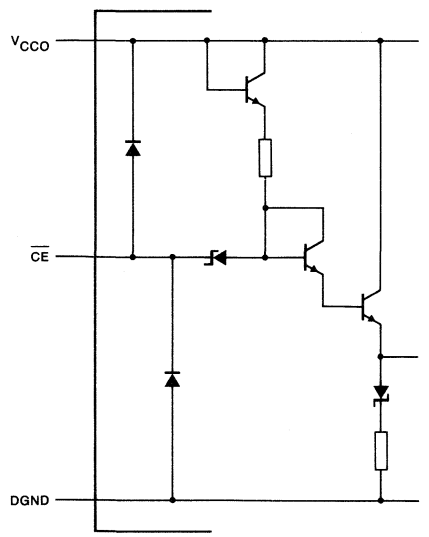


Fig.9 $\overline{CE}$ (3-state) input.

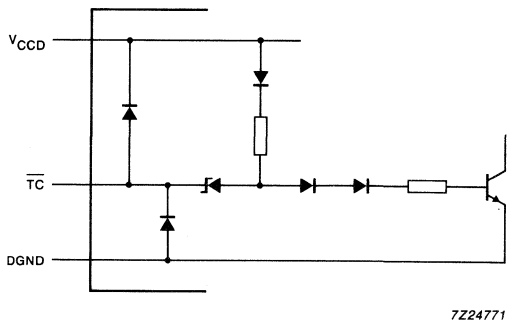


Fig.10 $\overline{TC}$ (two's complement) input.

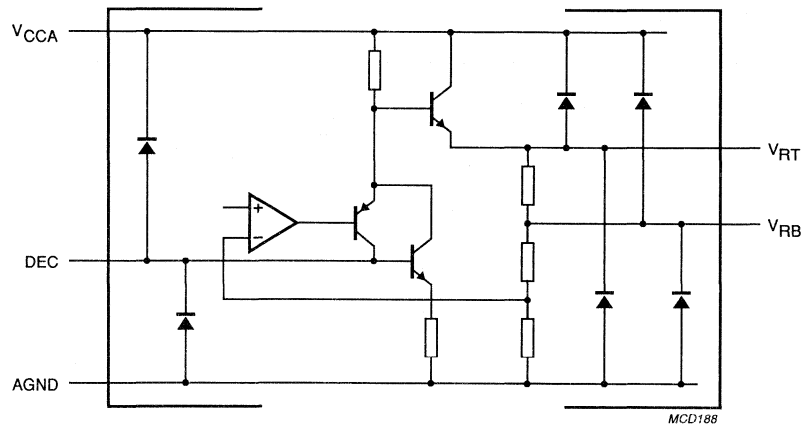


Fig.11 V_{RB}, V_{RT} and DEC.

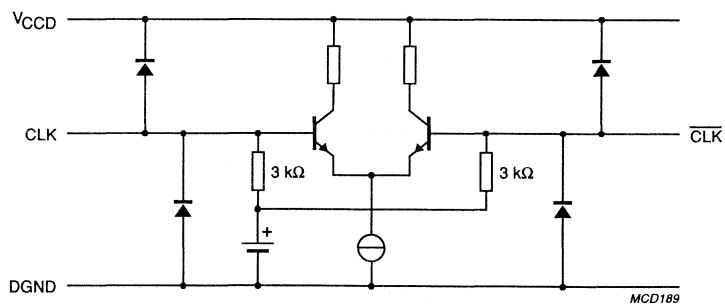


Fig.12 CLK and $\overline{CLK}$ inputs.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

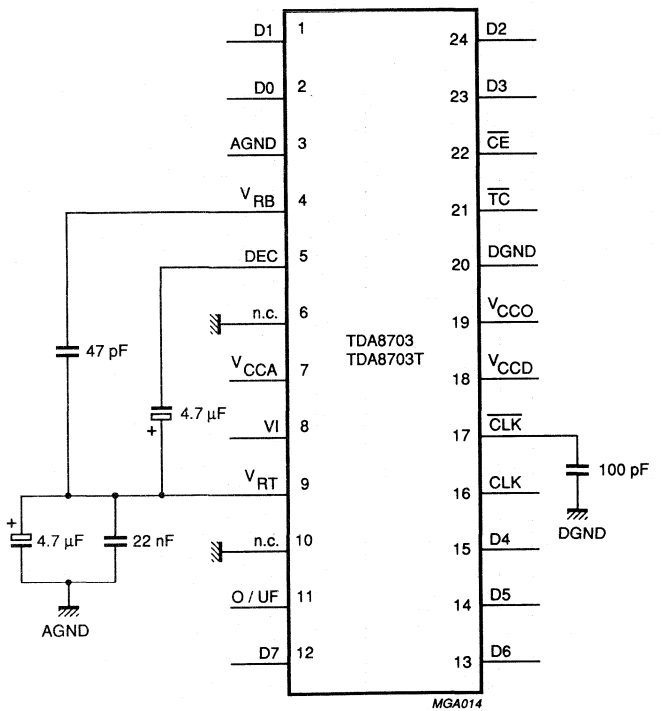


Fig.13 Application diagram.

Notes to Fig.13

1. CLK should be decoupled to the DGND with a 100 nF capacitor, if a TTL signal is used on CLK (see 'Notes to the characteristics', note 1).
2. CLK and $\overline{CLK}$ can be used in a differential mode (see 'Notes to the characteristics', note 1).
3. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder; do not draw current from these pins in order to achieve good linearity.
4. Analog and digital supplies should be separated and decoupled.
5. Pins 6 and 10 should be connected to AGND in order to prevent noise influence.

6-bit analog-to-digital converter with multiplexer and clamp

TDA8706

FEATURES

- 6-bit resolution
- Binary 3-state TTL outputs
- TTL compatible digital inputs
- 3 multiplexed video inputs
- Luminance and colour difference clamps
- Internal reference
- 300 mW power dissipation
- 20-pin plastic package

APPLICATIONS

- General purpose video applications
- Y, U and V signals
- Colour Picture-in-Picture (PIPCO) for TV
- Videophone
- Frame grabber

GENERAL DESCRIPTION

The TDA8706 is a monolithic bipolar 6-bit analog-to-digital converter (ADC) with a 3 analog input multiplexer and a clamp. All digital inputs and outputs are TTL compatible. Regulator with good temperature compensation.

FUNCTIONAL DESCRIPTION

The TDA8706 is a "like-flash" converter which produces an output code in one clock period. The device can withstand a duty clock cycle of 50 to 66.6% (clock HIGH). Luminance clamping level is fitted with 00 hex. code (output 000000). Chrominance clamping level is fitted with 20 Hex. code (output 100000).

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage (pin 2)		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage (pin 10)		4.5	5.0	5.5	V
I_{CCA}	analog supply current (pin 20)		–	32	39	mA
I_{CCD}	digital supply current (pin 10)		–	28	37	mA
ILE	integral linearity error		–	–	±0.75	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
f_{CLK}	maximum clock frequency		20	–	–	MHz
P_{tot}	total power dissipation		–	300	418	mW
T_{amb}	operating ambient temperature range		0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8706	20	DIL	plastic	SOT146EF4
TDA8706T	20	SO20L	plastic	SOT163AG7

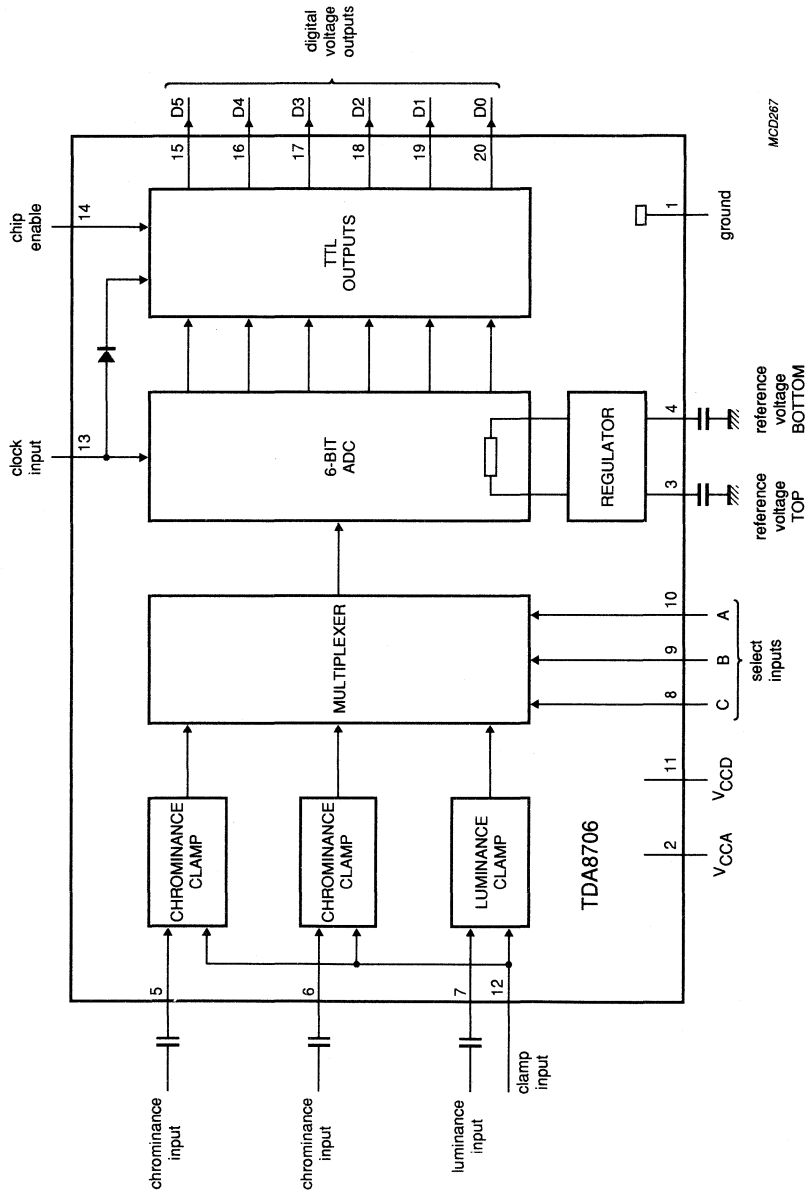


Fig.1 Block diagram.

6-bit analog-to-digital converter with multiplexer and clamp

TDA8706

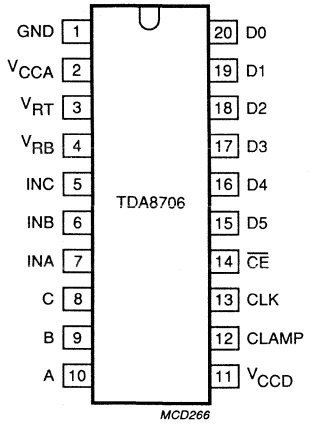


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
V_{CCA}	2	analog positive supply (+5 V)
V_{RT}	3	reference voltage TOP decoupling
V_{RB}	4	reference voltage BOTTOM decoupling
INC	5	chrominance input
INB	6	chrominance input
INA	7	luminance input
C	8	select input
B	9	select input
A	10	select input
V_{CCD}	11	digital positive supply voltage (+5 V)
CLAMP	12	clamp pulse input (positive pulse)
CLK	13	clock input
$\overline{CE}$	14	chip enable (active LOW)
D5	15	digital voltage output: most significant bit (MSB)
D4	16	digital voltage output
D3	17	digital voltage output
D2	18	digital voltage output
D1	19	digital voltage output
D0	20	digital voltage input: least significant bit (LSB)

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range (pin 2)	−0.3	7.0	V
V_{CCD}	digital supply voltage range (pin 10)	−0.3	7.0	V
V_{CCA}-V_{CCD}	supply voltage difference	1.0	–	V
V_I	input voltage range	−0.3	7.0	V
I_O	output current	–	10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C

CHARACTERISTICS (see Tables 1 and 2)

V_{CCA} = 4.5 V to 5.5 V; V_{CCD} = 4.5 V to 5.5 V = V_{CCD}; T_{amb} = 0 °C to +70°C; C_{VRB} = C_{VR1} = 100 nF; Typical values measured at V_{CCA} = V_{CCD} = 5 V and T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage (pin 2)		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage (pin 10)		4.5	5.0	5.5	V
I_{CCA}	analog supply current (pin 2)		–	32	39	mA
I_{CCD}	digital supply current (pin 10)	all outputs at LOW level	–	28	37	mA
Inputs						
CLOCK INPUT (PIN 13)						
V_{IL}	LOW level input voltage		0	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	µA
Z_I	input impedance	f_{CLK} = 20 MHz	–	4	–	kΩ
C_i	input capacitance	f_{CLK} = 20 MHz	–	2	–	pF
A, B, C, CLAMP AND CEN INPUTS (PINS 8, 9, 10, 12 AND 14)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	20	µA
Reference voltage (pins 3 and 4)						
V_{RT}	reference voltage TOP decoupling		3.22	3.35	3.44	V
V_{RB}	reference voltage BOTTOM decoupling		1.84	1.9	1.96	V
$V_{RT} - V_{RB}$	reference voltage TOP – BOTTOM decoupling		1.36	1.435	1.48	V
Analog inputs INA, INB, INC (pins 7, 6 and 5)						
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		840	900	940	mV
Z_I	input impedance	f_i = 4.43 MHz	100	–	–	kΩ
C_{clamp}	coupling clamp capacitance		1	10	1000	nF
Analog signal processing (pins 5, 6 and 7) (f_{CLK} = 20 MHz)						
f_1	fundamental harmonics (full scale)	f_i = 4.43 MHz	–	–	0	dB
f_{all}	harmonics (full scale); all components	f_i = 4.43 MHz	-	–45	-	dB
G_{diff}	differential gain	note 1	–	0.4	–	%
ϕ_{diff}	differential phase	note 1	–	1.0	–	deg
SVRR	supply voltage ripple rejection	note 2	–	–30	–	dB
Outputs						
DIGITAL VOLTAGE OUTPUTS (PINS 15 TO 20) (SEE TABLE 2)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH level ouptut voltage	I_O = 0.5 mA	2.7	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	20	µA
Switching characteristics						
CLOCK TIMING (SEE FIG.3)						
f_{CLK}	maximum clock frequency		20	–	–	MHz
f_{mux}	maximum multiplexing frequency		10	–	–	MHz
t_{CLK}	period		50	–	–	ns
	duty cycle	CLK = V_{IH}	45	50	66.6	%
t_{LOW}	LOW time	at 50%	16	–	–	ns
t_{HIGH}	HIGH time	at 50%	22.5	–	–	ns
t_{CLR}	rise time	at 10% to 90%	4	6	–	ns
t_{CLF}	fall time	at 90% to 10%	4	6	–	ns
Select signals, Clamp, Data (see Figs 4 and 5)						
t_S	set-up time select A, B and C		35	–	–	ns
t_r	rise time (A, B and C)	at 10% to 90%	4	6	–	ns
t_f	fall time (A, B and C)	at 90% to 10%	4	6	–	ns
t_{CLPS}	set-up time clamp asynchronous		0	–	–	
t_{CLPH}	hold time clamp asynchronous		0	–	–	
t_{CLPP}	clamp pulse	C_{CLP} = 10 nF	–	3	–	µs
t_d	data output delay time		–	15	24	ns
t_{DH}	data hold time		12	–	–	ns
Transfer function						
ILE	DC integral linearity error		–	–	±0.75	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
AILE	AC integral linearity error	note 3	–	–	±2	LSB
EB	effective bits	note 3	–	5.7	–	bits
Timing						
DIGITAL OUTPUTS						
T_{dt}	3-state delay time	see Fig.6	–	16	25	ns
T_{sto}	sampling time offset		–	2	–	ns

Notes to the characteristics

1. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V and f_i = 4.43 MHz) at the input.
2. Supply voltage ripple rejection (SVRR): variation of the input voltage produces output code 31 for a supply voltage variation of 1 V.

   $$SVRR = 20 \log \frac{\Delta V_{Vi31)}}{\Delta V_{CCA}}$$

3. Full-scale sinewave; f_i = 4.43 MHz, f_{CLK} = 20 MHz.

Table 1 Output coding

STEP	V_I (note 1) (TYP. value)	BINARY OUTPUTS D5 to D0
Underflow	< 2.2 V	000000
0	2.2 V	000000
1	2.215 V	000001
.		.....
.		.....
.		.....
62	3.072 V	111110
63	3.086 V	111111
Overflow	> 3.1 V	111111

Note

1. With clamping capacitance.

Table 2 Mode selection

CEN	D0 to D5
1	high impedance
0	active. Binary

Table 3 Clamp input A

A	CLAMP	DIGITAL OUTPUTS	$V_{in}A$
0	1	X	2.2
1	1	0	2.2

Note

X = don't care.

Table 4 Clamp input B and C

B/C	CLAMP	DIGITAL OUTPUTS	$V_{in}B/V_{in}C$
0	1	X	2.65
1	1	32	2.65

Note

X = don't care.

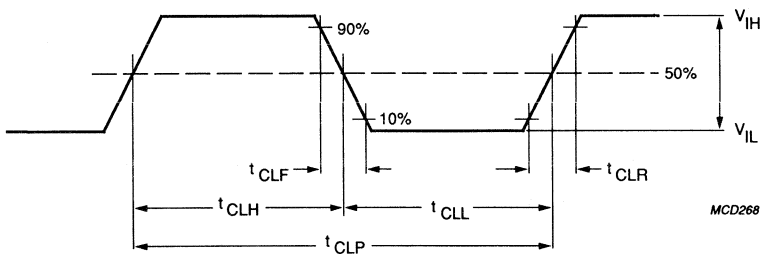


Fig.3 AC clock characteristics.

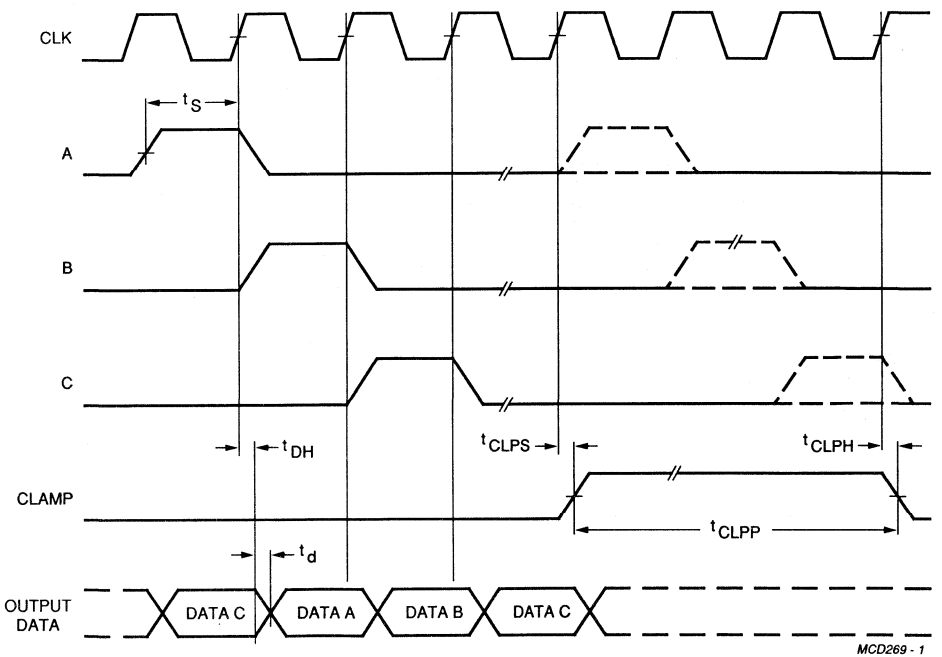


Fig.4 AC characteristics select signals; Clamp, Data.

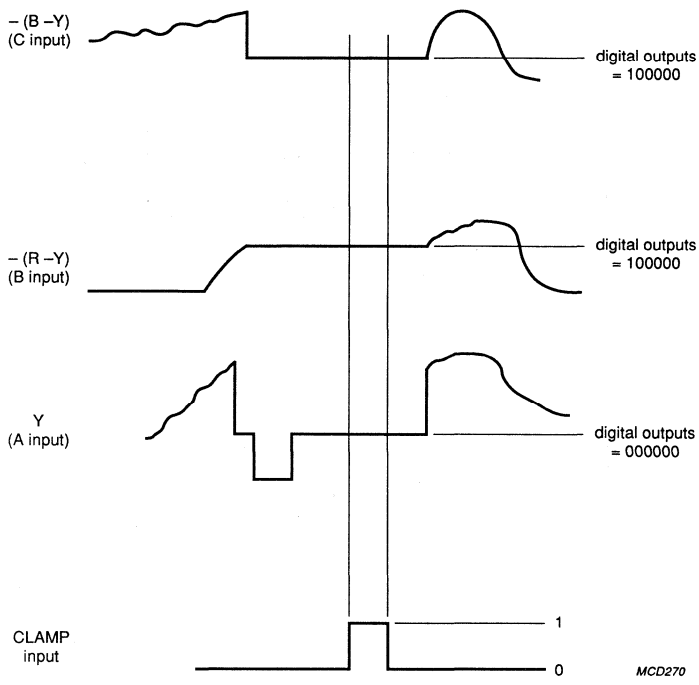


Fig.5 AC characteristics select signals; Clamp, Data.

Table 5 Clamp characteristic related to TV signals

PARAMETER	MIN.	TYP.	MAX.	UNIT
clamping time per line (signal active)	2.2	3.0	3.3	µs
input signals clamped to correct level after	–	3	10	lines

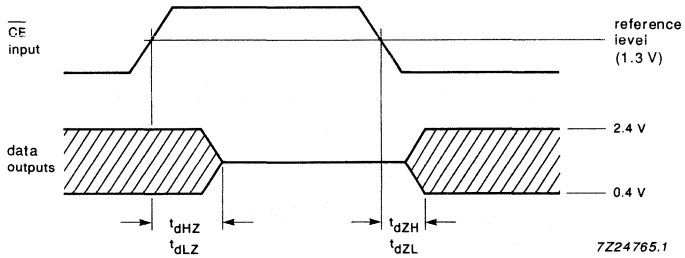


Fig.6 Timing diagram of 3-state delay.

Application information

Additional application information will be supplied on request (please quote reference number FTV/9112).

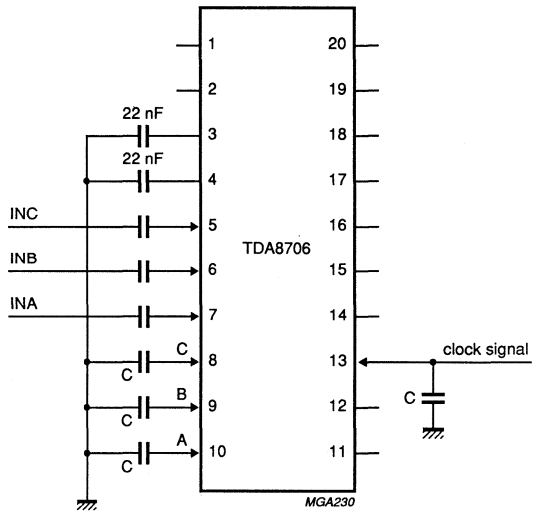


Fig.7 Application diagram.

Notes to figure 7

1. 'C' capacitors must be determined on the output capacitance of the circuits driving A, B and C or CLK pins
2. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder. Do not draw current from these pins in order to achieve good linearity
3. Analog and digital supplies should be separated and decoupled.

Video analog input interface TDA8708

FEATURES

- 8-bit resolution
- Sampling rate up to 30 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS signal
- No sample-and-hold circuit required

APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing

GENERAL DESCRIPTION

The TDA8708 is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 30 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	37	45	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum clock frequency	30	–	–	MHz
B	maximum –3 dB bandwidth (AGC amplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	365	500	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708	28	DIL	plastic	SOT117
TDA8708T	28	SO28	plastic	SOT136A

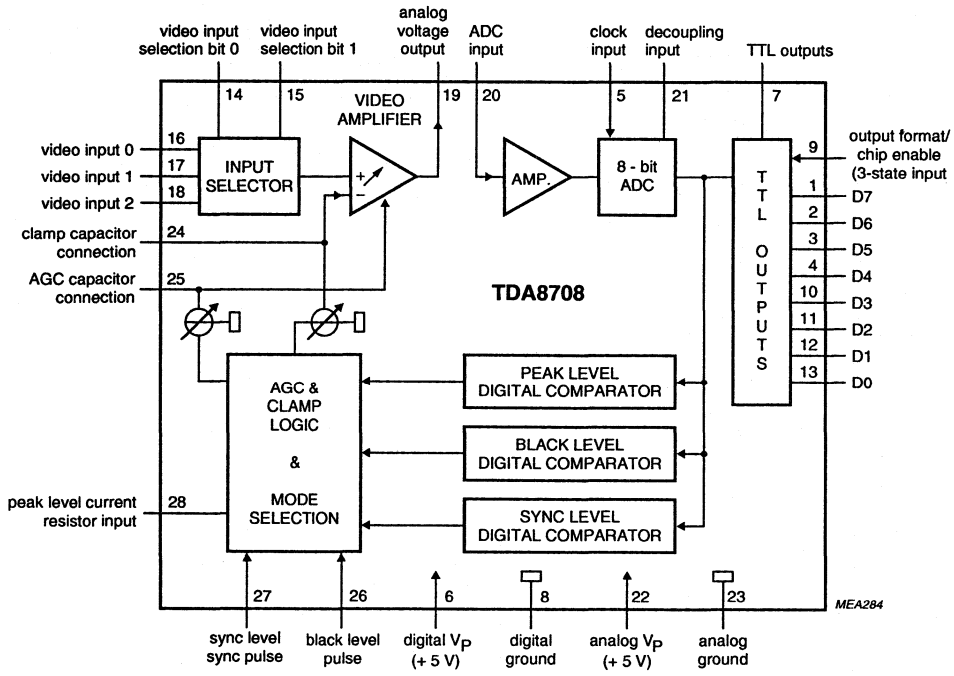


Fig.1 Block diagram.

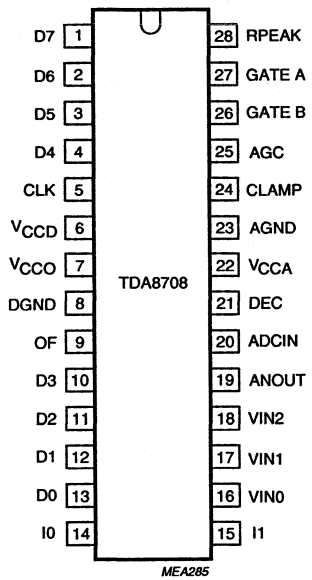


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output, bit 7 (MSB)
D6	2	data output, bit 6
D5	3	data output, bit 5
D4	4	data output, bit 4
CLK	5	clock input
V_{CCD}	6	digital positive supply voltage (5 V)
V_{CCO}	7	TTL outputs positive supply voltage (5 V)
DGND	8	digital ground
OF	9	output format/chip enable (3-state input)
D3	10	data output, bit 3
D2	11	data output, bit 2
D1	12	data output, bit 1
D0	13	data output, bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog positive supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
AGC	25	AGC capacitor connection
GATE B	26	black level synchronization pulse
GATE A	27	sync level synchronization pulse
RPEAK	28	peak level current resistor input

FUNCTIONAL DESCRIPTION

The TDA8708 provides a simple interface for decoding video signals.

The TDA8708 operates in configuration mode 1 (see Fig.4) when the video signals are weak (i.e. when the gain of the AGC amplifier has not yet reached its optimum value). This enables a fast recovery of the synchronization pulses in the decoder circuit. When the pulses at the GATE A and GATE B inputs become distinct (GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively) the TDA8708 automatically switches to configuration mode 2.

When the TDA8708 is in configuration mode 1, the gain of the AGC amplifier will be roughly adjusted (sync level to a digital output level of 0 and the peak level to a digital output level of 255).

In configuration mode 2 the digital output of the ADC is compared to internal digital reference levels. The resultant outputs control the charge or discharge current of a capacitor connected to the AGC pin. The voltage across this capacitor controls the gain of the video amplifier. This is the gain control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that the sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 0 at the converter output. As the black level is at digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The peak-white control loop is always active. If the video signal tends to exceed the digital code of 240, the gain will be limited to avoid any over-range of the converter.

The use of nominal signals will prevent the output from exceeding a digital code of 213 and the peak-white control loop will be non-active.

The clamp level control is accomplished by using the same techniques as used for the gain control. The black-level digital comparator is active during a positive-going pulse at the GATE B input. The clamp capacitor will be charged or discharged to adjust the digital output to code 64.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+7.0	V
V_{CCD}	digital supply voltage range	−0.3	+7.0	V
V_{CCO}	output supply voltage range	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage difference	−1.0	+1.0	V
$V_{CCO} - V_{CCD}$	supply voltage difference	−1.0	+1.0	V
$V_{CCA} - V_{CCO}$	supply voltage difference	−1.0	+1.0	V
V_I	input voltage range	−0.3	V_{CCA}	V
I_O	output current	0	+10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT117)	55 K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT136A)	70 K/W

CHARACTERISTICS

$V_{CCA} = V_{22} - V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6 - V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7 - V_8 = 4.2$ to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCA} - V_{CCO} = -0.5$ to +0.5 V; $T_{amb} = 0$ to +70 °C; Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	37	45	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	output supply current	TTL load (see Fig.8)	–	12	16	mA
Video amplifier inputs						
VIN(0-2) INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)		0.45	1.0	1.6	V
$\|Z_i\|$	input impedance	f = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	µA
GATE A AND GATE B TTL INPUTS (SEE FIGS 4 AND 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	µA
RPEAK INPUT (PIN 28)						
I_{28}	minimum peak level current	$R_{28} = 0$ Ω	–	80	150	µA
AGC INPUT (PIN 25)						
V_{25}	AGC voltage for minimum gain		–	2.8	–	V
V_{25}	AGC voltage for maximum gain		–	4.0	–	V
	AGC output current	see Table 2	–	–	–	
CLAMP INPUT (PIN 24)						
V_{24}	CLAMP voltage for code 128 output		–	3.5	–	V
I_{24}	CLAMP output current	see Table 3	–	–	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	output AC voltage (peak-to-peak value)	V_{VIN} = 1 V (p-p); V_{25} = 3.6 V	–	1.0	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1 V (p-p); note 1	-	-	1.0	mA
V_{19}	output DC voltage for black level	note 2	–	V_{CCA}–2.95	–	V
Z_{19}	output impedance		–	20	–	Ω
Video amplifier dynamic characteristics						
α	crosstalk between VIN inputs		–	–60	–55	dB
G_{diff}	differential gain	V_{VIN} = 1 V (p-p); V_{25} = 3.6 V	–	2	–	%
ϕ_{diff}	differential phase		–	2	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 3	60	–	–	dB
SVRR	supply voltage ripple rejection	note 4	–	45	–	dB
ΔG	gain range		–4.5	–	6.0	dB
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{CLK} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{CLK} = 10 MHz	–	4.5	–	pF
OF input (3-state) (see Table 4)						
V_{IL}	LOW level input voltage		0	–	0.2	V
V_{IH}	HIGH level input voltage		2.6	–	V_{CCD}	V
V_9	input voltage in HIGH-Z state		–	1.15	–	V
I_{IL}	LOW level input current		–370	–300	–	μA
I_{IH}	HIGH level input current		–	360	450	μA
ADCIN INPUT (PIN 20) (SEE TABLE 5)						
V_{20}	input voltage	digital out = 00	–	V_{CCA} –1.6	–	V
V_{20}	input voltage	digital out = 255	–	V_{CCA} –1.1	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	0.5	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D(0-7)						
V_L	LOW level output voltage	I_O = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	µA
Switching characteristics						
f_{CLK}	CLK input maximum frequency	see Fig.6; note 5	30	–	–	MHz
Analog signal processing (f_{CLK} = 30 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 0.5 V (p-p) ; note 6; Fig.3	–	2	–	%
ϕ_{diff}	differential phase	note 6; Fig.3	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 6	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz; note 6	–	–55	–	dB
SVRR	supply voltage ripple rejection	note 7	–	1	5	%/V
Transfer function (see Fig.8)						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 8	–	–	±2	LSB
Timing (f_{CLK} = 30 MHz; see Figs 7, 8 and 9)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA)						
t_{dS}	sampling delay		–	2	–	ns
t_{HD}	output hold time		6	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time - output enable		–	19	25	ns
t_{dDZ}	3-state delay time - output disable		–	14	20	ns

Notes to the characteristics

1. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referred to V_{CC} and defined as:

   AC impedance ≥ 1 kΩ and the DC impedance > 2.7 kΩ.

   The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
2. Control mode 2 is selected.
3. Signal-to-noise ratio measured with 5 MHz bandwidth

$$SN = 20 \log \frac{V_{ANNOUT(p-p)}}{V_{ANNOUT}\ noise\ RMS\ (B = 5\ MHz)}$$

Notes to the characteristics

4. The voltage ratio is expressed as:

$$SVRR = 20 \log \frac{\Delta V_{CCA}}{\Delta G/G}$$

for V_I = 1 V (p-p), 100 kHz gain = 1 and 1 V supply variation.

5. It is recommended that the rise and fall times of the clock are not less than 2 ns. In addition, a 'good lay-out' for the digital and analog grounds is recommended.
6. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
7. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR = \frac{\Delta[V_{IN(00)} - V_{IN(FF)}] \div [V_{IN(00)} - V_{IN(FF)}]}{\Delta V_{CCA}}$$

8. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}, $\overline{f_{CLK}}$ = 27 MHz).

Table 1 Video input selection (CVBS)

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 AGC output current

GATE A	GATE B	DIGITAL OUTPUT	I_{AGC}	MODE
1	1	output < 255 output > 255	−2.5 µA I_{PEAK}	1
0	X	output < 240 output > 240	0 I_{PEAK}	2; note 2
1	0	output < 0 0 < output < 240 output > 240	+2.5 µA −2.5 µA I_{PEAK}	2; note 2

Notes to Table 2

1. Where X = don't care
2. Mode 2 can only be initialized with successive pulses on GATE A and GATE B (see Fig.5)

Table 3 CLAMP output current

GATE A	GATE B	DIGITAL OUTPUT	I_{CLAMP}	MODE
1	1	output < 0 output > 0	I_{PEAK} −2.5 μA	1
X	0	X	0	2
0	1	output < 64 64 < output	+50 μA −50 μA	2

Note to Table 3

1. Where X = don't care

Table 4 OF input coding

OF	D0 TO D7
0	active, two's complement
1	high impedance
open circuit (note 1)	active, binary

Note to Table 4

1. Use C ≥ 10 pF to DGND

Table 5 ADC output current

		BINARY OUTPUTS								TWO'S COMPLEMENT							
STEP	V_{ADCIN}	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} - 1.6 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254		1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} - 1.1 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow		1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

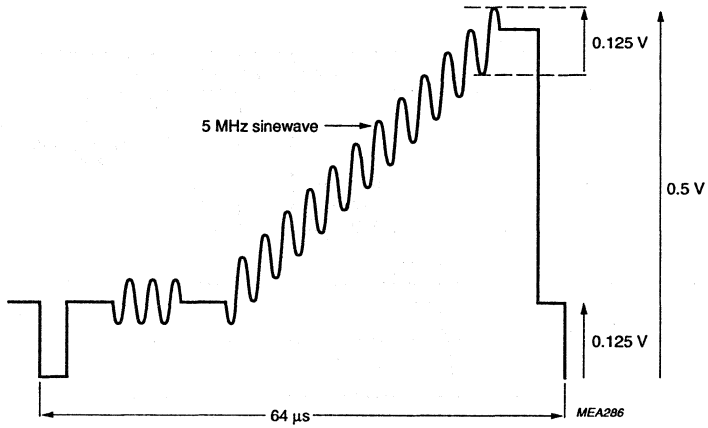


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

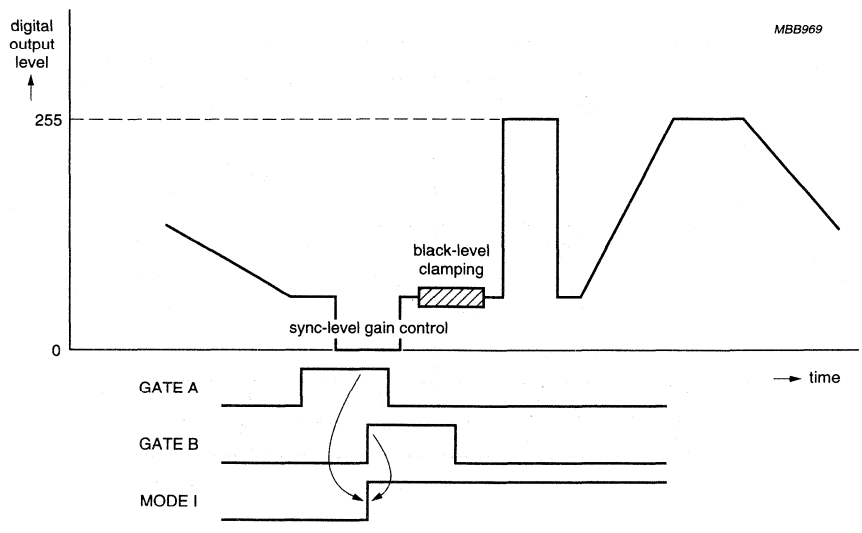


Fig.4 Control mode 1.

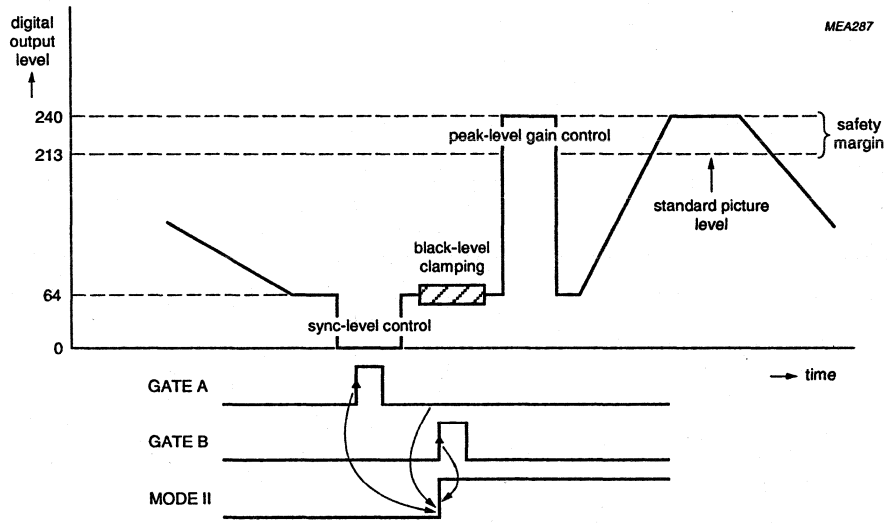


Fig.5 Control mode 2.

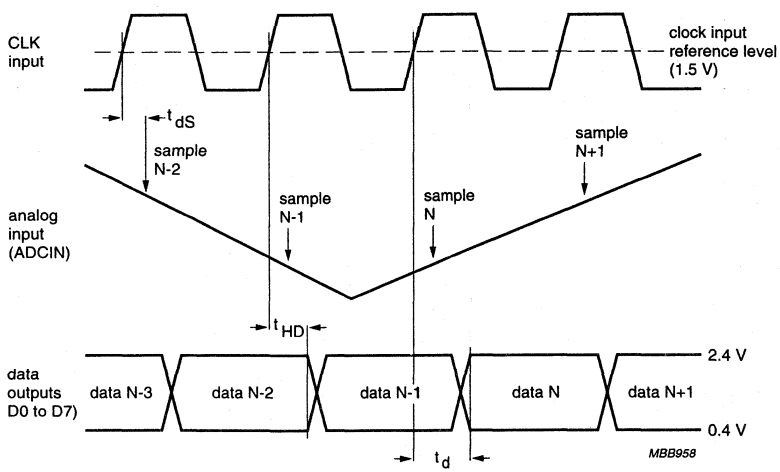


Fig.6 Timing diagram.

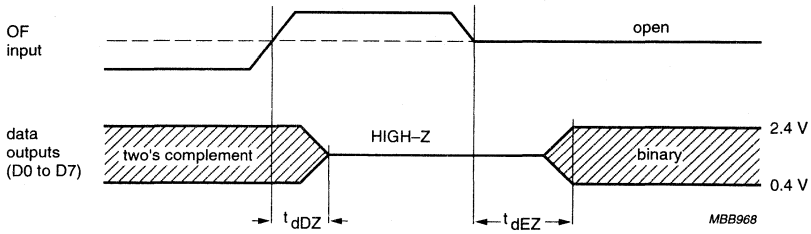


Fig.7 Output format timing diagram.

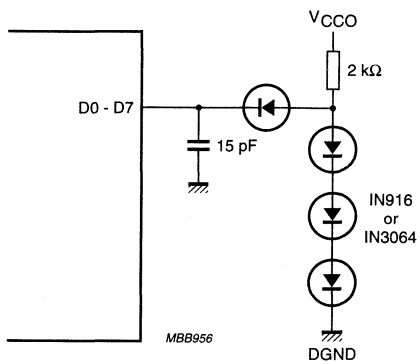


Fig.8 Load circuit for timing measurement; data outputs (OF = LOW or open-circuit).

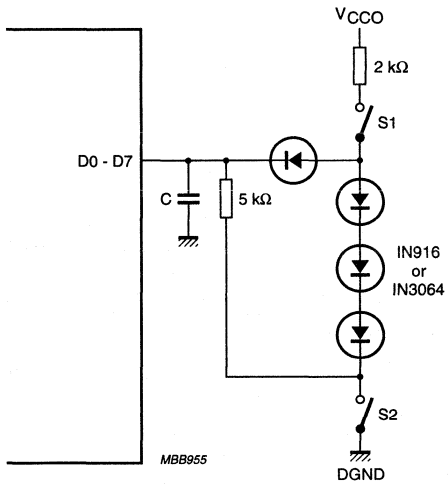


Fig.9 Load circuit for timing measurement; 3-state outputs (OF: f_i = 1 MHz; V_{OF} = 3 V).

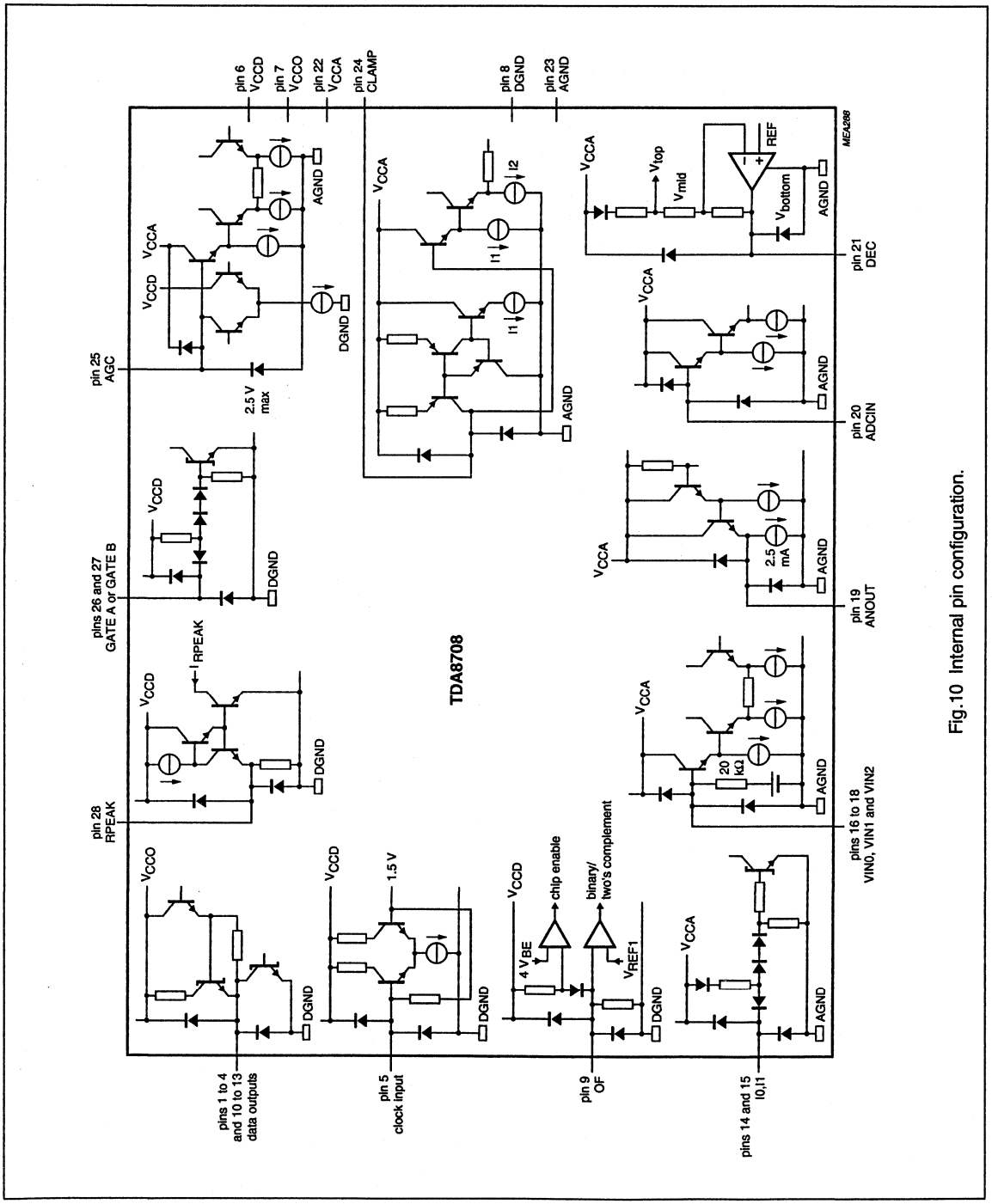
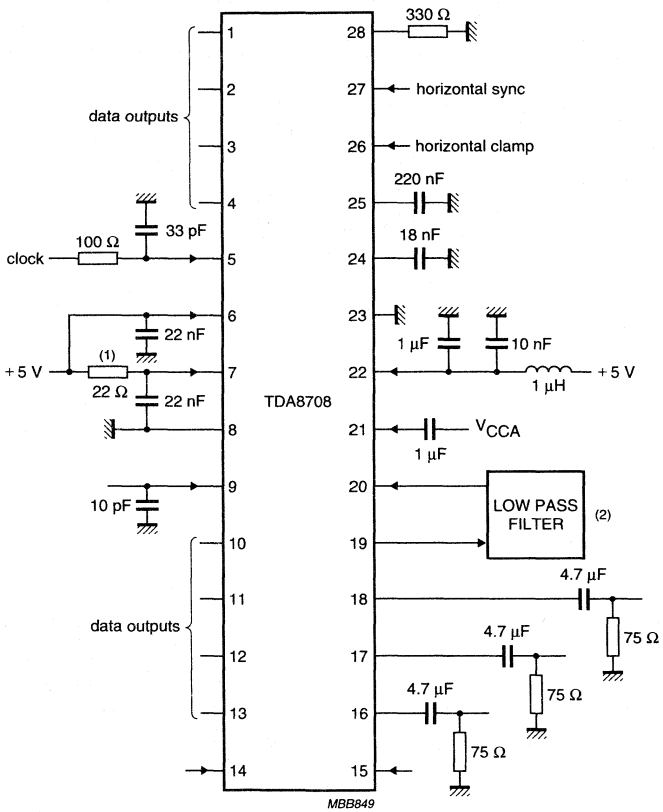


Fig.10 Internal pin configuration.

APPLICATION INFORMATION

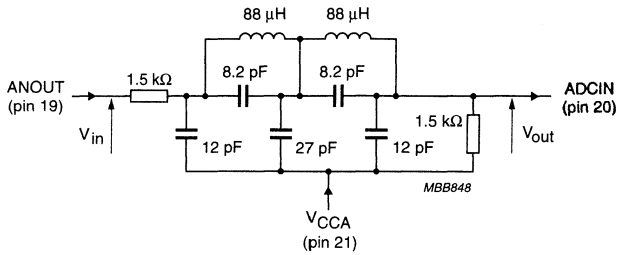
Additional information can be found in the laboratory report FTV/8902.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8708 interfaces with a capacitive CMOS load device.

(2) See Fig.12 for an example of the low pass filter.

Fig.11 Application diagram.



These filters can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 1.5 kΩ must in any case be applied.

Fig.12 Example of a low pass filter for CVBS signal.

Video analog input interface TDA8708A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS signal
- No sample-and-hold circuit required
- ADC input voltage amplitude 1.0 V as against 0.5 V (p-p) for TDA8708

APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing

GENERAL DESCRIPTION

The TDA8708AA is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	37	45	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (AGC amplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	365	500	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708A	28	DIL	plastic	SOT117
TDA8708AT	28	SO28	plastic	SOT136A

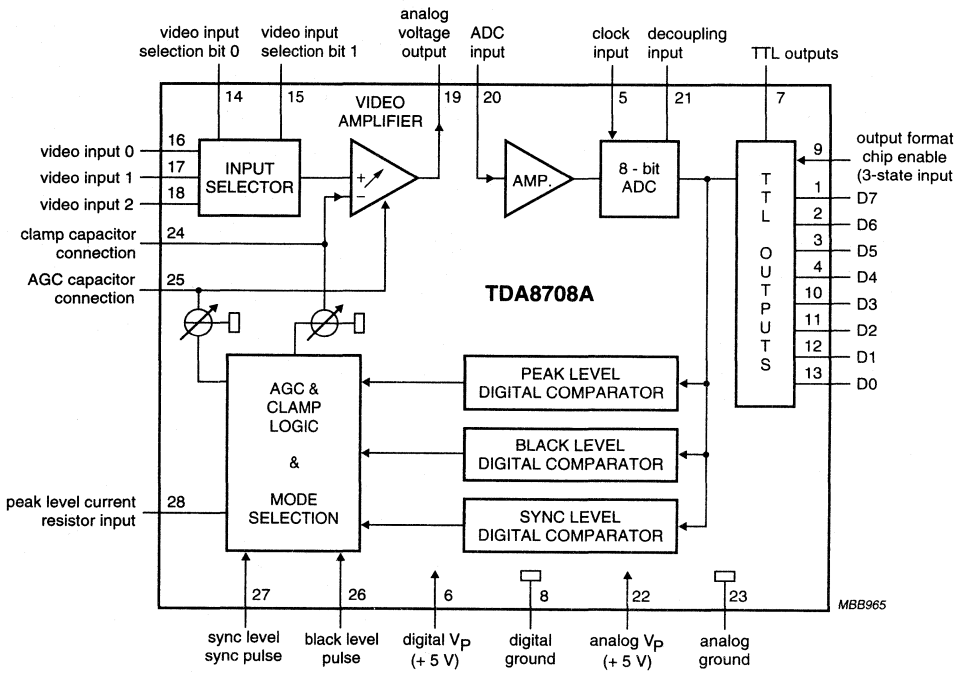


Fig.1 Block diagram.

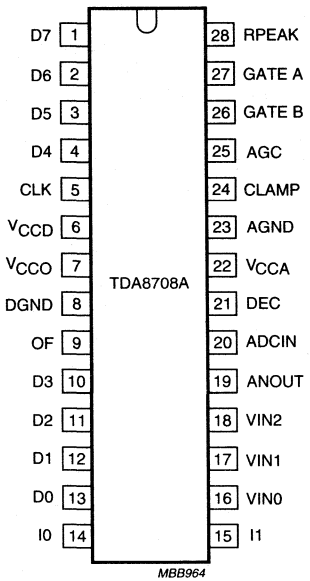


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output, bit 7 (MSB)
D6	2	data output, bit 6
D5	3	data output, bit 5
D4	4	data output, bit 4
CLK	5	clock input
V_{CCD}	6	digital positive supply voltage (5 V)
V_{CCO}	7	TTL outputs positive supply voltage (5 V)
DGND	8	digital ground
OF	9	output format/chip enable (3-state input)
D3	10	data output, bit 3
D2	11	data output, bit 2
D1	12	data output, bit 1
D0	13	data output, bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog positive supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
AGC	25	AGC capacitor connection
GATE B	26	black level synchronization pulse
GATE A	27	sync level synchronization pulse
RPEAK	28	peak level current resistor input

FUNCTIONAL DESCRIPTION

The TDA8708A provides a simple interface for decoding video signals.

The TDA8708A operates in configuration mode 1 (see Fig.4) when the video signals are weak (i.e. when the gain of the AGC amplifier has not yet reached its optimum value). This enables a fast recovery of the synchronization pulses in the decoder circuit. When the pulses at the GATE A and GATE B inputs become distinct (GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively) the TDA8708A automatically switches to configuration mode 2.

When the TDA8708A is in configuration mode 1, the gain of the AGC amplifier will be roughly adjusted (sync level to a digital output level of 0 and the peak level to a digital output level of 255).

In configuration mode 2 the digital output of the ADC is compared to internal digital reference levels. The resultant outputs control the charge or discharge current of a capacitor connected to the AGC pin. The voltage across this capacitor controls the gain of the video amplifier. This is the gain control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that the sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 0 at the converter output. As the black level is at digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The peak-white control loop is always active. If the video signal tends to exceed the digital code of 248, the gain will be limited to avoid any over-range of the converter.

The use of nominal signals will prevent the output from exceeding a digital code of 213 and the peak-white control loop will be non-active.

The clamp level control is accomplished by using the same techniques as used for the gain control. The black-level digital comparator is active during a positive-going pulse at the GATE B input. The clamp capacitor will be charged or discharged to adjust the digital output to code 64.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+7.0	V
V_{CCD}	digital supply voltage range	−0.3	+7.0	V
V_{CCO}	output supply voltage range	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage difference	−1.0	+1.0	V
$V_{CCO} - V_{CCD}$	supply voltage difference	−1.0	+1.0	V
$V_{CCA} - V_{CCO}$	supply voltage difference	−1.0	+1.0	V
V_I	input voltage range	−0.3	V_{CCA}	V
I_O	output current	0	+10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT117)	55 K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT136A)	70 K/W

CHARACTERISTICS

$V_{CCA} = V_{22} - V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6 - V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7 - V_8 = 4.2$ to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCA} - V_{CCO} = -0.5$ to +0.5 V; $T_{amb} = 0$ to +70 °C; Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	37	45	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	output supply current	TTL load (see Fig.8)	–	12	16	mA
Video amplifier inputs						
VIN(0-2) INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	AGC load with external capacitor; note 1	0.6	–	1.5	V
$\|Z_i\|$	input impedance	f = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	µA
GATE A AND GATE B TTL INPUTS (SEE FIGS 4 AND 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	µA
RPEAK INPUT (PIN 28)						
I_{28}	minimum peak level current	$R_{28} = 0$ Ω	–	80	150	µA
AGC INPUT (PIN 25)						
V_{25}	AGC voltage for minimum gain		–	2.8	–	V
V_{25}	AGC voltage for maximum gain		–	4.0	–	V
	AGC output current	see Table 2	–	–	–	
CLAMP INPUT (PIN 24)						
V_{24}	CLAMP voltage for code 128 output		–	3.5	–	V
I_{24}	CLAMP output current	see Table 3	–	–	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	output AC voltage (peak-to-peak value)	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	-	-	1.0	mA
V_{19}	output DC voltage for black level	note 3	–	V_{CCA}–2.24	–	V
Z_{19}	output impedance		–	20	–	Ω
Video amplifier dynamic characteristics						
α	crosstalk between VIN inputs		–	–60	–55	dB
G_{diff}	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	2	–	%
ϕ_{diff}	differential phase		–	2	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range		–4.5	–	6.0	dB
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{CLK} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{CLK} = 10 MHz	–	4.5	–	pF
OF input (3-state) (see Table 4)						
V_{IL}	LOW level input voltage		0	–	0.2	V
V_{IH}	HIGH level input voltage		2.6	–	V_{CCD}	V
V_9	input voltage in HIGH-Z state		–	1.15	–	V
I_{IL}	LOW level input current		–370	–300	–	μA
I_{IH}	HIGH level input current		–	360	450	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN INPUT (PIN 20) (SEE TABLE 5)						
V_{20}	input voltage	digital out = 00	–	V_{CCA}–2.41	–	V
V_{20}	input voltage	digital out = 255	–	V_{CCA}–1.41	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D(0-7)						
V_L	LOW level output voltage	I_O = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	μA
Switching characteristics						
f_{CLK}	CLK input maximum frequency	see Fig.6; note 6	30	32	–	MHz
Analog signal processing (f_{CLK} = 32 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); note 7; Fig.3	–	2	–	%
ϕ_{diff}	differential phase	note 7; Fig.3	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz; note 7	–	–55	–	dB
SVRR	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function (see Fig.8)						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{CLK} = 32 MHz; see Figs 6, 7 and 8)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA)						
t_{dS}	sampling delay		–	2	–	ns
t_{HD}	output hold time		6	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time - output enable		–	19	25	ns
t_{dDZ}	3-state delay time - output disable		–	14	20	ns

Notes to the characteristics

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)}$ = 1.33 V

Notes to the characteristics

2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referred to V_{CC} and defined as:

   AC impedance ≥ 1 kΩ and the DC impedance > 2.7 kΩ.

   The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Control mode 2 is selected.
4. Signal-to-noise ratio measured with 5 MHz bandwidth

$$SN = 20 \log \frac{V_{ANNOUT(p-p)}}{V_{ANNOUT}\ noise\ RMS\ (B = 5\ MHz)}$$

5. The voltage ratio is expressed as:

$$SVRR = 20 \log \frac{\Delta V_{CCA}}{\Delta G/G}$$

   for V_I = 1 V (p-p), 100 kHz gain = 1 and 1 V supply variation.
6. It is recommended that the rise and fall times of the clock are not less than 2 ns. In addition, a 'good lay-out' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR = \frac{\Delta[V_{IN(00)} - V_{IN(FF)}] + [V_{IN(00)} - V_{IN(FF)}]}{\Delta V_{CCA}}$$

9. Full-scale sinewave (f_I = 4.4 MHz; f_{CLK}, $f_{\overline{CLK}}$ = 27 MHz).

Table 1 Video input selection (CVBS)

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 AGC output current

GATE A	GATE B	DIGITAL OUTPUT	I_{AGC}	MODE
1	1	output < 255 output > 255	−2.5 μA I_{PEAK}	1
0	X	output < 248 output > 248	0 I_{PEAK}	2; note 2
1	0	output < 0 0 < output < 248 output > 248	+2.5 μA −2.5 μA I_{PEAK}	2; note 2

Notes to Table 2

1. Where X = don't care
2. Mode 2 can only be initialized with successive pulses on GATE A and GATE B (see Fig.5)

Table 3 CLAMP output current

GATE A	GATE B	DIGITAL OUTPUT	I_{CLAMP}	MODE
1	1	output < 0 output > 0	I_{PEAK} −2.5 μA	1
X	0	X	0	2
0	1	output < 64 64 < output	+50 μA −50 μA	2

Note to Table 3

1. Where X = don't care

Table 4 OF input coding

OF	D0 TO D7
0	active, two's complement
1	high impedance
open circuit (note 1)	active, binary

Note to Table 4

1. Use C ≥ 10 pF to DGND

Table 5 ADC output current

		BINARY OUTPUTS								TWO'S COMPLEMENT							
STEP	V_{ADCIN}	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} - 2.41 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254		1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} - 1.41 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow		1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

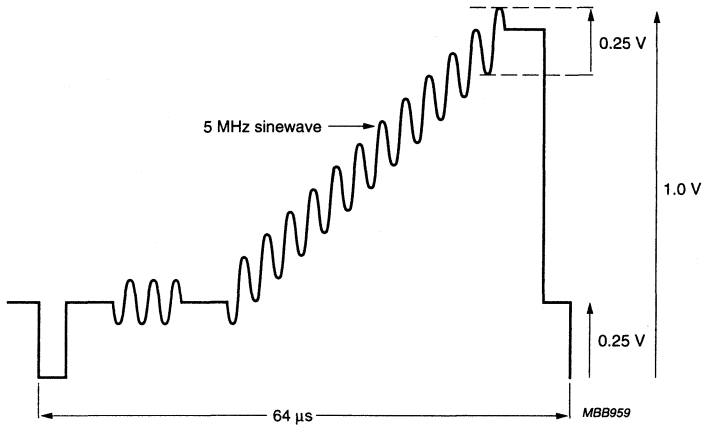


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

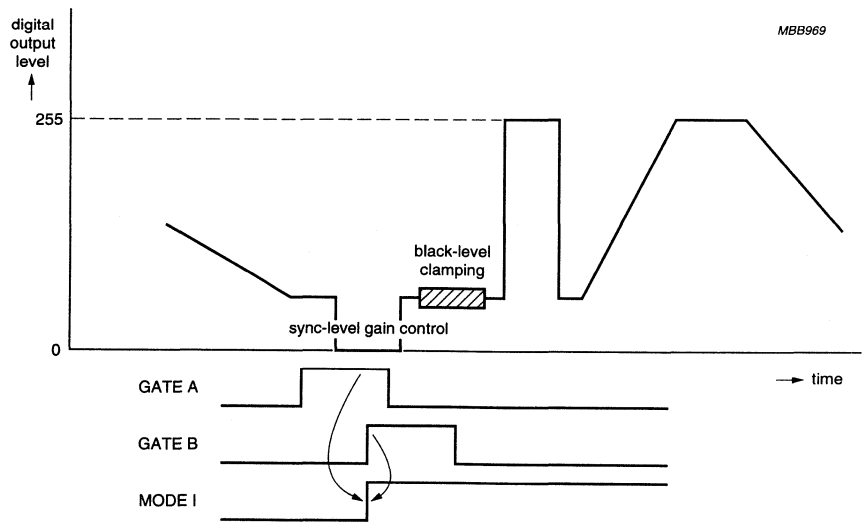


Fig.4 Control mode 1.

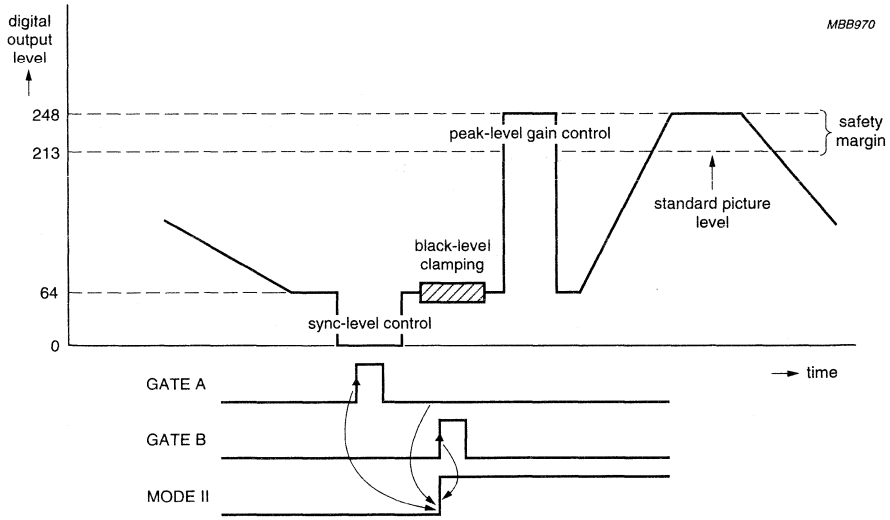


Fig.5 Control mode 2.

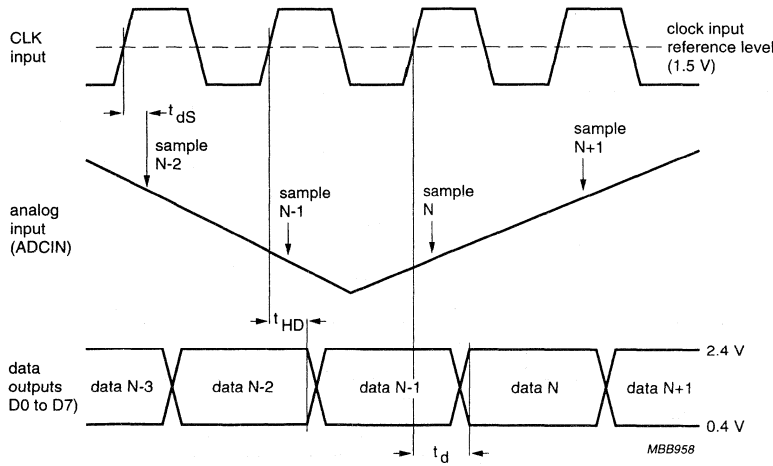


Fig.6 Timing diagram.

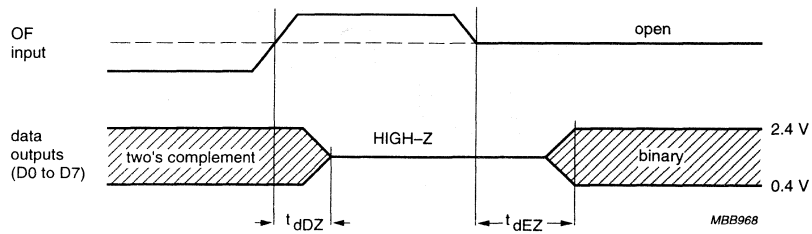


Fig.7 Output format timing diagram.

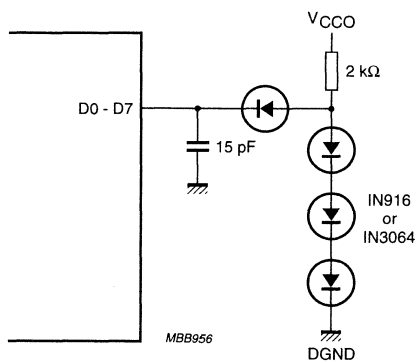


Fig.8 Load circuit for timing measurement; data outputs (OF = LOW or open-circuit).

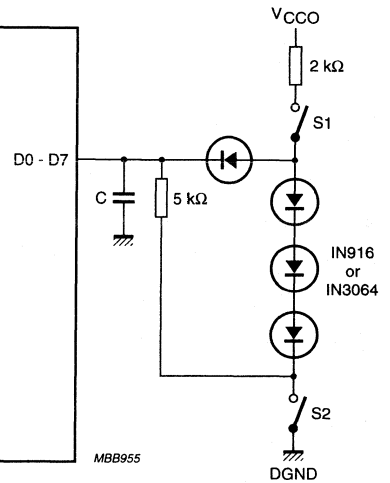


Fig.9 Load circuit for timing measurement; 3-state outputs (OF: f_i = 1 MHz; V_{OF} = 3 V).

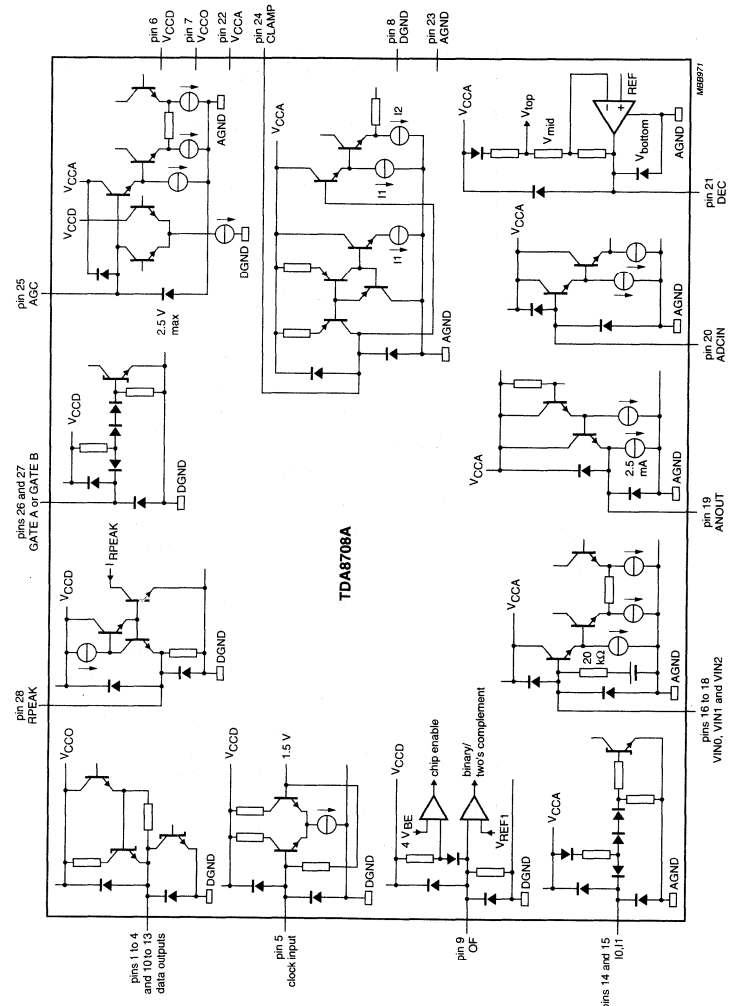
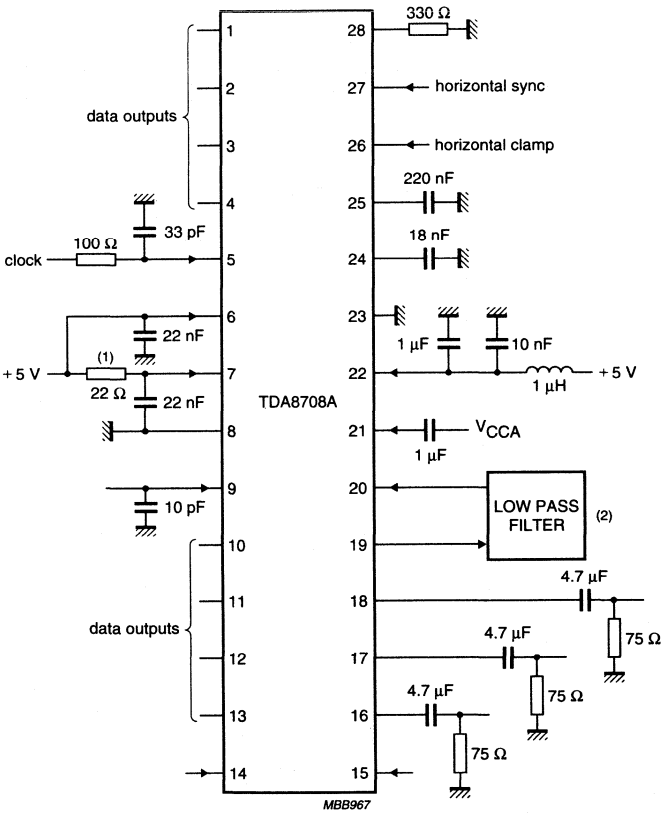


Fig.10 Internal pin configuration.

APPLICATION INFORMATION

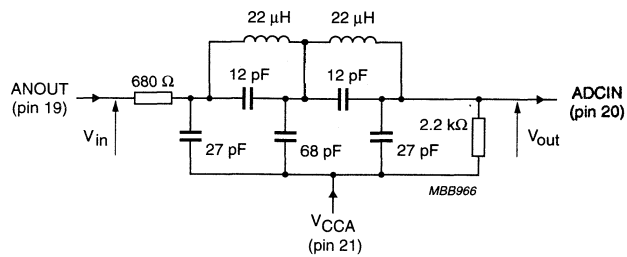
Additional information can be found in the laboratory report FTV/8902.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8708A interfaces with a capacitive CMOS load device.

(2) See Fig.12 for an example of the low pass filter.

Fig.11 Application diagram.



These filters can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ respectively must in any case be applied.

Fig.12 Example of a low pass filter for CVBS signal.

Video analog input interface TDA8709

FEATURES

- 8-bit resolution
- Sampling rate up to 30 MHz
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Low level AC clock inputs and outputs
- Clamp function with selection for '16' or '128'
- No sample-and-hold circuit required
- Three selectable video inputs

APPLICATIONS

- Video signal processing
- Digital picture processing
- Frame grabbing
- Colour difference signals (U, V)
- Y, R, G, B signals
- Chrominance signal (C)

DESCRIPTION

The TDA8709 is a bipolar analog input interface for video signal processing. It includes an input selector (1 out of three video signals), video amplifier with clamp and external gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 30 MHz.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	40	47	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum clock frequency	30	–	–	MHz
B	maximum –3 dB bandwidth (preamplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	380	512	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8709	28	DIL	plastic	SOT117
TDA8709T	28	SO28	plastic	SOT136A

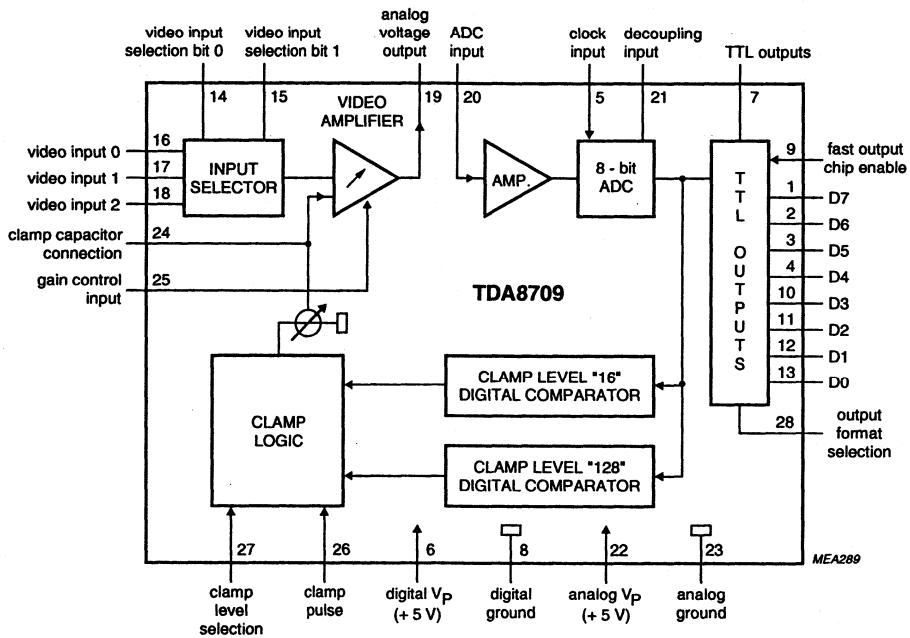


Fig.1 Block diagram.

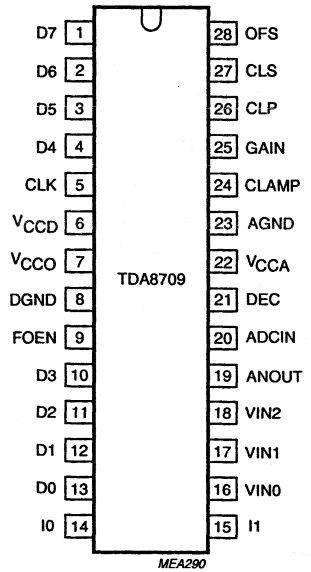


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output, bit 7 (MSB)
D6	2	data output, bit 6
D5	3	data output, bit 5
D4	4	data output, bit 4
CLK	5	clock input
V_{CCD}	6	digital positive supply voltage (+5 V)
V_{CCO}	7	TTL outputs positive supply voltage (+5 V)
DGND	8	digital ground
FOEN	9	fast output chip enable
D3	10	data output, bit 3
D2	11	data output, bit 2
D1	12	data output, bit 1
D0	13	data output, bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog positive supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
GAIN	25	gain control input
CLP	26	clamp pulse
CLS	27	clamp level selection
OFS	28	output format selection

FUNCTIONAL DESCRIPTION

The TDA8709 is an 8-bit ADC with internal clamping and a preamplifier with adjustable gain.

The clamping value is switched via pin 27 between digital 16 (for luminance or R, G, B signals) and digital 128 (for chrominance or colour difference signals). While clamping pulse at pin 27 is logic 1, the device will adjust the clamp level to the chosen value. The output format can be selected between binary and two's complement at pin 28.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+7.0	V
V_{CCD}	digital supply voltage range	−0.3	+7.0	V
V_{CCO}	output supply voltage range	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage difference	−0.5	+0.5	V
$V_{CCO} - V_{CCD}$	supply voltage difference	−0.5	+0.5	V
$V_{CCA} - V_{CCO}$	supply voltage difference	−1.0	+1.0	V
V_I	input voltage range	−0.3	+7.0	V
I_O	output current	−	+10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT117)	55 K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT136A)	70 K/W

CHARACTERISTICS

$V_{CCA} = V_{22} - V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6 - V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7 - V_8 = 4.2$ to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCA} - V_{CCO} = -0.5$ to +0.5 V; $T_{amb} = 0$ to +70 °C; Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	40	47	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	output supply current	TTL load (see Fig.8)	–	12	16	mA
Preamplifier inputs						
VIN(0-2) INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)		0.3	1	1.6	V
$\|Z_i\|$	input impedance	f = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	µA
CLS, OFS, CLP, TTL INPUTS (SEE FIG 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	µA
GAIN INPUT (PIN 25)						
V_{25}	voltage for minimum gain	see Fig.3	–	1.5	–	V
V_{25}	voltage for maximum gain	see Fig.3	–	4.2	–	V
I_I	input current		–	1.0	–	µA
	stability gain/temperature	see Fig.3	–	6	–	%
CLAMP INPUT (PIN 24)						
I_{24}	CLAMP output current	see Table 2	–	–	–	
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	output AC voltage (peak-to-peak value)	$V_{VIN} = 1$ V (p-p); $V_{25} = 3$ V	–	1.0	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	$V_{ANOUT} = 1$ V (p-p); note 1	-	-	1.0	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{19}	output DC voltage for black level	CLS = logic 1	–	V_{CCA}–2.65	–	V
V_{19}	output DC voltage for black level	CLS = logic 0	–	V_{CCA}–3.1	–	V
Z_{19}	output impedance		–	20	–	Ω
Preamplifier dynamic characteristics						
α	crosstalk between VIN inputs	note 2	–	–60	–55	dB
G_d	differential gain	V_{VIN} = 1 V (p-p); V_{25} = 3 V	–	2	–	%
ϕ_d	differential phase		–	2	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 3	60	–	–	dB
SVRR	supply voltage ripple rejection	note 4	–	45	–	dB
ΔG	gain range		–4.5	–	10	dB
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{CLK} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{CLK} = 10 MHz	–	4.5	–	pF
FOEN TTL input (see Table 3)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_9 = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_9 = 2.7 V	–	–	+20	μA
ADCIN INPUT (PIN 20) (SEE TABLE 4)						
V_{20}	input voltage	digital out = 00	–	V_{CCA} –1.6	–	V
V_{20}	input voltage	digital out = 255	–	V_{CCA} –1.1	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	0.5	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D(0-7)						
V_{OL}	LOW level output voltage	I_O = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics						
f_{CLK}	CLK input maximum frequency	see Fig.6; note 5	30	–	–	MHz
Analog signal processing (f_{CLK} = 30 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 0.5 V (p-p); note 6; see Fig.4	–	2	–	%
ϕ_{diff}	differential phase	note 6; see Fig.4	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 6	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz; note 6	–	–55	–	dB
SVRR	supply voltage ripple rejection	note 7	–	1	5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 8	–	–	±2	LSB
Timing (f_{CLK} = 30 MHz; see Figs 6, 7 and 8)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA)						
t_{dS}	sampling delay		–	2	–	ns
t_{HD}	output hold time		–	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time - output enable		–	16	25	ns
t_{dDZ}	3-state delay time - output disable		–	12	25	ns

Notes to the characteristics

1. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referred to V_{CC} and is defined as:

   AC impedance ≥ 1 kΩ and DC impedance > 2.7 kΩ

   The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
2. Input signals with the same amplitude. Gain is adjusted to obtain ANOUT = 1 V (p-p)
3. Signal-to-noise ratio measured with 5 MHz bandwidth

   $$SN = 20 \log \frac{V_{ANNOUT(p\text{-}p)}}{V_{ANNOUT}\ noise\ RMS\ (B = 5\ MHz)}$$
4. The voltage ratio is expressed as:

   $$SVRR = 20 \log \frac{\Delta V_{CCA}}{\Delta G/G}$$

   for V_i = 1 V (p-p), 100 kHz gain = 1 and 1 V supply variation.

Notes to the characteristics

5. It is recommended that the rise and fall times of the clock are not less than 2 ns. In addition, a 'good lay-out' for the digital and analog grounds is recommended.
6. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
7. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR = \frac{\Delta[V_{IN(00)} - V_{IN(FF)}] + [V_{IN(00)} - V_{IN(FF)}]}{\Delta V_{CCA}}$$

8. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}, $f_{\overline{CLK}}$ = 27 MHz).

Table 1 Video input selection (CVBS)

I1	I0	SELECTED INPUT
0	0	VIN0
1	0	VIN2
0	1	VIN1
1	1	VIN1

Table 2 CLAMP output current

CLS	CLP	DIGITAL OUTPUT	I_{CLAMP}
1	1	output < 128 output > 128	+50 µA −50 µA
X	0	X	0
0	1	output < 16 16 < output	+50 µA −50 µA

Table 3 FOEN input current

FOEN	D0 TO D7
0	active
1	high impedance

Note

Where; X = don't care

Table 4 ADC output current

		OFS = 0 BINARY OUTPUTS								OFS = 1 TWO'S COMPLEMENT							
STEP	V_{ADCIN}	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} - 1.6 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254		1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} - 1.1 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow		1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

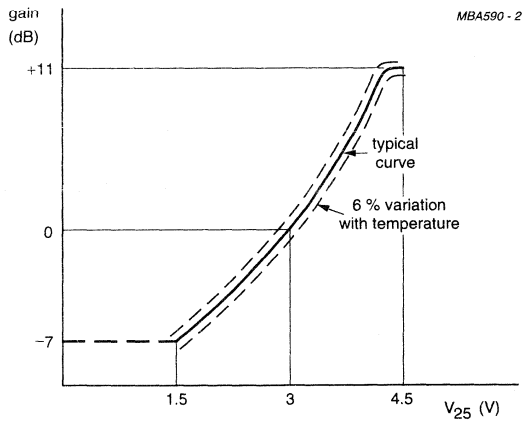


Fig.3 Typical gain control curve as a function of gain voltage.

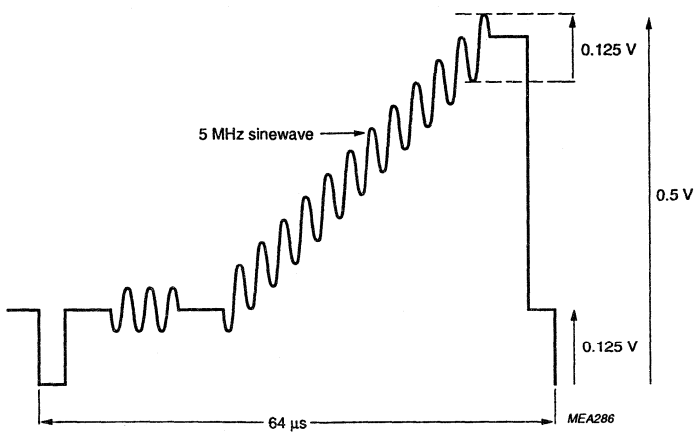


Fig.4 Test signal on the ADCIN pin for differential gain and phase measurements.

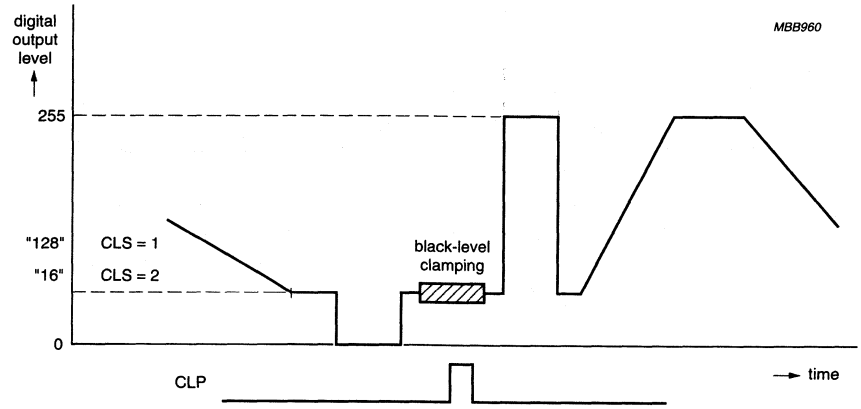


Fig.5 Control mode selection.

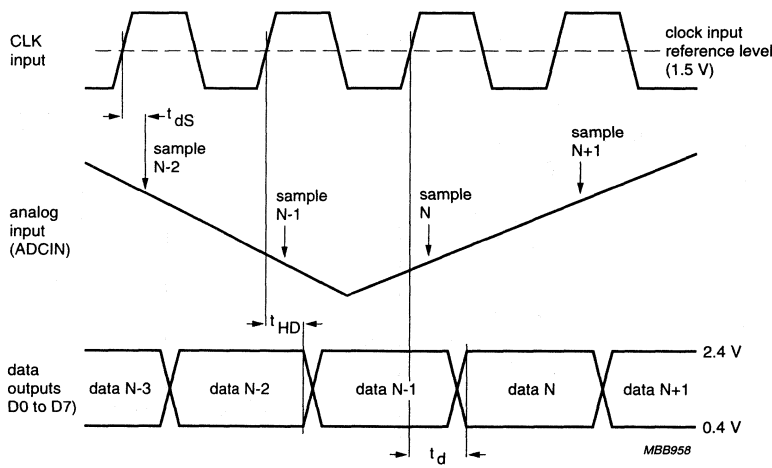


Fig.6 Timing diagram.

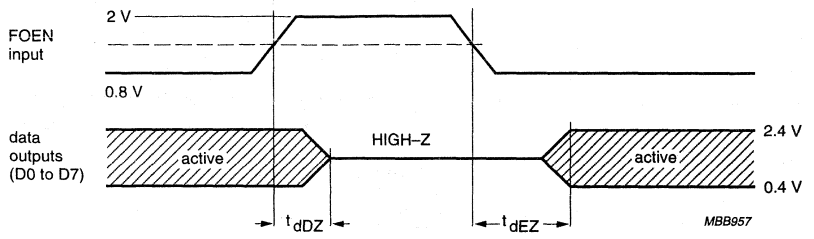


Fig.7 Output format timing diagram.

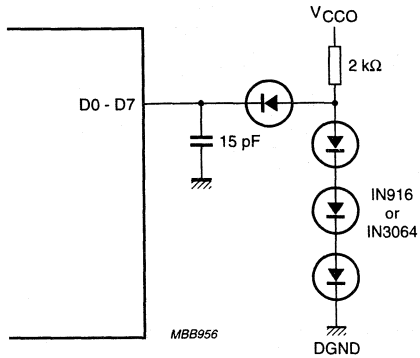


Fig.8 Load circuit for timing measurement; data outputs (FOEN = LOW).

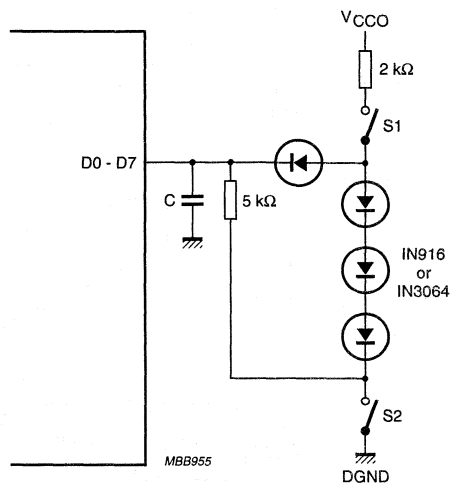


Fig.9 Load circuit for timing measurement; 3-state outputs (FOEN: f_i = 1 MHz; V_{FOEN} = 3 V).

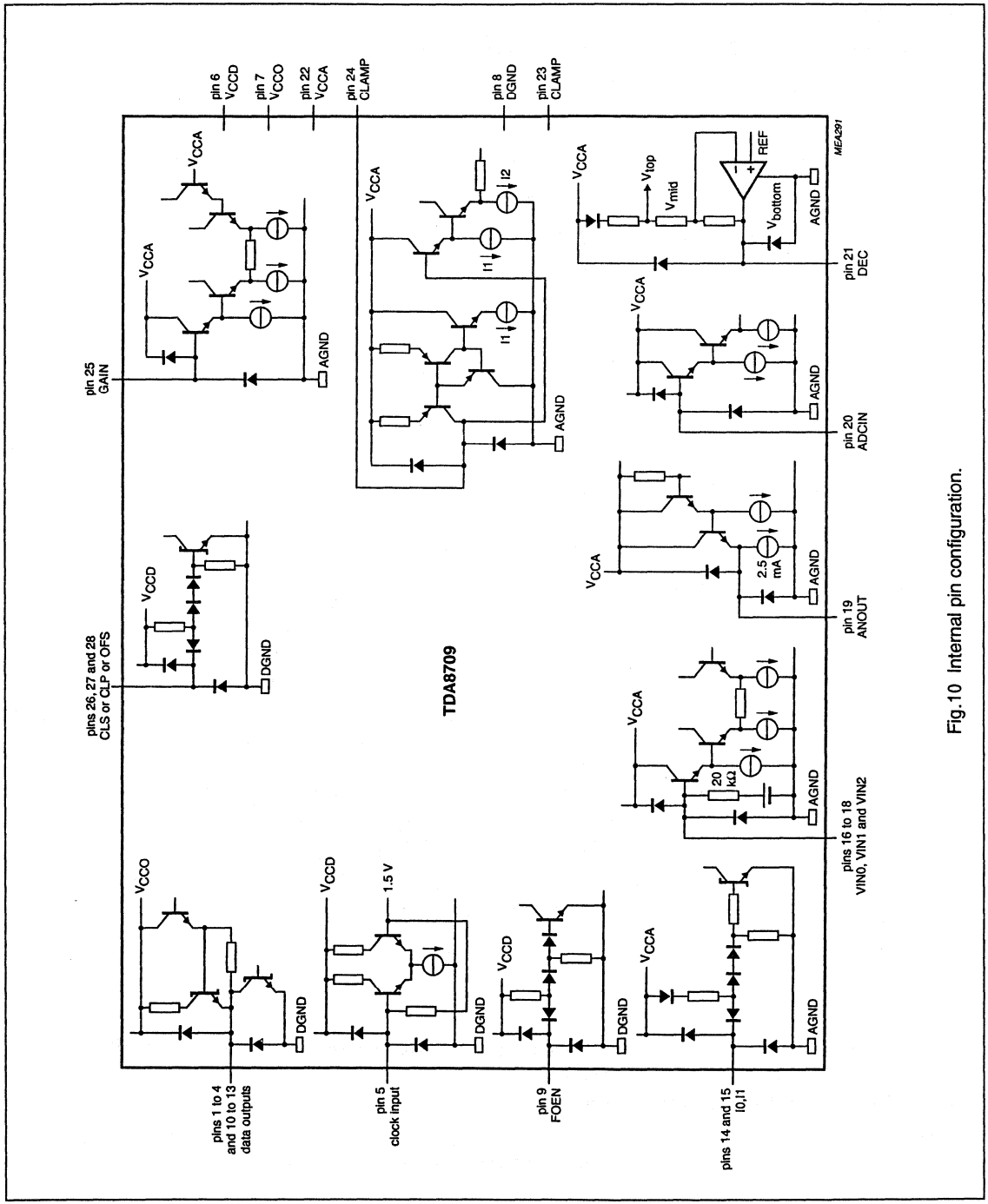
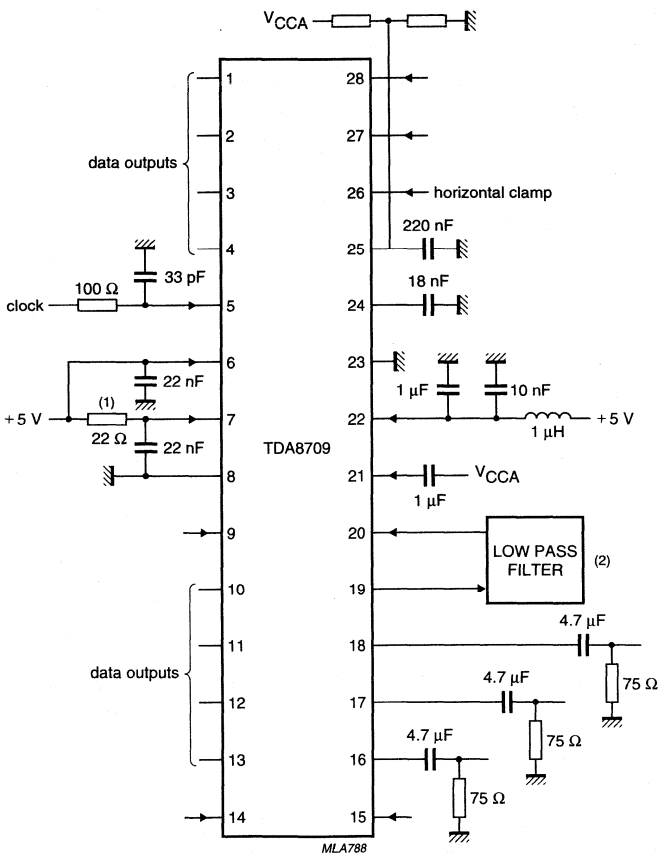


Fig.10 Internal pin configuration.

APPLICATION INFORMATION

Additional information can be found in the laboratory report FTV/9002.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8709 interfaces with a capacitive CMOS load device.

(2) See Figs 12 and 13 for filter examples.

Fig.11 Application diagram.

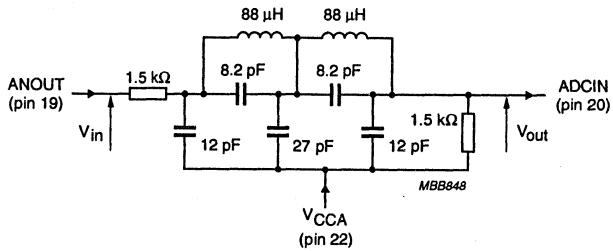


Fig.12 Example of lowpass filter for Y and C signals.

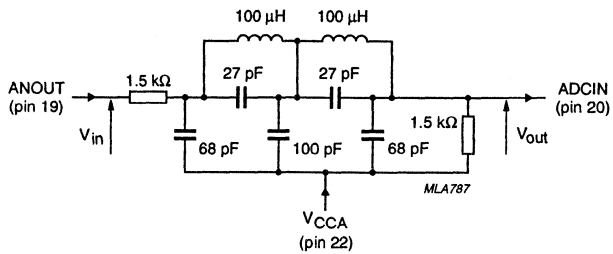


Fig.13 Example of lowpass filter for U, V and RGB signals.

Note to figures 12 and 13

These filters can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 1.5 kΩ must in any case be applied.

Video analog input interface TDA8709A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Low level AC clock inputs and outputs
- Clamp function with selection for '16' or '128'
- No sample-and-hold circuit required
- Three selectable video inputs
- ADC input voltage amplitude 1.0 V (p-p) as against 0.5 V for TDA8709

APPLICATIONS

- Video signal processing
- Digital picture processing
- Frame grabbing
- Colour difference signals (U, V)
- Y, R, G, B signals
- Chrominance signal (C)

DESCRIPTION

The TDA8709A is a bipolar analog input interface for video signal processing. It includes an input selector (1 out of three video signals), video amplifier with clamp and external gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	40	47	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (preamplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	380	512	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8709A	28	DIL	plastic	SOT117
TDA8709A	28	SO28	plastic	SOT136A

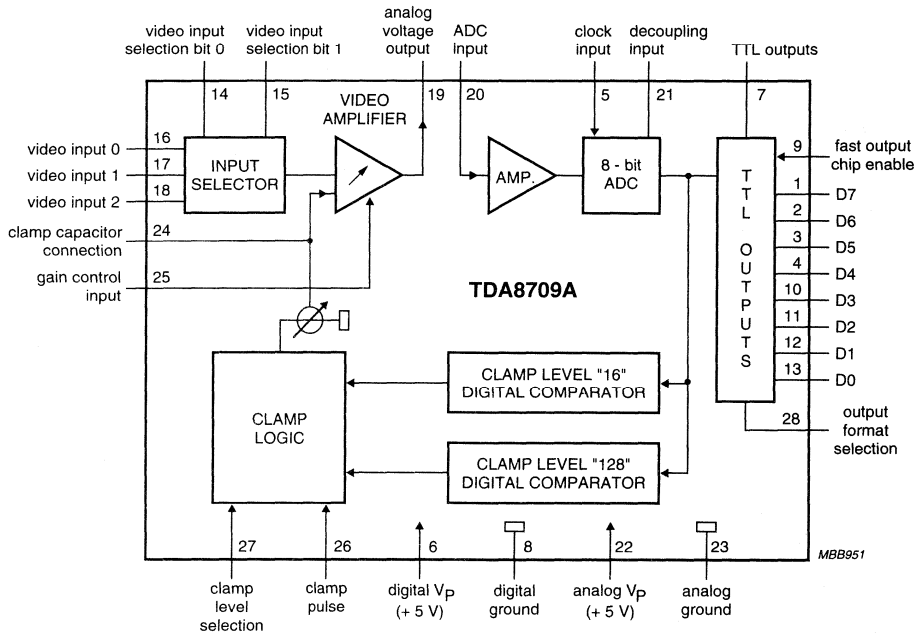


Fig.1 Block diagram.

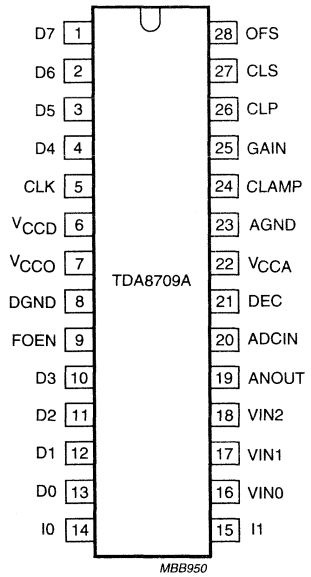


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output, bit 7 (MSB)
D6	2	data output, bit 6
D5	3	data output, bit 5
D4	4	data output, bit 4
CLK	5	clock input
V_{CCD}	6	digital positive supply voltage (+5 V)
V_{CCO}	7	TTL outputs positive supply voltage (+5 V)
DGND	8	digital ground
FOEN	9	fast output chip enable
D3	10	data output, bit 3
D2	11	data output, bit 2
D1	12	data output, bit 1
D0	13	data output, bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog positive supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
GAIN	25	gain control input
CLP	26	clamp pulse
CLS	27	clamp level selection
OFS	28	output format selection

FUNCTIONAL DESCRIPTION

The TDA8709A is an 8-bit ADC with internal clamping and a preamplifier with adjustable gain.

The clamping value is switched via pin 27 between digital 16 (for luminance or R, G, B signals) and digital 128 (for chrominance or colour difference signals). While clamping pulse at pin 27 is logic 1, the device will adjust the clamp level to the chosen value. The output format can be selected between binary and two's complement at pin 28.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+7.0	V
V_{CCD}	digital supply voltage range	−0.3	+7.0	V
V_{CCO}	output supply voltage range	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage difference	−0.5	+0.5	V
$V_{CCO} - V_{CCD}$	supply voltage difference	−0.5	+0.5	V
$V_{CCA} - V_{CCO}$	supply voltage difference	−1.0	+1.0	V
V_I	input voltage range	−0.3	+7.0	V
I_O	output current	−	+10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT117)	55 K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT136A)	70 K/W

CHARACTERISTICS

$V_{CCA} = V_{22} - V_{23}$ = 4.5 to 5.5 V; $V_{CCD} = V_6 - V_8$ = 4.5 to 5.5 V; $V_{CCO} = V_7 - V_8$ = 4.2 to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD}$ = −0.5 to +0.5 V; $V_{CCO} - V_{CCD}$ = −0.5 to +0.5 V; $V_{CCA} - V_{CCO}$ = −0.5 to +0.5 V; T_{amb} = 0 to +70 °C; Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	40	47	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	output supply current	TTL load (see Fig.8)	–	12	16	mA
Preamplifier inputs						
VIN(0-2) INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	note 1	0.6	–	1.5	V
$\|Z_I\|$	input impedance	f = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	µA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	µA
CLS, OFS, CLP, TTL INPUTS (SEE FIG 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	µA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	µA
GAIN INPUT (PIN 25)						
V_{25}	voltage for minimum gain	see Fig.3	–	1.8	–	V
V_{25}	voltage for maximum gain	see Fig.3	–	3.8	–	V
I_I	input current		–	1.0	–	µA
	stability gain/temperature	see Fig.3	–	6	–	%
CLAMP INPUT (PIN 24)						
I_{24}	CLAMP output current	see Table 2	–	–	–	
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	output AC voltage (peak-to-peak value)	V_{OF} = 1.33 V (p-p); V_{25} = 3 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	–	–	1.0	mA
V_{19}	output DC voltage for black level	CLS = logic 1	–	V_{CCA}–2.02	–	V
V_{19}	output DC voltage for black level	CLS = logic 0	–	V_{CCA}–2.6	–	V
Z_{19}	output impedance		–	20	–	Ω
Preamplifier dynamic characteristics						
α	crosstalk between VIN inputs	note 3	–	–60	–55	dB
G_d	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3 V	–	2	–	%
ϕ_d	differential phase		–	2	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range		–4.5	–	10	dB
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{CLK} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{CLK} = 10 MHz	–	4.5	–	pF
FOEN TTL input (see Table 3)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_9 = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_9 = 2.7 V	–	–	+20	μA
ADCIN INPUT (PIN 20) (SEE TABLE 4)						
V_{20}	input voltage	digital out = 00	–	V_{CCA}–2.52	–	V
V_{20}	input voltage	digital out = 255	–	V_{CCA}–1.52	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D(0-7)						
V_{OL}	LOW level output voltage	I_O = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.4	–	V_{CCD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	–	+20	µA
Switching characteristics						
f_{CLK}	CLK input maximum frequency	see Fig.6; note 6	30	32	–	MHz
Analog signal processing (f_{CLK} = 32 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); note 7; see Fig.4	–	2	–	%
ϕ_{diff}	differential phase	note 7; see Fig.4	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz; note 7	–	−55	–	dB
SVRR	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{CLK} = 32 MHz; see Figs 6, 7 and 8)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA)						
t_{dS}	sampling delay		–	2	–	ns
t_{HD}	output hold time		–	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time - output enable		–	16	25	ns
t_{dDZ}	3-state delay time - output disable		–	12	25	ns

Notes to the characteristics

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)}$ = 1.33 V
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referred to V_{CC} and is defined as:

   AC impedance ≥ 1 kΩ and DC impedance > 2.7 kΩ

   The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Input signals with the same amplitude. Gain is adjusted to obtain ANOUT = 1.33 V (p-p)
4. Signal-to-noise ratio measured with 5 MHz bandwidth

$$SN = 20 \log \frac{V_{ANNOUT(p-p)}}{V_{ANNOUT}\ noise\ RMS\ (B = 5\ MHz)}$$

5. The voltage ratio is expressed as:

$$SVRR = 20 \log \frac{\Delta V_{CCA}}{\Delta G/G}$$

for V_I = 1 V (p-p), 100 kHz gain = 1 and 1 V supply variation.

Notes to the characteristics

6. It is recommended that the rise and fall times of the clock are not less than 2 ns. In addition, a 'good lay-out' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR = \frac{\Delta[V_{IN(00)} - V_{IN(FF)}] + [V_{IN(00)} - V_{IN(FF)}]}{\Delta V_{CCA}}$$

9. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}, $f_{\overline{CLK}}$ = 27 MHz).

Table 1 Video input selection (CVBS)

I1	I0	SELECTED INPUT
0	0	VIN0
1	0	VIN2
0	1	VIN1
1	1	VIN1

Table 2 CLAMP output current

CLS	CLP	DIGITAL OUTPUT	I_{CLAMP}
1	1	output < 128 output > 128	+50 μA −50 μA
X	0	X	0
0	1	output < 16 16 < output	+50 μA −50 μA

Table 3 FOEN input current

FOEN	D0 TO D7
0	active
1	high impedance

Note

Where; X = don't care

Table 4 ADC output current

		OFS = 0 BINARY OUTPUTS								OFS = 1 TWO'S COMPLEMENT							
STEP	V_{ADCIN}	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} − 2.52 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254		1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} − 1.52 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow		1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

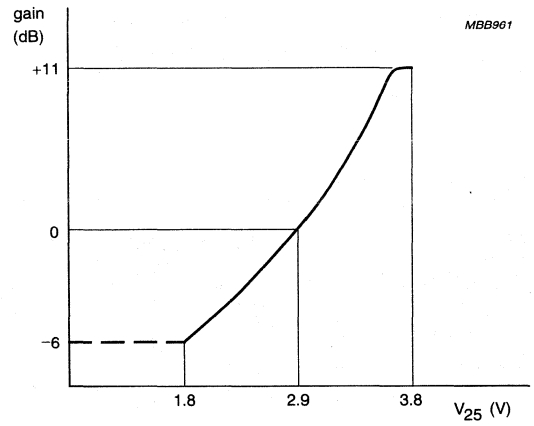


Fig.3 Typical gain control curve as a function of gain voltage ($V_{CCA} = V_{CCD} = 5$ V; $T_{amb} = 25$ °C).

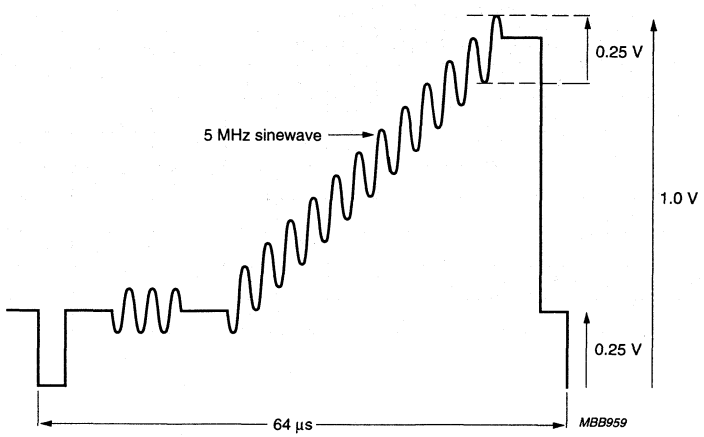


Fig.4 Test signal on the ADCIN pin for differential gain and phase measurements.

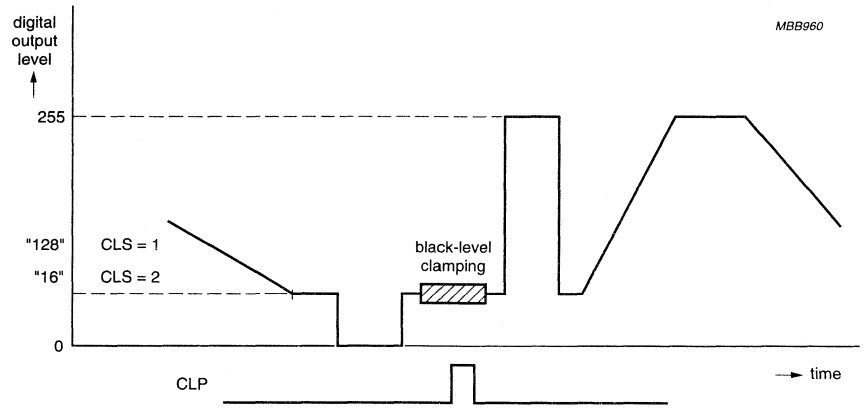


Fig.5 Control mode selection.

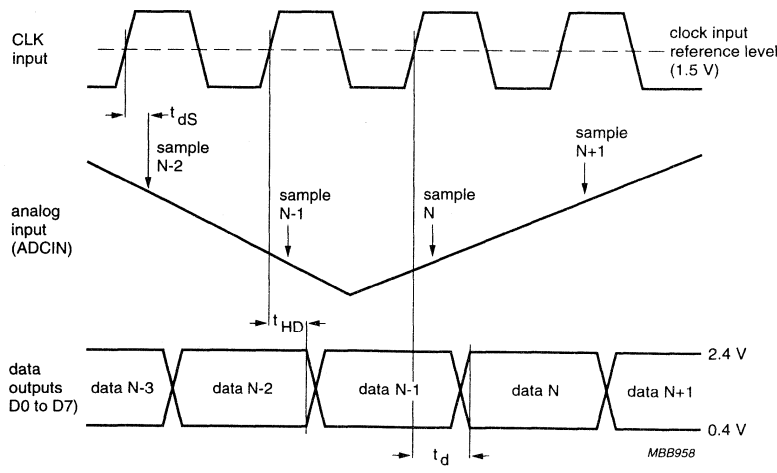


Fig.6 Timing diagram.

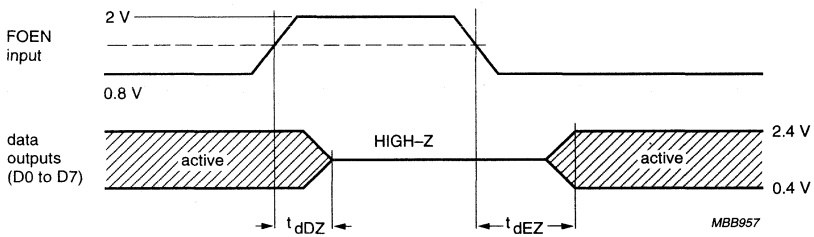


Fig.7 Output format timing diagram.

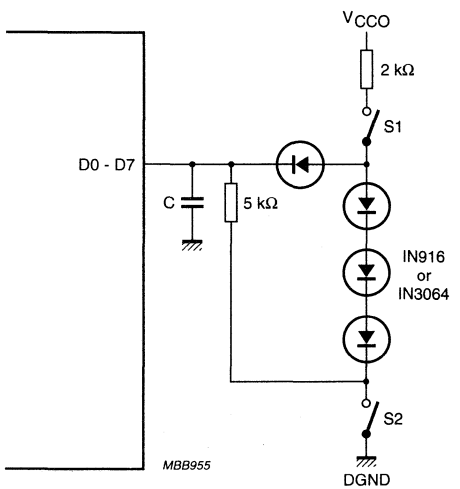


Fig.8 Load circuit for timing measurement; data outputs (FOEN = LOW).

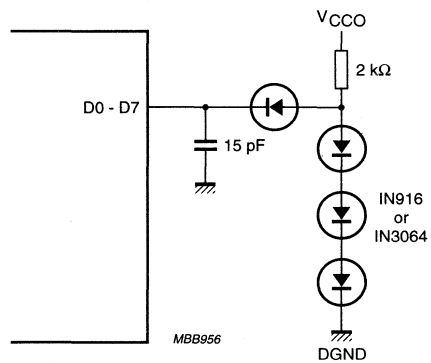


Fig.9 Load circuit for timing measurement; 3-state outputs (FOEN: f_i = 1 MHz; V_{FOEN} = 3 V).

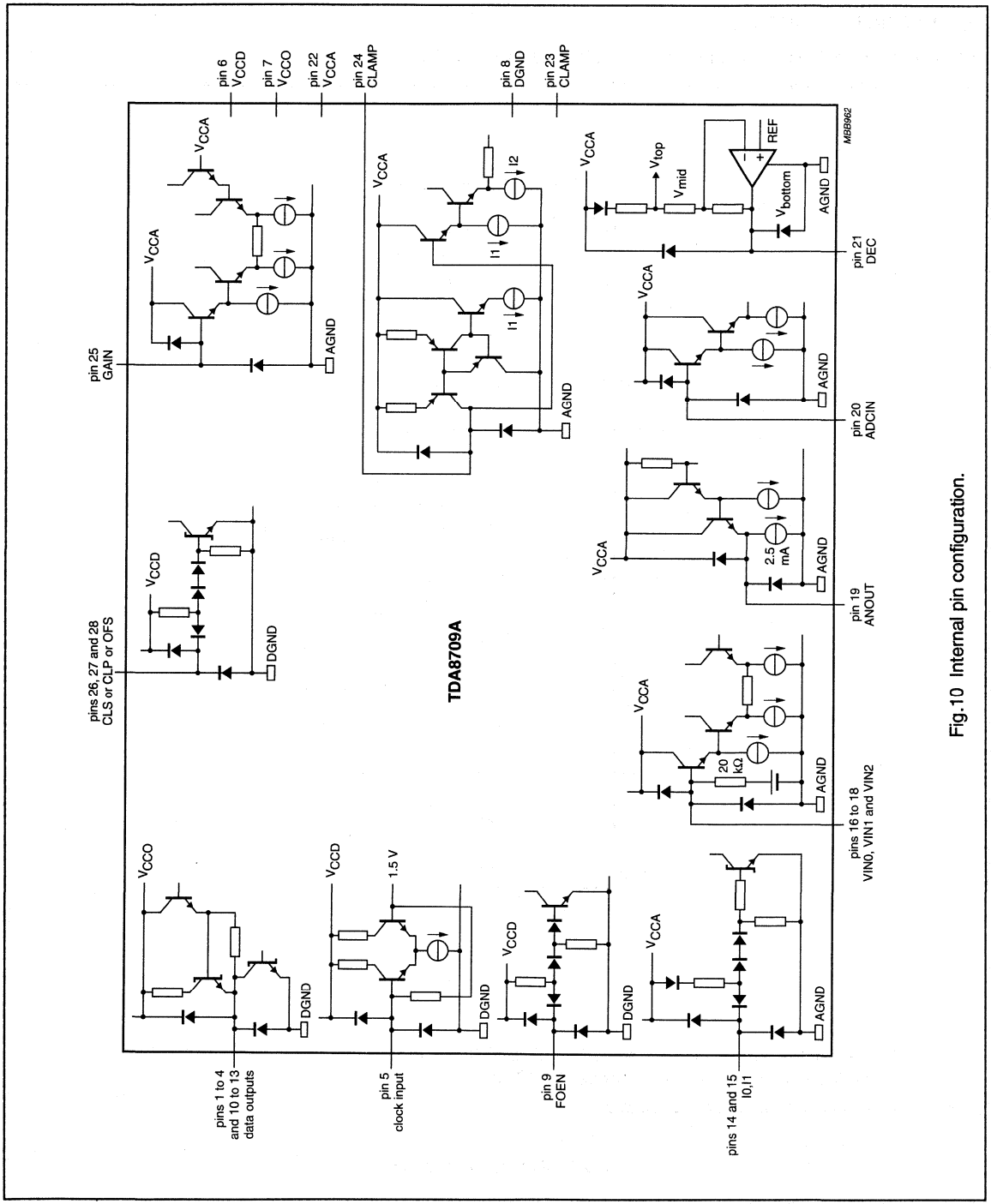
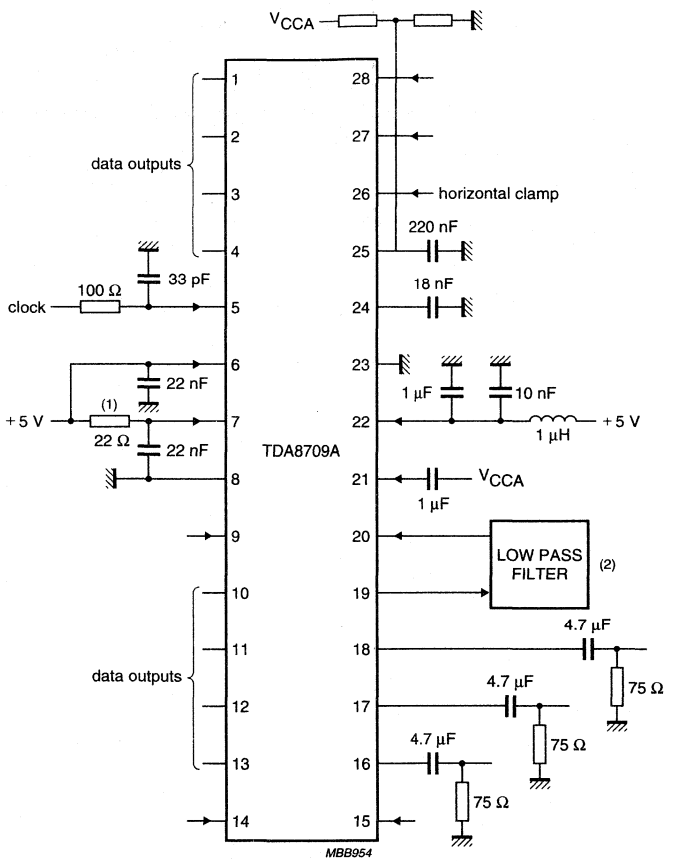


Fig.10 Internal pin configuration.

APPLICATION INFORMATION

Additional information can be found in the laboratory report FTV/9002.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8709A interfaces with a capacitive CMOS load device.

(2) See Figs 12 and 13 for filter examples.

Fig.11 Application diagram.

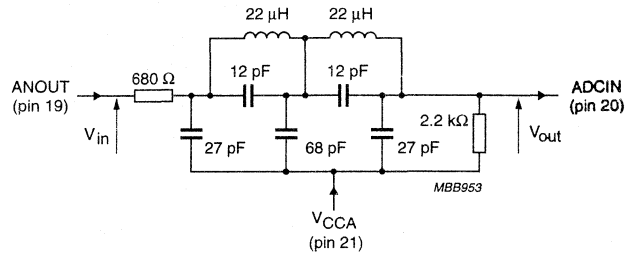


Fig.12 Example of lowpass filter for Y and C signals.

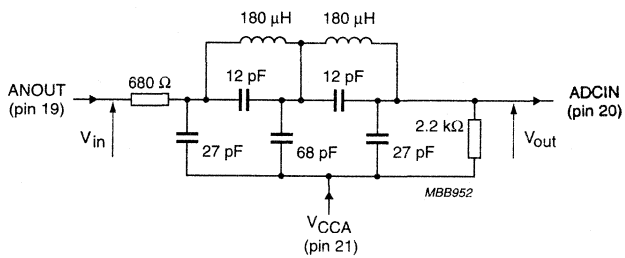


Fig.13 Example of lowpass filter for U, V and RGB signals.

Note to figures 12 and 13

These filters can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ respectively must in any case be applied.

8-bit video digital-to-analog converter

TDA8712

FEATURES

- 8-bit resolution
- Conversion rate up to 50 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglichting circuit required
- Internal input register
- Low power dissipation
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High speed digital-to-analog conversion
- Digital TV including:
  - field progressive scan
  - line progressive scan
- Subscriber TV decoders
- Satellite TV decoders
- Digital VCRs.

GENERAL DESCRIPTION

The TDA8712 is a monolithic bipolar 8-bit digital-to-analog converter (DAC) for video and other applications. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 50 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	–	26	32	mA
I_{CCD}	digital supply current	note 1	–	23	30	mA
V_{OUT}–$\overline{V_{OUT}}$	full-scale analog output voltage (peak-to-peak value)					
		Z_L = 10 kΩ	–1.45	–1.60	–1.75	V
		Z_L = 75 Ω	–0.72	–0.80	–0.88	V
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
f_{CLK}	maximum conversion rate		–	–	50	MHz
B	–3 dB bandwidth	f_{CLK} = 50 MHz	–	150	–	MHz
P_{tot}	total power dissipation		–	250	340	mW

Note to the Quick Reference Data

1. D0 to D7 are connected to V_{CCD}; CLK is connected to DGND.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8712	16	DIL	plastic	SOT38
TDA8712T	16	SO16L	plastic	SOT162A

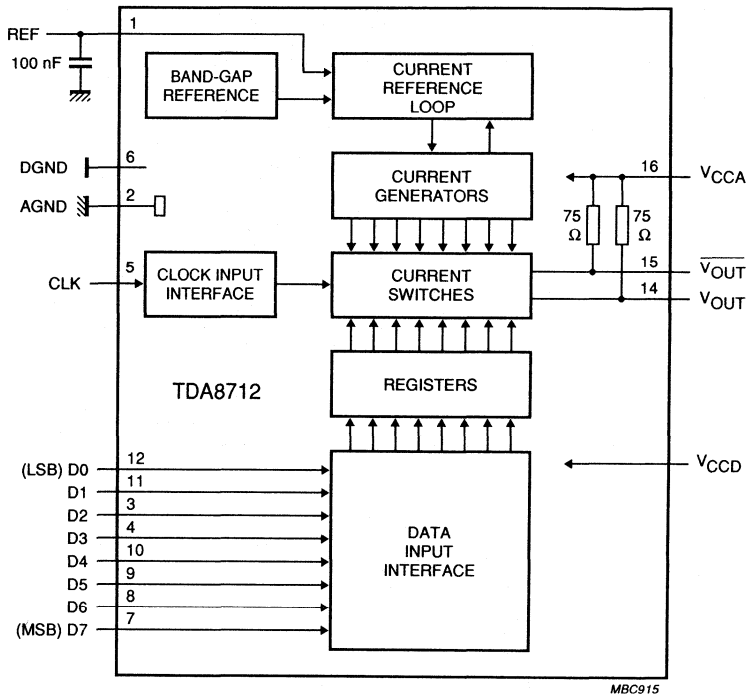


Fig.1 Block diagram.

8-bit video digital-to-analog converter

TDA8712

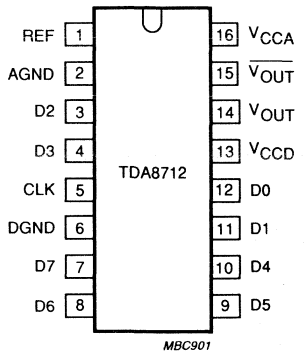


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input, bit 2
D3	4	data input, bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input, bit 7
D6	8	data input, bit 6
D5	9	data input, bit 5
D4	10	data input, bit 4
D1	11	data input, bit 1
D0	12	data input, bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$V_{\overline{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+7.0	V
V_{CCD}	digital supply voltage range	−0.3	+7.0	V
$V_{CCA}-V_{CCD}$	supply voltage differential	−0.5	+0.5	V
AGND–DGND	ground voltage differential	−0.1	+0.1	V
V_I	input voltage range (pins 3 to 5 and 7 to 12)	−0.3	V_{CCD}	V
$I_{OUT}/I_{\overline{OUT}}$	total output current range (pins 14 and 15)	−5	+26	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
T_j	junction temperature	−	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	
	SOT38	85 K/W
	SOT162A	110 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2 = 4.5$ V to 5.5 V; $V_{CCD} = V_{13} - V_6 = 4.5$ V to 5.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; V_{REF} decoupled to AGND by a 100 nF capacitor; $T_{amb} = 0$ °C to +70 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = 5$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	–	26	32	mA
I_{CCD}	digital supply current	note 1	–	23	30	mA
AGND–DGND	ground voltage differential		–0.1	–	+0.1	V
Inputs						
DIGITAL INPUTS (D7 TO D0) AND CLOCK INPUT (CLK)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–	–0.3	–0.4	mA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	0.01	20	µA
f_{CLK}	maximum clock frequency		50	–	–	MHz
Outputs (note 2; referenced to V_{CCA})						
V_{OUT}–$V_{\overline{OUT}}$	full-scale analog output voltages (peak-to-peak value)	$Z_L = 10$ kΩ $Z_L = 75$ Ω	–1.45 –0.72	–1.60 –0.80	–1.75 –0.88	V V
V_{OS}	analog offset output voltage	code = 0	–	–3	–25	mV
V_{OUT}/TC	full-scale analog output voltage temperature coefficient		–	–	200	µV/K
V_{OS}/TC	analog offset output voltage temperature coefficient		–	–	20	µV/K
B	–3 dB bandwidth	note 3; $f_{CLK} = 50$ MHz	–	150	–	MHz
G_{diff}	differential gain		–	0.6	–	%
Φ_{diff}	differential phase		–	1	–	deg
Z_o	output impedance		–	75	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
Switching characteristics (f_{CLK} = 50 MHz; notes 4 and 5; see Figs 3, 4 and 5)						
$t_{SU;DAT}$	data set-up time		−0.3	–	–	ns
$t_{HD;DAT}$	data hold time		2.0	–	–	ns
t_{PD}	propagation delay time		–	–	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	–	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	–	6.5	8.0	ns
t_d	input to 50% output delay time		–	3.0	5.0	ns
Output transients (glitches; (f_{CLK} = 50 MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	–	–	30	ns

Notes to the characteristics

1. D0 to D7 are connected to V_{CCD}, CLK is connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$ are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is 75 Ω (typ.).
3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).
4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $V_{\overline{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data is latched at the rising edge of the clock. The output voltage remains stable (independent of input data variations) during the HIGH level of the clock (CLK = HIGH). During a LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages (see Fig.5).
5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising edge of the clock and still be recognized. The data hold time ($t_{HD;DAT}$) is the minimum period following the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising edge of the clock and still be recognized.
6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of the offset voltage)

CODE	INPUT DATA (D7 to D0)	DAC OUTPUT VOLTAGES			
		Z_L = 10 kΩ		Z_L = 75 Ω	
		V_{OUT}	$\overline{V_{OUT}}$	V_{OUT}	$\overline{V_{OUT}}$
0	000 00 00	0	−1.6	0	−0.8
1	000 000 01	−0.006	−1.594	−0.003	−0.797
	.....				
128	100 000 00	−0.8	−0.8	−0.4	−0.4
	.....				
254	111 111 10	−1.594	−0.006	−0.797	−0.003
255	111 111 11	−1.6	0	−0.8	0

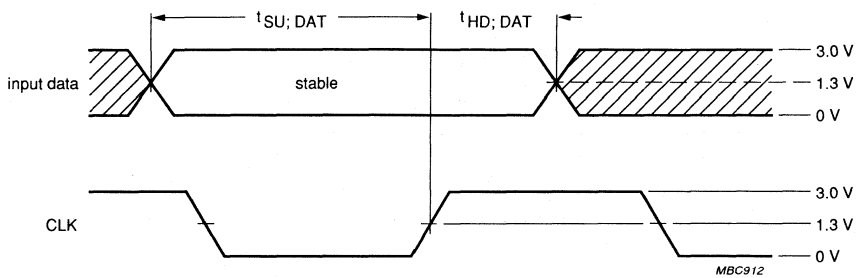


Fig.3 Data set-up and hold times.

Note to Figure 3

The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns after the first rising edge of the clock ($t_{SU;DAT}$ is negative; −0.3 ns). Data must be held at least 2 ns after the rising edge ($t_{HD;DAT}$ = +2 ns).

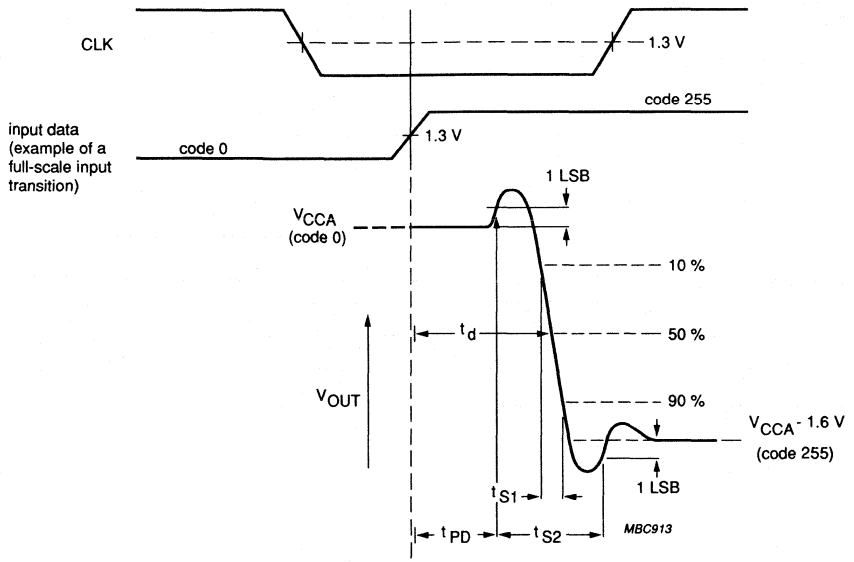


Fig.4 Switching characteristics.

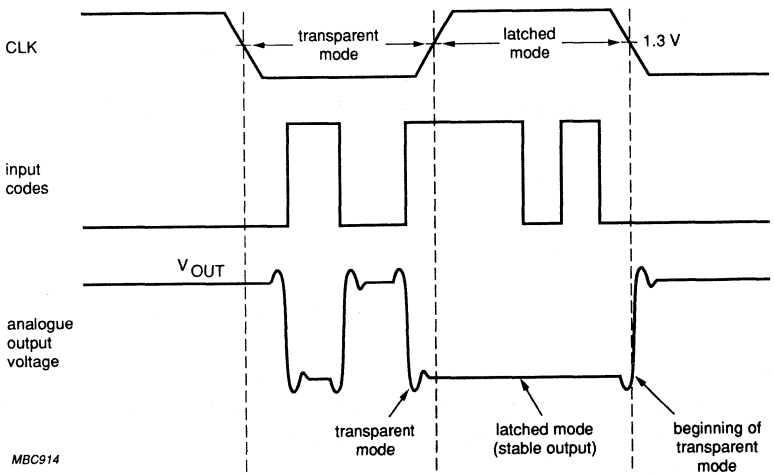
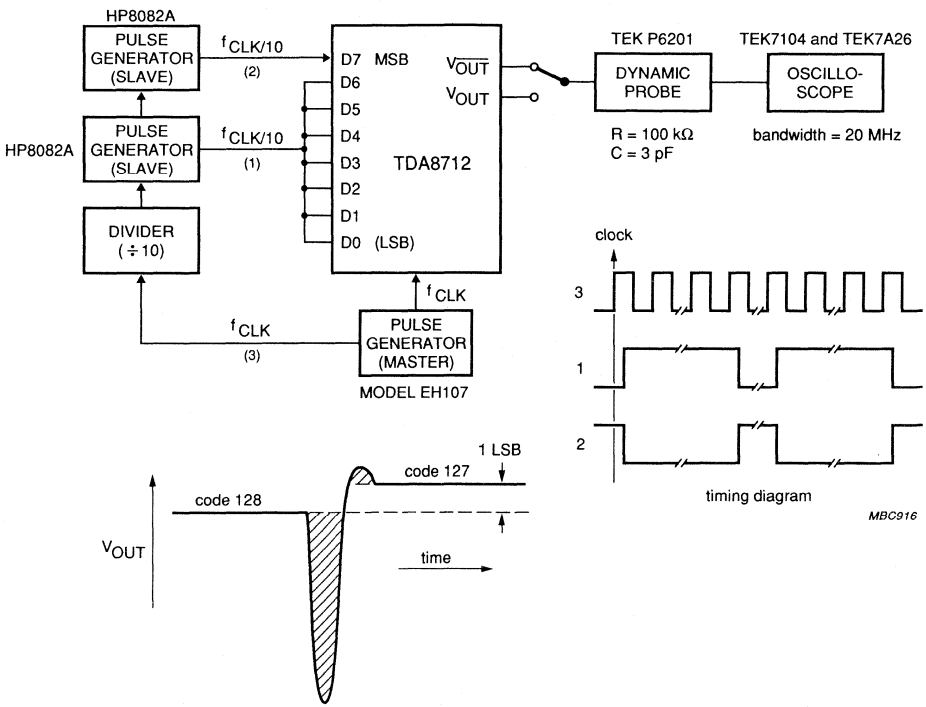


Fig.5 Latched and transparent mode.

Note to Figure 5

During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable regardless of any change at the input. A change of input data during the latched mode will be seen on the falling edge of the clock (beginning of the transparent mode).



The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

Fig.6 Glitch energy measurement.

INTERNAL PIN CONFIGURATIONS

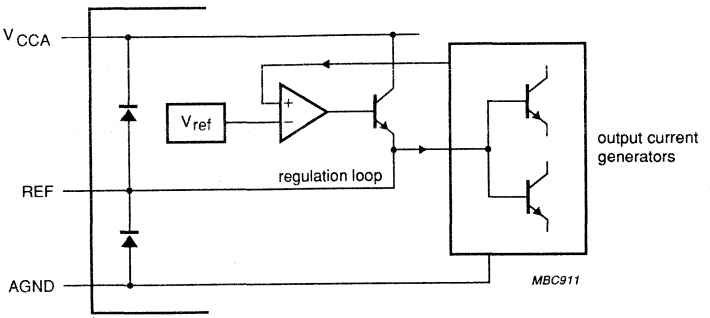


Fig.7 Reference voltage generator decoupling.

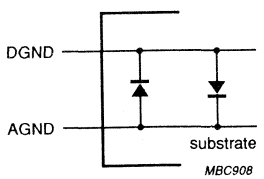


Fig.8 AGND and DGND.

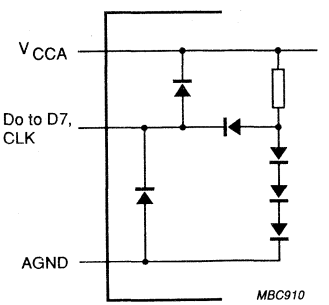


Fig.9 D7 to D0 and CLK.

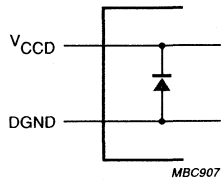


Fig.10 Digital supply.

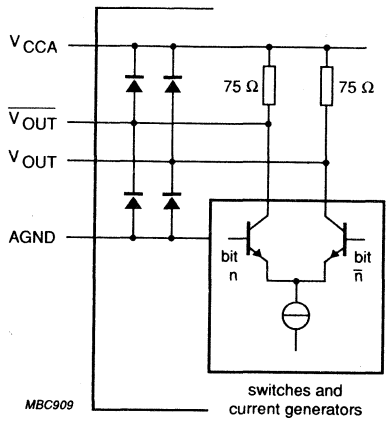


Fig.11 Analog outputs.

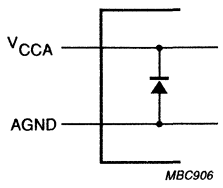


Fig.12 Analog supply.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

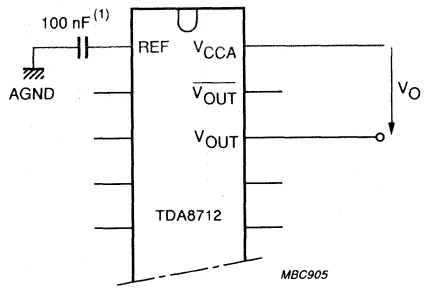


Fig.13 Analog output voltage without external load ($V_O = -V_{\overline{OUT}}$; see Table 1, Z_L = 10 kΩ).

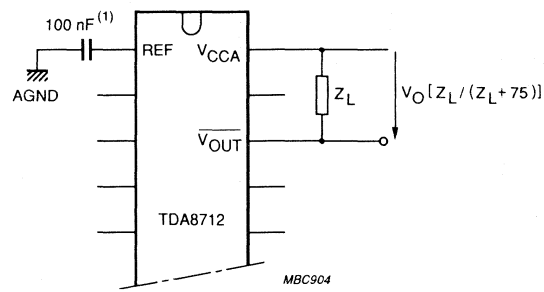


Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).

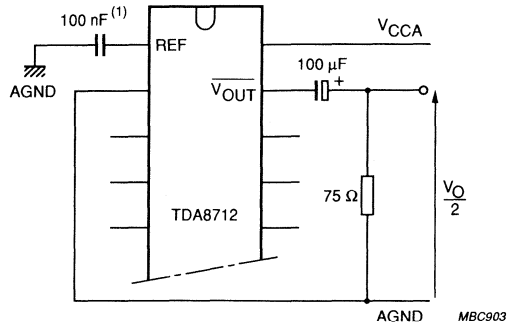


Fig.15 Analog output with AGND as reference.

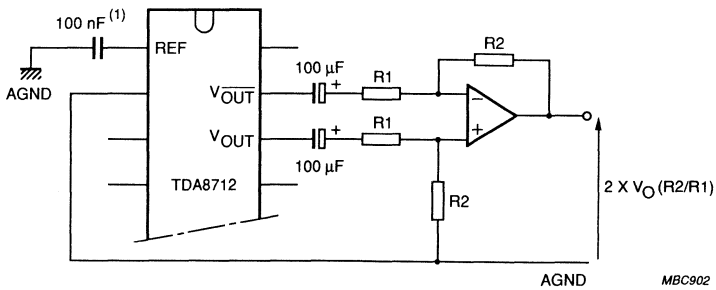


Fig.16 Differential mode (improved supply voltage ripple rejection).

Note to Figs 13, 14, 15 and 16

1. This is a recommended value for decoupling pin 1.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	November 1990

TDA8713

8-bit high-speed analog-to-digital converter

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 40 MHz clock frequency
- Binary or two's complement 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- External reference voltage generator
- Power dissipation only 290 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - video data digitizing
  - radar pulse analysis
  - transient signal analysis
  - high energy physics research
  - $\Sigma\Delta$ modulators
  - medical imaging

DESCRIPTION

The TDA8713 is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8713	24	DIL	plastic	SOT101
TDA8713T	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		-	18	26	mA
I_{CCD}	digital supply current		-	19	25	mA
I_{CCO}	output stages supply current		-	11	14	V
ILE	DC integral linearity error		-	-	±0.75	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
AILE	AC integral linearity error	note 1	-	-	±2	LSB
B	−3 dB bandwidth	note 2; f_{CLK} = 40 MHz	-	19.5	-	MHz
$f_{CLK}/f_{\overline{CLK}}$	maximum clock frequency	note 3	50	-	-	MHz
P_{tot}	total power dissipation		-	290	415	mW

Notes to the Quick Reference Data

1. Full-scale sinewave (f_i = 4.4 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 27 MHz).

2. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at input).

3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:

   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak- to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

     If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

8-bit high-speed analog-to-digital converter TDA8713

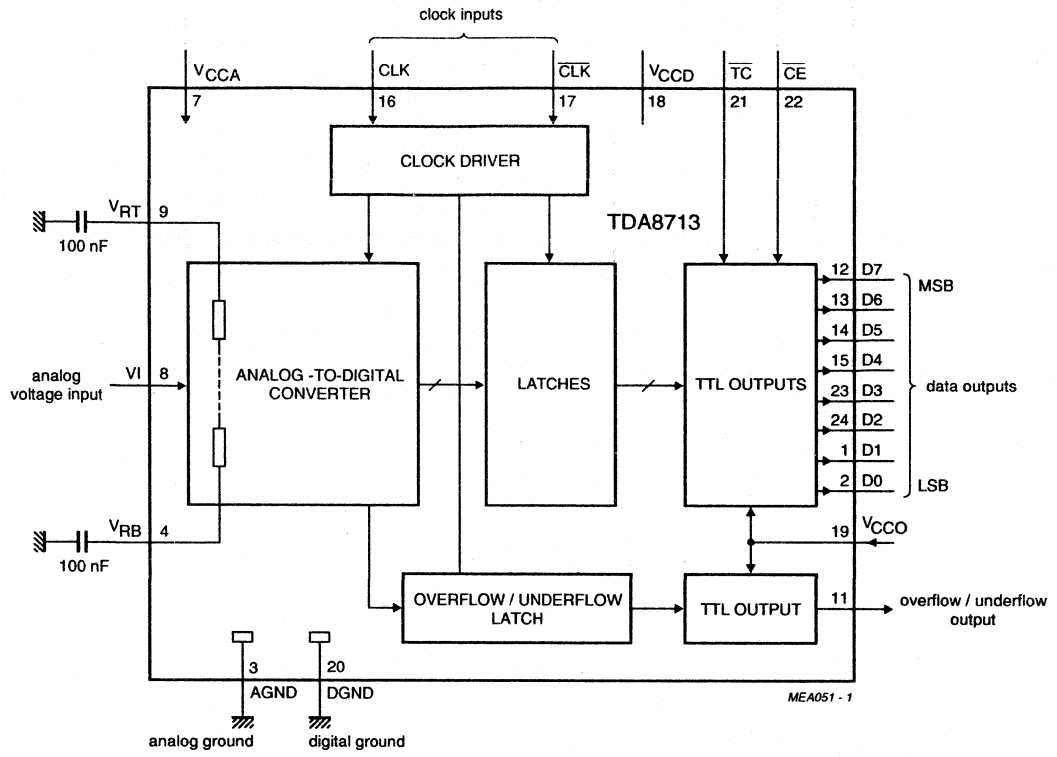


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter TDA8713

PIN CONFIGURATION

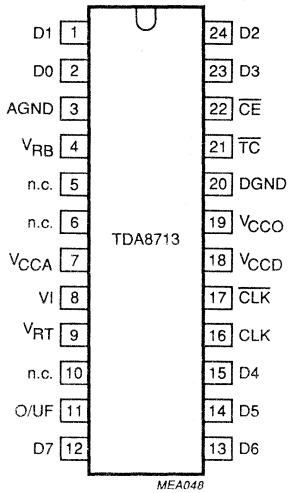


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
AGND	3	analog ground
V_{RB}	4	reference voltage bottom (decoupling)
n.c.	5	not connected
n.c.	6	not connected
V_{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output, bit 7 (MSB)
D6	13	data output, bit 6
D5	14	data output, bit 5
D4	15	data output, bit 4
CLK	16	clock input
$\overline{CLK}$	17	complementary clock input
V_{CCD}	18	positive supply voltage for digital circuits (+5 V)
V_{CCO}	19	positive supply voltage for output stages (+5 V)
DGND	20	digital ground
$\overline{TC}$	21	input for two's complement output (TTL level input, active LOW)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output, bit 3
D2	24	data output, bit 2

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	see note 1	−0.3	7.0	V
V_{CCD}	digital supply voltage range	see note 1	−0.3	7.0	V
V_{CCO}	output stages supply voltage	see note 1	−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		−1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	1.2	7.0	V
V_{CLK}/ $\overline{V_{CLK}}$	AC input voltage for switching (peak-to-peak value)	see note 2; referenced to DGND	-	2.0	V
I_O	output current		-	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		0	+70	°C
T_j	junction temperature		-	+125	°C

Notes to the Ratings

1. The supply voltages V_{CCA} and V_{CCD} may have any value between −0.3 V and +7.0 V as long as the difference V_{CCA} - V_{CCD} lies between −1 V and + 1 V.

2. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:

- TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
- TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
- AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT101	+ 55	K/W
$R_{th\ j\text{-}a}$	SOT137A	+ 75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_3 = 4.75$ V to 5.25 V; $V_{CCD} = V_{18} - V_{20} = 4.75$ V to 5.25 V; $V_{CCO} = V_{19} - V_{20} = 4.75$ V to 5.25 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $T_{amb} = 0$ °C to +70 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		-	18	26	mA
I_{CCD}	digital supply current		-	19	25	mA
I_{CCO}	output stage supply current	all outputs LOW	-	11	14	mA
Inputs CLOCK INPUT CLK AND $\overline{CLK}$ (note 1; referenced to DGND)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V	−400	-	-	µA
I_{IH}	input current HIGH	$V_{CLK}/V_{\overline{CLK}} = 2.7$ V	-	-	100	µA
		$V_{CLK}/V_{\overline{CLK}} = V_{CCD}$	-	-	300	µA
Z_o	input impedance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	-	4	-	kΩ
C_i	input capacitance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	-	4.5	-	pF
$V_{CLK(p-p)} - V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)	note 1; DC level = 1.5 V	0.5	-	2.0	V
INPUTS $\overline{TC}$ AND $\overline{CE}$ (referenced to DGND)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_{IL} = 0.4$ V	−400	-	-	µA
I_{IH}	input current HIGH	$V_{IH} = 2.7$ V	-	-	20	µA
VI (analog input voltage referenced to AGND)						
I_{IL}	input current LOW	$V_{VI} = 1.6$ V	-	0	-	µA
I_{IH}	input current HIGH	$V_{VI} = 3.8$ V	60	120	180	µA
Z_o	input impedance	$f_i = 1$ MHz	-	10	-	kΩ
C_i	input capacitance	$f_i = 1$ MHz	-	14	-	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltages for the resistor ladder						
V_{RB}	reference voltage LOW		1.5	1.6	1.9	V
V_{RT}	reference voltage HIGH		3.5	3.8	3.9	V
V_{REF}	differential reference voltage V_{RT}-V_{RB}		2	2.2	-	V
I_{REF}	reference current		-	10	-	mA
R_{LAD}	resistor ladder		-	200	-	Ω
R_{TLC}	temperature coefficient of the ladder		-	0.24	-	Ω/°C
V_{OB}	voltage offset bottom	note 5	-	258	-	mV
V_{OBTC}	voltage offset bottom temperature coefficient	note 5	-	0.1	-	mV/°C
V_{OT}	voltage offset top	note 5	-	132	-	mV
V_{OTTC}	voltage offset top temperature coefficient	note 5	-	−0.3	-	mV/°C
Outputs DIGITAL OUTPUTS (D7 - D0) (referenced to DGND)						
V_{OL}	output voltage LOW	I_O = 1 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_O = −0.4 mA	2.7	-	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	-	20	µA
Switching characteristics (note 1,2; see Fig.3)						
$f_{CLK}/f_{\overline{CLK}}$	maximum clock frequency		50	-	-	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	−3 dB bandwidth	note 3	-	19.5	-	MHz
G_d	differential gain	note 4	-	0.3	2.0	%
ϕ_d	differential phase	note 4	-	0.4	1.5	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	0	0	0	dB
F_{even}	even harmonics (full-scale)	f_i = 4.43 MHz	-	−65	-	dB
F_{odd}	odd harmonics (full scale)	f_i = 4.43 MHz	-	−55	-	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		-	-	± 0.75	LSB
DLE	DC differential linearity error		-	-	± 1/2	LSB
AILE	AC integral linearity error	note 6	-	-	± 2	LSB
EB	effective bits f_i = 1 MHz	f_{CLK} = 20MHZ	-	7.8	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 40MHZ	-	7.5	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 50MHZ	-	7.2	-	bits
Timing (note 7; see Figs 3 to 6; f_{CLK} = 50 MHz)						
t_{dS}	sampling delay		-	-	2	ns
t_{HD}	output hold time		6	-	-	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	-	8	10	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	-	14	16	ns
t_{dZH}	3-state output delay times	enable-to-HIGH	-	19	25	ns
t_{dZL}	3-state output delay times	enable-to-LOW	-	16	20	ns
t_{dHZ}	3-state output delay times	disable-to-HIGH	-	14	20	ns
t_{dLZ}	3-state output delay times	disable-to-LOW	-	9	12	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

   If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.
2. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 2 ns.
3. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
4. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
5. Analog input voltages producing code 00 up to and including FF
   - V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C.
   - V_{OBTC} (voltage offset bottom temperature coefficient) is the dependence of V_{OB} with temperature.
   - V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
   - V_{OTTC} (voltage offset top temperature coefficient) is the dependence of V_{OT} with temperature.
6. Full-scale sinewave (f_i = 4.4 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 27 MHz).
7. Output data acquisition
   - Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
   - Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; referenced to AGND, V_{RB} = 1.6 V, V_{RT} = 3.8 V)

			BINARY OUTPUT BITS								TWO'S COMPLEMENT OUTPUT BITS							
STEP	$V_{VI(P-P)}$	O/UF	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow	<1.858	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1.858	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.668	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow	>3.668	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{TC}$	$\overline{CE}$	D7 - D0	O/UF
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

Where: X = don't care.

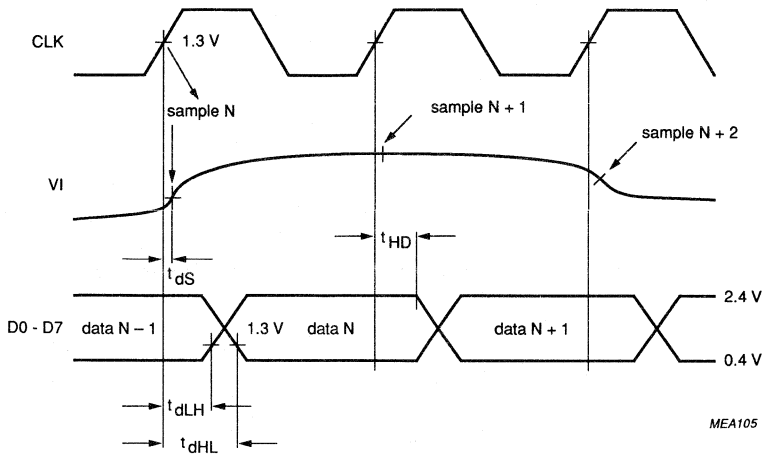


Fig.3 Timing diagram.

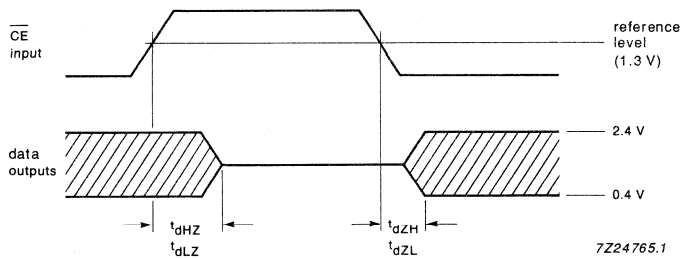


Fig.4 3-state delay timing diagram.

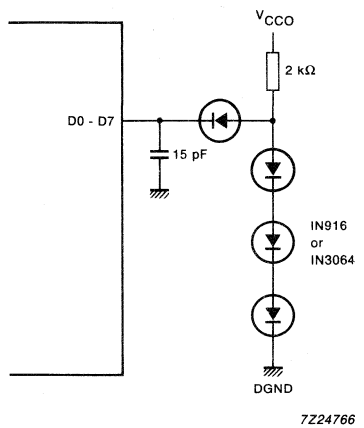


Fig.5 Load circuit for timing measurement; data outputs ($\overline{CE}$ = LOW).

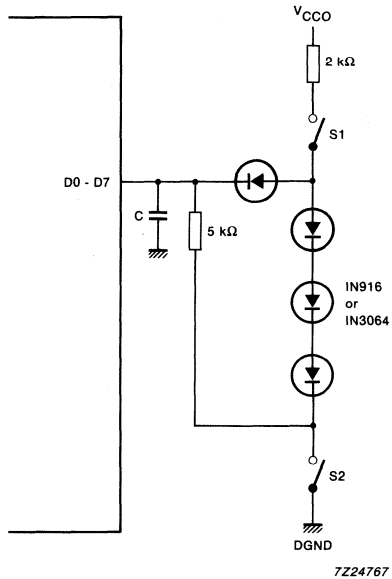


Fig.6 Load circuit for timing measurement; 3-state outputs ($\overline{CE}$: f_i = 1 MHz; V_{VI} = 3 V).

Note to Fig.6

TIMING MEASUREMENT	SWITCH S1	SWITCH S2	CAPACITOR C
t_{dZH}	open	closed	15 pF
t_{dZL}	closed	open	15 pF
t_{dHZ}	closed	closed	5 pF
t_{dLZ}	closed	closed	5 pF

INTERNAL PIN CONFIGURATIONS

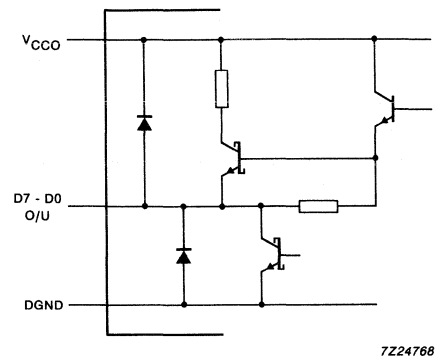


Fig.7 TTL data and overflow/underflow outputs.

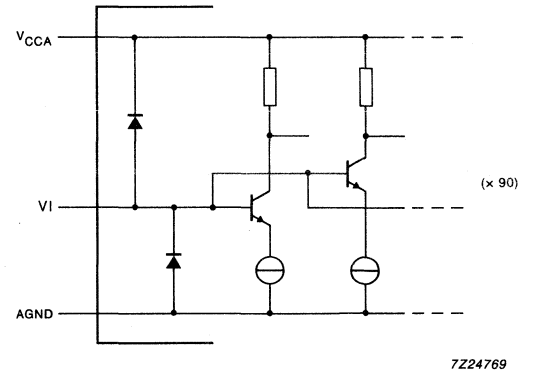


Fig.8 Analog inputs.

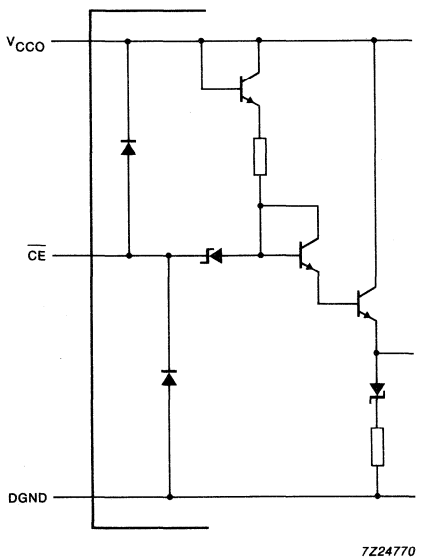


Fig.9 $\overline{CE}$ (3-state) input.

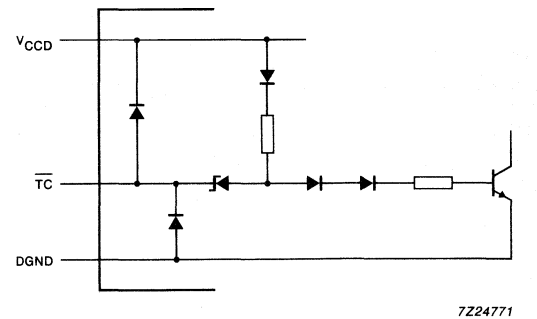


Fig.10 $\overline{TC}$ (two's complement) input.

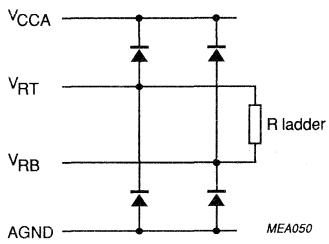


Fig.11 V_{RB}, V_{RT}.

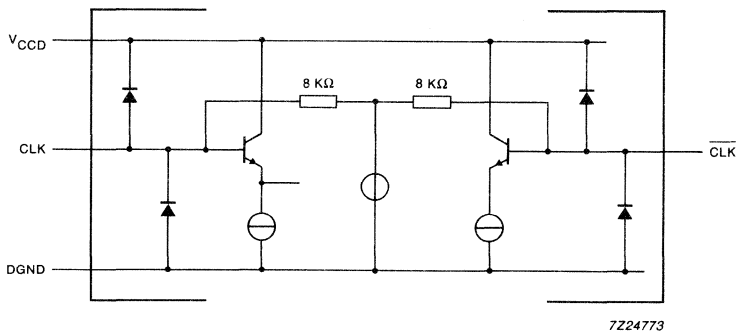


Fig.12 CLK and $\overline{CLK}$ inputs.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/9001).

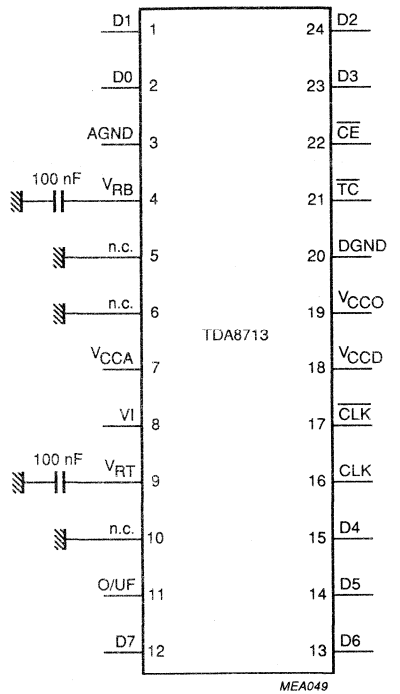


Fig.13 Application diagram.

Notes to Fig.13

1. $\overline{CLK}$ should be decoupled to the DGND with a 100 nF capacitor, if pin CLK is used (see 'Notes to the characteristics', note 1).

2. CLK and $\overline{CLK}$ can be used in a differential mode (see 'Notes to the characteristics', note 1).

3. V_{RB} and V_{RT} are decoupled to AGND.

4. Analog and digital supplies should be separated and decoupled.

5. Pins 5,6 and 10 should be connected to AGND in order to prevent noise influence.

6. The external voltage regulator must be build in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.

8-bit high-speed analog-to-digital converter

TDA8715

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 40 MHz clock frequency)
- ECL (10KH family) compatible digital inputs and outputs
- Overflow/underflow ECL output
- Low-level AC clock input signal allowed
- Power dissipation only 325 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - -video data digitizing
  - -radar pulse analysis
  - -transient signal analysis
  - -high energy physics research
  - -ΣΔ modulators
  - -medical imaging

GENERAL DESCRIPTION

The TDA8715 is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for profesional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are 10KH ECL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		–4.7	–5.2	–5.7	V
V_{EED}	digital supply voltage		–4.7	–5.2	–5.7	V
I_{EEA}	analog supply current		–	20	25	mA
I_{EED}	digital supply current	see note	–	52	60	mA
ILE	DC integral linearity error		–	±0.4	±0.75	LSB
DLE	DC differential linearity error		–	±0.25	±0.5	LSB
EB	effective bits	f_i = 4.43 MHz; f_{CLK} = 50 MHz	–	7.2	–	bits
f_{CLK}; $\overline{f_{CLK}}$	maximum clock frequency		50	–	–	MHz
T_{amb}	operating ambient temperature range		0	–	+125	°C
P_{tot}	total power dissipation	see note	–	325	425	mW

Note to the Quick Reference Data

All digital outputs are connected to V_{EED} via 2.2 kΩ resistors.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8715	18	DIL	plastic	SOT102
TDA8715T	20	SO20	plastic	SOT163A

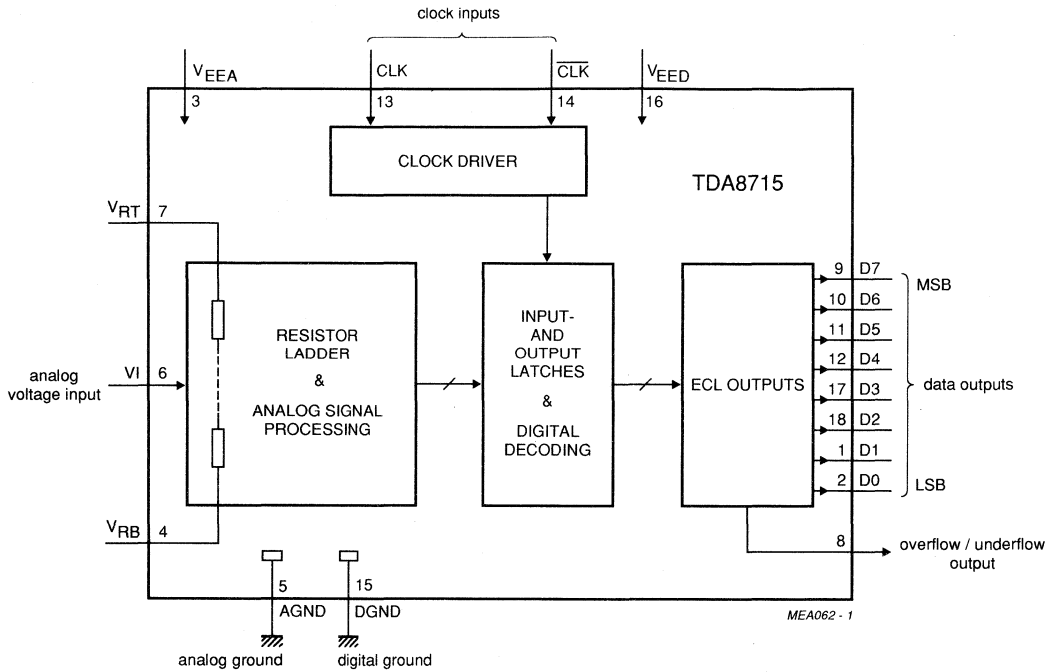


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter

TDA8715

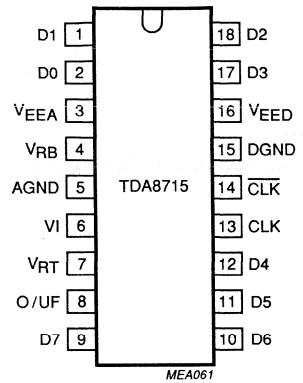


Fig.2 Pin configuration (TDA8715).

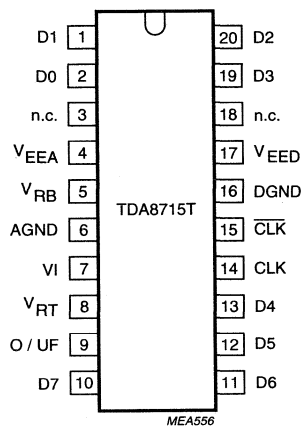


Fig.3 Pin configuration (TDA8715T).

PINNING

SYMBOL	DIL	SO	DESCRIPTION
D1	1	1	data output, bit 1
D0	2	2	data output, bit 0 (LSB)
n.c.	–	3	not connected
V_{EEA}	3	4	analog negative supply voltage (–5.2 V)
V_{RB}	4	5	reference voltage bottom input
AGND	5	6	analog ground
V_I	6	7	analog voltage input
V_{RT}	7	8	reference voltage top input
O/UF	8	9	overflow/underflow data output
D7	9	10	data output, bit 7(MSB)
D6	10	11	data output, bit 6
D5	11	12	data output, bit 5
D4	12	13	data output, bit 4
CLK	13	14	clock input
$\overline{CLK}$	14	15	complementary clock input
DGND	15	16	digital ground
V_{EED}	16	17	digital negative supply voltage (–5.2 V)
n.c.	–	18	not connected
D3	17	19	data output, bit 3
D2	18	20	data output, bit 2

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage range		−7	0.3	V
V_{EED}	digital supply voltage range		−7	0.3	V
V_I	input voltage range		−7	0.3	V
V_{CLK}; $V_{\overline{CLK}(p\text{-}p)}$	AC input voltage for switching (peak-to-peak value)	see note	−	2.0	V
I_O	output current		−15	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		0	70	°C
T_j	junction temperature		−	+140	°C

Note to the Limiting Values

The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals or with two complementary sinewave signals, imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- Asymmetrical drive modes; When driving the CLK input directly with an ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- When driving the CLK input with an ECL signal only (Asymmetrical drive modes), it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT102)	65 K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT163A)	80 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{EEA} = V_3 - V_5 = -4.7$ V to -5.7 V; $V_{EED} = V_{16} - V_{15} = -4.7$ V to -5.7 V; AGND and DGND shorted together; $T_{amb} = 0$ °C to 70 °C; unless otherwise specified (typical values measured at $V_{EEA} = -5.2$V; $V_{EED} = -5.2$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage		−4.7	−5.2	−5.7	V
V_{EED}	digital supply voltage		−4.7	−5.2	−5.7	V
I_{EEA}	analog supply current		–	20	25	mA
I_{EED}	digital supply current	note 1	–	52	60	mA
V_{EEA}–V_{EED}	supply voltage difference		−0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	LOW level reference voltage		−3.2	−3.0	−2.7	V
V_{RT}	HIGH level reference voltage		−0.9	−0.6	−0.4	V
V_{ref}	differential reference voltage V_{RT}–V_{RB}		2.3	2.4	–	V
I_{ref}	reference current		–	12.6	–	mA
R_{LAD}	resistor ladder		–	200	–	Ω
TC_{RL}	temperature coefficient of the ladder		–	0.24	–	Ω/K
V_{OB}	voltage offset bottom	note 2	–	317	–	mV
TC_{VOB}	temperature coefficient voltage offset bottom	note 2	–	0.1	–	mV/K
V_{OT}	voltage offset top	note 2	–	174	–	mV
TC_{VOT}	temperature coefficient voltage offset top	note 2	–	−0.3	–	mV/K
Inputs						
CLK INPUT (NOTE 3)						
V_{IL}	LOW level input voltage		−1.85	−1.77	−1.65	V
V_{IH}	HIGH level input voltage		−0.96	−0.88	−0.81	V
I_{IL}	LOW level input current	$V_{CLK} = -1.77$ V	–	−240	–	µA
I_{IH}	HIGH level input current	$V_{CLK} = -0.88$ V	–	−14	–	µA
R_I	input resistance	$f_{CLK} = 10$ MHz	–	7	–	kΩ
		$f_{CLK} = 50$ MHz	–	3.5	–	kΩ
C_I	input capacitance	$f_{CLK} = 10$ MHz	–	1.8	–	pF
		$f_{CLK} = 50$ MHz	–	1.55	–	pF
$\overline{CLK}$ INPUT CLK (NOTE 3)						
V_{IL}	LOW level input voltage		−1.85	−1.77	−1.65	V
V_{IH}	HIGH level input voltage		−0.96	−0.88	−0.81	V
I_{IL}	LOW level input current	$V_{\overline{CLK}} = -1.77$ V	–	−140	–	µA
I_{IH}	HIGH level input current	$V_{\overline{CLK}} = -0.88$ V	–	75	–	µA
R_I	input resistance	$f_{\overline{CLK}} = 10$ MHz	–	9.3	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
		$f_{\overline{CLK}}$ = 50 MHz	–	4.5	–	kΩ
C_I	input capacitance	$f_{\overline{CLK}}$ = 10 MHz	–	2.6	–	pF
		$f_{\overline{CLK}}$ = 50 MHz	–	2.4	–	pF
$V_{CLK(p-p)} - V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)		0.5	0.9	1.1	V
V_I (ANALOG INPUT; V_{RB} = –3.1 V AND V_{RT} = –0.6 V)						
I_{IL}	LOW level input current	data output 00	–	0	–	μA
I_{IH}	HIGH level input current	data output FF	–	120	–	μA
R_I	input resistance	f_i = 1 MHz	–	9.4	–	kΩ
C_I	input capacitance	f_i = 1 MHz	–	13.7	20	pF
Outputs						
DIGITAL OUTPUTS (D7 - D0 AND 0/UF) (DIGITAL 10KH ECL OUTPUTS)						
V_{OL}	LOW level output voltage	T_{amb} = 25 °C	–1.95	–1.77	–1.65	V
V_{OH}	HIGH level output voltage	T_{amb} = 25 °C	–0.96	–0.88	–0.81	V
I_{OL}	LOW level output current		–	1.8	4	mA
I_{OH}	HIGH level output current		–	1.8	4	mA
Switching characteristics						
f_{CLK}; $f_{\overline{CLK}}$	maximum clock frequency		50	–	–	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	–3 dB bandwidth	note 4	–	20.5	–	MHz
G_{diff}	differential gain	note 5	–	0.3	2.0	%
ϕ_{diff}	differential phase	note 5	–	0.4	1.5	deg
	harmonics (full-scale)	f_i = 4.43 MHz				
	fundamental		0	0	0	dB
	even		–	–60	–	dB
	odd		–	–50	–	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		–	–	±0.75	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
AILE	AC integral linearity error	note 6	–	±0.75	–	LSB
EB	effective bits					
	f_i = 600 kHz	f_{CLK} = 20 MHZ	–	7.8	–	bits
	f_i = 4.43 MHz	f_{CLK} = 50 MHZ	–	7.2	–	bits
	f_i = 7 MHz	f_{CLK} = 50 MHZ	–	6.9	–	bits
Timing (note 7; see Fig. 3)						
t_{dS}	sampling delay		–	1	3	ns
t_{HD}	output hold time		3	4	–	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	4	5	8	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	6	7	10	ns

Notes to the characteristics

1. All digital outputs connected to V_{EED} via 2.2 kΩ resistors.
2. Analog input voltages producing code 00 up to and including FF

   V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C.

   TC_{VOB} (voltage offset bottom temperature coefficient) is dependent on V_{OB} with temperature.

   V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.

   TC_{VOT} (voltage offset top temperature coefficient) is dependent on V_{OT} with temperature.
3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

   Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals or with two complementary sinewave signals, imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.

   Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.

   When driving the CLK input with a ECL signal only (Asymmetrical drive modes), it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.
4. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
5. Low frequency ramp signal ($V_{I(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{I(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
6. Full-scale sinewave (f_i = 4.43 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 50 MHz).
7. Output data acquisition

   Output data is available after the maximum delay of t_{dHL} and t_{dLH}.

   Output data is fully stable during the LOW level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH})

Table 1 Output coding

STEP	V_I (TYP. value)	BINARY OUTPUTS D7 to D0	$\overline{O}$/UFL
Underflow	< –2.789 V	00000000	1
0	–2.783 V	00000000	0
1	–2.775 V	00000001	0
.	.	.....	.
.	.	.....	.
.	.	.....	.
254	.	11111110	0
255	–0.774 V	11111111	0
Overflow	> –0.770 V	11111111	1

Note to Table 1

Typical values: V_{RB} = –3 V, V_{RT} = –0.6 V and V_I referenced to AGND

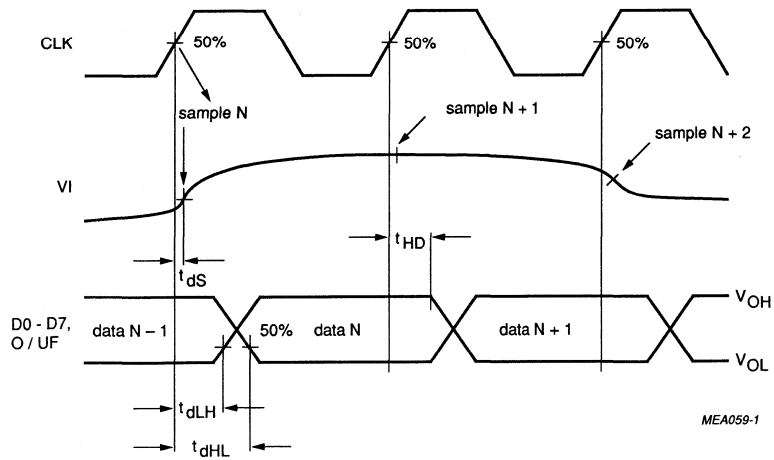


Fig.4 Timing diagram.

INTERNAL PIN CONFIGURATIONS

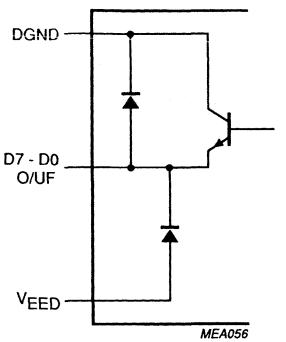


Fig.5 ECL data outputs.

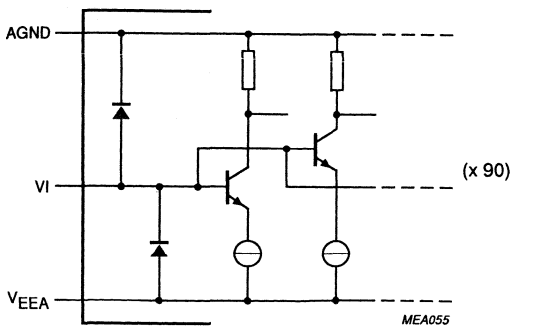


Fig.6 Analog input.

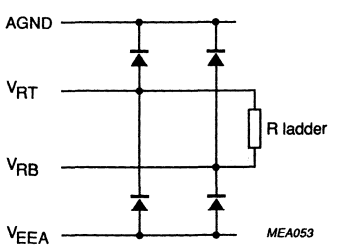


Fig.7 V_{RT} and V_{RB} inputs.

APPLICATION INFORMATION

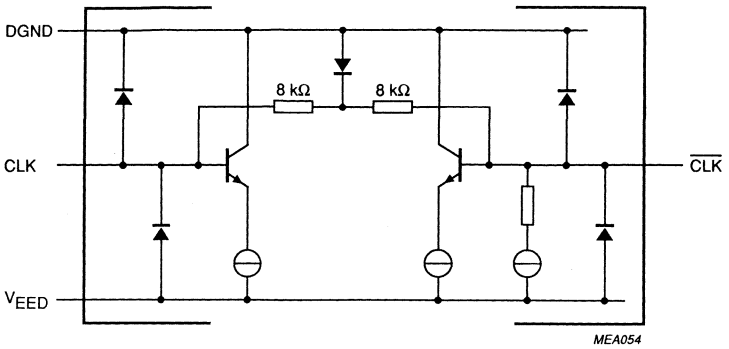


Fig.8 CLK and $\overline{CLK}$ input.

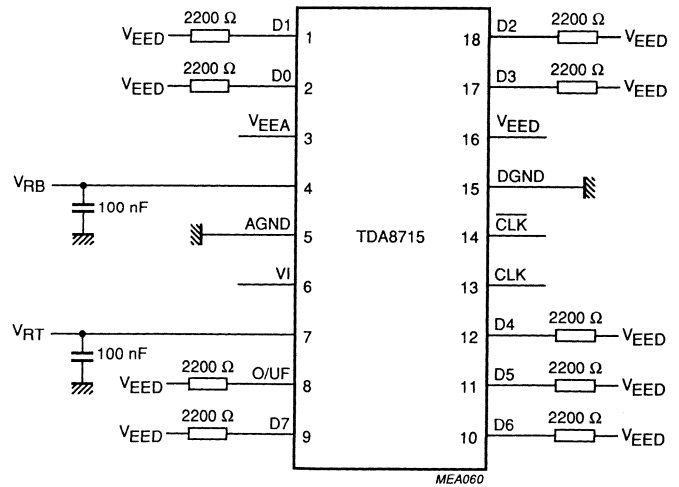


Fig.9 Application diagram.

Notes to Fig.8

1. All resistors have a value of 2.2 kΩ; all capacitors have a value of 100 nF
2. Analog and digital supplies should be separated and decoupled.
3. The external voltage regulator should be configured in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.
4. $V_{EEA} = V_{EED} = -5.2$ V; $V_{RB} = -3.0$ V; $V_{RT} = -0.6$ V.

8-bit high-speed analog-to-digital converter

TDA8716

FEATURES

- 8-bit resolution
- Sampling rate up to 120 MHz
- ECL (10 K family) compatible digital inputs and outputs
- Overflow/Underflow output
- Low power dissipation
- Low input capacitance (13 pF typ.)

APPLICATIONS

- High speed analog-to-digital convertion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research
- Medical systems
- Industrial instrumentation

GENERAL DESCRIPTION

The TDA8716 is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) designed for HDTV and professional applications. The device converts the analog input signal into 8-bit binary coded digital words at a sampling rate of 120 MHz. All digital outputs are ECL compatible.

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		–5.45	–5.2	–4.95	V
V_{EED}	digital supply voltage		–5.45	–5.2	–4.95	V
I_{EEA}	analog supply current		–	50	55	mA
I_{EED}	digital supply current		–	100	110	mA
I_{EEO}	output supply current	R_L = 2.2 kΩ	–	20	25	mA
V_{RB}	reference voltage BOTTOM		–	–3.130	–	V
V_{RT}	reference voltage TOP		–	–1.870	–	V
ILE	integral linearity error	see Fig.8	–	±0.5	±1	LSB
DLE	DC differential linearity error	see Fig.9	–	±0.25	±0.45	LSB
EB	effective bit	f_i = 20 MHz; f_{CLK} = 100 MHz	–	7	–	bits
f_{CLK}	maximum clock frequency		120	–	–	MHz
P_{tot}	total power dissipation	excluding load	–	780	900	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8716	24	DIL	plastic	SOT101
TDA8716T	32	SO32L	plastic	SOT287

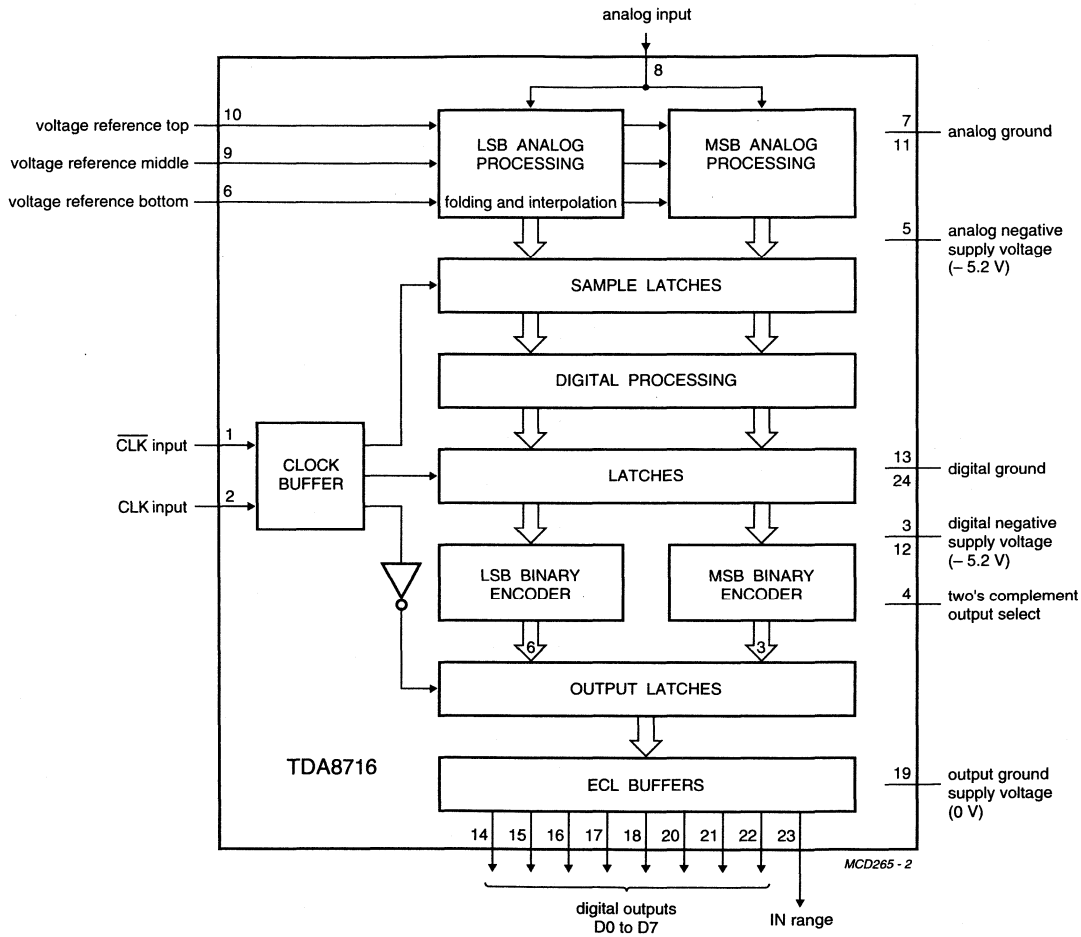


Fig.1 Block diagram (TDA8716).

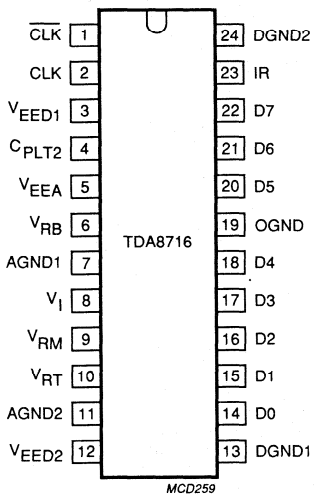


Fig.2 Pin configuration (TDA8716).

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{CLK}$	1	complementary clock input
CLK	2	clock input
V_{EED1}	3	digital negative supply voltage (−5.2 V)
C_{PLT2}	4	two's complement output select (active HIGH)
V_{EEA}	5	analog negative supply voltage (−5.2 V)
V_{RB}	6	reference voltage BOTTOM
AGND1	7	analog ground 1
V_I	8	analog input
V_{RM}	9	reference voltage MIDDLE decoupling
V_{RT}	10	reference voltage TOP
AGND2	11	analog ground 2
V_{EED2}	12	digital negative supply voltage (−5.2 V)
DGND1	13	digital ground 1
D0	14	digital output (LSB)
D1	15	digital output
D2	16	digital output
D3	17	digital output
D4	18	digital output
OGND	19	output ground supply voltage (0 V)
D5	20	digital output
D6	21	digital output
D7	22	digital output (MSB)
IR	23	IN range
DGND2	24	digital ground 2

8-bit high-speed analog-to-digital converter

TDA8716

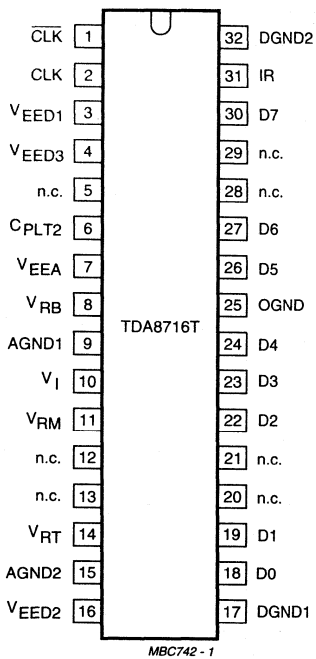


Fig.3 Pin configuration (TDA8716T).

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{CLK}$	1	complementary clock input
CLK	2	clock input
V_{EED1}	3	digital negative supply voltage (–5.2 V)
V_{EED3}	4	digital negative supply voltage (–5.2 V)
n.c.	5	not connected
C_{PLT2}	6	two's complement output select (active HIGH)
V_{EEA}	7	analog negative supply voltage (–5.2 V)
V_{RB}	8	reference voltage BOTTOM
AGND1	9	analog ground 1
V_I	10	analog input
V_{RM}	11	reference voltage MIDDLE decoupling
n.c.	12	not connected
n.c.	13	not connected
V_{RT}	14	reference voltage TOP
AGND2	15	analog ground 2
V_{EED2}	16	digital negative supply voltage (–5.2 V)
DGND1	17	digital ground 1
D0	18	digital output (LSB)
D1	19	digital output
n.c.	20	not connected
n.c.	21	not connected
D2	22	digital output
D3	23	digital output
D4	24	digital output
OGND	25	output ground supply voltage (0 V)
D5	26	digital output
D6	27	digital output
n.c.	28	not connected
n.c.	29	not connected
D7	30	digital output (MSB)
IR	31	IN range
DGND2	32	digital ground 2

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage range		−7.0	+0.3	V
V_{EED1}, V_{EED2}	digital supply voltage range		−7.0	+0.3	V
$V_{EEA}-V_{EED1}$; $V_{EEA}-V_{EED2}$	supply voltage differences		−1	+1	V
V_I	input voltage range	referenced to AGND	V_{EEA}	0	V
$V_{CLK;}$ $\overline{CLK}$(p-p)	input voltage for differential clock drive (peak-to-peak value)	note 1	−	2.0	V
I_O	output current (each output stage)		−	10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		0	+70	°C
T_j	junction temperature		−	140	°C

Note to the limiting values

1. The circuit has two clock inputs: CLK and $\overline{CLK}$. Sampling takes place on the rising edge of the clock input signal: CLK and $\overline{CLK}$ are two's complementary ECL signals.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air (SOT101)	35 K/W
$R_{th\ j-a}$	from junction to ambient in free air (SOT287) (see Fig.4)	65 K/W

CHARACTERISTICS

V_{EEA} = −4.95 V to −5.45 V; V_{EED1}, V_{EED2} = −4.95 V to −5.45 V; AGND, DGND and OGND shorted together; T_{amb} = 0 °C to +70°C; unless otherwise specified. (Typical values taken at V_{EEA} = −5.2 V; V_{EED1}, V_{EED2} = −5.2 V; T_{amb} = 25 °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage		−5.45	−5.2	−4.95	V
V_{EED1},V_{EED2}	digital supply voltage		−5.45	−5.2	−4.95	V
I_{EEA}	analog supply current		–	50	55	mA
I_{EED1},I_{EED2}	digital supply current		–	100	110	mA
I_{EE}	output supply current	R_L = 2.2 kΩ	–	20	25	mA
V_{diff}	supply voltage differential	$V_{EEA} - V_{EED1}$; $V_{EEA} - V_{EED2}$	−0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	reference voltage BOTTOM		−3.5	−3.13	–	V
V_{RT}	reference voltage TOP		–	−1.87	−1.5	V
V_{ref}	reference voltage differential	$V_{RT} - V_{RB}$	–	1.26	–	V
V_{OB}	voltage offset BOTTOM	note 1	–	130	–	mV
V_{OT}	voltage offset TOP	note 1	–	130	–	mV
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		0.95	1.0	1.5	V
I_{ref}	reference current		–	15	–	mA
R_{LAD}	resistor ladder		–	85	–	Ω
TC_{RL}	temperature coefficient of the resistor ladder		–	0.18	–	Ω/K
Inputs						
CLK AND $\overline{CLK}$ INPUT						
V_{IL}	LOW level input voltage		−1850	−1770	−1650	mV
V_{IH}	HIGH level input voltage		−960	−880	−810	mV
I_{IL}	LOW level input current	V_{CLK} = −1.77 V	–	1	–	μA
I_{IH}	HIGH level input current	V_{CLK} = −0.88 V	–	10	–	μA
R_I	input resistance		–	20	–	kΩ
C_I	input capacitance		–	2	–	pF
$V_{CLK(p-p)}$	differential clock input $V_{CLK} - V_{\overline{CLK}}$ (peak-to-peak value)		–	900	–	mV
ANALOG INPUT; V_{RB} = −3.13 V, V_{RT} = −1.87 V; NOTE 2						
I_{IB}	input current BOTTOM	V_I = −3.13 V	–	0	–	μA
I_{IT}	input current TOP	V_I = −1.87 V	–	170	–	μA
R_I	input resistance		–	7	–	kΩ
C_I	input capacitance		–	13	20	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs (R_L = 2.2 kΩ)						
DIGITAL 10 K ECL OUTPUTS (D0 TO D7; IR)						
V_{OL}	LOW level output voltage		−1850	−1770	−1600	mV
V_{OH}	HIGH level output voltage		−960	−880	−810	mV
I_{OL}	LOW level output current		−	1.8	4.0	mA
I_{OH}	HIGH level output current		−	2.0	4.0	mA
Timing (f_{CLK} = 100 MHz; R_L = 2.2 kΩ; see Fig.5)						
t_{ds}	sampling delay		−	1	3	ns
t_{HD}	output hold time		3	4	−	ns
t_d	output delay time		4	6	8	ns
t_{aj}	aperture jitter		−	15	−	ps

DYNAMIC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics						
f_{CLK}; $\overline{f_{CLK}}$	maximum clock frequency		120	−	−	MHz
Analog signal processing (f_{CLK} = 100 MHz)						
G_{diff}	differential gain	note 3	−	0.3	−	%
ϕ_{diff}	differential phase	note 3	−	0.4	−	°C
	harmonics (full scale)	f_i = 10 MHz; f_{CLK} = 100 MHz				
	fundamental		−	0	−	dB
	even harmonics		−	−60	−	dB
	odd harmonics		−	−50	−	dB
Transfer function						
ILE	DC integral linearity error		−	±0.5	±1	LSB
DLE	DC differential linearity error		−	±0.25	±0.45	LSB
AILE	AC integral linearity error	note 3	−	±1	±1.5	LSB
EFF_B	effective bits	Figs 13 and 14; note 4; f_{CLK} = 100 MHz				
	f_i = 4.43 MHz	Fig.10	-	7.7	−	bits
	f_i = 10 MHz	Fig.11	-	7.5	−	bits
	f_i = 20 MHz	Fig.12	-	7.0	−	bits
	f_i = 30 MHz		-	6.5	−	bits
BER	bit error code	f_{CLK} = 100 MHz; f_i = 10 MHz; V_i = ±8 LSB at code 128; 50% clock duty factor	−	10^{-11}	−	times/ samples

Notes to the characteristics

1. Voltage offset BOTTOM (V_{OB}) is the difference between the analog input which produces data outputs equal to 00 and the reference voltage BOTTOM (V_{RB}), at T_{amb} = 25 °C. Voltage offset TOP (V_{OT}) is the difference between reference voltage TOP (V_{RT}) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
2. The analog input is not internally biased. It should be externally biased between V_{RB} and V_{RT} levels.
3. Full-scale sinewave; f_i = 4.43 MHz; f_{CLK}, $f_{\overline{CLK}}$ = 100 MHz.
4. Effective bits are obtained via a Fast Fourier Transformer (FFT) treatment taking 4 K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to SNR: EB = SNR (dB) x 6.02 + 1.76

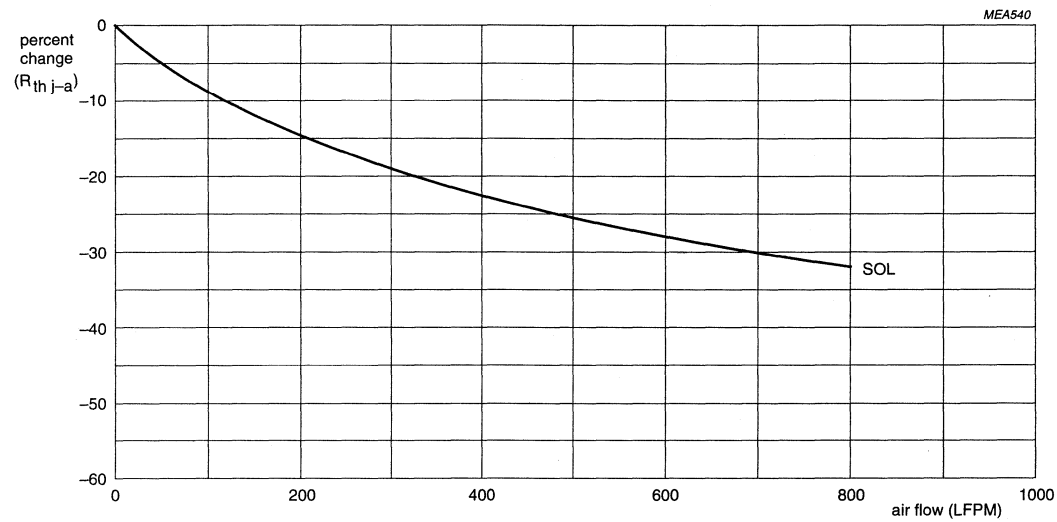


Fig.4 Average effect of air flow on thermal resistance.

Table 1 Output coding (CPLT2 HIGH)

STEP	V_I (TYP.)	BINARY OUTPUTS D7 to D0	IR
Underflow	< –3 V	00000000	0
0	–3 V	00000000	1
1	.	00000001	1
.	.	.....	.
.	.	.....	.
.	.	.....	.
254	.	11111110	1
255	–2 V	11111111	1
Overflow	> –2 V	11111111	0

Table 2 Two's complement coding

C_{PLT2}	D7 (MSB)
1 (V_{IH})	non inverted
0 (V_{IL})	inverted

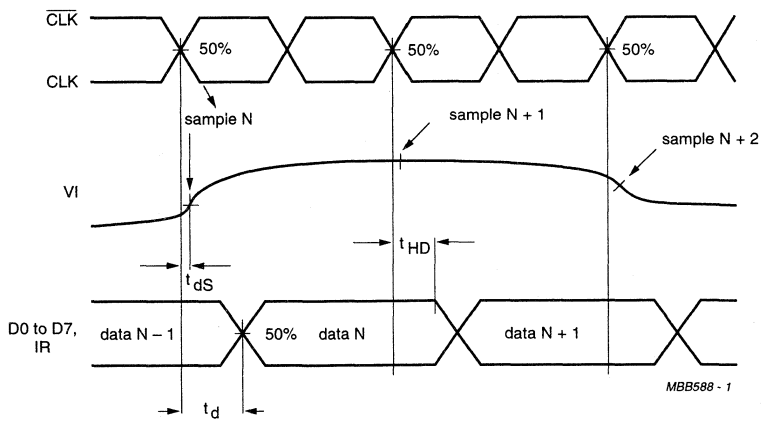


Fig.5 Timing diagram.

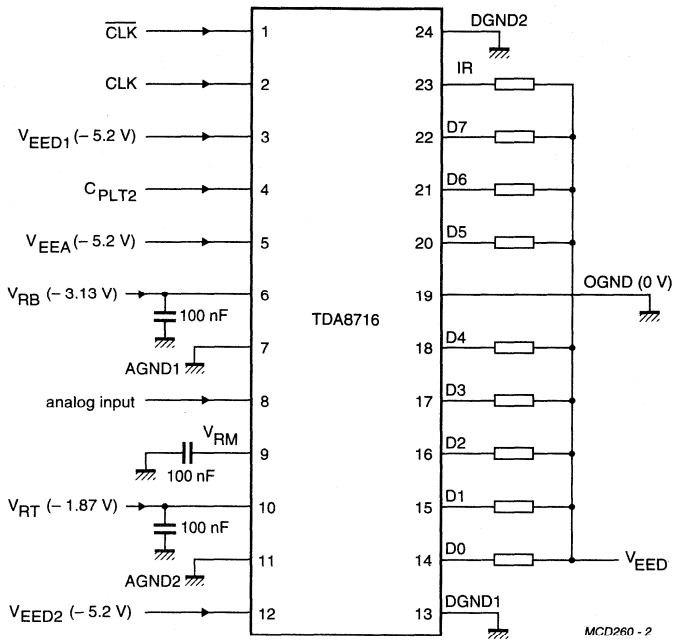
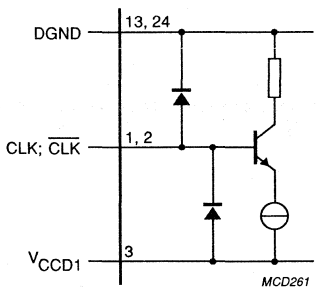


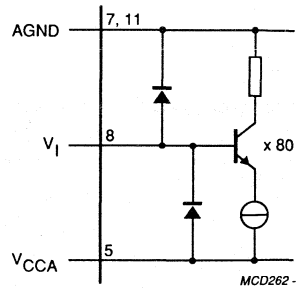
Fig.6 Application diagram (TDA8716).

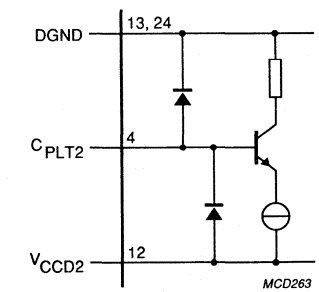
APPLICATION INFORMATION

Additional application information will be supplied upon request, please quote reference number FTV/AN 9109.

1. Typical value for resistors = 2.2 kΩ
2. V_{RB}, V_{RT} and V_M are decoupled to AGND
3. Analog, digital and output supplies should be separated and decoupled
4. The external voltage regulator must be constructed in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.







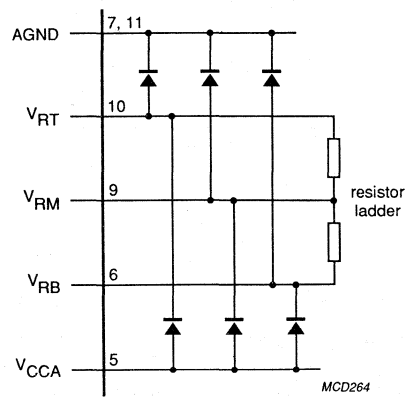


Fig.7 Internal pin configuration diagram.

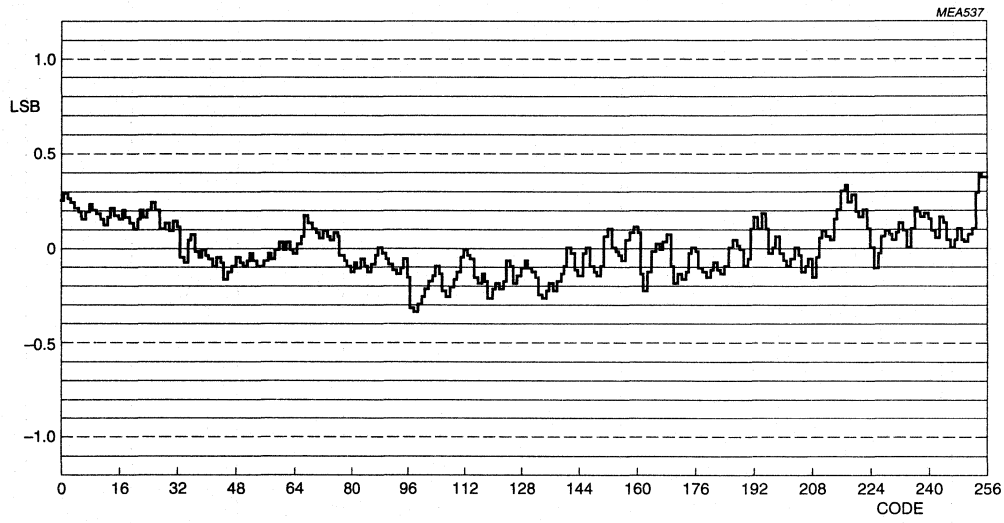


Fig.8 DC Integral linearity error (ILE).

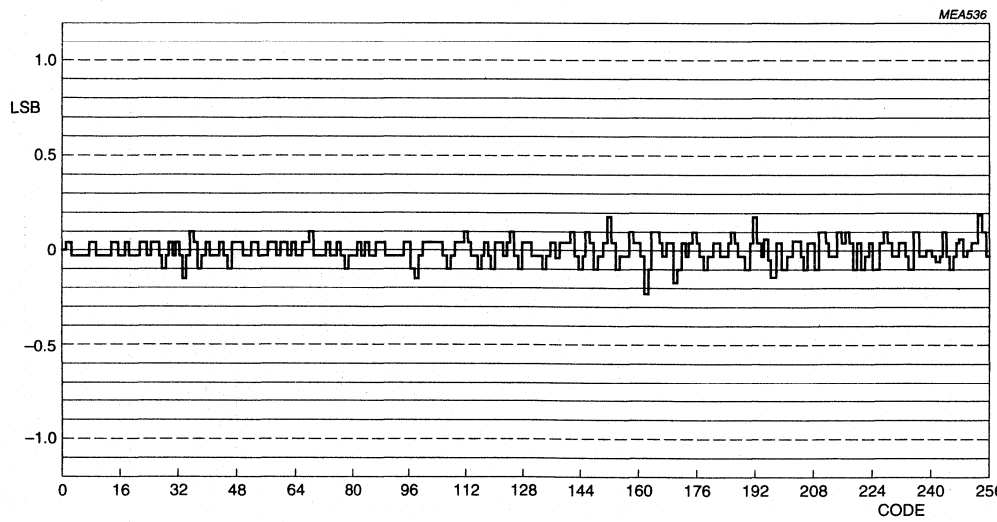
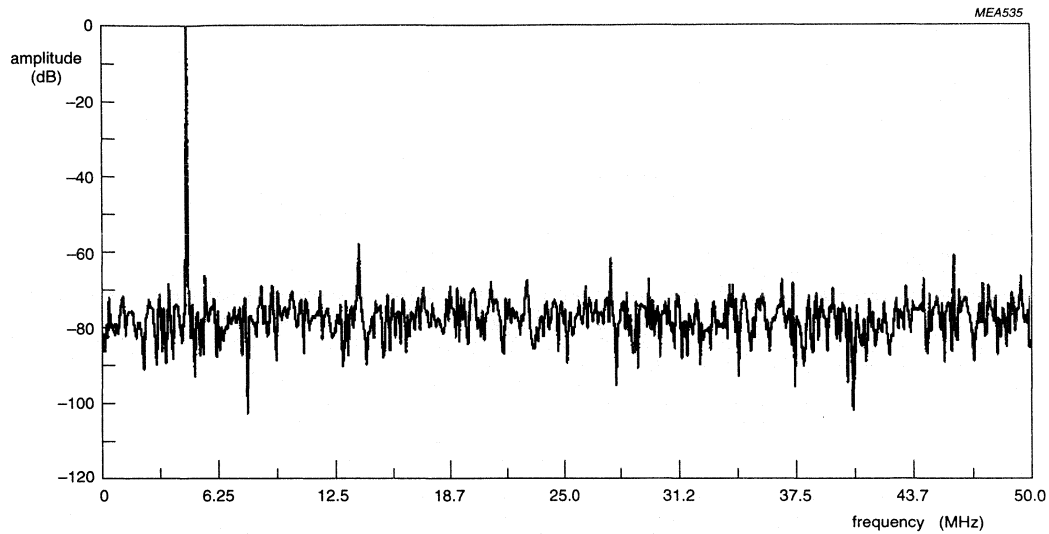
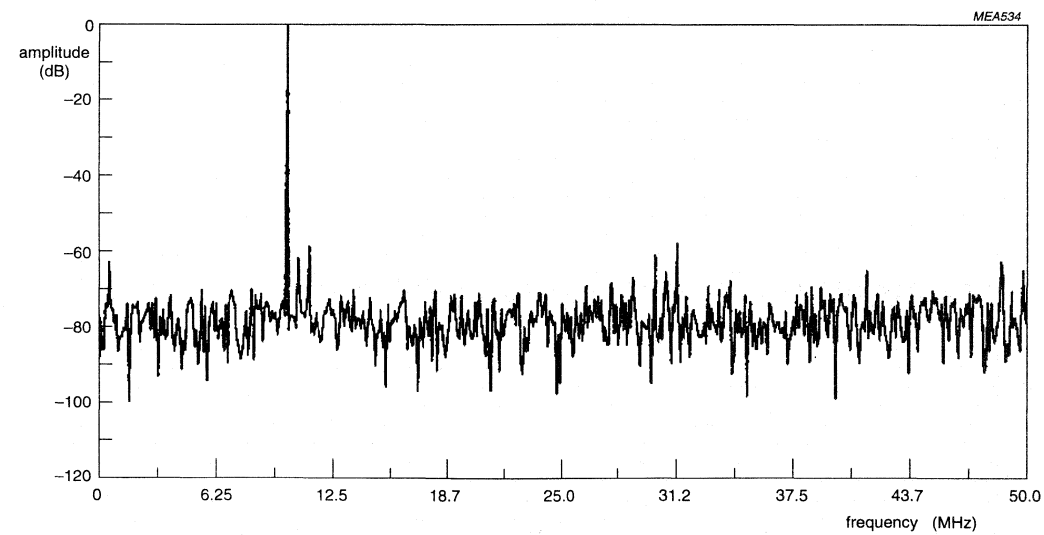


Fig.9 DC differential linearity error (DLE).



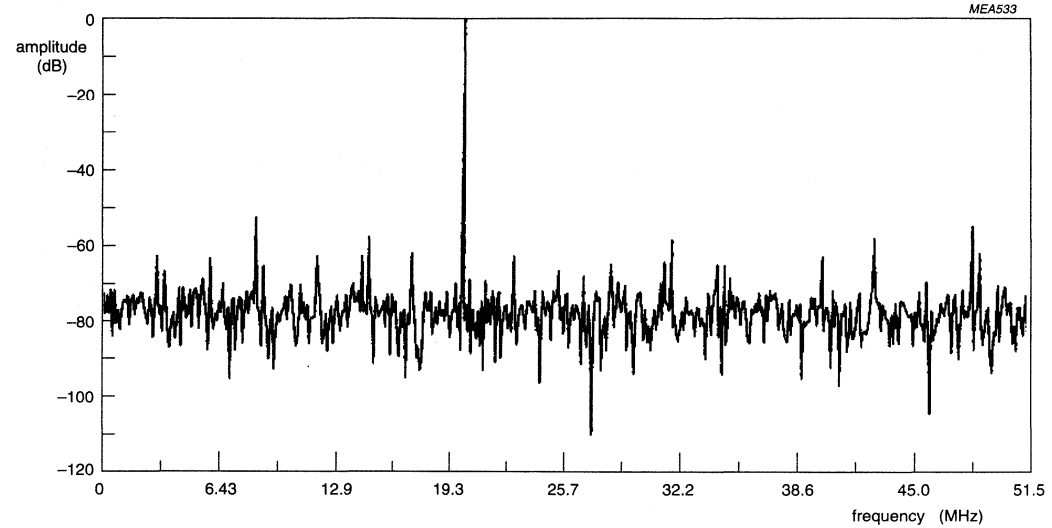
Effective bits: 7.74; Harmonic levels (in dB): 2nd = −69.34; 3rd = −58.85; 4th = −82.55; 5th = −68.16 and 6th = −63.01

Fig.10 Fast fourier transformer (f_{CLK} = 100 MHz; f_i = 4.43 MHz).



Effective bits: 7.57; Harmonic levels (in dB): 2nd = −82.07; 3rd = −61.90; 4th = −75.70; 5th = −65.61 and 6th = −72.50

Fig.11 Fast fourier transformer (f_{CLK} = 100 MHz; f_i = 10 MHz).



Effective bits: 7.04; Harmonic levels (in dB): 2nd = −61.36; 3rd = −56.66; 4th = −61.97; 5th = −62.79 and 6th = −61.52

Fig.12 Fast fourier transformer (f_{CLK} = 100 MHz; f_i = 20 MHz).

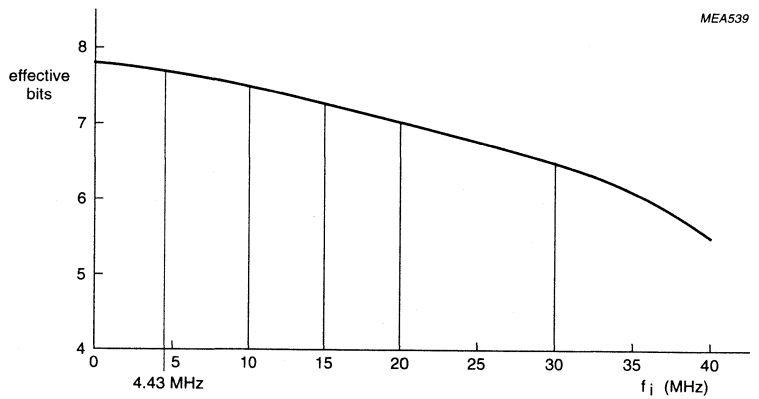


Fig.13 Typical effective bit as a function of input signal at f_{CLK} = 100 MHz.

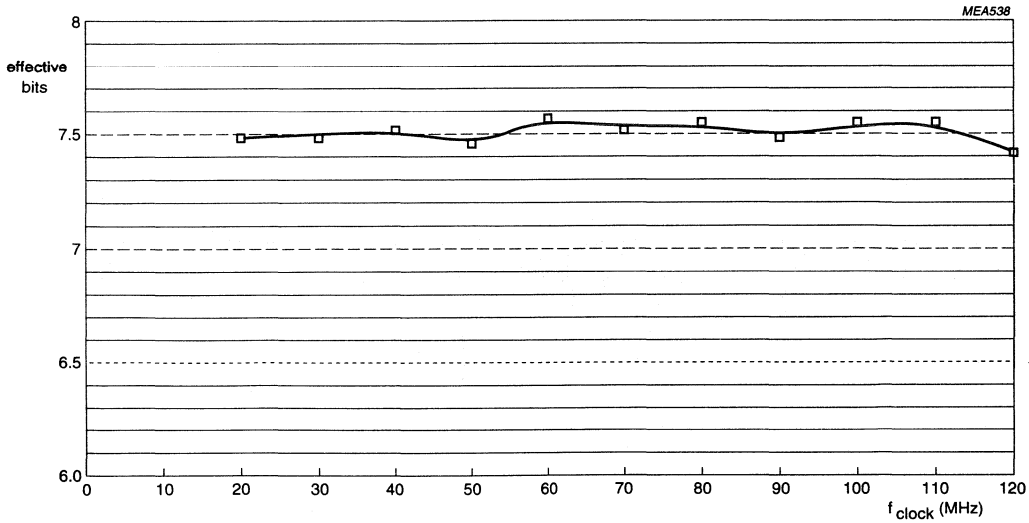


Fig.14 Typical effective bits as a function of clock frequency at f_{IN} = 10 MHz.

8-bit high-speed analog-to-digital converter

TDA8718

FEATURES

- 8-bit resolution
- Sampling rate up to 600 MHz
- ECL (10 k family) compatible for digital inputs and outputs
- Overflow/Underflow output
- 50 Ω load drive capability
- 28-pin PLCC package

GENERAL DESCRIPTION

The TDA8718 is a monolithic BiCMOS 8-bit analog-to-digital converter (ADC) designed for professional applications. The device converts the analog input signal into 8-bit binary coded digital words at a sampling rate of 600 MHz. It has an effective 8-bit bandwidth of 100 MHz. All digital outputs are ECL compatible.

APPLICATIONS

- High speed analog-to-digital conversion
- Industrial instrumentation
- Data communication
- RF communication

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		–4.2	–4.5	–4.8	V
V_{EED}	digital supply voltage		–4.2	–4.5	–4.8	V
I_{EEA}	analog supply current		–	70	tbf	mA
I_{EED}	digital supply current		–	110	tbf	mA
I_{EEO}	output supply current	R_L = 50 Ω	–	160	–	mA
ILE	DC integral linearity error		–	±0.5	–	LSB
DLE	DC differential linearity error		–	±0.5	–	LSB
EB	effective bits	f_i = 100 MHz; f_{CLK} = 600 MHz	–	7.5	–	bits
f_{CLK}	maximum clock frequency		600	–	–	MHz
P_{tot}	total power dissipation (excluding load)		–	850	–	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8718K	28	PLCC	plastic	SOT261

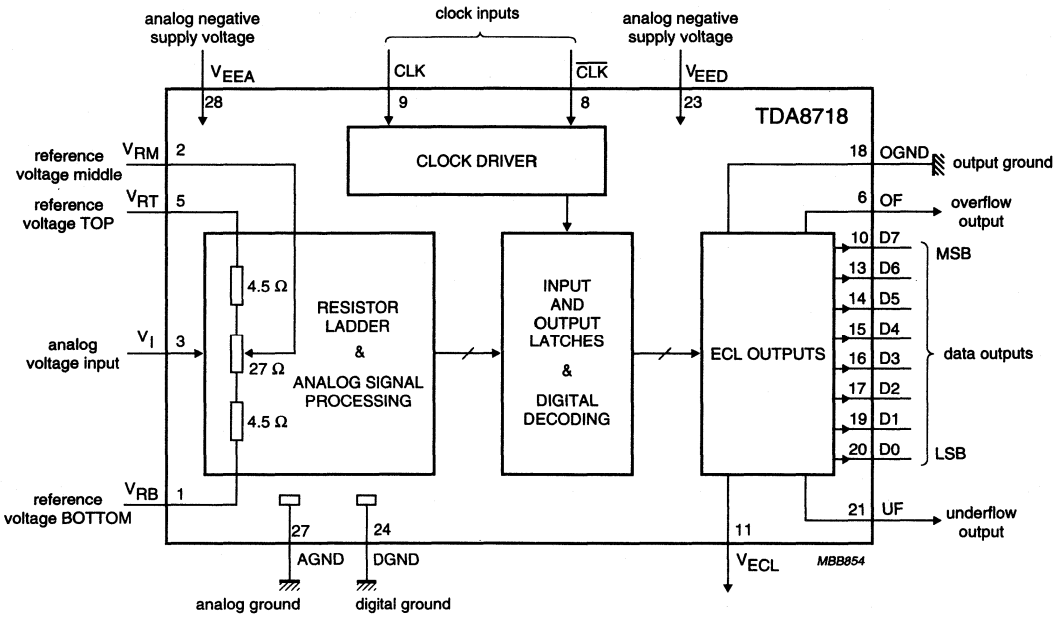


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter

TDA8718

PINNING

SYMBOL	PIN	DESCRIPTION
V_{RB}	1	reference voltage BOTTOM
V_{RM}	2	reference voltage middle decoupling
V_I	3	analog input
n.c.	4	not connected
V_{RT}	5	reference voltage TOP
OF	6	overflow digital output
n.c.	7	not connected
$\overline{CLK}$	8	complementary clock input
CLK	9	clock input
D7	10	digital output (MSB)
V_{ECL}	11	ECL reference voltage
n.c.	12	not connected
D6	13	digital output
D5	14	digital output
D4	15	digital output
D3	16	digital output
D2	17	digital output
OGND	18	output ground (0 V)
D1	19	digital output
D0	20	digital output (LSB)
UF	21	underflow digital output
n.c.	22	not connected
V_{EED}	23	digital negative supply voltage (−4.5 V)
DGND	24	digital ground
n.c.	25	not connected
n.c.	26	not connected
AGND	27	analog ground
V_{EEA}	28	analog negative supply voltage (−4.5 V)

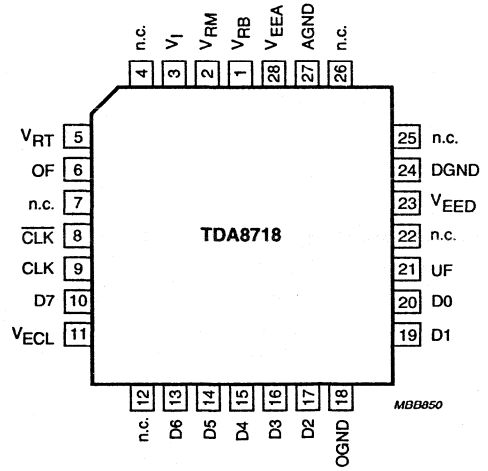


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

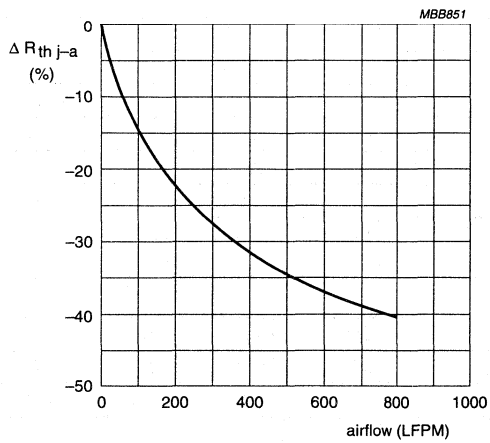
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage range (pin 28)		−4.2	−6.0	V
V_{EED}	digital supply voltage (pin 23)		−4.2	−6.0	V
V_{EEA}-V_{EED}	supply voltage difference		0	0.1	V
V_I	input voltage range	referenced to AGND	tbf	tbf	V
CLK; $\overline{CLK}$(p-p)	input voltage for differential clock drive (peak-to-peak value)	referenced to V_{EED}; note 1	0.2	2.0	V
I_O	output current		−	tbf	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		0	+70	°C
T_j	junction temperature		−	+125	°C

Note to the limiting values

1. The circuit has two clock inputs: CLK and $\overline{CLK}$. Sampling takes place on the falling edge of the clock input signal: CLK and $\overline{CLK}$ are two complementary signals.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT261)	45 K/W



Test conditions: PCB (2.24 x 2.24 x 0.062 inches)

Fig.3 Average effect of air flow on $R_{th\ j\text{-}a}$.

CHARACTERISTICS

V_{EEA} = –4.2 V to –4.8 V; V_{EED} = –4.2 V to –4.8 V; AGND and DGND shorted together; T_{amb} = 0 to +70 °C; unless otherwise specified. (Typical readings taken at V_{EEA} = –4.5 V; V_{EED} = –4.5 V; T_{amb} = 25 °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage (pin 28)		–4.2	–4.5	–4.8	V
V_{EED}	digital supply voltage (pin 23)		–4.2	–4.5	–4.8	V
I_{EEA}	analog supply current (pin 28)		–	70	tbf	mA
I_{EED}	digital supply current (pin 23)		–	110	tbf	mA
I_{EEO}	output supply current	R_L = 50 Ω	–	160	–	mA
Reference voltages for the resistor ladder						
I_{ref}	reference current (pin 5)		25	60	80	mA
V_{RB}	reference voltage BOTTOM (pin 1)		–	–3.6 Ω x I_{ref}	–	V
V_{RT}	reference voltage TOP (pin 5)		–	0	–	V
R_{LAD}	resistor ladder		–	36	–	Ω
R_{LTC}	temperature coefficient of the resistor ladder		–	tbf	–	Ω/°C
V_{OB}	voltage offset BOTTOM	note 1	–	4.5 Ω x I_{ref}	–	mV
V_{OT}	voltage offset TOP	note 1	–	4.5 Ω x I_{ref}	–	mV
Inputs						
CLK INPUT (PIN 9); $\overline{CLK}$ INPUT (PIN 8)						
V_{IL}	LOW level input voltage	T_{amb} = 25 °C	–	–3.4	–	V
V_{IH}	HIGH level input voltage	T_{amb} = 25 °C	–	–2.5	–	V
I_{IL}	LOW level input current	V_{CLK} = –1.77 V	–	tbf	–	µA
I_{IH}	HIGH level input current	V_{CLK} = –0.88 V	–	tbf	–	µA
R_I	input resistance	f_{CLK} = 600 MHz	–	tbf	–	kΩ
C_I	input capacitance	f_{CLK} = 600 MHz	–	tbf	–	pF
$\Delta V_{CLK(p-p)}$	clock input differential V_{CLK} - $V_{\overline{CLK}}$ (peak-to-peak value)	DC level –2 to –4 V	tbf	900	tbf	mV
ANALOG INPUT (PIN 3); NOTE 2						
I_{IL}	LOW level input current	data output = 00	20	40	80	µA
I_{IH}	HIGH level input current	data output = FF	100	200	400	µA
R_I	input resistance		–	tbf	–	kΩ
C_I	input capacitance		–	tbf	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs (R_L = 50 Ω)						
DIGITAL 10 K ECL OUTPUTS (D0 TO D7; OF; UF)						
V_{OL}	LOW level output voltage	T_{amb} = 25 °C	−1810	−1705	−1630	mV
V_{OH}	HIGH level output voltage	T_{amb} = 25 °C	−1025	−955	−880	mV
V_{ECL}	ECL reference voltage		−	−1.35	−	V
I_{OL}	LOW level output current		4	6	8	mA
I_{OH}	HIGH level output current		10	20	25	mA

DYNAMIC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics						
f_{CLK}; $f_{\overline{CLK}}$	maximum clock frequency		600	−	−	MHz
t_r	clock rise time	f_{CLK} = 600 mHz; f_i = 100 MHz	−	250	−	ps
t_f	clock fall time	f_{CLK} = 600 mHz; f_i = 100 MHz	−	750	−	ps
Analog signal processing						
dG	differential gain		−	tbf	−	%
dp	differential phase		−	tbf	−	deg
	harmonics (full scale)	f_{CLK} = 600 MHz				
f_1	fundamental		−	0	−	dB
f_2	even		−	−56	−	dB
f_3	odd		−	−52	−	dB
Transfer function						
ILE	DC integral linearity error		−	±0.5	−	LSB
DLE	DC differential linearity error		−	±0.5	−	LSB
AILE	AC integral linearity error		−	tbf	−	LSB
EFFB	effective bits	f_{CLK} = 600 MHz; f_i = 100 MHz	−	7.5	−	bits

Notes to the characteristics

1. Voltage offset BOTTOM (V_{OB}) is the difference between the analog input which produces data outputs equal to 00 and the reference voltage BOTTOM (V_{RB}), at T_{amb} = 25 °C. Voltage offset TOP (V_{OT}) is the difference between reference voltage TOP (V_{RT}) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
2. The analog input is not internally biased. It should be externally biased between V_{RT} and V_{RB} levels.

Table 1 Output coding

STEP	V_I (TYP. value)	BINARY OUTPUTS D5 to D0	0/UFL
Underflow	$< -31.5\ \Omega \times I_{ref}$	000000	1
0	$-31.5\ \Omega \times I_{ref}$	000000	0
1	.	000001	0
.	.	.....	.
.	.	.....	.
.	.	.....	.
254	.	111110	0
255	$-4.5\ \Omega \times I_{ref}$	111111	0
Overflow	$> -4.5\ \Omega \times I_{ref}$	111111	1

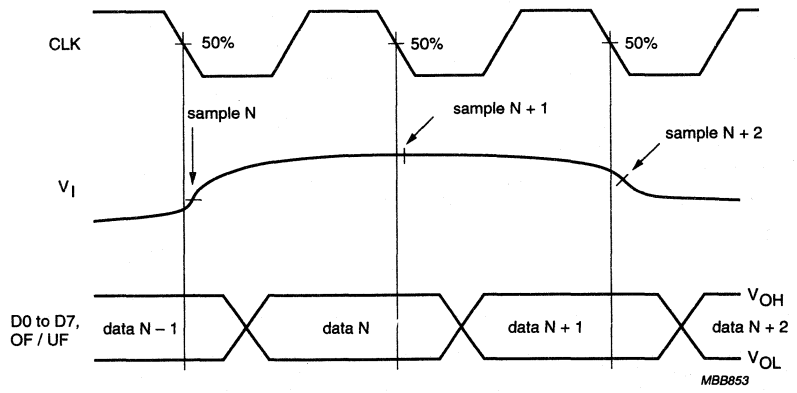


Fig.4 Timing diagram.

APPLICATION INFORMATION

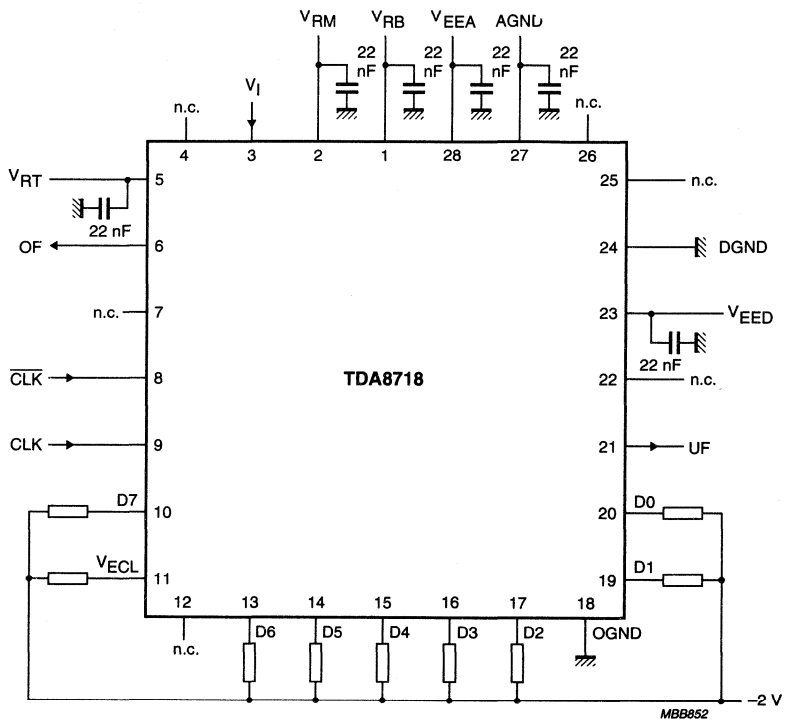


Fig.5 Application diagram.

PLL FM demodulator for DBS signals

TDA8730

GENERAL DESCRIPTION

The TDA8730 is a sensitive PLL demodulator for the second IF and direct broadcasting satellite (DBS) receivers. It provides AGC output and threshold adjustment for optimal signal level at the input of the demodulator.

FEATURES

- Broadband IF amplifier
- PLL demodulator, consisting of:
  - a multiplier
  - a voltage controlled oscillator
  - a loop amplifier
- AGC detector and DC amplifier
- LOW impedance video and data output
- Power supply voltage stabilizer

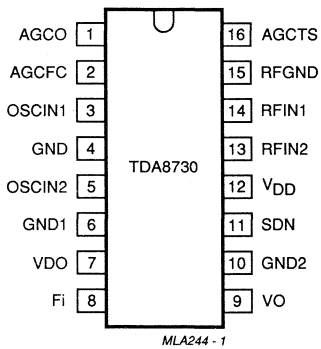


Fig.1 Pinning diagram.

APPLICATIONS

Direct broadcasting satellite (DBS) receivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		-	9	-	V
I_{DD}	supply current		-	75	-	mA
V_I	input voltage level		-	70	-	dBµV
f_{osc}	minimum oscillator frequency		-	130	-	MHz
f_{osc}	maximum oscillator frequency		-	720	-	MHz
V_O	video output signal amplitude (peak-to-peak value)	note 1	-	1.1	-	V
V_{AGC}	AGC output voltage		1.8	-	V_{DD}	V

Note

1. Δf = 13.5 MHz(peak-to-peak value)

PINNING

SYMBOL	PIN	DESCRIPTION
AGCO	1	AGC output
AGCFC	2	AGC frequency compensation
OSCIN1	3	oscillator input 1
GND	4	GND
OSCIN2	5	oscillator input 2
GND1	6	ground 1
VDO	7	variable capacitor drive output
FI	8	feedback input
VO	9	video output
GND2	10	ground 2
SDN	11	stabilizer decoupling node
V_{DD}	12	supply voltage +9 V
RFIN2	13	RF input 2
RFIN1	14	RF input 1
RFGND	15	RF ground
AGCTS	16	AGC threshold setting

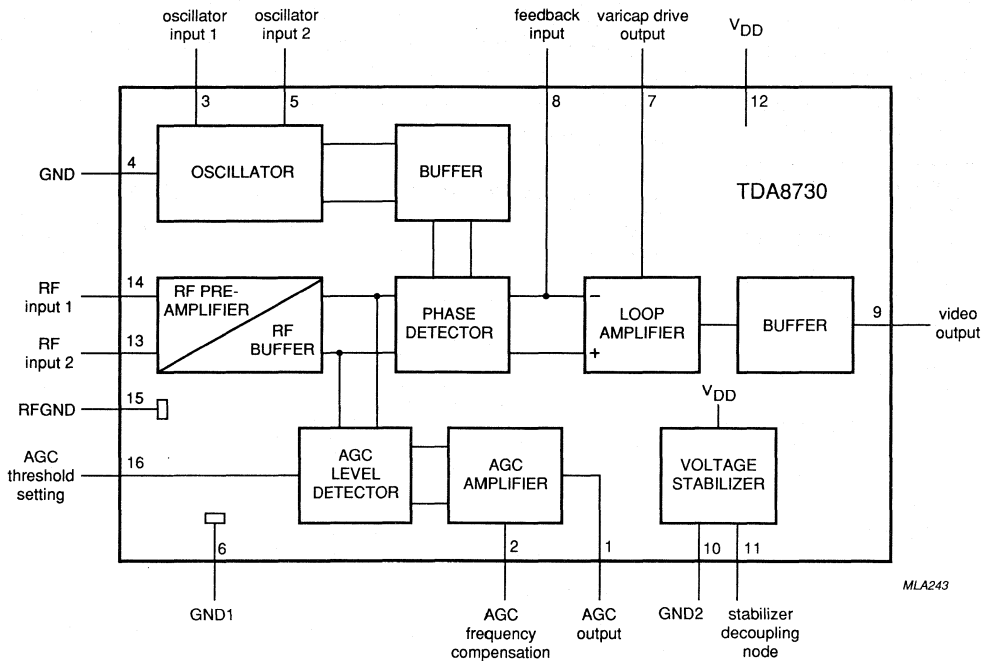


Fig.2 Block diagram.

PLL FM demodulator for DBS signals

TDA8730

FUNCTIONAL DESCRIPTION

The TDA8730 is a PLL FM demodulator intended for use in satellite tuners. It can demodulate frequency deviations ranging from 13.5 $MHz_{(p-p)}$ (DBS services) up to 25 $MHz_{(p-p)}$ (FSS services) and offers a high demodulation linearity. The circuit is optimized for operation at 479.5 MHz (the European IF for satellite tuners) and can handle the various broadcasting standards that are in use (including MAC).
Due to the PLL principle, demodulation noise threshold extension is possible. The high sensitivity of the balanced IF input reduces the additional gain, required in the tuner.
An on-chip AGC circuit delivers a gain control signal for use by the tuner IF amplifier, and a voltage regulator makes the circuit insensitive to supply voltage changes.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8730	16	DIL	plastic	SOT38GE

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.3	11	V
I_{DD}	input voltage	–0.3	V_{DD}	V
$I_{O(source)}$	output source current	-	10	mA
V_{AGC}	AGC output voltage	-	11	V
t_{sc}	max short circuit time of outputs	10	-	s
$V_{AGC(adj)}$	AGC threshold adjustment voltage	–0.3	V_{DD}	V
T_{stg}	storage temperature	–55	150	°C
T_j	junction temperature	-	150	°C
T_{amb}	operating ambient temperature	–25	85	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j-a}$	from-junction-to-ambient in free air	55	-	K/W

CHARACTERISTICS

V_{DD} = 9 V; T_{amb} = 25 °C; f = 480 MHz; Input level 70 dBμV; measured in circuit of Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	$V_{pin\ 12}$ to pin 10 or pin15	8.1	9.0	9.9	V
I_{DD}	supply current	$I_{pin\ 12}$; note 1	-	75	90	mA
Frequency demodulator						
f_{osc}	minimum oscillator frequency	-	-	130	-	MHz
f_{osc}	maximum oscillator frequency	-	-	720	-	MHz
V_i	operating input level	pin 13; note 2	-	70	74	DBμV
S11	input reflection coefficient |S11| unbalanced; pin 14 decoupled (50 Ω reference)	pin 13; note 3	-	0.07	-	
	balanced; 100 Ω reference	pin 13 to pin 14	-	0.11	-	
Kd	phase detector constant	(level at pin 13 is 70 dBμV)	-	0.45	-	V/rad.
Ko	VCO constant		-	12	-	MHz/V
Ao	open loop gain of loop amplifier	pin 7 to pin 8	-	40	-	dB
f-3 dB	open loop bandwidth of loop amplifier		-	2.8	-	MHz
Z_{in}	input impedance of feedback input	pin 8	-	930	-	Ω
Z_{out}	output impedance of loop amplifier	pin 7	-	30	50	Ω
le	VCO linearity error over Δf = ±10 MHz	note 4	-	1	-	%
	shift of DC level at video output for ΔV_{DD} = ±10% with unmodulated 480 MHz input signal	pin 9	-	-	±50	mV
	drift of DC level at video output for T_{amb} = 25 to 50 °C with unmodulated 480 MHz input signal	pin 9	-	-	+50	mV
V_{VCO}	VCO capture range		±14	-	-	MHz
G_d	differential gain	note 5	-	-	±4	%
ϕ_d	differential phase	note 5	-	-	±2	deg.
MOD	intermodulation	note 6	-	–70	-	dB
AGC						
V_{IAGC}	AGC threshold (IAGC = 0 mA) as a function of voltage applied to pin 16 V_{pin16} = 0.8 V	pin 13	-	-	67	dBμV
	$V_{pin\ 16}$ = 9.0 V	note 7	73	-	-	dBμV
	AGC steepness	pin 1; note 8	-	18	-	mA/dB
	AGC output saturation voltage HIGH at I = –0.2 mA	$V_{pin\ 1}$ to pin 10 or pin 15	V_{DD}-0.5	-	V_{DD}	V
	AGC output saturation voltage LOW at I = 0.2 mA		-	1.8	2.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video output						
V_O	video output signal amplitude (Δf = 13.5 MHz p-p)	pin 9 to pin 10 or pin 15	-	1.1	-	V
$V_{O(DC)}$	DC level of video output	pin 9 to pin 10 or pin 15; note 9	3.1	3.5	3.9	V
Z_O	output impedance	pin 9	-	30	50	Ω
Z_L	AC load impedance	pin 9; note 10	600	-	-	Ω
Voltage regulator						
V_{ref}	reference voltage for | load| ≤ 1 mA	pin 11; note 11	-	7	-	V
V_{reg}	line regulation 8.1 V ≤ VIN ≤ 9.9 V	pin 11	-	70	-	mV
I_{load}	allowable load current	pin 11	–1	-	0	mA

Notes

1. The supply current is the consumption of the circuit only.
   The current consumption of this application is given by the addition of the supply current of the circuit plus the current consumption of external components in the application given. In this event (Fig.4) the typical current is 80 mA.
2. The circuit of Fig.4 is designed for an input level of 70 dBμV.
   The maximum allowable input level for PLL design is 74 dBμV.
   However, for levels other than 70 dBμV the optimum loop filter values will be different from those given in Fig.4.
3. In the application circuit of Fig.4 the RF input is asymmetrically driven.
   In order to reduce the influence of oscillator signal coupling to the RF inputs, it is recommended to use a symmetrical drive at both inputs.
4. The linearity is specified as the maximum difference between the slope df/dV at the channel centre frequency (480 MHz) and the slope at 480 MHz ± 10 MHz.
5. Measurements with test signals in accordance with CCIR Rec. 473-3; Fm signal with DBS parameters: pre-and de-emphasis in accordance with CCIR Rec. 405-1, 625 lines PAL TV system. Modulator sensitive 13.5 MHz/V at pre-emphasis cross over frequency 1 V(p-p) video signal at pre-emphasis filter input.
6. For the intermodulation measurement, an FM test signal is applied having the following modulating components: 1.5 MHz reference sinewave with a deviation of 9.45 MHz(p-p), 5.5 and 5.75 MHz sinewaves with deviation 5.6 MHz(p-p) (so 4.5 dB below the reference, see Fig. 3). At the demodulator output the 2nd order intermodulation is defined according to Fig. 3. The video output is loaded with 500 Ω resistor + DC blocking capacitor.
7. The voltage applied at pin 16 is allowed to be higher than the minimum supply voltage (8.1 V).
8. The voltage at the AGC output (pin 1) decreases when the RF input level at pin 13 increases above the adjusted AGC threshold.
9. The DC level at the video output decreases when the RF input frequency increases.
   The DC level at the video output (pin 9) is measured with the VCO switched off because when the oscillator is operating, the DC level is dependent on the application (oscillator into the input).
10. The load impedance must have at least the minimum value for a frequency range from DC to the bandwidth of the i.f. filter (usually 27 MHz) since wide-band noise components will also appear at the video output.
11. It is possible to use the regulator output voltage (pin 11). The maximum current allowed is 1 mA.
    Possible application as voltage reference source for AFC circuit.

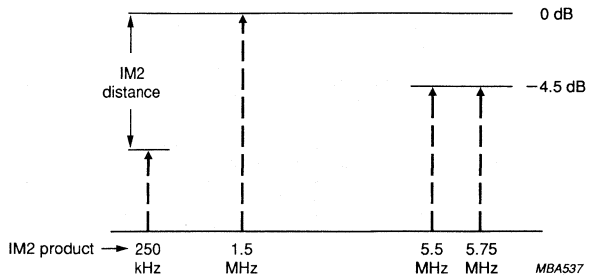


Fig.3 IM2 product.

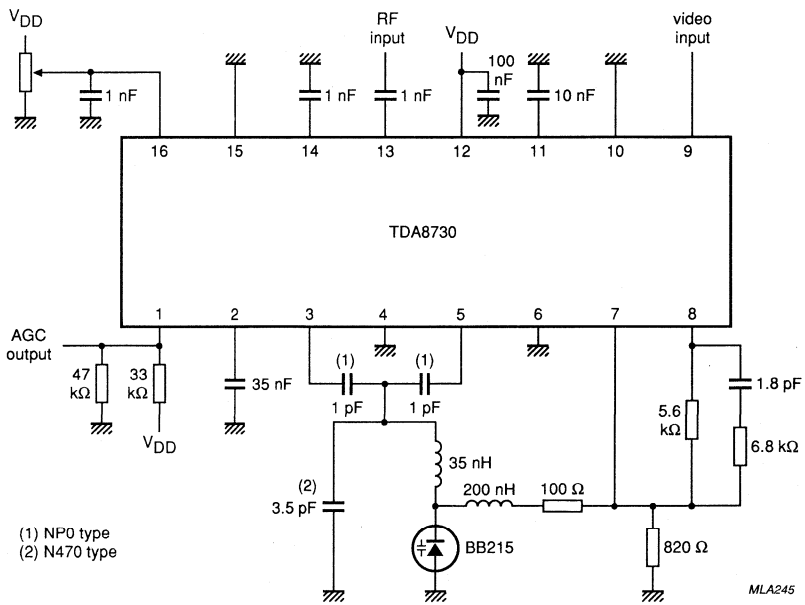


Fig.4 Application information.

NICAM-728 demodulator (NIDEM) TDA8732

FEATURES

- 5 V supplies for analog and digital circuitry
- Low cost application
- Improved noise behaviour
- Limiting amplifier for QPSK input
- Suitable with PAL B, G and I NICAM-728 systems.

APPLICATIONS

- NICAM-728 systems

GENERAL DESCRIPTION

The NIDEM is a dedicated device providing a DQPSK (Differential Quadrature Phase Shift Keying) demodulator for a NICAM-728 system.
The device interfaces with NICAM-728 decoders and provides data synchronized to a 728 kHz clock (either supplied externally or by the on-board clock).
The device consists of a costas loop quadrature demodulator, a bit-rate clock recovery and differential decoder with parallel to serial conversion.
The Voltage Controlled Oscillator (VCO) used in the costas loop is realized with a single pin crystal oscillator.
A second single pin crystal oscillator with a divider chain provides signals at 5.824 MHz and at 728 kHz.
The NIDEM is suitable for PAL B, G (carrier oscillator crystal at 11.7 MHz) and PAL I (carrier oscillator crystal at 13.104 MHz).

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5	5.5	V
V_{CCD}	digital supply voltage	4.5	5	5.5	V
V_{CCA}	analog supply voltage	4.5	5	5.5	V
$V_{CCA}-V_{CCD}$	differential supply voltage	−0.5	-	0.5	V
I_{CCA}	analog supply current	-	12.5	-	mA
I_{CCD}	digital supply current	-	14.5	-	mA
V_3	QPSK input level (peak-to-peak value)	30	100	300	mV
R_I	input impedance	1.75	2.5	3.25	kΩ
C_I		-	2	-	pF
f_{CAROSC}	carrier oscillator frequency	11.5	-	13.5	MHz
	crystal frequency for PAL B, G	-	11.7	-	MHz
	crystal frequency for PAL I	-	13.104	-	MHz
f_{CLKOSC}	clock oscillator frequency	-	11.648	-	MHz
f_{C5M}	C5M output frequency	-	5.824	-	MHz

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8732	20	DIL	plastic	SOT146

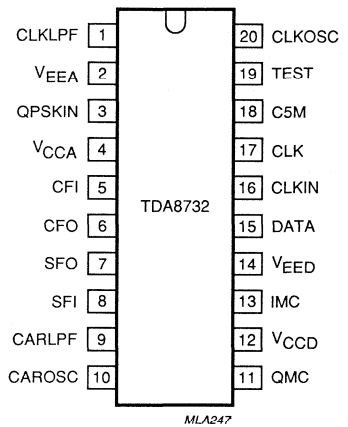


Fig.1 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLKLPF	1	transconductance output for bit-rate loop low-pass filter
V_{EEA}	2	ground for analog circuitry
QPSKIN	3	QPSK modulated data input
V_{CCA}	4	power supply for analog circuitry
CFI	5	baseband cosine channel input after filtering
CFO	6	demodulated cosine channel output to low-pass filter
SFO	7	demodulated sine channel output to low-pass filter
SFI	8	baseband sine channel input after filtering
CARLPF	9	transconductance output for carrier loop low-pass filter
CAROSC	10	crystal input for carrier oscillator (frequency is 11.7 MHz or 13.104 MHz)
QMC	11	monostable components connection for quadrature data transition detector
V_{CCD}	12	power supply for digital circuitry
IMC	13	monostable components connection for in-phase data transition detector
V_{EED}	14	ground for digital circuitry
DATA	15	728 kbit/s demodulated and differentially decoded serial data output
CLKIN	16	bit-rate clock input at 728 kHz, phase-locked to the data
CLK	17	output clock frequency at 728 kHz
C5M	18	reference frequency output at 5.824 MHz (8 x CLK)
TEST	19	input for test purpose (grounded for normal operation)
CLKOS	20	crystal input for clock oscillator (frequency is 11.648 MHz)

FUNCTIONAL DESCRIPTION

QPSK demodulator

The DQPSK signal input to the demodulator (QPSKIN) is limited and fed into the costas loop demodulator. A single-pin carrier oscillator (CAROSC), at twice the carrier frequency, supplies a differential signal to the divider circuitry, which drives the demodulators with both 0° and 90° phase shift. This produces cosine and sine signals which are required for the carrier recovery. Cosine (In-phase) and sine (in Quadrature) channel baseband filters are then provided externally between pins CFO and CFI, and SFO and SFI respectively. The two filtered baseband signals are then processed to provide an error signal, the magnitude and which of which bear a fixed relationship to the phase error of the carrier, regardless of which of the four rest-states the signal occupies. The carrier recovery loop is closed with the aid of a single pin loop filter connection at CARLPF, which filters the error voltage signal to control the 728 kHz according to the application diagrams of Fig.4 or 5.

Bit-rate clock recovery loop

The CFI and SFI channels are processed using edge detectors and monostables, with externally derived time constants (see Fig.3), to generate a signal with a coherent component at the data bit symbol rate. This signal is compared with the clock derived from CLKIN and used to produce an error signal at the transconductance output CLKLPF. This error signal is loop-filtered and used to control the clock generator (at CLKOSC if the on-board clock is used). See application diagram of Fig.5.

Clock oscillator and timing generator

A voltage-controlled oscillator on-board the NIDEM runs at 11.648 MHz and is divided down to produce a 728 kHz (bit-rate) clock output (CLK) which is phase locked to the pulse stream and may be used as an alternative clock input for NIDEM. A reference clock at 5.824 MHz is provided at pin C5M (TTL levels).

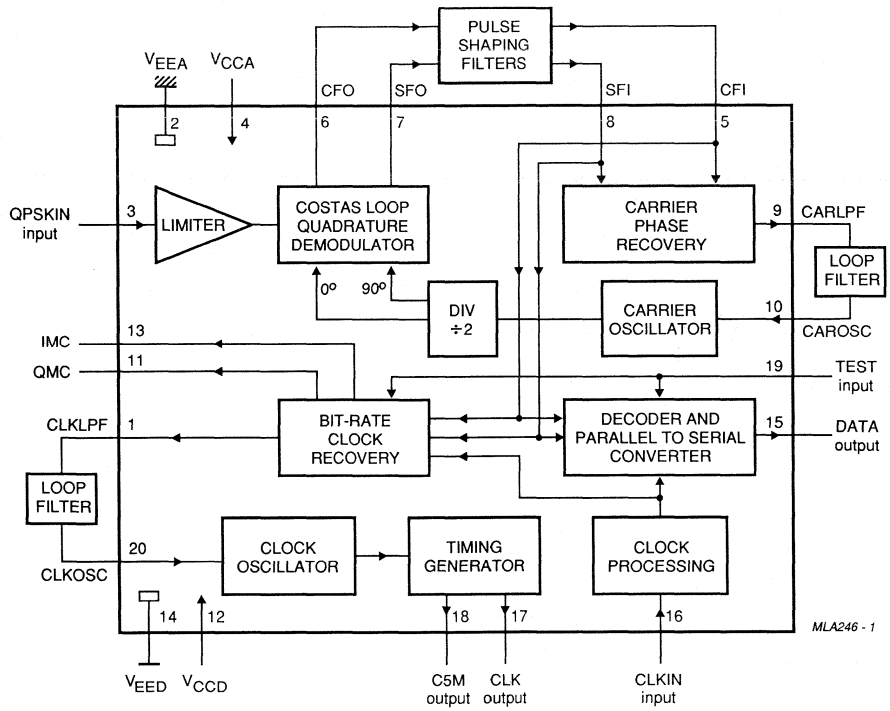


Fig.2 Block diagram.

Differential decoder and parallel to serial converter

The recovered symbol-rate clocking-signal (364 kHz) produced internally is passed to the demodulator where it samples the sliced raised cosine pulse stream. The recovered bit-rate clocking-signal is passed to the decoder and is used to differentially decode the demodulated data signal and reform it into a serial bit-stream.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	6	V
V_{CCD}	digital supply voltage range	−0.3	6	V
QPSKIN	input voltage range	−0.3	5.5	V
CFI,SFI	input voltage range	−0.3	V_{CCA}	V
CFO,SFO	output voltage range	−0.3	5.5	V
CAROSC CLKOSC	input voltage range	−0.3	5.5	V
QMC,IMC	output voltage range	−0.3	V_{CCD}	V
DATA CLK,C5M	output voltage range	−0.3	5.5	V
CLKIN	input voltage range	−0.3	6	V
TEST	input voltage range	−0.3	6	V
CLKLPF CARLPF	output voltage range	−0.3	5.5	V
T_{stg}	storage temperature range	−40	+125	°C
T_j	maximum junction temperature	-	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient in free air	-	80	K/W

CHARACTERISTICS

V_{CCA} = 5 V ±10%; V_{CCD} = 5 V ±10%; −0.5 V < V_{CCA} - V_{CCD} < 0.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5	5.5	V
V_{CCD}	digital supply voltage		4.5	5	5.5	V
V_{CCA}–V_{CCD}	differential supply voltage		−0.5	-	0.5	V
I_{CCA}	analog supply current		-	13	17	mA
I_{CCD}	digital supply current		-	13	17	mA
P_{tot}	total power dissipation		-	130	187	mW
T_{amb}	ambient temperature range		0	-	70	°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
CLKIN						
V_{IH}	input voltage HIGH		2	-	V_{CCD}	V
V_{IL}	input voltage LOW		-	-	0.8	V
I_{IL}	input current LOW	V_I = 0 V	–400	-	-	µA
I_{IH}	input current HIGH	V_I = 5 V	-	-	10	µA
QPSKIN						
f_{QPSKIN}	input frequency range		5	-	7	MHz
R_I	input impedance	f = 364 kHz	70	100	130	kΩ
C_I		f = 364 kHz	-	2	-	pF
SFI, CFI						
I_b	input bias current	V_{SFI} = 4.3 V V_{CFI} = 4.3 V	-	-	5	µA
R_I	input impedance	f = 364 kHz	70	100	130	kΩ
C_I		f = 364 kHz	-	2	-	pF
CAROSC						
f_{car}	oscillator frequency		11.5	-	13.5	MHz
CARRIER OSCILLATOR CRYSTAL						
-	holder			RW 43		
$f_{PAL\ I}$	nominal frequency with specified load	PAL I; C_L = 15 pF	-	13.104	-	MHz
$f_{PAL\ B,\ G}$		PAL B, G; C_L = 15 pF	-	11.7	-	MHz
-	vibration mode			note 1		
-	circuit condition			note 2		
-	adjustment tolerance on frequency at 25 °C		–30	-	+30	10^{-6}
-	temperature range		0	-	70	°C
-	frequency stability over temperature		–30	-	+30	10^{-6}
C_I	load capacitance		-	15	-	pF
R_s	resonance resistance	note 3	15	-	40	Ω
C_m	motional capacitance		-	21	-	fF
C_p	parallel capacitance		-	-	5	pF
-	drive power level		-	-	0.5	mW
CLKOSC						
f_{clk}	oscillator frequency	C_I = 15 pF	-	11.648	-	MHz
BIT-RATE OSCILLATOR CRYSTAL						
-	holder			RW 43		
$f_{PAL\ I}$	nominal frequency with specified load	PAL I; C_L = 15 pF	-	11.648	-	MHz
$f_{PAL\ B,\ G}$		PAL B, G; C_L = 15 pF				

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLKOSC						
-	vibration mode			note 1		
-	circuit condition			note 2		
-	adjustment tolerance on frequency at 25 °C		–30	-	+30	10^{-6}
-	temperature range		0	-	70	°C
-	frequency stability over temperature		–30	-	+30	10^{-6}
C_l	load capacitance		-	15	-	pF
R_s	resonance resistance	note 3	15	-	40	kΩ
C_m	motional capacitance		-	21	-	fF
C_p	parallel capacitance		-	-	5	pF
-	drive level		-	-	0.5	mW

Notes to the characteristics

1. Fundamental.
2. Series resonance.
3. Only the maximum value is relevant in case of a resistor of 15 Ω in series with the crystal (due to the application requirements).

CHARACTERISTICS

V_{CCA} = 5 V ±10%; V_{CCD} = 5 V ±10%; –0.5 V < V_{CCA} - V_{CCD} < 0.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
CFO, SFO						
R_O	output impedance	f = 364 kHz	-	110	200	Ω
-	signal amplitude (peak-to-peak value)		0.8	1	-	V
CARLPF						
V_{OL}	output voltage LOW	I_{OL} = 100 µA	-	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = –100 µA	V_{CCD} - 1 V	-	-	V
gm ϕ1	phase comparator transconductance gain	V_O = 0.4 V to V_{CCD} - 1 V	100	125	-	µA/rd
I_{LO}	leakage current for π/4 phase shift		–5	-	5	µA
CLKLPF						
V_{OL}	output voltage LOW	I_{OL} = 100 µA	-	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = –100 µA	V_{CCD} - 1 V	-	-	V
gm ϕ2	phase comparator transconductance gain	V_O = 0.4 V to V_{CCD} - 1 V	50	65	-	µA/rd
I_{LO}	off-state leakage current		–5	-	5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
IMC, QMC						
t_{REC}	monostable recovery time	typical RC network R = 22 kΩ C = 150 pF	-	-	600	ns
t_{on}	monostable time		-	1.37	-	µs
CLK, C5M						
V_{OL}	output voltage LOW	I_{OL} = 1 mA	-	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −100 µA	2.4	-	V_{CCD}	V
t_r	rise time; see Fig. 3	C_L = 15 pF	-	20	-	ns
t_f	fall time; see Fig. 3	C_L = 15 pF	-	20	-	ns
f_{C5M}	C5M reference frequency		-	5.824	-	MHz
DATA						
V_{OL}	output voltage LOW	I_{OL} = 1 mA	-	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −100 µA	2.4	-	V_{CCD}	V
t_r	rise time; see Fig. 3	C_L = 15 pF	-	30	-	ns
t_f	fall time; see Fig. 3	C_L = 15 pF	-	30	-	ns
CLOCK TIMING						
t_d	CLK to C5M delay (pin 17 to 18)		-	15	-	ns
t_d	CLKIN to DATA delay (pin 16 to 15)	V_{CCD} = 4.5 V	-	520	585	ns

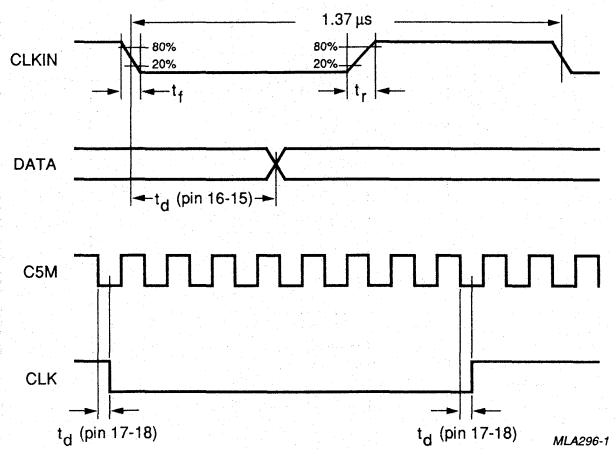
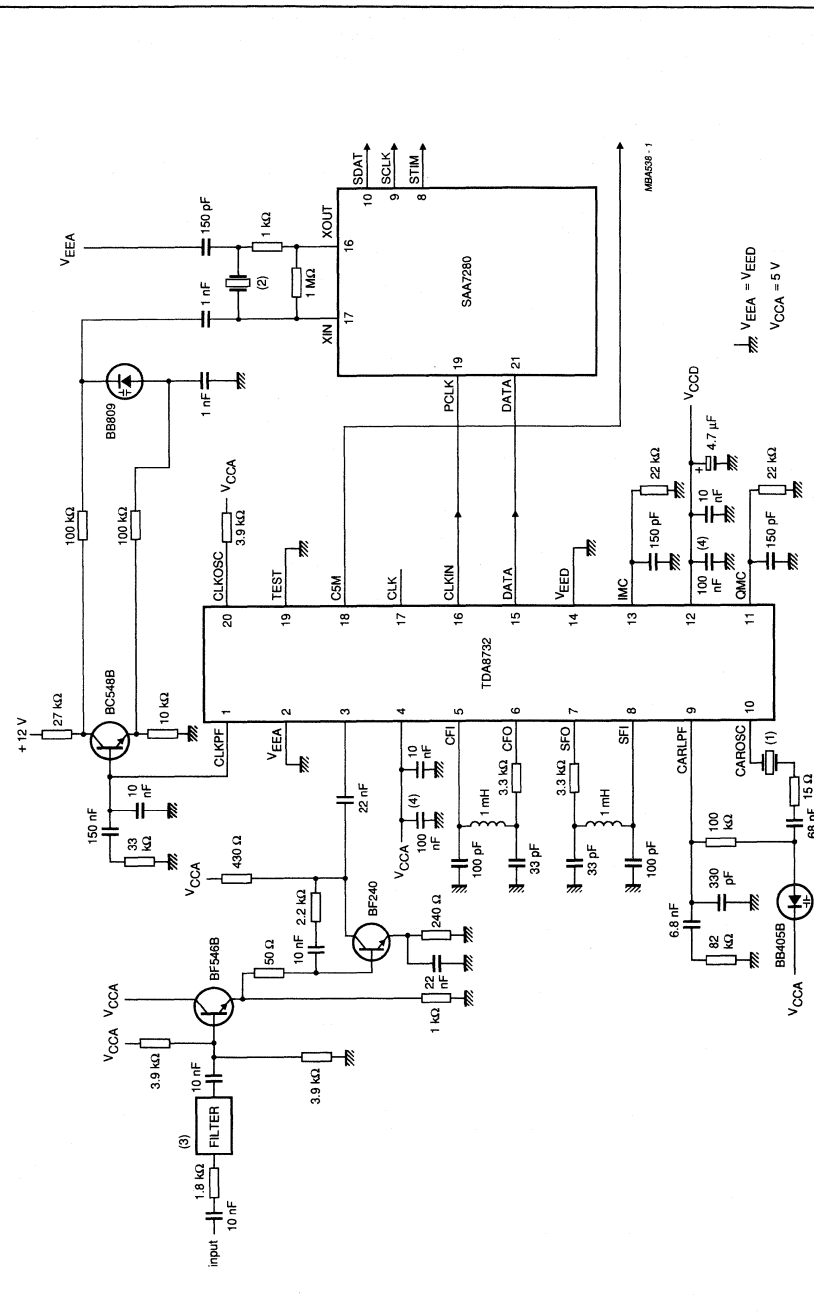


Fig.3 Data timing diagram.



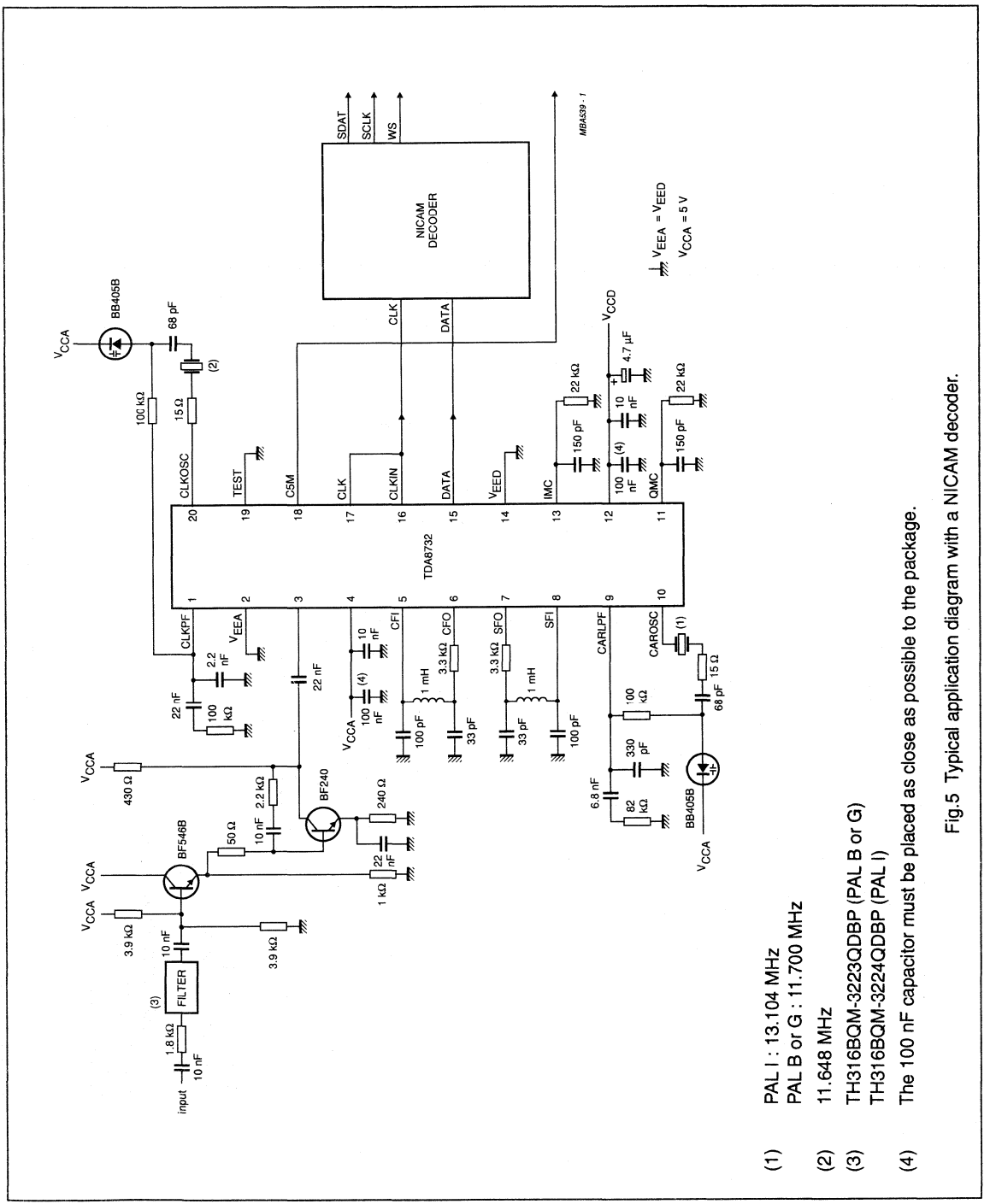
(1) PAL I : 13.104 MHz
PAL B or G : 11.700 MHz

(2) 17.472 MHz

(3) TH316BQM-3223QDBP (PAL B or G)
TH316BQM-3224QDBP (PAL I)

(4) The 100 nF capacitor must be placed as close as possible to the package.

Fig.4 Typical application diagram with the SAA7280.



(1) PAL I : 13.104 MHz
PAL B or G : 11.700 MHz

(2) 11.648 MHz

(3) TH316BQM-3223QDBP (PAL B or G)
TH316BQM-3224QDBP (PAL I)

(4) The 100 nF capacitor must be placed as close as possible to the package.

Fig.5 Typical application diagram with a NICAM decoder.

MACAN TDA8734

FEATURES

- Single supply voltage
- Video amplifier with AGC and manual gain control
- System clock outputs.

GENERAL DESCRIPTION

The TDA8734 is an analog signal input conditioner interface which has been designed for use in a multi-standard MAC decoder. The device incorporates a video amplifier with grey level clamping and automatic gain control, an adaptive data slicer and a phase locked crystal oscillator. The output from the oscillator is divided to provide clock outputs.

FUNCTIONAL DESCRIPTION

In the multi-standard MAC decoder, the time multiplexed MAC signal is applied to the video (pin 9) and data (pin 13) inputs of the TDA8734. The video signal is grey level clamped and AGC adjusted in the device. The AGC action is based on measurements of the data signal amplitude, and with a further fixed gain trim (at pin 6) it is possible to match the absolute value of the video signals to the following A-to-D conversions. The grey level is defined by a voltage (on pin 8) which is derived from the reference voltages (TOP and BOTTOM) of the A-to-D converter.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage range	4.5	-	5.5	V
V_{CCD}	digital supply voltage range	4.5	-	5.5	V
V_{XTAL}	crystal supply voltage range	4.5	-	5.5	V
P_{tot}	total power dissipation	-	-	375	mW
B	video amplifier 3 dB bandwidth	12	-	-	MHz
ΔG	gain control range	−3	-	+3	dB
T_{amb}	operating ambient temperature range	0	-	+70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8734T	24	SO	plastic	SOT137A

Clock timing information as well as clean sliced data are extracted from the data of the multiplexed signal. A 40.5 MHz master oscillator on the IC is locked to the incoming sliced data, and its output is divided and buffered to provide outputs at 10.125 MHz (pin 23) and 20.25 MHz (pin 21) which are used as clocks throughout the rest of the decoder. Fig.11 illustrates the Clock recovery timing. Fig.12 provides a typical application diagram.

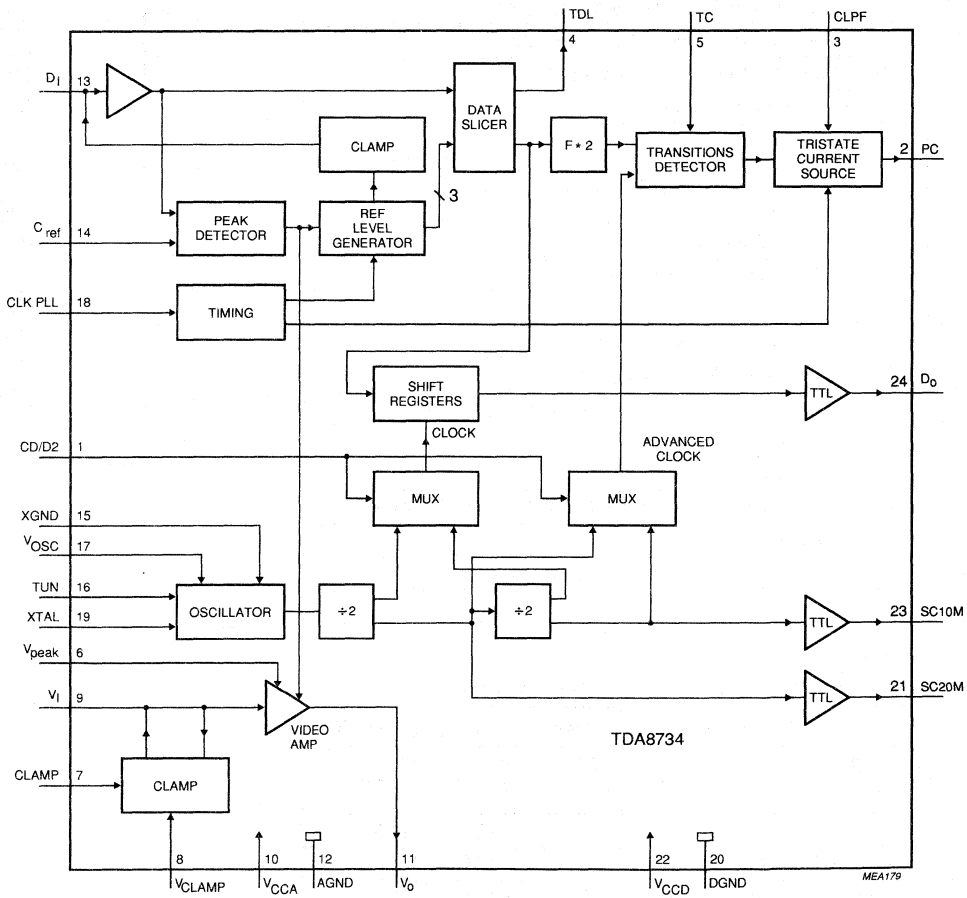


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CD/D2	1	selection of bit rate
PC	2	phase comparator output
CLPF	3	PLL low pass filter capacitor connection
TDL	4	test point, recovery of data slicers
TC	5	time constant adjustment
V_{peak}	6	control point of video amplifier gain
CLAMP	7	clamp during grey period of video
V_{CLAMP}	8	clamp reference voltage input
V_I	9	video amplifier input
V_{CCA}	10	analog supply
V_O	11	video amplifier output
AGND	12	analog ground
D_I	13	data signal input
C_{ref}	14	store point of peak data
XGND	15	crystal oscillator ground
TUN	16	tuning circuit connection
V_{OSC}	17	crystal oscillator supply
CLK PLL	18	gate signal to slicer and phase comparator
XTAL	19	crystal connection
DGND	20	digital ground
SC20M	21	system clock output (oscillator clock divided by 2)
V_{CCD}	22	digital supply
SC10M	23	system clock output (oscillator clock divided by 4)
D_O	24	data output

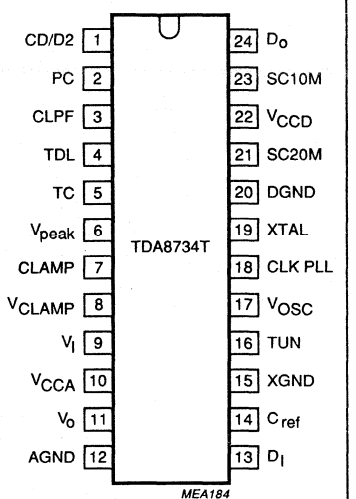


Fig.2 Pinning diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	6.5	V
V_I	input voltage	0	V_{CC}	V
P_{tot}	total power dissipation	-	375	mW
T_{stg}	storage temperature range	–55	+125	°C
t_j	junction temperature range	–55	+125	°C

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 1 (method 3015.5)

SYSTEM CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage (pin 10)		4.5	5.0	5.5	V
V_{OSC}	oscillator supply voltage (pin 17)		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage (pin 22)		4.5	5.0	5.5	V
TTL inputs: CLAMP (pin 7); CLK PLL (pin 18); CD/D2 (pin 1)						
V_{IL}	input voltage LOW		-	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	-	V
Video amplifier						
C_9	video input coupling capacitor (pin 9)		-	33	-	nF
V_{pp}	black-to-white amplitude on video input (pin 9)	note 1	-	1.0	1.4	V
V_{CLAMP}	V_{CLAMP} voltage range (pin 8)		-	2.5	-	V
Data slicer						
C_{13}	data input coupling capacitor (pin 13)		-	100	-	nF
V_{pp}	amplitude voltage on data input (pin 13)	note 1	-	1.0	1.4	V
C_{14}	peak level storage capacitor (between pins 14 and 20)		-	100	-	nF
Phase comparator						
C_3	PLL low pass filter capacitor (pin 3)		-	220	-	pF
RC	time constant for data transition detector (between pins 5 and 22)		-	15	-	ns
T_{amb}	operating ambient temperature range		0	-	+70	°C

Note

1. In accordance with the specifications of the D-MAC/PACKET and D2-MAC/PACKET systems.

DEVICE CHARACTERISTICS

V_{CCA}, V_{OSC}, and V_{CCD} = 5.0 V; AGND, DGND and XGND = 0 V; T_{amb} = 25 °C; unless otherwise specified

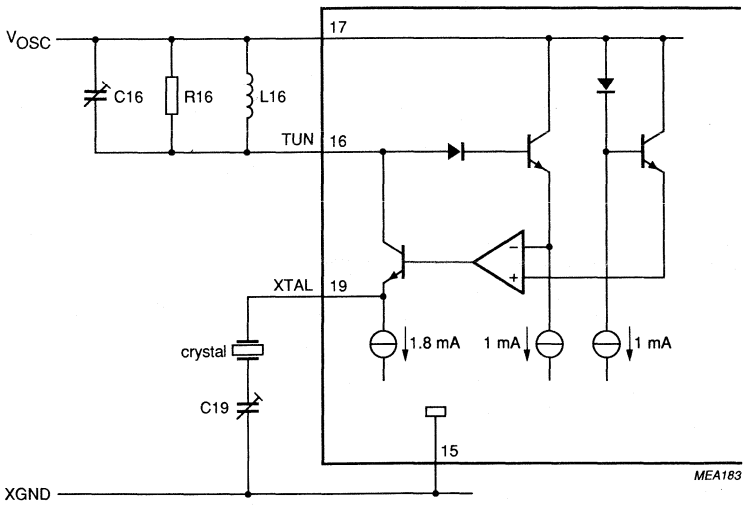
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current (between pins 10 and 12)		7.0	11.5	16	mA
I_{CCD}	digital supply current (between pins 22 and 20)		14	25.5	40	mA
I_{OSC}	oscillator supply current (between pins 17 and 15)		3.5	8	12	mA
Oscillator TUN = tuning circuit connection; see Fig.3						
I_{16}	DC current in tuning circuit	$V_{16} = V_{OSC}$	1.0	1.6	2.3	mA
R_{16}	input resistance	f = 40.5 MHz	-	60	-	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator XTAL crystal connection (pin 19); see Fig.3						
R_{19}	resistance at tuned frequency		-	680	-	Ω
V_{19}	DC voltage	I_{19} = 0 mA; V16 = V_{OSC}	-	1.6	-	V
Clock outputs SC20M (pin 21); SC10M (pin 23); see Figs 4 and 5						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH}= tbf	2.4	-	-	V
I_{OS}	output short-circuit current	V_O = 0 V; note 1	-	–35	-	mA
t_{LH}	transition time LOW to HIGH	note 2	-	-	4	ns
t_{HL}	transition time HIGH to LOW	note 2	-	-	3	ns
DC	duty factor	note 2	0.40	-	0.60	%
Phase comparator TC: time constant adjustment (pin 5); see Fig.9						
I_5	maximum input current		-	3.5	-	mA
Phase comparator PC: output (pin 2)						
$\|I_2\|$	maximum output current		-	650	1000	µA
R_2	output resistance		-	1	-	kΩ
V_2	output voltage		-	2.5	-	V
$\|I_{leak}\|$	leakage current during OFF condition		-	-	10	µA
Phase comparator CLPF PLL: low pass filter connection (pin 3); see Fig.10						
I_3	input current	$V_3 = V_{CCD}$	-	300	-	µA
Data Slicer D_I = data input (pin 13); see Fig.8						
V_{13}	DC restoration voltage	I_{13} = 0	1.5	2.0	-	V
I_{13}	DC restoration current	V_{13} = 1.5 V	-	-	–7.0	mA
I_{13}	input current	V_{13} = 3.5 V	-	-	40	µA
Data Slicer C_{ref}: store point of peak data (pin 14)						
I_{14}	input current	V_{14} = 3 V; V_{13} = 2 V	-	-	40	µA
I_{14}	maximum peak detection current		-	-	–7.0	mA
ΔV	DC offset (between pins 14 and 13)	V_{13} = 2 V; I_{14} = 0 V	-	-	200	mV
Selection of bit rate CD/D2 (pin 1)						
I_{IL}	input current LOW	V_{IL} = 0.8 V; note 3	–150	-	-	µA
I_{IH}	input current HIGH	V_{IH} = 2.0 V; note 3	-	-	10	µA
Data Output D_O (pin 24); see Fig.5						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = 100 µA	2.4	-	-	V
I_{OS}	output short-circuit current	V_O = 0 V; note 1	-	–35	-	mA
t_{LH}	transition time LOW to HIGH	note 2	-	-	4	ns
t_{HL}	transition time HIGH to LOW	note 2	-	-	3	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLK PLL: gate signal input (pin 18)						
I_{IL}	input current LOW	V_{IL} = 0.8 V; note 3	−150	-	-	µA
I_{IH}	input current HIGH	V_{IH} = 2.0 V; note 3	-	-	10	µA
Video amplifier V_I: video amplifier input (pin 9)						
$\|I_{CLAMP}\|$	maximum current during clamp period	V_7 = 2.0 V	300	500	750	µA
I_9	input current	V_7 = 0.8 V V_9 = 2.5 V	-	-	3	µA
E_{att}	dispersal energy attenuation	C_9 = 33 nF	-	30	-	dB
Video amplifier V_O: video amplifier output (pin 11)						
B	3 dB bandwidth		12	-	-	MHz
α	maximum cross-talk caused by clock signals		-	−50	-	dB
V_{pp}	black-to-white output voltage		-	1.34	-	V
R_{11}	output resistance	f = 5 MHz	-	50	-	Ω
Video amplifier V_{CLAMP}: clamp reference voltage input (pin 8)						
$\|I_8\|$	input current	V8 = 2.5 V	-	-	500	nA
Video amplifier V_{peak}: control point of video amplifier gain (pin 6)						
V_6	input voltage for nominal gain		-	3	-	V
ΔG	gain range		−3	-	+3	dB
R_6	input resistance		-	1	-	kΩ
Video amplifier CLAMP: clamp pulse input (pin 7)						
I_{IL}	input current LOW	V_{IL} = 0.8 V; note 3	−1200	-	-	µA
I_{IH}	input current HIGH	V_{IH} = 2 V; note 3	-	-	10	µA

Notes

1. Duration of the short-circuit should not exceed one second.
2. The timing measurements are defined as indicated on Fig.6 and T_{amb} = 25 °C.
3. The simplified schematic of the TTL input circuit is shown in Fig.7.
   On pin 1 (CD/D2): supply = V_{CCD}; ground = D_{GND};
   input LOW: the clock used in the circuit is the oscillator clock divided by 4;
   input HIGH: the clock used in the circuit is the oscillator clock divided by 2.
   On pin 7 (CLAMP): supply = V_{CCA}; ground = A_{GND};
   input LOW: the clamp circuit is not active;
   input HIGH: the clamp circuit is active.
   On pin 18 (CLK PLL): supply = V_{CCD}; ground = D_{GND};
   input LOW: the data slicer and the phase comparator output are not gated;
   input HIGH: the data slicer and the phase comparator output are gated.



The tuned circuit is connected between pins 17 (V_{OSC}) and 16 (TUN).
The value of the components are R16 = 2 kΩ and f_{TUN} = 40.5 MHz.
The input resistance at pin 19 (XTAL) is measured at f = 40.5 MHz.

Fig.3 Simplified schematic of oscillator circuit.

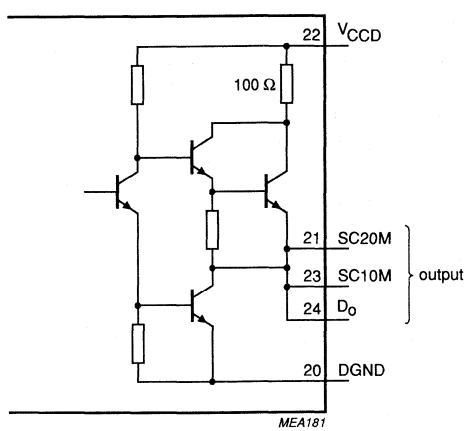


Fig.4 Simplified schematic of TTL outputs.

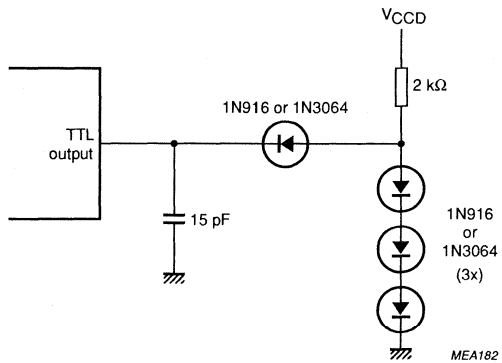
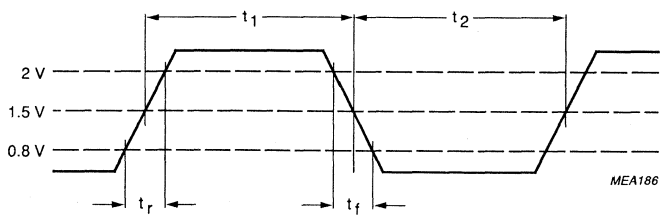


Fig.5 Output load circuit for TTL output timing measurements.



duty factor = $\frac{t_1}{t_1 + t_2}$

transition time (t_f) = t_{HL} (HIGH to LOW)
transition time (t_r) = t_{LH} (LOW to HIGH)

Fig.6 Timing measurements.

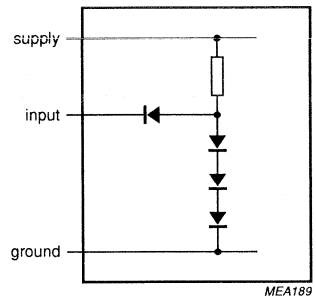
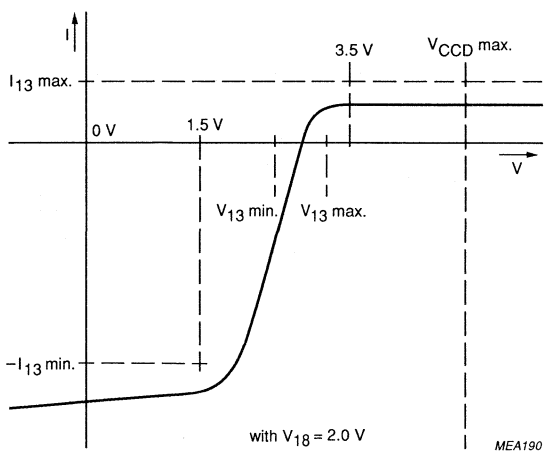


Fig.7 Simplified schematic of TTL input circuit.



CLK PLL = HIGH

Fig.8 I-V curve of data input circuit.

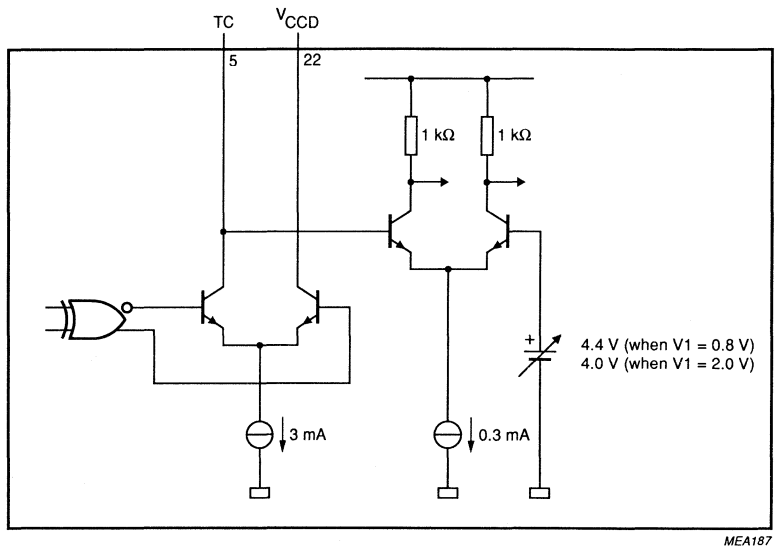


Fig.9 Simplified schematic of TC output.

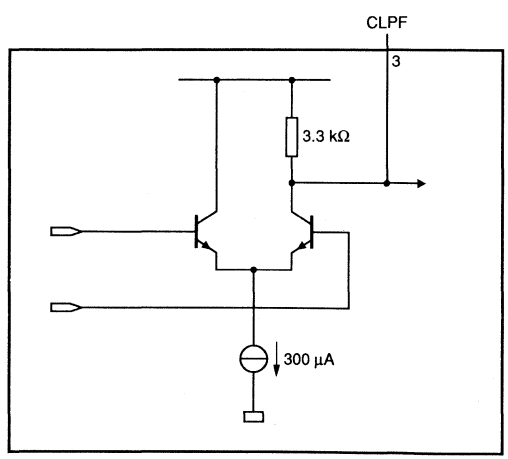


Fig.10 Simplified schematic of CLPF output.

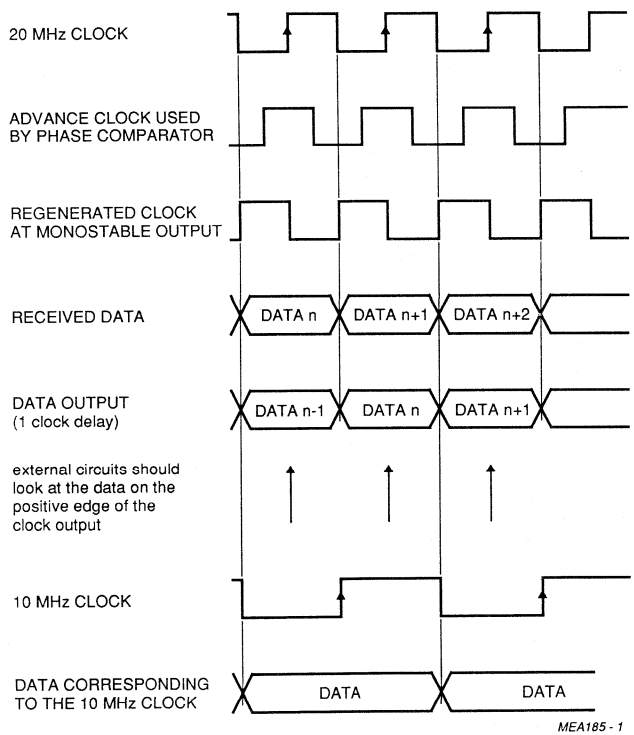


Fig.11 Clock recovery timing.

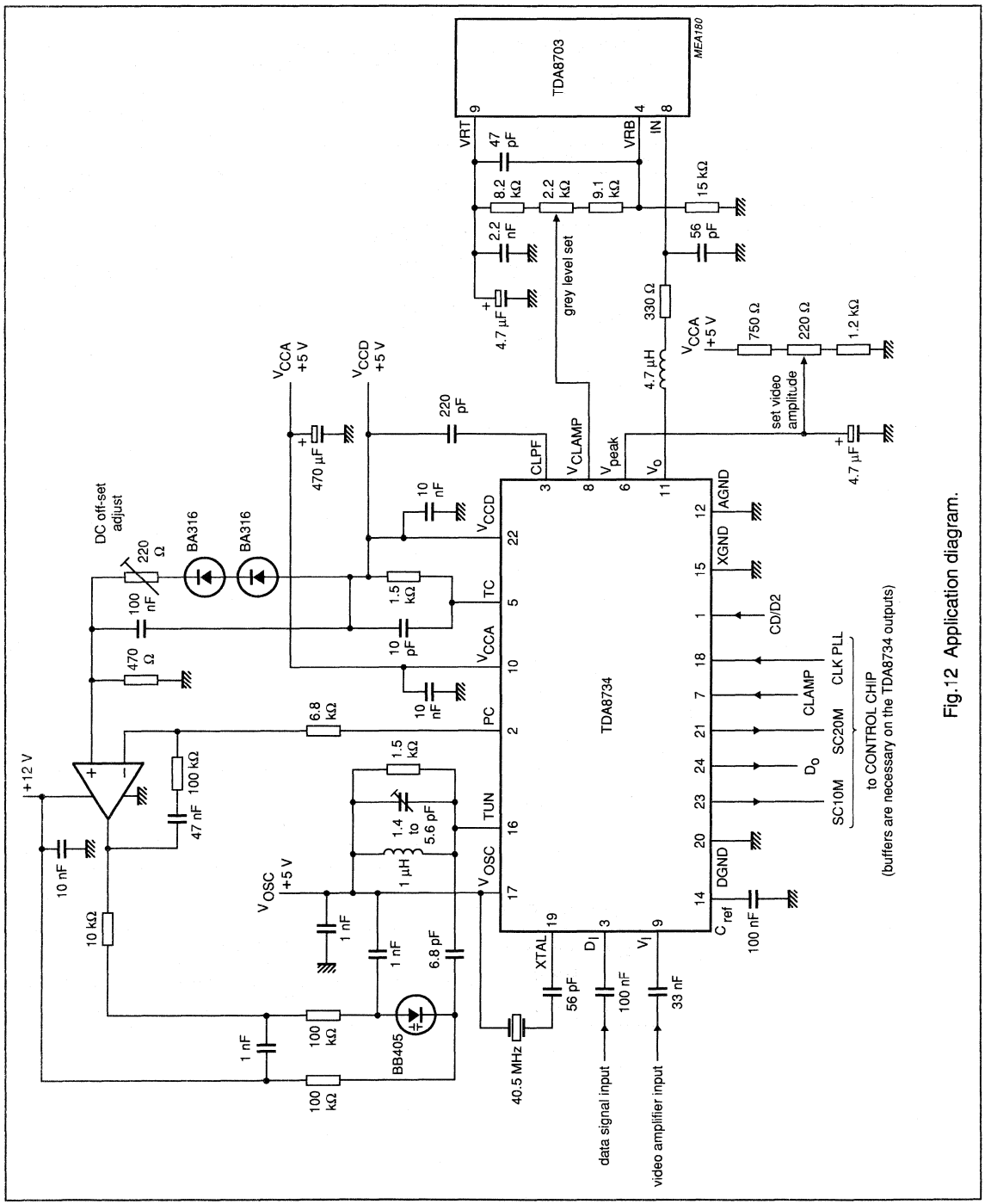


Fig.12 Application diagram.

Satellite sound circuit with noise reduction TDA8740

FEATURES

- Demodulation of main audio signal by means of wide band PLL (lock range selectable)
- Demodulation of secondary audio signals by means of wide band PLL
- HF input selection: two-out-of eight secondary audio signals can be selected
- Noise reduction of the secondary audio signals
- Output selection: stereo, language 1, language 2, main audio, external
- Mute control
- Line outputs (SCART level)

APPLICATIONS

- Satellite receivers
- TV sets
- Video recorders

GENERAL DESCRIPTION

The TDA8740 is a multi-function sound IC for use in satellite receivers, television sets and video recorders.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	operating supply voltage		8	12	13.2	V
Main channel						
$V_{18(RMS)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	-	1.0	2.0	mV
Δf_{OM}	lock range PLL demodulator	either: or:	5.5 10.0	- -	7.5 11.5	MHz MHz
V_{23}	output voltage		–8	–6	–4	dBV
S/N(A)	signal-to-noise ratio	A-weighted	62	70	-	dB
Secondary channels						
$V_{2...16(RMS)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	-	0.8	1.5	mV
$\Delta f_{OS1;\ 2}$	lock range PLL demodulators		6.0	-	8.5	MHz
$V_{24,\ 25}$	output voltage		–8	–6	–4	dBV
S/N(A)	signal-to-noise ratio	A-weighted	72	80	-	dB
Crosstalk						
$\alpha_{S/M}$	crosstalk from secondary to main channel		-	74	-	dB
$\alpha_{M/S}$	crosstalk from main to secondary channel		-	74	-	dB
$\alpha_{S/S}$	crosstalk between secondary channels		-	74	-	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8740	42	SDIL	plastic	SOT270

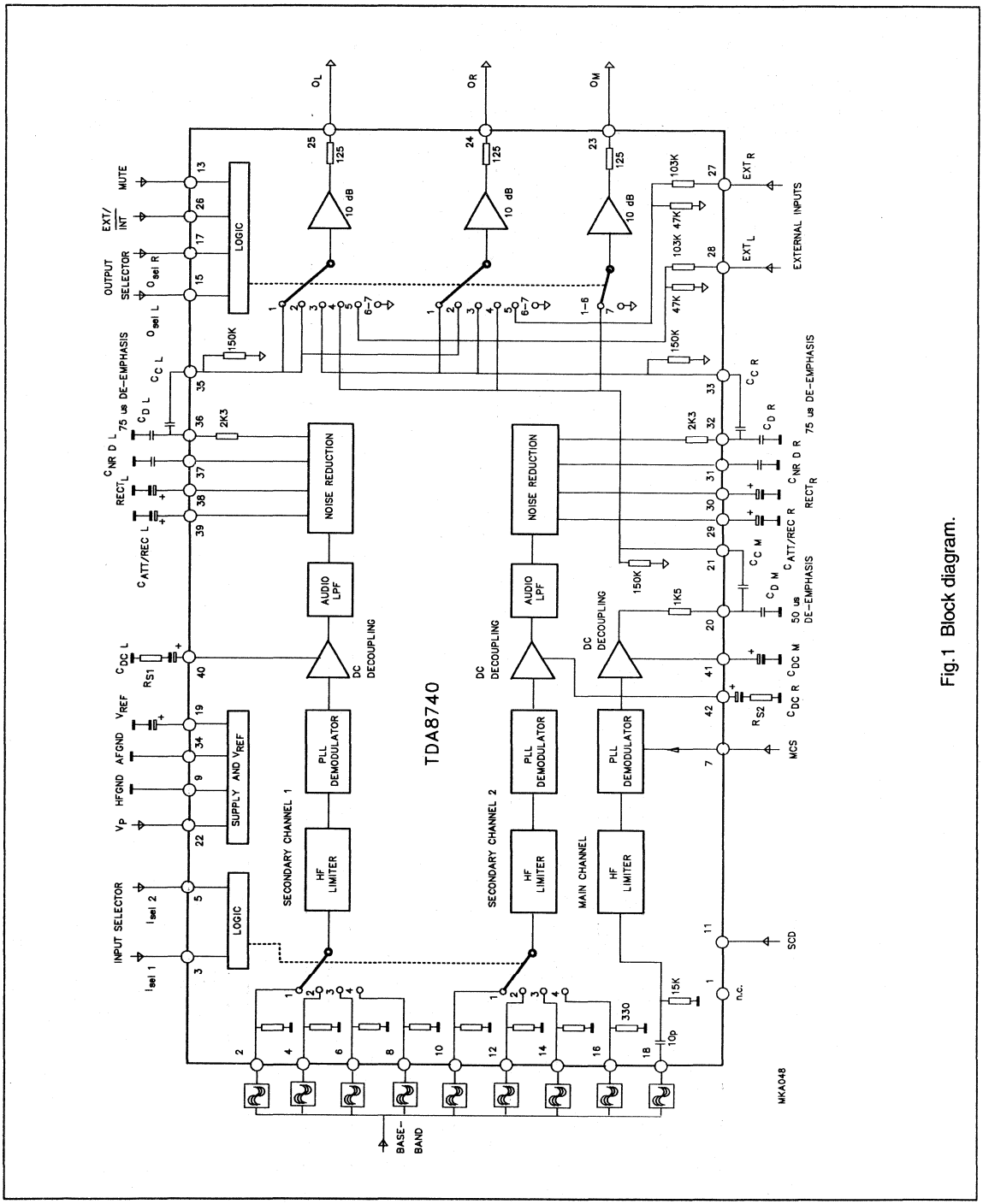


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
IN-1A	2	intercarrier input A for channel 1 (left)
$I_{sel\ 1}$	3	input select switch bit 1
IN-1B	4	intercarrier input B for channel 1 (left)
$I_{sel\ 2}$	5	input select switch bit 2
IN-1C	6	intercarrier input C for channel 1 (left)
MCS	7	main channel PLL lock-in range select
IN-1D	8	intercarrier input D for channel 1 (left)
HFGND	9	ground for HF section
IN-2A	10	intercarrier input A for channel 2 (right)
SCD	11	secondary channels PLLs disable
IN-2B	12	intercarrier input B for channel 2 (right)
MUTE	13	mute switch
IN-2C	14	intercarrier input C for channel 2 (right)
$O_{sel\ L}$	15	output select switch bit 1 (left)
IN-2D	16	intercarrier input D for channel 2 (right)
$O_{sel\ R}$	17	output select switch bit 2 (right)
IN-3	18	intercarrier input for main channel
V_{REF}	19	decoupling capacitor for reference voltage
$C_{D\ M}$	20	de-emphasis capaitor for main channel
$C_{C\ M}$	21	audio pass-through capacitor input for main channel
V_P	22	positive supply voltage
O_M	23	main channel output
O_R	24	right channel output
O_L	25	left channel output
EXT/INT	26	output switch bit 3 (external/internal)
EXT_R	27	external audio input (right)
EXT_L	28	external audio input (left)
$C_{ATT/REC\ R}$	29	attack/recovery capacitor (right)
$RECT_R$	30	rectifier DC decoupling (right)
$C_{NR\ D\ R}$	31	noise reduction de-emphasis capacitor (right)
$C_{D\ R}$	32	fixed de-emphasis capacitor (right)
$C_{C\ R}$	33	audio pass-through capacitor input for right channel
AFGND	34	ground for AF section
$C_{C\ L}$	35	audio pass-through capacitor input for left channel
$C_{D\ L}$	36	fixed de-emphasis capacitor (left)
$C_{NR\ D\ L}$	37	noise reduction de-emphasis capacitor (left)
$RECT_L$	38	rectifier DC decoupling (left)
$C_{ATT/REC\ L}$	39	attack/recovery capacitor (left)

SYMBOL	PIN	DESCRIPTION
$C_{DC\ L}$	40	DC decoupling capacitor (left)
$C_{DC\ M}$	41	DC decoupling capacitor (main)
$C_{DC\ R}$	42	DC decoupling capacitor (right)

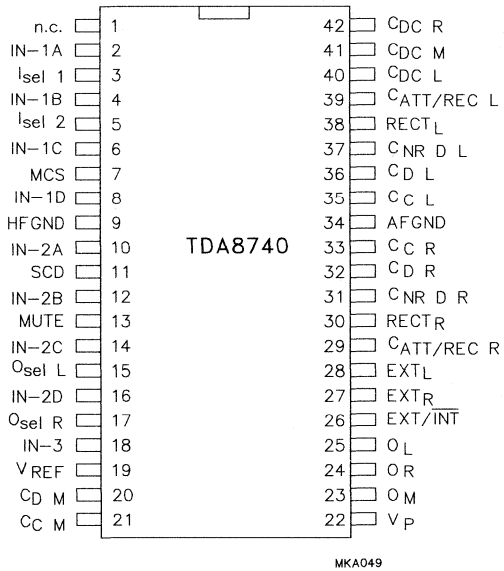


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Satellite sound

The baseband signal coming from a satellite tuner comprises the demodulated video signal and a number of sound carriers in case of reception of a PAL/NTSC/SECAM satellite signal.
Nearest to the video is the main sound carrier. It carries the mono sound related to the video. This is a FM modulated carrier with a fixed pre-emphasis. This carrier frequency can be in the range of 5.8 to 6.8 MHz. Furthermore a number of optional secondary sound carriers may be present. These can be used for stereo- or multi language sound related to the video, or for unrelated radio sound. These carriers are also FM modulated, but for better sound quality (improved signal-to-noise performance) broadcast satellites (e.g. 'ASTRA') use a noise reduction system (adaptive pre-emphasis circuit, combined with a fixed pre-emphasis).

These carrier frequencies can be in the range of 6.30 to 8.28 MHz. The TDA8740 holds all circuitry for the processing of the main channel and of two secondary channels, from baseband signal to line (SCART) output drivers. By means of bandpass filtering the desired frequencies can be routed to the TDA8740.

Main channel (see Fig. 1, block diagram)

The lock-in range of the main channel PLL can be switched between 5.5 to 7.5 MHz and 10.0 to 11.5 MHz by means of the MCS signal at pin 7. (Pin 7 is logic '0' : lock-in range is 5.5 to 7.5 MHz and pin 7 is logic '1' : lock-in range 10.0 to 11.5 MHz).
If only one fixed carrier frequency for the main channel is to be demodulated (e.g. 6.5 MHz), the lock-in range of the PLL should be switched to 5.5 to 7.5 MHz. The baseband signal is applied to the main channel input, pin 18 via a 6.5 MHz ceramic bandpass filter. If on the other hand it is desired to demodulate different main channel frequencies, these frequencies can be transferred to a fixed intermediate frequency (e.g. 10.7 MHz) using an external mixer and oscillator-frequency synthesizer. In that case the lock-in range of the PLL should be switched to 10.0 to 11.5 MHz. The IF signal is applied to the main channel input, pin 18 via a 10.7 MHz ceramic bandpass filter.

The filtered signal is AC-coupled to a limiter/amplifier and then to a PLL demodulator. The PLL FM demodulator ensures that the demodulator is alignment free. High amplification and DC error signals of the PLL which are superimposed on the demodulator output require DC decoupling. A buffer amplifier amplifies the signal to the same level as that of the secondary channels and decouples DC by means of an electrolytic capacitor connected to pin 41. The demodulator output signal is fed to pin 20 via an internal resistor. The output signal can be de-emphasized by means of this resistor and an external capacitor to ground. Capacitor value = de-emphasis time constant/1500 (for 50 µs: 33 nF). From here the signal is fed to the output selectors. The signal is amplified to 500 mV (RMS) (i.e. –6 dBV) in the output amplifiers.

Secondary channels

Up to eight secondary channel inputs are available (pins 2, 4, 6, 8, 10, 12, 14 and 16). External ceramic bandpass filters tuned to the desired secondary sound carrier frequencies, route these signals to the inputs.
For stereo purpose the TDA8740 contains two identical secondary sound processing channels. For each channel a selection can be made out of four inputs (IN-A, IN-B, IN-C, IN-D) by the input selector (see Logic Table 1). With the input switch several stereo signals or languages can be selected for demodulation. It should be noticed that the inputs are identical and can freely be interchanged (secondary channel 1 will also be referred to as 'LEFT' or 'LANGUAGE 1' and secondary channel 2 will also be referred to as 'RIGHT' or 'LANGUAGE 2').

From the input selector switch the signals are coupled to limiter/amplifiers and then to the PLL demodulators. Processing is similar to the main channel. The demodulator output signal is amplified in a buffer amplifier and DC decoupled by means of electrolytic capacitors connected to pins 40 (left) and 42 (right). Output level is set with a resistor in series with the capacitor.

High frequency components in the amplified PLL output signal are filtered out in the audio LPF block (4th order Butterworth low-pass filter) to prevent unwanted influence on the noise reduction.

NOISE REDUCTION (NR)

The NR can be regarded as an input level dependent low-pass filter (adaptive de-emphasis system) followed by a fixed de-emphasis. With maximum input level (= 0 dB) the frequency response of the first part (i.e. without fixed de-emphasis) is nearly flat. As the input level is x-dB lowered, the higher output frequencies will be reduced an extra x-dB w.r.t. to the lower frequencies (1 : 2 expansion).

The NR output signal is fed to pin 36 (left) and pin 32 (right) via an internal resistor.

Fixed de-emphasis is achieved by these resistors and external capacitors to ground. The signals are DC decoupled via pins 36/35 and 32/33 and then routed to the output selectors.

OUTPUT SECTION

With the ouput selector (see Logic Table 2) the outputs (pin 25 and 24) can be switched to the different channels. Both outputs can be switched to both secondary channels, to the main channel and to the external inputs (pin 28 and 27) for IC chaining purposes.

Pin 23 is a separate output which delivers the main channel only, creating the possibility to have three different output channels simultaneously, e.g. for use in HiFi VCR's.

Outputs 25 and 24 can be muted by setting the MUTE signal (pin 13) logic '1' (switch positions 6 and 7).

Output 23 can be muted by setting the MUTE signal and the EXT/INT signal (pin 26) both logic '1' (switch position 7).

All outputs (pins 23, 24 and 25) are line drivers with scart level capability and are short-circuit protected by 125 Ω output resistors.

Output level of all channels is –6 dBV typically when frequency deviation of FM signal is 54% of maximum frequency deviation (i.e. 0.54 x 85 kHz = 46 kHz for the main channel and 0.54 x 50 kHz = 27 kHz for the secondary channels) at 1 kHz modulation frequency (reference level).

ABBREVIATIONS

f_{MOD} = modulating frequency
Δf_M = frequency deviation of the main channel
Δf_{S1} = frequency deviation of secondary channel 1 (left)
Δf_{S2} = frequency deviation of secondary channel 2 (right)
f_{OM} = carrier frequency of main channel
f_{OS1} = carrier frequency of secondary channel 1
f_{OS2} = carrier frequency of secondary channel 2
LPF = Low-Pass Filter
NR = Noise Reduction
PLL = Phase-Locked-Loop

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (note 1)	0	13.2	V
V_x	voltage on any pin (note 1)	0	V_P	V
T_{stg}	storage temperature range	–65	+150	°C
T_{amb}	operating ambient temperature range	–20	+70	°C

Note to the limiting values

1. All voltages with reference to ground (pins 9 and 34).

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient	53 K/W

CHARACTERISTICS

All voltages with reference to ground (pins 9 and 34)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 22)		8	12	13.2	V

DC CHARACTERISTICS

All voltages with reference to ground (pins 9 and 34)
Measured in test set-up Fig. 3; V_P = 12 V; T_{amb} = 25 °C; $\Delta f_M = \Delta f_{S1} = \Delta f_{S2}$ = 0 kHz (no modulation); f_{OM} = 6.5 MHz; f_{OS1} = 7.02 MHz; f_{OS2} = 7.20 MHz; HF level at pin 18: 40 mV (RMS); HF level at selected secondary inputs: 20 mV (RMS); MCS = '0' (V_7 = 0 V); SCD = '0' (V_{11} = 0 V); unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_P	supply current		-	38	45	mA
P_{tot}	total power dissipation		-	-	600	mW
$V_{23,24,25}$	voltage on pins 23, 24 and 25		-	3.8	-	V
$V_{27,28}$	voltage on pins 27 and 28		-	3.8	-	V
$V_{33,35}$	voltage on pins 33 and 35		-	3.8	-	V
$V_{32,36}$	voltage on pins 32 and 36		-	3.8	-	V
$V_{30,38}$	voltage on pins 30 and 38		-	3.8	-	V
V_{21}	voltage on pin 21		-	3.8	-	V
V_{20}	voltage on pin 20		-	3.8	-	V
V_{19}	voltage on pin 19		3.7	3.8	3.9	V
$V_{2,4,6,8}$	voltage on pins 2, 4, 6 and 8		-	0	-	V
$V_{10,12,14,16}$	voltage on pins 10, 12, 14 and 16		-	0	-	V
$V_{40,42}$	voltage on pins 40 and 42		-	2.7	-	V
V_{41}	voltage on pin 41		-	2.8	-	V
I_{18}	input current at pin 18		-	-	1	µA

AC CHARACTERISTICS

All voltages with reference to ground (pins 9 and 34)
Measured in test set-up Fig. 3; V_P = 12 V; T_{amb} = 25 °C; f_{MOD} = 1 kHz; f_{OM} = 6.5 MHz; Δf_M = 46 kHz; $\Delta f_{S1} = \Delta f_{S2}$ = 27 kHz (reference levels); f_{OS1} = 7.02 MHz; f_{OS2} = 7.20 MHz; HF level at pin 18: 40 mV (RMS); HF level at selected secondary inputs: 20 mV (RMS); MCS = '0' (V_7 = 0 V); SCD = '0' (V_{11} = 0 V); unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Main channel - HF input (pin 18) and limiter						
$V_{18(RMS)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	-	1.0	2.0	mV
$V_{18(RMS)}$	input signal (RMS value)		-	-	200	mV
R_{18}	input resistance		-	15	-	kΩ
Main channel - PLL FM demodulator and DC decoupling amplifier						
f_{CCO}	free-running frequency		-	6.5	-	MHz
f_{CCO}	free-running frequency	MCS = '1'	-	10.7	-	MHz
Δf_{OM}	lock range of PLL	note 1	5.5	-	7.5	MHz
Δf_{OM}	lock-in range of PLL	MCS = '1'; note 1	10.0	-	11.5	MHz
R_{20}	output resistance for 50 µs de-emphasis (pin 20)		1.3	1.5	1.7	kΩ
V_{20}	output voltage (pin 20)		−17.5	−16.0	−14.5	dBV
ΔV_{20}	spread of PLL output voltage over lock range		-	-	±1	dB
R_{21}	input resistance of output amplifier (pin 21)		100	150	200	kΩ
Main channel - overall performance (output selector in position 4)						
$V_{23.24.25}$	output voltage	all PLLs locked	−8	−6	−4	dBV
THD	total harmonic distortion	all PLLs locked	-	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; all PLLs locked	62	70	-	dB
$V_{23(15\ kHz)}/V_{23(1\ kHz)}$	15 kHz frequency response with respect to 1 kHz	no de-emphasis connected	−0.5	0	+0.5	dB
$R_{23.24.25}$	output resistance		100	125	150	Ω
$\alpha_{S/M}$	crosstalk attenuation from secondary channels to main	note 2	-	74	-	dB
α_M	mute attenuation	output selector in position 7	74	-	-	dB
RR	supply voltage ripple rejection	V_{RR} = tbf V; f = tbf Hz	-	tbf	-	dB
Secondary channels 1 and 2 - HF inputs (pins 2, 4, 6, 8, 10, 12, 14, 16) and limiters						
$V_{2..16(RMS)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	-	0.8	1.5	mV
$V_{2..16(RMS)}$	input signal (RMS value)		-	-	200	mV
$R_{2..16}$	input resistance		280	330	380	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Secondary channels 1 and 2 - PLL FM demodulators (input selector in position 1)						
f_{CCO1}	free running frequency PLL1		-	7.0	-	MHz
f_{CCO2}	free running frequency PLL2		-	7.2	-	MHz
$\Delta f_{OS1/2}$	lock range of PLL's	note 3	6.0	-	8.5	MHz
$R_{S1,S2}$	series resistances for optimal frequency response afjustment		0	0.47	1.0	kΩ
$V_{40,42(RMS)}$	PLL output voltage (RMS value); pins 40 and 42	pins 40 and 42 to be left open-circuit	tbf	7	tbf	mV
$\Delta V_{40,42}$	spread of PLL output voltage over lock range		-	-	±1	dB
Secondary channels - overall performance of LPF and NR (in- and output selectors in position 1)						
$R_{36,32}$	output resistance for 75 µs de-emphasis (pins 36 and 32)		2.0	2.3	2.6	kΩ
$R_{35,33}$	input resistance of output amplifiers (pins 35 and 33)		100	150	200	kΩ
$V_{25,24}$	output voltage (pins 25 and 24)	note 4	–8	–6	–4	dBV
THD	total harmonic distortion	note 4	-	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; note 4	72	80	-	dB
$R_{25,24}$	output resistance (pins 25 and 24)	note 4	100	125	150	Ω
α_M	mute attenuation	output selector in position 6; note 4	74	-	-	dB
$\alpha_{S/S}$	crosstalk attenuation between secondary channels	note 5	-	74	-	dB
$\alpha_{M/S}$	crosstalk attenuation from main channel to secondary	note 6	-	74	-	dB
$V_{offset(DC)}$	offset voltage on attack/recovery capacitors (pins 39 and 29); DC value	all PLLs locked; $\Delta f = 0$	14	16	18	mV
RR	supply voltage ripple rejection	V_{RR} = tbf V; f = tbf Hz	-	tbf	-	dB
Secondary channels - low-pass filter						
$V_{38,30(50\ kHz)}/V_{38,30(1\ kHz)}$	50 kHz frequency response with respect to 1 kHz	note 7	–21	–16	–11	dB
Secondary channels - noise reduction						
$V_{25,24}$	output voltage (pins 25 and 24) at 0 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2}$ = 50 kHz; no fixed de-emphasis connected; note 4	–1	+1	+3	dBV
$V_{25,24(15\ kHz)}/V_{25,24(1\ kHz)}$	15 kHz frequency response with respect to 1 kHz at 0 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2}$ = 50 kHz; no fixed de-emphasis connected; note 4	–2	0	+2	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Secondary channels - noise reduction						
$V_{25,24}$	output voltage (pins 25 and 24) at –20 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2}$ = 5 kHz; no fixed de-emphasis connected; note 4	–29	–26	–24	dBV
$V_{25,24(15\ kHz)}/V_{25,24(1\ kHz)}$	15 kHz frequency response with respect to 1 kHz at –20 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2}$ = 5 kHz; no fixed de-emphasis connected; note 4	–13	–11.5	–10	dB
External inputs - pin 28 (left) and pin 27 (right) - overall performance (output selector in position 5)						
$V_{27,28}$	input signal		-	-	6	dBV
$R_{27,28}$	input resistance		100	150	200	kΩ
$V_{25,24}$	output level	$V_{27,28}$ = –6 dBV	–6.5	–6.0	–5.5	dBV
THD	total harmonic distortion	$V_{27,28}$ = –6 dBV; f = 1 kHz	-	-	0.1	%
S/N(A)	signal-to-noise ratio	A-weighted; $V_{27,28}$ = –6 dBV	80	-	-	dB
$\alpha_{L/R}$, $\alpha_{R/L}$	crosstalk	f = 1 kHz	-	80	-	dB
Input selector control circuit (pins 3 and 5; see also Logic Table 1) and secondary channels PLLs disable (SCD pin 11); pins 3, 5 and 11 left open = logic HIGH						
V_{IL}	LOW level input voltage		0	-	1.5	V
V_{IH}	HIGH level input voltage		3.5	-	V_P	V
$R_{3.5.11}$	input resistance	connected to V_P	70	100	130	kΩ
Output selector control circuit (see also Logic Table 2) and main channel PLL lock-in range select (MCS pin 7); pins 15, 17, 26, 13 and 7 MOST inputs, should not be left open						
V_{IL}	LOW level input voltage		0	-	1.5	V
V_{IH}	HIGH level input voltage		3.5	-	V_P	V
I_{IL}	LOW level input current	V_{IL} = 0 V	-	<–1	-	µA
I_{IH}	HIGH level input current	V_{IH} = 5 V	-	<1	-	µA

Notes to the AC characteristics

1. At pin 20 the demodulated 1 kHz signal should be present with a typical level of 158 mV (RMS) (–16 dBV), and THD of max. 0.5 %; 8 V < V_P < 13.2 V; 0 °C < T_{amb} < 70 °C.
2. Modulation of main channel is off; modulation of secondary channels is on.
3. The electrolytic capacitors at pins 40 and 42 are removed and 1500 pF capacitors between pin 40 and ground and between pin 42 and ground are connected. At pins 40 and 42 the demodulated 1 kHz signals should be present with typical levels of 7 mV (RMS) and THD of max. 0.5 % ; 8 V < V_P < 13.2 V; 0 °C < T_{amb} < 70 °C.
4. All PLLs locked; R_{S1}= R_{S2} = 470 Ω.
5. Modulation of secondary channel being measured and main channel is off; modulation of other secondary channel is on.
6. Modulation of main channel is on; modulation of secondary channels is off.
7. Measured at pins 38 (left) and 30 (right) and no electrolytic capacitors connected to these pins.

LOGIC TABLES

Table 1 Truth table for input selector

SWITCH POSITION	STATE	PIN 3	PIN 5
1	pins 2 and 10 (IN-A)	0	0
2	pins 4 and 12 (IN-B)	0	1
3	pins 6 and 14 (IN-C)	1	0
4	pins 8 and 16 (IN-D)	1	1

Table 2 Truth table for output selector

SWITCH POSITION	STATE	PIN 15	PIN 17	PIN 26	PIN 13
		OUTSEL L	OUTSEL R	EXT/INT	MUTE
1	stereo	1	1	0	0
2	left	1	0	0	0
3	right	0	1	0	0
4	main	0	0	0	0
5	external	X	X	1	0
6	mute secondary	X	X	0	1
7	mute all	X	X	1	1

X = don't care.

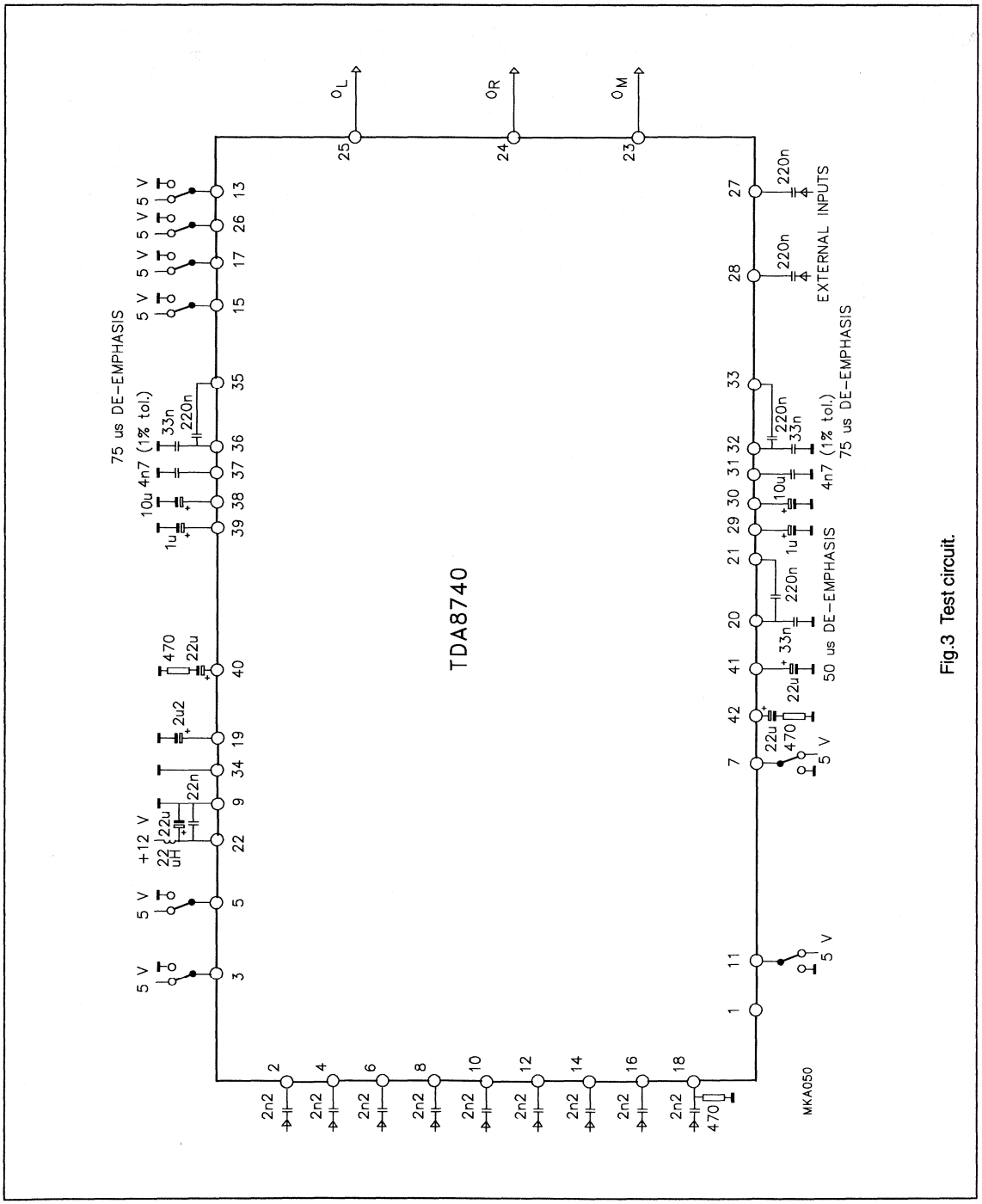


Fig.3 Test circuit.

APPLICATION INFORMATION

MCS (pin 7) = '0' (Fig. 4):

The lock-in range of the main channel PLL is 5.5 to 7.5 MHz. The satellite baseband signal is routed to nine bandpass filters: eight for the secondary channels and one for the main channel. For the secondary channels the bandpass filter terminating resistors are integrated on-chip (330 Ω typically) so no external terminating resistors are required. For the main channel this is not done. Filters with different characteristics can be used here.

MCS (pin 7) = '1' (Fig. 5):

The lock-in range of the main channel PLL is now 10.0 to 11.5 MHz. The carrier frequency for the main channel is transferred to 10.7 MHz by an external frequency synthesizer and mixer; e.g., if a 6.65 MHz carier is to be demodulated this frequency is mixed to 10.7 MHz by tuning the frequency synthesizer to 17.35 MHz. If the synthesizer is tuned to 17.20 MHz a 6.5 MHz carrier can be demodulated.
In this case the main audio output level should be adjusted to −6 dBV by inserting a 680 Ω resistor in series with the electrolytic capacitor on pin 41.

For the main channel the baseband signal is routed to the mixer, and to eight ceramic bandpass filters for the secondary channels.
For high-end applications the input level of the NR can be adjusted to give optimal performance. 0 dB is the maximum input level which corresponds to the maximum frequency deviation of the incoming FM signal (50 kHz for secondary channels). If the NR input signal is too low (high) the NR will attenuate (favour) the higher audio frequencies too much due to the expansion character. In general: 1 dB error in NR input level will give a 1 dB difference between low (50 Hz) and high (15 kHz) audio frequencies. With R_{S1} (R_{S2}) the input level and so the frequency response of the NR can be adjusted: at **0 dB input level** (which corresponds to a frequency deviation of 50 kHz) the output level of an 15 kHz modulated signal should be 0.25 dB lower than that of an 50 Hz modulated signal.

If only the main channel is to be demodulated the PLLs of the secondary channels can be disabled by making SCD (pin 11) logic '1'.

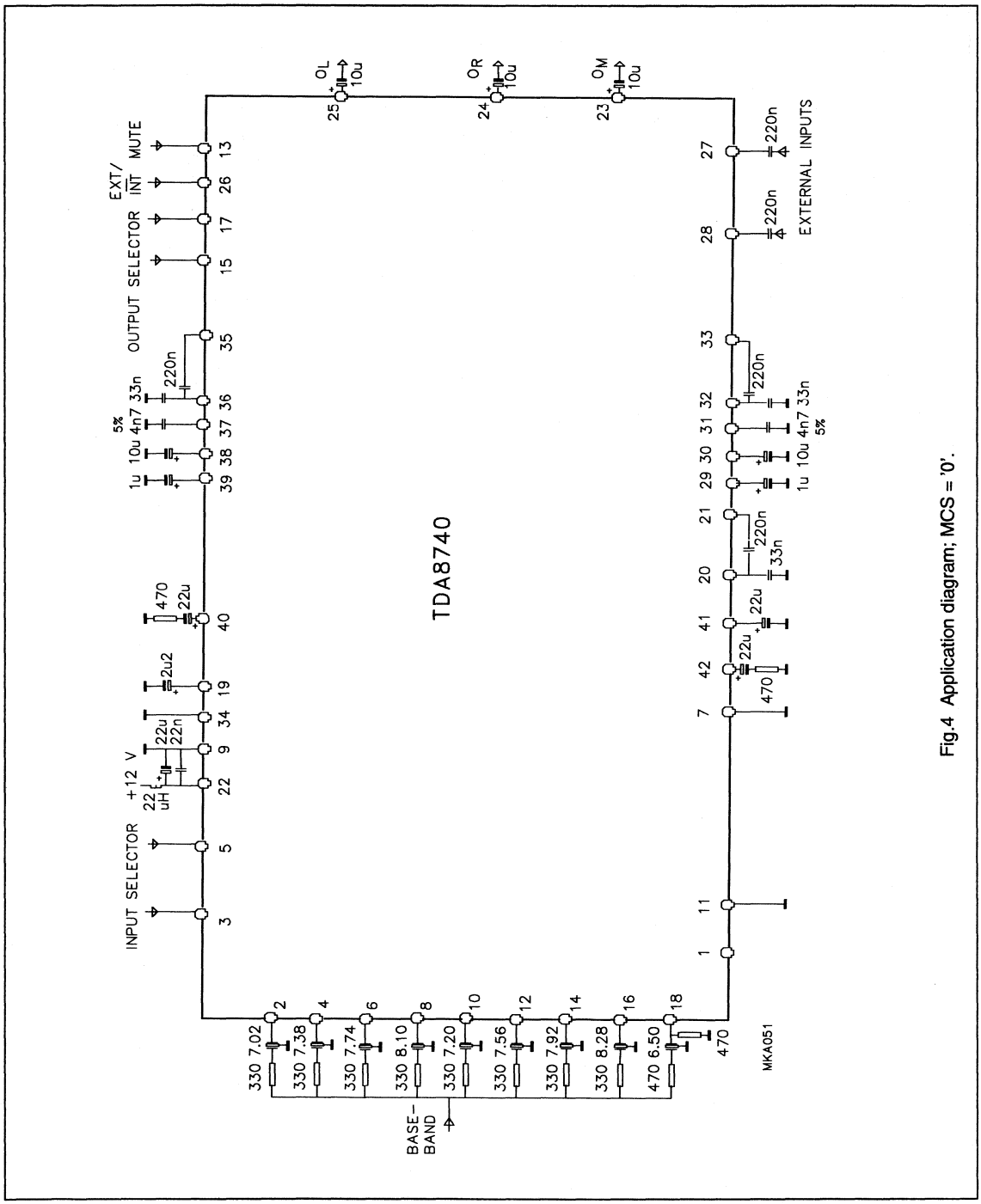


Fig.4 Application diagram; MCS = '0'.

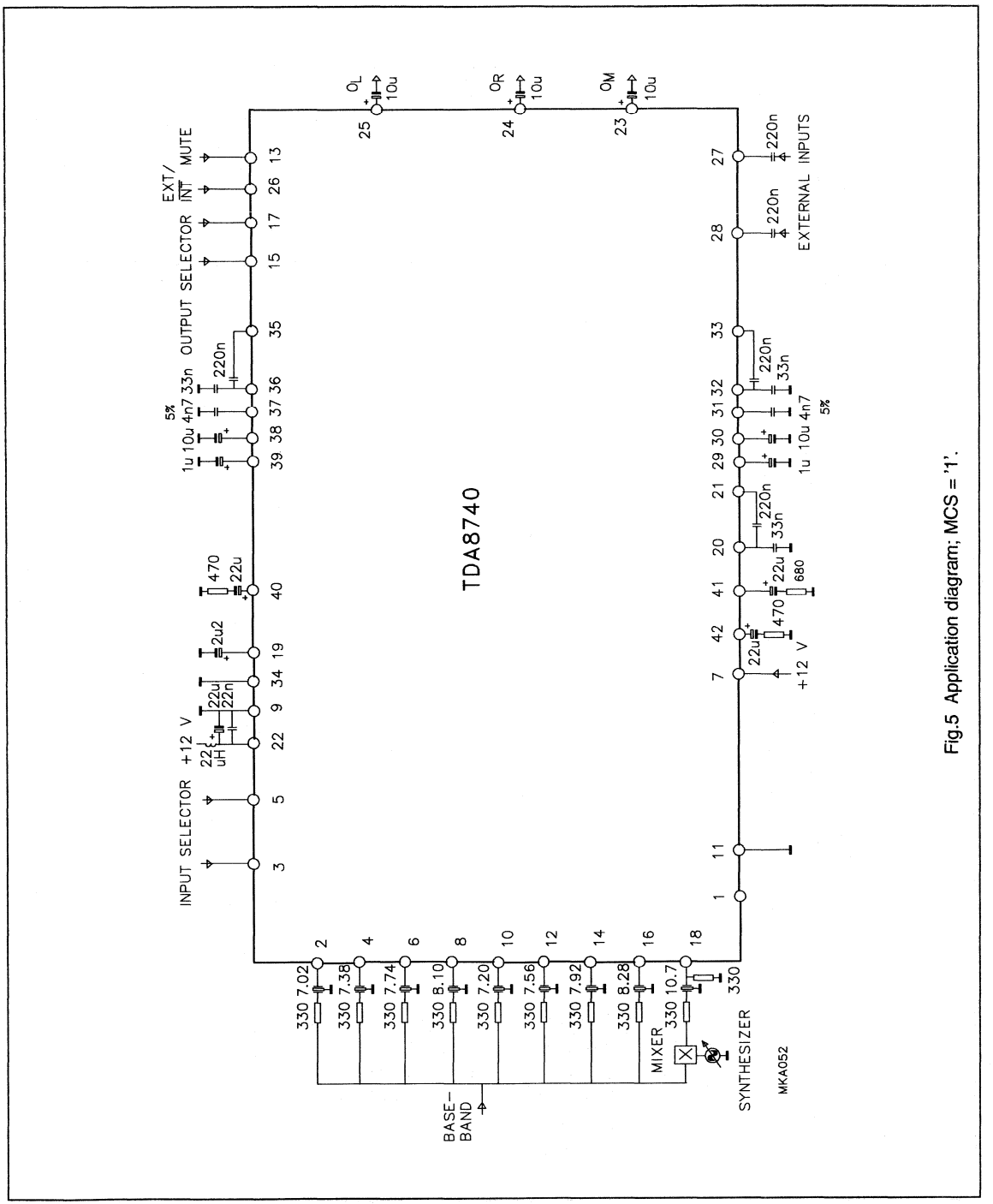


Fig.5 Application diagram; MCS = '1'.

Satellite sound circuit with noise reduction TDA8741

FEATURES

- Demodulation of main audio signal by means of wide band PLL (lock range selectable)
- Demodulation of secondary audio signals by means of wide band PLL
- Noise reduction of the secondary audio signals
- Output selection: stereo, language 1, language 2, main audio, external
- Mute control
- Line outputs (SCART level)

APPLICATIONS

- Satellite receivers
- TV sets
- Video recorders

GENERAL DESCRIPTION

The TDA8741 is a multi-function sound IC for use in satellite receivers, television sets and video recorders.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	operating supply voltage		8	12	13.2	V
Main channel						
$V_{18(RMS)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	-	1.0	2.0	mV
Δf_{OM}	lock range PLL demodulator	either: or:	5.5 10.0	- -	7.5 11.5	MHz MHz
V_{23}	output voltage		–8	–6	–4	dBV
S/N(A)	signal-to-noise ratio	A-weighted	62	70	-	dB
Secondary channels						
$V_{8,16(RMS)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	-	0.8	1.5	V
$\Delta f_{OS1;\ 2}$	lock range PLL demodulators		10.0	-	11.5	MHz
$V_{24,\ 25}$	output voltage		–8	–6	–4	dBV
S/N(A)	signal-to-noise ratio	A-weighted	72	80	-	dB
Crosstalk						
$\alpha_{S/M}$	crosstalk from secondary to main channel		-	74	-	dB
$\alpha_{M/S}$	crosstalk from main to secondary channel		-	74	-	dB
$\alpha_{S/S}$	crosstalk between secondary channels		-	74	-	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8741	42	SDIL	plastic	SOT270

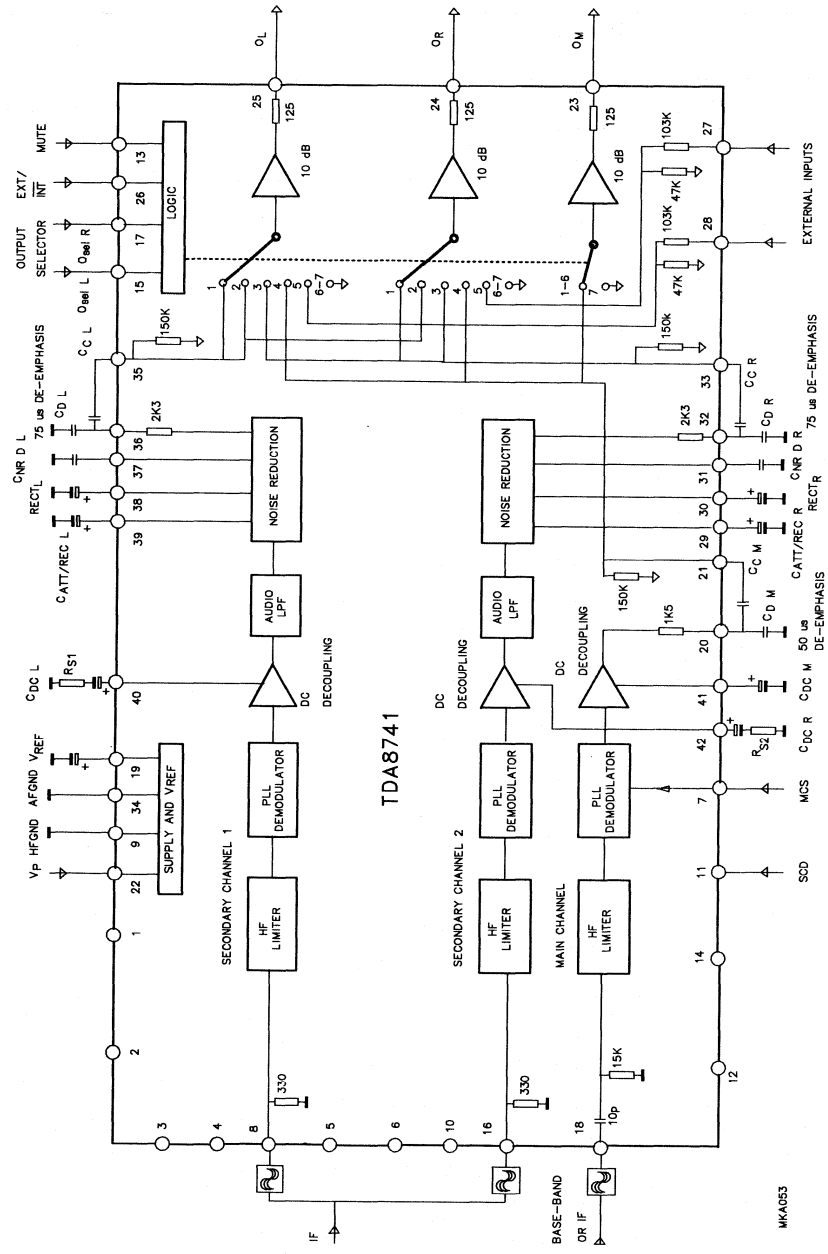


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
n.c.	3	not connected
n.c.	4	not connected
n.c.	5	not connected
n.c.	6	not connected
MCS	7	main channel PLL lock-in range select
IN-1	8	intercarrier input for secondary channel 1 (left)
HFGND	9	ground for HF section
n.c.	10	not connected
SCD	11	secondary channels PLLs disable
n.c.	12	not connected
MUTE	13	mute switch
n.c.	14	not connected
$O_{sel\ L}$	15	output select switch bit 1 (left)
IN-2	16	intercarrier input for secondary channel 2 (right)
$O_{sel\ R}$	17	output select switch bit 2 (right)
IN-3	18	intercarrier input for main channel
V_{REF}	19	decoupling capacitor for reference voltage
$C_{D\ M}$	20	de-emphasis capacitor for main channel
$C_{C\ M}$	21	audio pass-through capacitor input for main channel
V_P	22	positive supply voltage
O_M	23	main channel output
O_R	24	right channel output
O_L	25	left channel output
EXT/INT	26	output switch bit 3 (external/internal)
EXT_R	27	external audio input (right)
EXT_L	28	external audio input (left)
$C_{ATT/REC\ R}$	29	attack/recovery capacitor (right)
$RECT_R$	30	rectifier DC decoupling (right)
$C_{NR\ D\ R}$	31	noise reduction de-emphasis capacitor (right)
$C_{D\ R}$	32	fixed de-emphasis capacitor (right)
$C_{C\ R}$	33	audio pass-through capacitor input for right channel
AFGND	34	ground for AF section
$C_{C\ L}$	35	audio pass-through capacitor input for left channel
$C_{D\ L}$	36	fixed de-emphasis capacitor (left)
$C_{NR\ D\ L}$	37	noise reduction de-emphasis capacitor (left)
$RECT_L$	38	rectifier DC decoupling (left)

SYMBOL	PIN	DESCRIPTION
$C_{ATT/REC\ L}$	39	attack/recovery capacitor (left)
$C_{DC\ L}$	40	DC decoupling capacitor (left)
$C_{DC\ M}$	41	DC decoupling capacitor (main)
$C_{DC\ R}$	42	DC decoupling capacitor (right)

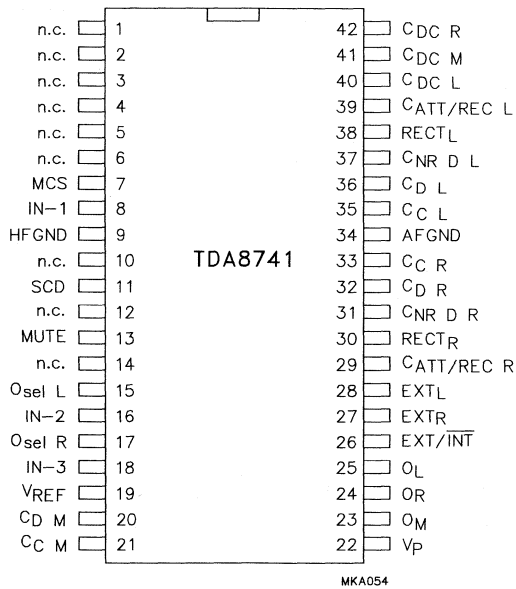


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Satellite sound

The baseband signal coming from a satellite tuner comprises the demodulated video signal and a number of sound carriers in case of reception of a PAL/NTSC/SECAM satellite signal.
Nearest to the video is the main sound carrier. It carries the mono sound related to the video. This is a FM modulated carrier with a fixed pre-emphasis. This carrier frequency can be in the range of 5.8 to 6.8 MHz. Furthermore a number of optional secondary sound carriers may be present. These can be used for stereo- or multi language sound related to the video, or for unrelated radio sound. These carriers are also FM modulated, but for better sound quality (improved signal-to-noise performance) broadcast satellites (e.g. 'ASTRA') use a noise reduction system (adaptive pre-emphasis circuit, combined with a fixed pre-emphasis).

These carrier frequencies can be in the range of 6.30 to 8.28 MHz. For accurate tuning to the many sound carriers an external frequency synthesizer and mixer is used to transfer the sound carriers to intermediate frequencies of 10.7 and 10.52 MHz. The TDA8741 holds all circuitry for the processing of the main channel and of two secondary channels, from IF signal-to-line (SCART) output drivers. By means of band pass filtering the desired frequencies can be routed to the TDA8741.

Main channel (see Fig. 1, block diagram)

The lock-in range of the main channel PLL can be switched between 5.5 to 7.5 MHz and 10.0 to 11.5 MHz by means of the MCS signal at pin 7. (Pin 7 is logic '0' : lock-in range is 5.5 to 7.5 MHz and pin 7 is logic '1' : lock-in range 10.0 to 11.5 MHz).
If only one fixed carrier frequency for the main channel is to be demodulated (e.g. 6.5 MHz), the lock-in range of the PLL should be switched to 5.5 to 7.5 MHz. The baseband signal is applied to the main channel input, pin 18 via a 6.5 MHz ceramic bandpass filter. If on the other hand it is desired to demodulate different main channel frequencies, these frequencies can be transferred to a fixed intermediate frequency (e.g. 10.7 MHz) using an external mixer and oscillator-frequency synthesizer. In that case the lock-in range of the PLL should be switched to 10.0 to 11.5 MHz. The IF signal is applied to the main channel input, pin 18 via a 10.7 MHz ceramic bandpass filter.

The filtered signal is AC-coupled to a limiter/amplifier and then to a PLL demodulator. The PLL FM demodulator ensures that the demodulator is alignment free. High amplification and DC error signals of the PLL which are superimposed on the demodulator output require DC decoupling. A buffer amplifier amplifies the signal to the same level as that of the secondary channels and decouples DC by means of an electrolytic capacitor connected to pin 41. The demodulator output signal is fed to pin 20 via an internal resistor. The output signal can be de-emphasized by means of this resistor and an external capacitor to ground. Capacitor value = de-emphasis time constant/1500. (for 50 µs: 33 nF). From here the signal is fed to the output selectors. The signal is amplified to 500 mV (RMS) (i.e. –6 dBV) in the output amplifiers.

Secondary channels

An external mixer and oscillator frequency synthesizer transfers the secondary sound carriers to fixed intermediate frequencies e.g. 10.7 and 10.52 MHz. Two secondary channel inputs are available (pins 8 and 16). External ceramic bandpass filters tuned to the desired intermediate frequencies, route these signals to the inputs.
For stereo purpose the TDA8741 contains two identical secondary sound processing channels. (secondary channel 1 will also be referred to as 'LEFT' or 'LANGUAGE 1' and secondary channel 2 will also be referred to as 'RIGHT' or 'LANGUAGE 2') .

From the inputs the signals are coupled to limiter/amplifiers and then to the PLL demodulators. Processing is similar to the main channel. The demodulator output signal is amplified in a buffer amplifier and DC decoupled by means of electrolytic capacitors connected to pins 40 (left) and 42 (right). Output level is set with a resistor in series with the capacitor.

High frequency components in the amplified PLL output are filtered out in the audio LPF block (4th order butterworth low pass filter) to prevent unwanted influence on the noise reduction.

NOISE REDUCTION (NR)

The NR can be regarded as an input level dependent low-pass filter (adaptive de-emphasis system) followed by a fixed de-emphasis. With maximum input level (= 0 dB) the frequency response of the first part (i.e. without the fixed de-emphasis) is nearly flat. As the input level is x-dB lowered, the higher output frequencies will be reduced an extra x-dB w.r.t. to the lower frequencies. (1 : 2 expansion).

The NR output signal is fed to pin 36 (left) and pin 32 (right) via an internal resistor.

Fixed de-emphasis is achieved by these resistors and external capacitors to ground.
The signals are DC decoupled via pins 36/35 and 32/33 and then routed to the output selectors.

OUPUT SELECTION

With the ouput selector (see Logic Table) the outputs (pin 25 and 24) can be switched to the different channels. Both outputs can be switched to both secondary channels, to the main channel and to the external inputs (pin 28 and 27) for IC chaining purposes.

Pin 23 is a separate output which delivers the main channel only, creating the possibility to have three different output channels simultaneously e.g. for use in HiFi VCR's.

Outputs 25 and 24 can be muted by setting the MUTE signal (pin 13) logic '1' (switch positions 6 and 7).

Output 23 can be muted by setting the MUTE signal and the EXT/INT signal (pin 26) both logic '1' (switch position 7).

All outputs (pins 23, 24 and 25) are line drivers with scart level capability and are short-circuit protected by 125 Ω output resistors.

Output level of all channels = –6 dBV typical when frequency deviation of FM signal is 54% of maximum frequency deviation (i.e. 0.54 x 85 kHz = 46 kHz for the main channel and 0.54 x 50 kHz = 27 kHz for the secondary channels) at 1 kHz modulation frequency (reference level).

ABBREVIATIONS

f_{MOD} = modulating frequency
Δf_M = frequency deviation of the main channel
Δf_{S1} = frequency deviation of secondary channel 1 (left)
Δf_{S2} = frequency deviation of secondary channel 2 (right)
f_{OM} = carrier frequency of main channel
f_{OS1} = carrier frequency of secondary channel 1
f_{OS2} = carrier frequency of secondary channel 2
LPF = Low-Pass Filter
NR = Noise Reduction
PLL = Phase-Locked-Loop

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (note 1)	0	13.2	V
V_x	voltage on any pin (note 1)	0	V_P	V
T_{stg}	storage temperature range	–65	+150	°C
T_{amb}	operating ambient temperature range	–20	+70	°C

Note to the limiting values

1. All voltages with reference to ground (pins 9 and 34).

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient	53 K/W

CHARACTERISTICS

All voltages with reference to ground (pins 9 and 34)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 22)		8	12	13.2	V

DC CHARACTERISTICS

All voltages with reference to ground (pins 9 and 34)
Measured in test set-up Fig. 3; V_P = 12 V; T_{amb} = 25 °C; $\Delta f_M = \Delta f_{S1} = \Delta f_{S2}$ = 0 kHz (no modulation); f_{OM} = 6.5 MHz; f_{OS1} = 10.7 MHz; f_{OS2} = 10.52 MHz; HF level at pin 18: 40 mV (RMS); HF level at pins 8 and 16: 20 mV (RMS); MCS = '0' (V_7 = 0 V); SCD = '0' (V_{11} = 0 V); unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_P	supply current		-	38	45	mA
P_{tot}	total power dissipation		-	-	600	mW
$V_{23.24.25}$	voltage on pin 23, 24 and 25		-	3.8	-	V
$V_{27.28}$	voltage on pins 27 and 28		-	3.8	-	V
$V_{33.35}$	voltage on pins 33 and 35		-	3.8	-	V
$V_{32.36}$	voltage on pins 32 and 36		-	3.8	-	V
$V_{30.38}$	voltage on pins 30 and 38		-	3.8	-	V
V_{21}	voltage on pin 21		-	3.8	-	V
V_{20}	voltage on pin 20		-	3.8	-	V
V_{19}	voltage on pin 19		3.7	3.8	3.9	V
$V_{8.16}$	voltage on pins 8 and 16		-	0	-	V
$V_{40.42}$	voltage on pins 40 and 42		-	3.0	-	V
V_{41}	voltage on pin 41		-	2.8	-	V
I_{18}	input current at pin 18		-	-	1	µA

AC CHARACTERISTICS

All voltages with reference to ground (pins 9 and 34)

Measured in test set-up Fig. 3; V_P = 12 V; T_{amb} = 25 °C; f_{MOD} = 1 kHz; f_{OM} = 6.5 MHz; Δf_M = 46 kHz; $\Delta f_{S1} = \Delta f_{S2}$ = 27 kHz (reference levels); f_{OS1} = 10.7 MHz; f_{OS2} = 10.52 MHz; HF level at pin 18: 40 mV (RMS); HF level at pins 8 and 16: 20 mV (RMS); MCS = '0' (V_7 = 0 V); SCD = '0' (V_{11} = 0 V); unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Main channel - HF input (pin 18) and limiter						
$V_{18(RMS)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	-	1.0	2.0	mV
$V_{18(RMS)}$	input signal (RMS value)		-	-	200	mV
R_{18}	input resistance		-	15	-	kΩ
Main channel - PLL FM demodulator and DC decoupling amplifier						
f_{CCO}	free-running frequency		-	6.5	-	MHz
f_{CCO}	free-running frerquency	MCS = '1'	-	10.7	-	MHz
Δf_{OM}	lock-in range of PLL	note 1	5.5	-	7.5	MHz
Δf_{OM}	lock-in range of PLL	MCS = '1'; note 1	10.0	-	11.5	MHz
R_{20}	output resistance for 50 µs de-emphasis (pin 20)		1.3	1.5	1.7	kΩ
V_{20}	output voltage (pin 20)		−17.5	−16.0	−14.5	dBV
ΔV_{20}	spread of PLL output voltage over lock range		-	-	±1	dB
R_{21}	input resistance of output amplifier (pin 21)		100	150	200	kΩ
Main channel - overall performance (output selector in position 4)						
$V_{23,24,25}$	output voltage	all PLLs locked	−8	−6	−4	dBV
THD	total harmonic distortion	all PLLs locked	-	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; all PLLs locked	62	70	-	dB
$V_{23(15\ kHz)}/V_{23(1\ kHz)}$	15 kHz frequency response with respect to 1 kHz	no de-emphasis connected	−0.5	0	+0.5	dB
$R_{23,24,25}$	output resistance		100	125	150	Ω
$\alpha_{S/M}$	crosstalk attenuation from secondary channels to main	note 2	-	74	-	dB
α_M	mute attenuation	output selector in position 7	74	-	-	dB
RR	supply voltage ripple rejection	V_{RR} = tbf V; f = tbf Hz	-	tbf	-	dB
Secondary channels 1 and 2 - HF inputs (pins 8 and 16) and limiters						
$V_{8,16(RMS)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	-	0.8	1.5	mV
$V_{8,16(RMS)}$	input signal (RMS value)		-	-	200	mV
$R_{8,16}$	input resistance		280	330	380	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Secondary channels 1 and 2 - PLL FM demodulators						
f_{CCO1}	free running frequency PLL1		-	10.7	-	MHz
f_{CCO2}	free running frequency PLL2		-	10.52	-	MHz
$\Delta f_{OS1/2}$	lock range of PLL's	note 3	10	-	11.5	MHz
$R_{S1,S2}$	series resistances for optimal frequency response adjustment		0	1.0	2.2	kΩ
$V_{40,42(RMS)}$	PLL output voltage (RMS value); pins 40 and 42	pins 40 and 42 to be left open-circuit	tbf	9	tbf	mV
$\Delta V_{40,42}$	spread of PLL output voltage over lock range		-	-	±1	dB
Secondary channels - overall performance of LPF and NR (output selectors in position 1)						
$R_{36,32}$	output resistance for 75 µs de-emphasis (pins 36 and 32)		2.0	2.3	2.6	kΩ
$R_{35,33}$	input resistance of output amplifiers (pins 35 and 33)		100	150	200	kΩ
$V_{25,24}$	output voltage (pins 25 and 24)	note 4	–8	–6	–4	dBV
THD	total harmonic distortion	note 4	-	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; note 4	72	80	-	dB
$R_{25,24}$	output resistance (pins 25 and 24)	note 4	100	125	150	Ω
α_M	mute attenuation	output selector in position 6; note 4	74	-	-	dB
$\alpha_{S/S}$	crosstalk attenuation between secondary channels	note 5	-	74	-	dB
$\alpha_{M/S}$	crosstalk attenuation from main channel to secondary	note 6	-	74	-	dB
$V_{offset(DC)}$	offset voltage on attack/recovery capacitors (pins 39 and 29); DC value	all PLLs locked; $\Delta f = 0$	14	16	18	mV
RR	supply voltage ripple rejection	V_{RR} = tbf V; f = tbf Hz	-	tbf	-	dB
Secondary channels - low-pass filter						
$V_{38,30(50\ kHz)}/V_{38,30(1\ kHz)}$	50 kHz frequency response with respect to 1 kHz	note 7	–21	–16	–11	dB
Secondary channels - noise reduction						
$V_{25,24}$	output voltage (pins 25 and 24) at 0 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2}$ = 50 kHz; no fixed de-emphasis connected; note 4	–1	+1	+3	dBV
$V_{25,24(15\ kHz)}/V_{25,24(1\ kHz)}$	15 kHz frequency response with respect to 1 kHz at 0 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2}$ = 50 kHz; no fixed de-emphasis connected; note 4	–2	0	+2	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Secondary channels - noise reduction						
$V_{25,24}$	output voltage (pins 25 and 24) at –20 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2}$ = 5 kHz; no fixed de-emphasis connected; note 4	–29	–26	–23	dBV
$V_{25,24(15\ kHz)}/V_{25,24(1\ kHz)}$	15 kHz frequency response with respect to 1 kHz at –20 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2}$ = 5 kHz; no fixed de-emphasis connected; note 4	–13	–11.5	–10	dB
External inputs - pin 28 (left) and pin 27 (right) - overall performance (output selector in position 5)						
$V_{27,28}$	input signal		-	-	6	dBV
$R_{27,28}$	input resistance		100	150	200	kΩ
$V_{25,24}$	output level	$V_{27,28}$ = –6 dBV	–6.5	–6.0	–5.5	dBV
THD	total harmonic distortion	$V_{27,28}$ = –6 dBV f = 1 kHz	-	-	0.1	%
S/N(A)	signal-to-noise ratio	A-weighted; $V_{27,28}$ = –6 dBV	80	-	-	dB
$\alpha_{L/R}$, $\alpha_{R/L}$	crosstalk	f = 1 kHz	-	80	-	dB
Secondary channels PLL's disable (SCD pin 11); pin 11 left open = logic HIGH						
V_{IL}	LOW level input voltage		0	-	1.5	V
V_{IH}	HIGH level input voltage		3.5	-	V_P	V
R_{11}	input resistance	connected to V_P	70	100	130	kΩ
Output selector control circuit (see also Logic Table) and main channel PLL lock-in select (MCS pin 7); pins 15, 17, 26, 13 and 7 MOST inputs, should not be left open						
V_{IL}	LOW level input voltage		0	-	1.5	V
V_{IH}	HIGH level input voltage		3.5	-	V_P	V
I_{IL}	LOW level input current	V_{IL} = 0 V	-	<–1	-	μA
I_{IH}	HIGH level input current	V_{IH} = 5 V	-	<1	-	μA

Notes to the AC characteristics

1. At pin 20 the demodulated 1 kHz signal should be present with a typical level of 158 mV (RMS) (–16 dBV), and THD of max. 0.5 %; 8 V < V_P < 13.2 V; 0 °C < T_{amb} < 70 °C.
2. Modulation of main channel is off; modulation of secondary channels is on.
3. The electrolytic capacitors at pins 40 and 42 are removed and 1500 pF capacitors between pin 40 and ground and between pin 42 and ground are connected. At pins 40 and 42 the demodulated 1 kHz signals should be present with typical levels of 9 mV (RMS) and THD of max. 0.5 % ; 8 V < V_P < 13.2 V; 0 °C < T_{amb} < 70 °C.
4. All PLLs locked; R_{S1}= R_{S2} = 1 kΩ.
5. Modulation of secondary channel being measured and main channel is off; modulation of other secondary channel is on.
6. Modulation of main channel is on; modulation of secondary channels is off.
7. Measured at pins 38 (left) and 30 (right) and no electrolytic capacitors connected to these pins.

LOGIC TABLE

Table 1 Truth table for output selector

SWITCH POSITION	STATE	PIN 15	PIN 17	PIN 26	PIN 13
		OUTSEL L	OUTSEL R	EXT/INT	MUTE
1	stereo	1	1	0	0
2	left	1	0	0	0
3	right	0	1	0	0
4	main	0	0	0	0
5	external	X	X	1	0
6	mute secondary	X	X	0	1
7	mute all	X	X	1	1

X = don't care.

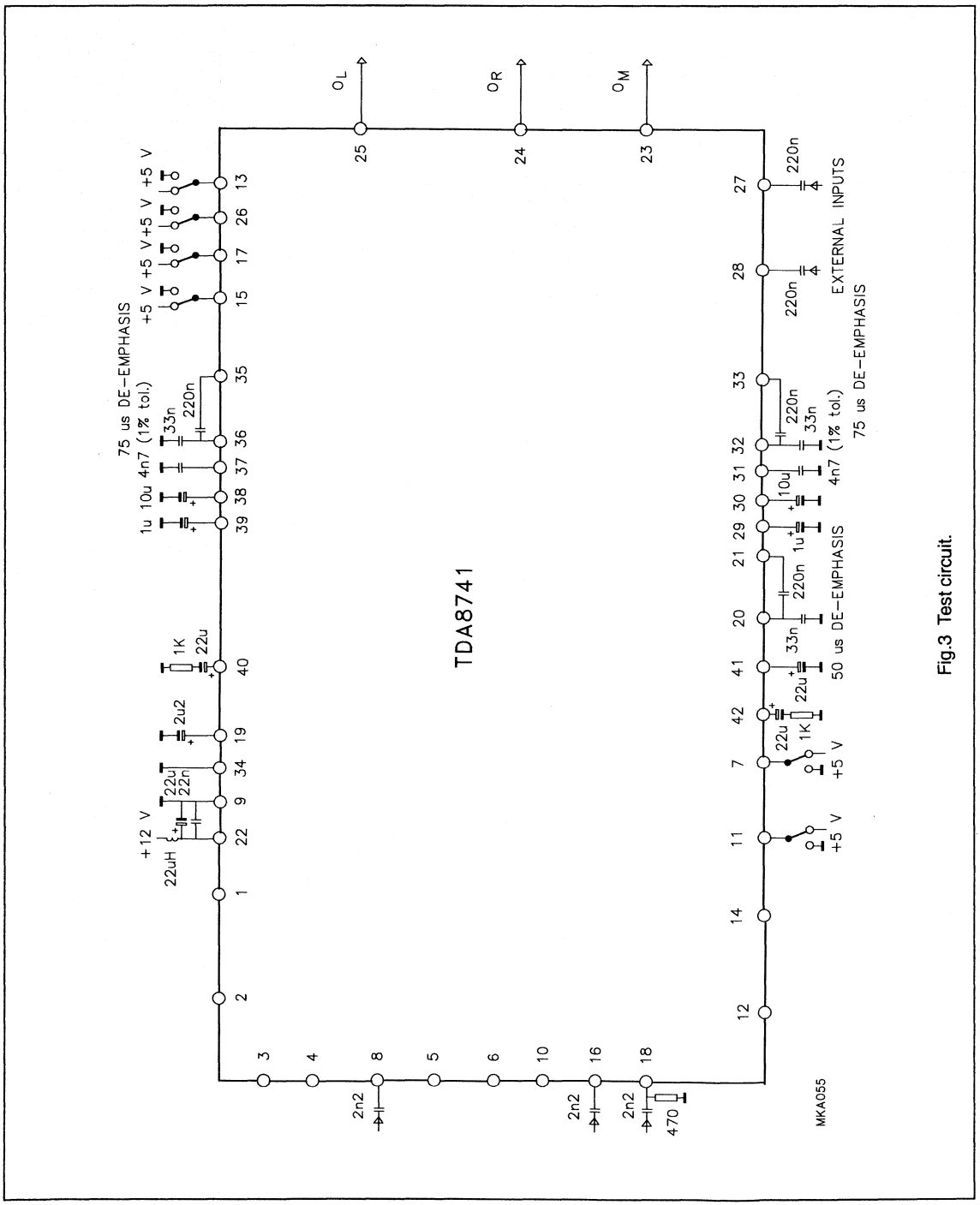


Fig.3 Test circuit.

APPLICATION INFORMATION

The satellite baseband signal is routed to a mixer to transfer the various secondary channels to fixed intermediate frequencies of 10.7 and 10.52 MHz. Tuning to the desired carrier frequencies can be achieved by varying the oscillator frequency; e.g. tuning to 7.02 and 7.20 MHz carrier frequencies requires an oscillator frequency of 17.72 MHz and tuning to 7.38 and 7.56 MHz requires an oscillator frequency of 18.08 MHz. The IF signals are routed to the inputs (pin 8 and 16) via 10.7 and 10.52 MHz ceramic bandpass filters. For the secondary channels the bandpass filter terminating resistor are integrated on the chip (330 Ω typical) so no external resistors are required.

MCS (pin 7) = '0' (Fig. 4):

The lock-in range of the main channel PLL is 5.5 to 7.5 MHz. For the main channel a ceramic bandpass filter (e.g. 6.5 MHz) is used to filter out the main sound carrier directly from the baseband signal. Simultaneous demodulation of one main channel and various secondary channels is now possible with a minimum of external components. As no bandpass filter terminating resistor for the main channel (pin 18) is integrated on-chip, an external resistor is required.

MCS (pin 7) = '1' (Fig 5):

The lock-in range of the main channel PLL is now 10.0 to 11.5 MHz. The carrier frequency of the main channel is also transferred to a fixed intermediate frequency. In this case the main audio output level should be adjusted to –6 dBV by inserting a 680 Ω resistor in series with the electrolytic capacitor on pin 41.

If simultaneous demodulation of main- and secondary sound carriers is not required, a low cost solution as given in Fig. 5 can be considered. One mixer and frequency synthesizer are used to transfer all sound carriers to intermediate frequencies of 10.7 and 10.52 MHz. When the bandwith of the main channel is larger than the secondary channel bandwidth, a separate (e.g. 10.7 MHz) ceramic filter plus resistors are required for the main channel.
The secondary sound carriers can be demodulated as described above. If e.g. a 6.65 MHz main sound carrier is to be demodulated, this frequency is mixed to 10.7 MHz by tuning the frequency synthesizer to 17.35 MHz. If the synthesizer is tuned to 17.20 MHz a 6.5 MHz main sound carrier can be demodulated. When main sound is to be demodulated and this IF signal is also available on the secondary channel 1 input the PLLs of the secondary channels can be disabled by making SCD (pin 11) 'HIGH'. The ouput selector should be in position 4 (main sound on all outputs) if output pins 25 and 24 are used.

For high-end applications the input level of the NR can be adjusted to give optimal performance. 0 dB is the maximum input level which corresponds to the maximum frequency deviation of the incoming FM signal (50 kHz for secondary channels). If the NR input signal is too low (high) the NR will attenuate (favour) the higher audio frequencies too much due to the expansion character. In general: 1 dB error in NR input level will give a 1 dB difference between low (50 Hz) and high (15 kHz) audio frequencies. With R_{S1} (R_{S2}) the input level and so the frequency response of the NR can be adjusted: at **0 dB input level** (which corresponds to a frequency deviation of 50 kHz) the output level of an 15 kHz modulated signal should be 0.25 dB lower than that of an 50 Hz modulated signal.

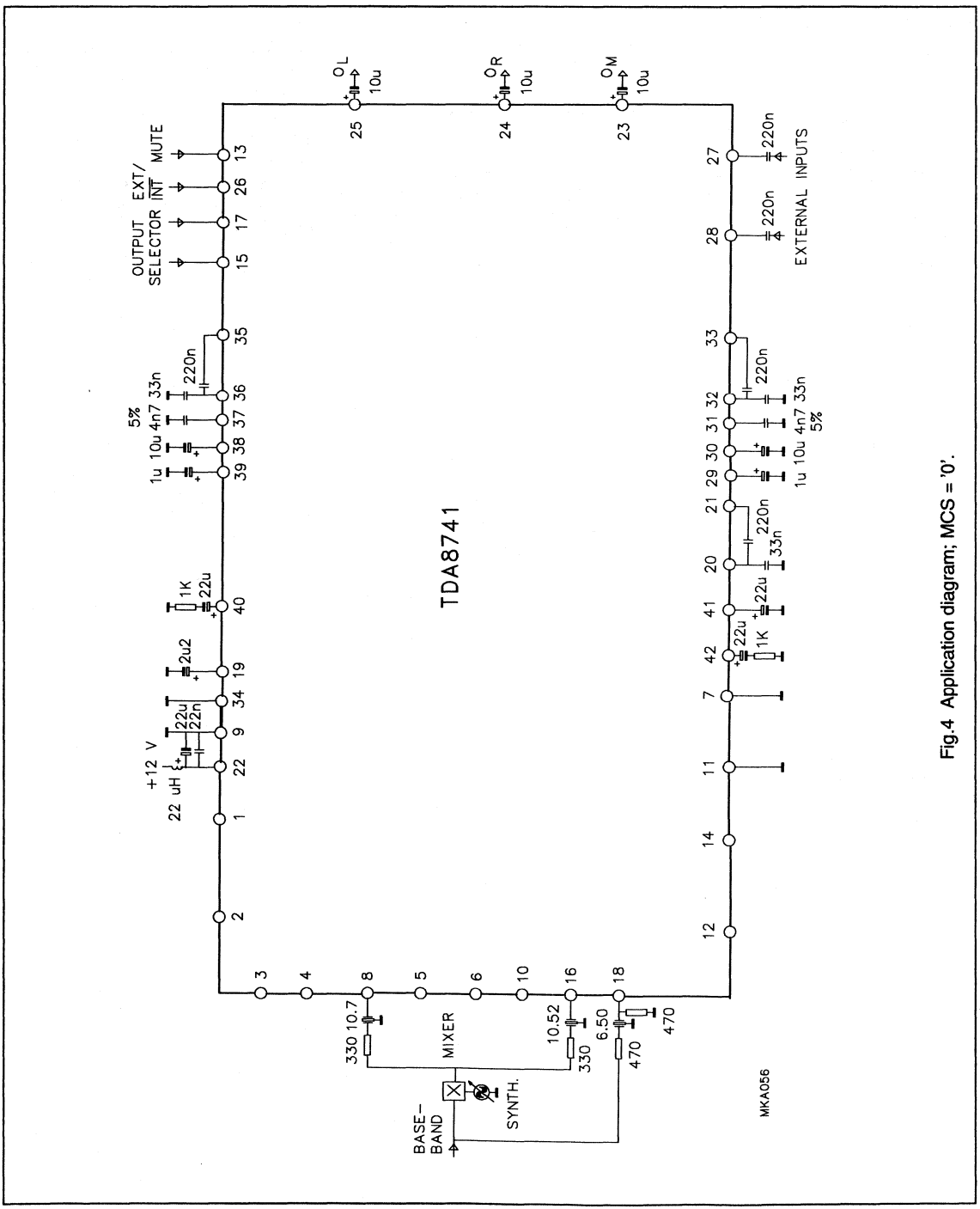


Fig.4 Application diagram; MCS = '0'.

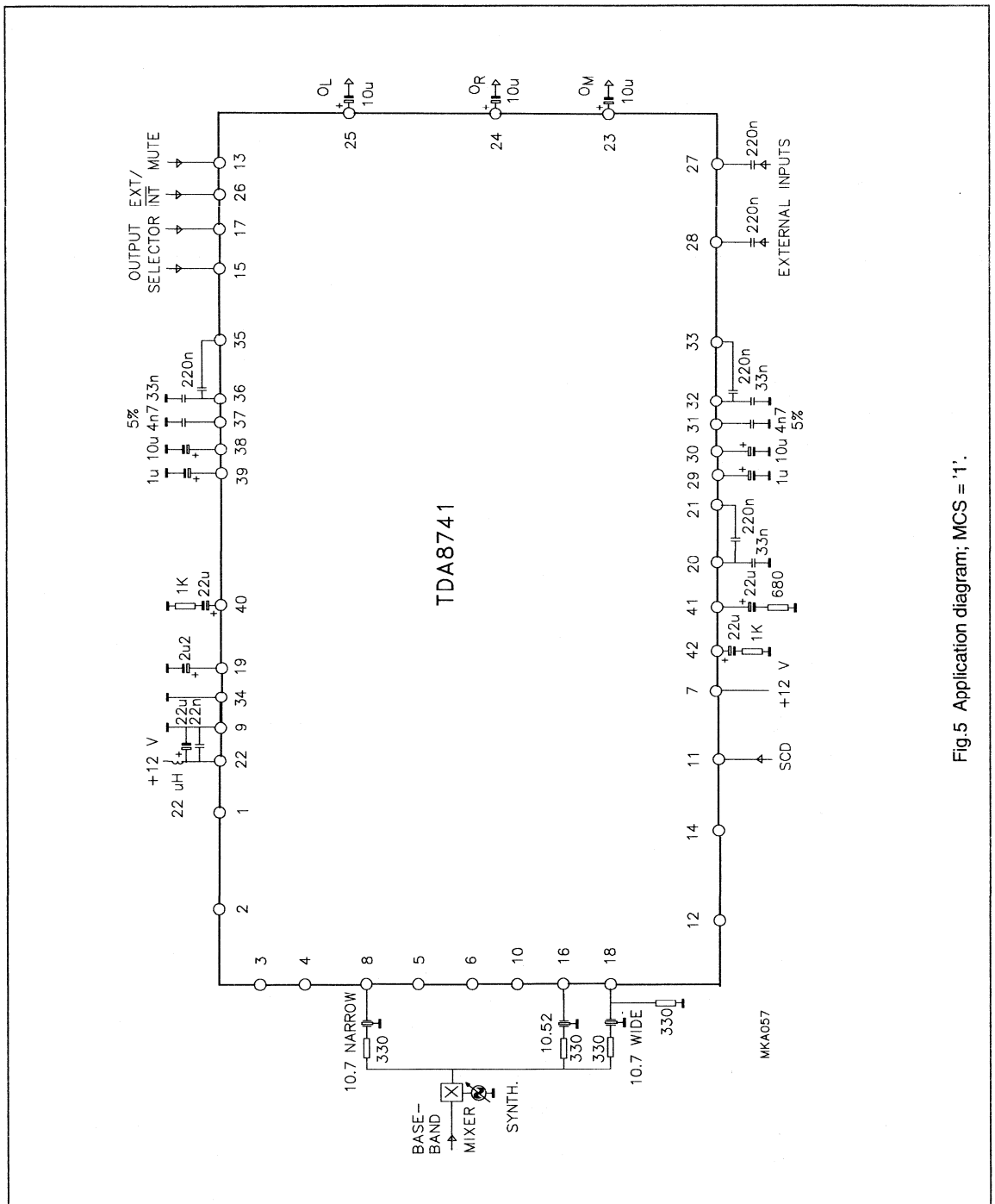


Fig.5 Application diagram; MCS = '1'.

Triple 8-bit video digital-to-analog converter

TDA8771

FEATURES

- 8-bit resolution
- Sampling rate up to 35 MHz
- Internal reference voltage generator
- No deglitching circuit required
- Large output voltage range
- 1 kΩ output load
- Single 5 V power supply
- Power dissipation only 200 mW (typical)
- 44-pin QFP package

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing

GENERAL DESCRIPTION

The TDA8771 is a monolithic triple 8-bit video digital-to-analog converter (DAC). It converts the digital input signals into analog voltage outputs at a maximum conversion rate of 35 MHz. The D/A converters are based on resistor-string architecture with integrated output buffers. The output voltage range is determined by a built-in reference source.
The device is fabricated in a 5 V, 1 µm CMOS process that ensures high functionality with low power dissipation

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	33	–	mA
I_{DDD}	digital supply current	–	7	–	mA
ILE	integral linearity error	–	–	±1/2	LSB
DLE	differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum conversion rate	35	–	–	MHz
P_{tot}	total power dissipation (without load)	–	200	–	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8771G	44	QFP	plastic	SOT307

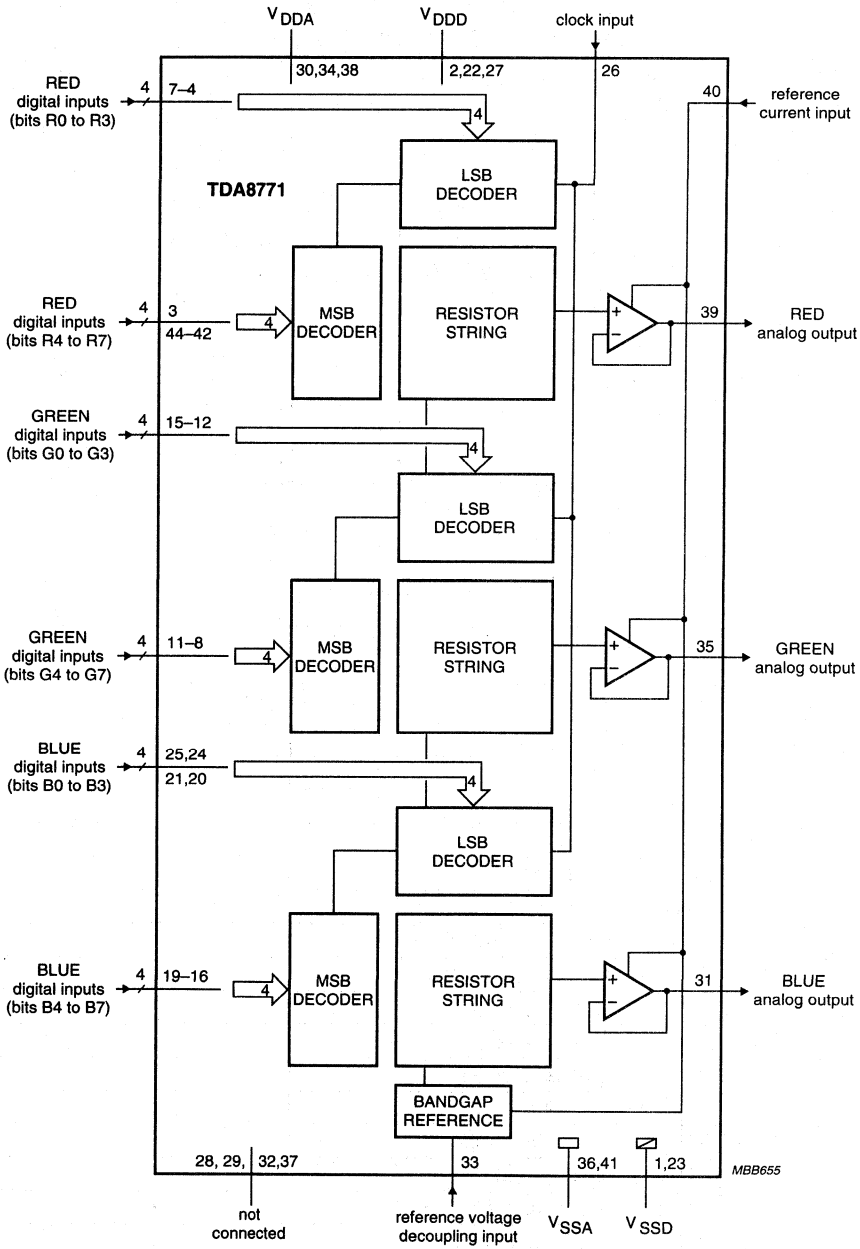


Fig.1 Block diagram.

Triple 8-bit video digital-to-analog converter

TDA8771

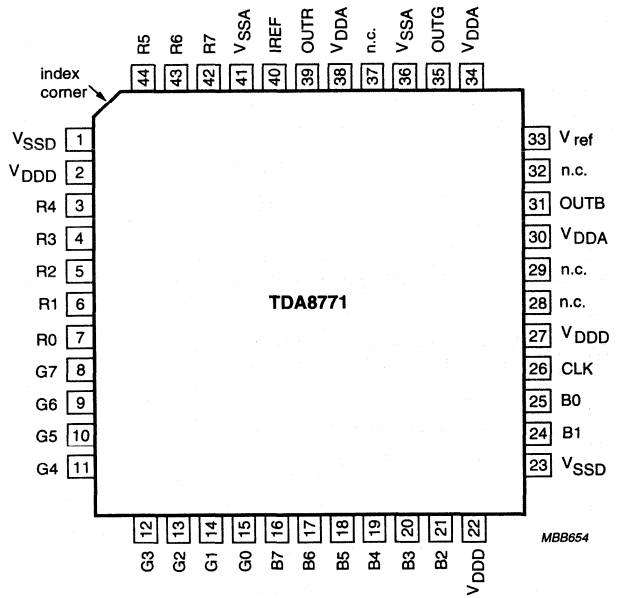


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSD}	1	digital supply ground
V_{DDD}	2	digital supply voltage
R4	3	RED digital input data, bit 4
R3	4	RED digital input data, bit 3
R2	5	RED digital input data, bit 2
R1	6	RED digital input data, bit 1
R0	7	RED digital input data, bit 0 (LSB)
G7	8	GREEN digital input data, bit 7 (MSB)
G6	9	GREEN digital input data, bit 6
G5	10	GREEN digital input data, bit 5
G4	11	GREEN digital input data, bit 4
G3	12	GREEN digital input data, bit 3
G2	13	GREEN digital input data, bit 2
G1	14	GREEN digital input data, bit 1
G0	15	GREEN digital input data, bit 0 (LSB)
B7	16	BLUE digital input data, bit 7 (MSB)
B6	17	BLUE digital input data, bit 6
B5	18	BLUE digital input data, bit 5

PINNING

SYMBOL	PIN	DESCRIPTION
B4	19	BLUE digital input data, bit 4
B3	20	BLUE digital input data, bit 3
B2	21	BLUE digital input data, bit 2
V_{DDD}	22	digital supply voltage
V_{SSD}	23	digital supply ground
B1	24	BLUE digital input data, bit 1
B0	25	BLUE digital input data, bit 0 (LSB)
CLK	26	clock input
V_{DDD}	27	digital supply voltage
n.c.	28	not connected
n.c.	29	not connected
V_{DDA}	30	analog supply voltage
OUTB	31	BLUE analog output
n.c.	32	not connected
V_{ref}	33	decoupling input for reference voltage
V_{DDA}	34	analog supply voltage
OUTG	35	GREEN analog output
V_{SSA}	36	analog supply ground
n.c.	37	not connected
V_{DDA}	38	analog supply voltage
OUTR	39	RED analog output
IREF	40	reference current input for output buffers
V_{SSA}	41	analog supply ground
R7	42	RED digital input data, bit 7 (MSB)
R6	43	RED digital input data, bit 6
R5	44	RED digital input data, bit 5

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage range	−0.5	7.0	V
V_{DDD}	digital supply voltage range	−0.5	7.0	V
$V_{DDA} - V_{DDD}$	supply voltage differences	−1.0	1.0	V
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
T_j	junction temperature	−	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	75 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{DDA} = V_{DDD}$ =4.5 V to 5.5 V; V_{SSA} and V_{SSD} shorted together; $V_{DDA} - V_{DDD}$ = –0.5 V to +0.5 V; T_{amb} = 0 °C to +70 °C; unless otherwise specified (typical values measured at $V_{DDA} = V_{DDD}$ = 5 V and T_{amb} = 25 °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	R7-R0, G7-G0, B7-B0 = logic 0	–	33	–	mA
I_{DDD}	digital supply current	f_{CLK} = 35 MHz	–	7	–	mA
Inputs						
CLOCK INPUT (PIN 26)						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
R,G,B DIGITAL INPUTS (PINS 42-44, 3-21, 24 AND 25)						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
IREF BUFFER SUPPLY CURRENT						
I_I	input current		–	0.8	–	mA
Timing (see Fig.3)						
f_{CLK}	maximum clock frequency		35	–	–	MHz
k_{CLK}	clock duty factor		40	–	60	%
t_r	clock rise time		–	tbf	–	ns
t_f	clock fall time		–	tbf	–	ns
$t_{SU;DAT}$	input data set-up time		–	tbf	–	ns
$t_{HD;DAT}$	input data hold time		–	tbf	–	ns
Voltage reference (pin 33, referenced to V_{SSA})						
V_{ref}	output voltage reference		tbf	1.2	tbf	V

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
OUTB, OUTR, OUTG ANALOG OUTPUTS (PINS 31, 35 AND 39, REFERENCED TO V_{SSA}) FOR 1 kΩ LOAD; SEE TABLES 1 AND 2						
FSR	full-scale output voltage range		tbf	3.0	tbf	V
V_{os}	offset of analog voltage output		tbf	0.2	tbf	V
$V_{OUT(max)}$	maximum output voltage	data inputs = logic 1; note 1	tbf	3.20	tbf	V
$V_{OUT(min)}$	minimum output voltage	data inputs = logic 0; note 1	tbf	0.21	tbf	V
B	−3 dB analog output bandwidth	f_{CLK} = 35 MHz	–	15	–	MHz
Z_L	output load impedance		–	1	–	kΩ
Transfer function						
ILE	integral linearity error	f_{CLK} = 10 MHz	–	–	±1/2	LSB
DLE	differential linearity error	f_{CLK} = 10 MHz	–	–	±1/2	LSB
CT	crosstalk DAC to DAC		–	−45	–	dB
	DAC to DAC matching		–	2	–	%
Switching characteristics (for 1 kΩ output load; see Fig.4)						
t_{pd}	propagation delay time	1 LSB input to output	–	tbf	–	ns
t_{s1}	settling time	10% to 90% full-scale change	–	15	–	ns
t_{s2}	settling time	to ±1 LSB	–	tbf	–	ns
Output transients (glitches)						
V_g	area for 1 LSB change		–	tbf	–	LSB.ns

Note to the characteristics

1. V_{OUT} is directly proportional to V_{ref}.

Table 1 Input coding and DAC output voltages

BINARY INPUT DATA (SYNC = BLANK = 0)	CODE	DAC OUTPUT VOLTAGES OUTB, OUTR, OUTG Z_L = 1 kΩ
0000 0000	0	0.212
0000 0001	1	0.224
....	.	..
1000 0000	128	1.718
....	.	..
1111 1110	254	3.188
1111 1111	255	3.200

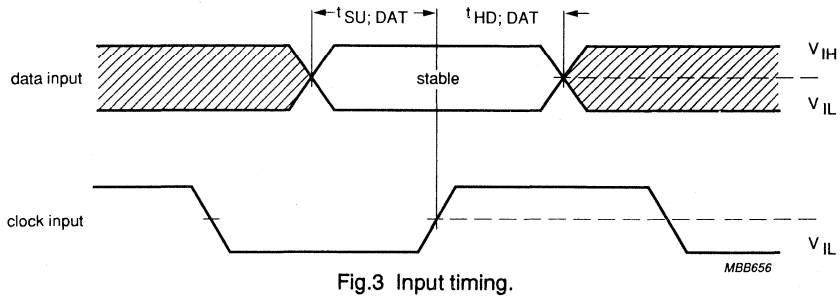


Fig.3 Input timing.

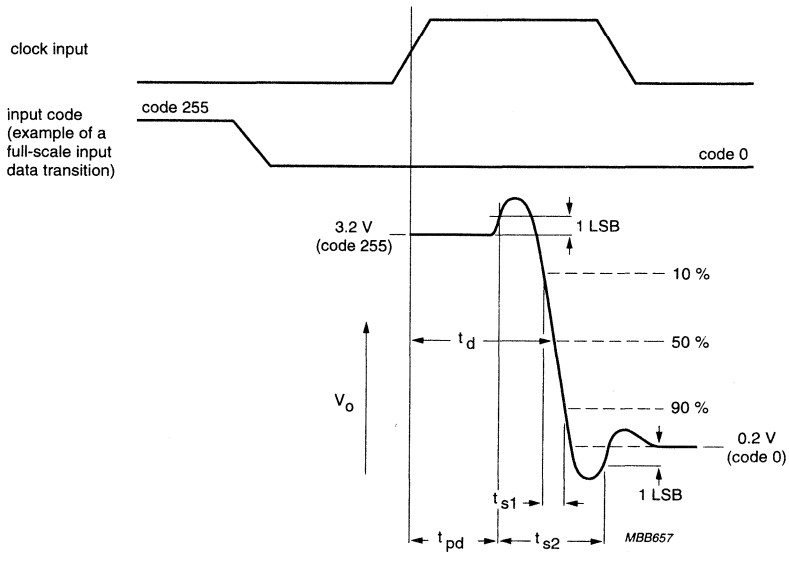


Fig.4 Switching timing.

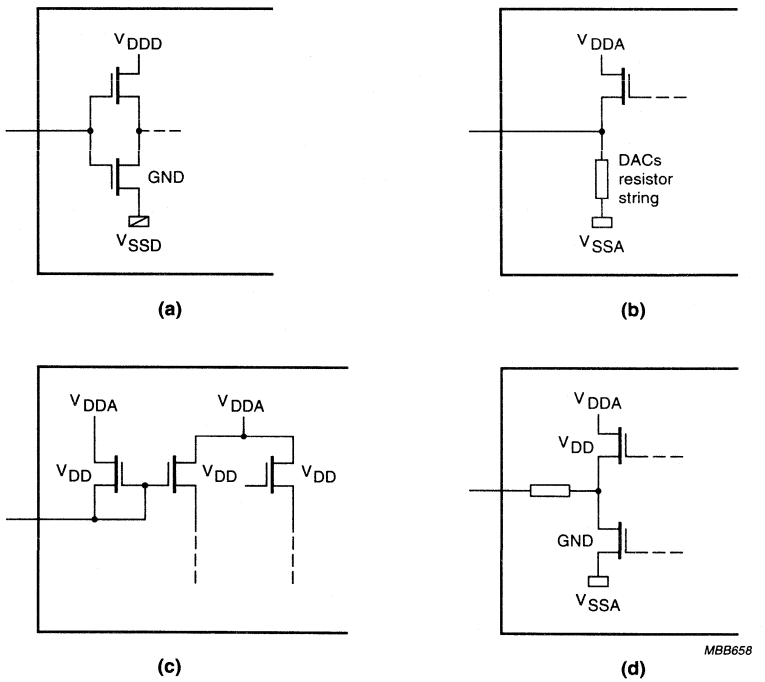


Fig.5 Internal circuitry (a) digital inputs; pins 3-21, 24-26, 28, 29, 42-44 (b) V_{ref}; pin 33 (c) IREF; pin 40 (d) OUTR, G, B; pins 31, 35, 39

APPLICATION INFORMATION

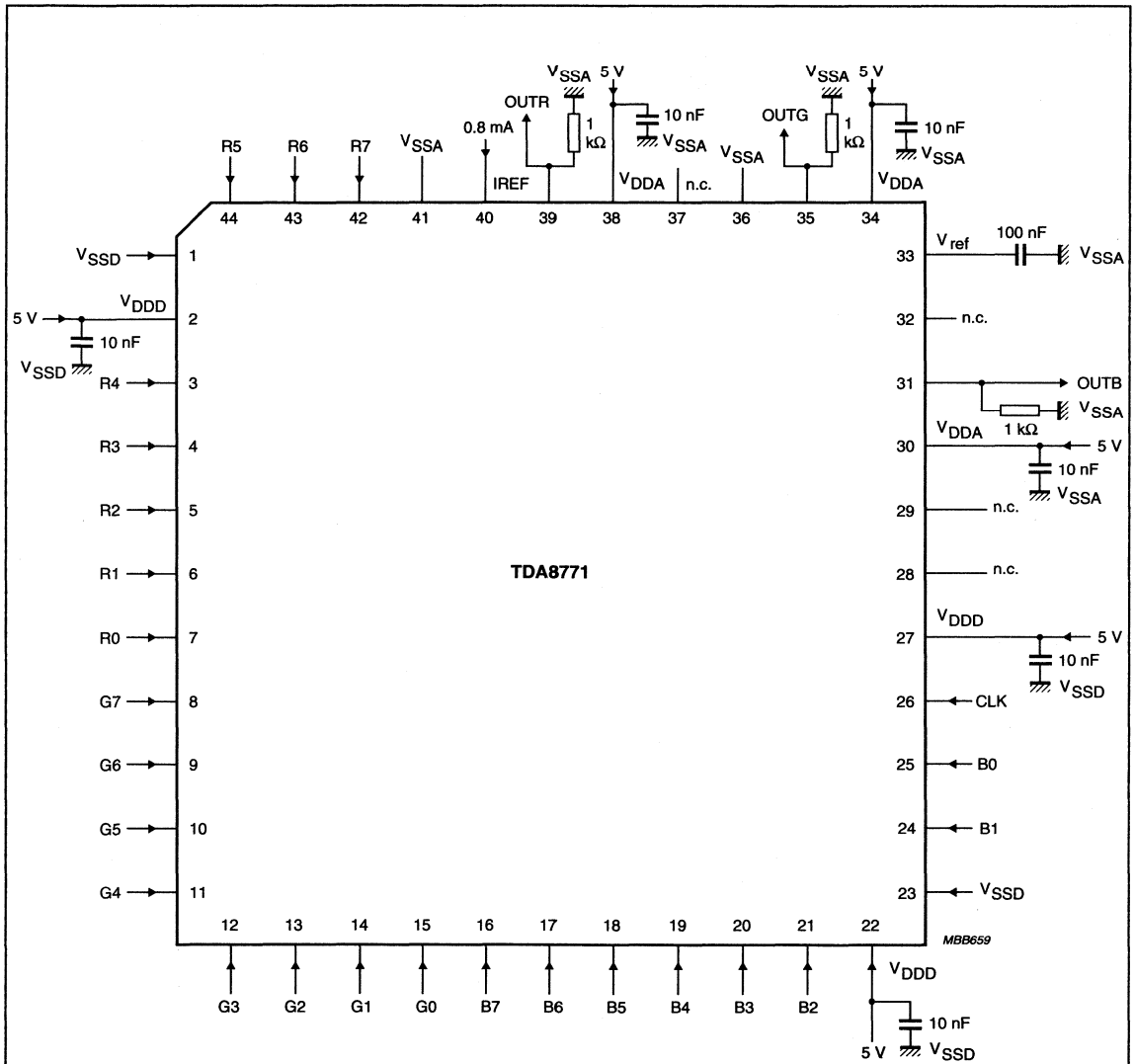


Fig.6 Application diagram.

Notes to Fig.6

1. Analog and digital supplies should be separated and decoupled.
2. Supplies are not connected internally; also applicable to grounds.
3. Pins 28, 29, 32 and 37 should be connected to V_{DDA}.

Triple 8-bit video digital-to-analog converter

TDA8772

FEATURES

- 8-bit resolution
- Sampling rate up to
  35 MHz for TDA8772G-35
  85 MHz for TDA8772G-85
- Internal reference voltage generator
- No deglitching circuit required
- $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ control inputs
- Drive capability with 3 different clocks
- 1 V output voltage range
- 75 Ω output load
- Single 5 V power supply
- 44-pin QFP package

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing

GENERAL DESCRIPTION

The TDA8772 is a monolithic triple 8-bit video digital-to-analog converter (DAC). It converts the digital input signals into analog voltage outputs at a maximum conversion rate of 35 MHz (TDA8772G-35) and 85 MHz (TDA8772G-85).
The D/A converters are based on resistor-string architecture with integrated output buffers. The output voltage range is determined by a built-in reference source.
The device is fabricated in a 5 V, 1 µm CMOS process that ensures high functionality with low power dissipation

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	33	–	mA
I_{DDD}	digital supply current				
	TDA8772G-35	–	7	–	mA
	TDA8772G-85	–	16	–	mA
ILE	integral linearity error	–	–	±1/2	LSB
DLE	differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum conversion rate				
	TDA8772G-35	35	–	–	MHz
	TDA8772G-85	85	–	–	MHz
P_{tot}	total power dissipation (without load)				
	TDA8772G-35	–	200	–	mW
	TDA8772G-85	–	250	–	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8772G-35	44	QFP	plastic	SOT307
TDA8772G-85	44	QFP	plastic	SOT307

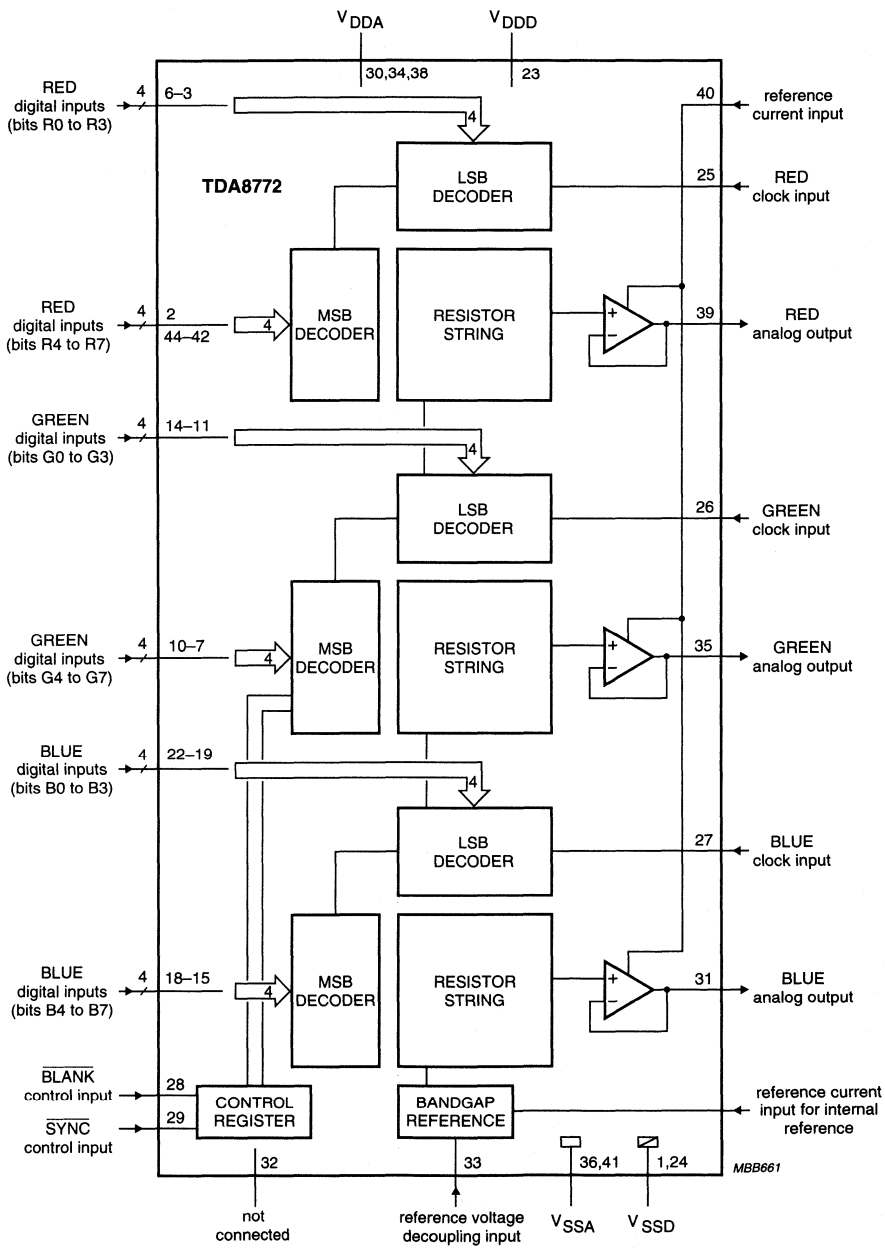


Fig.1 Block diagram.

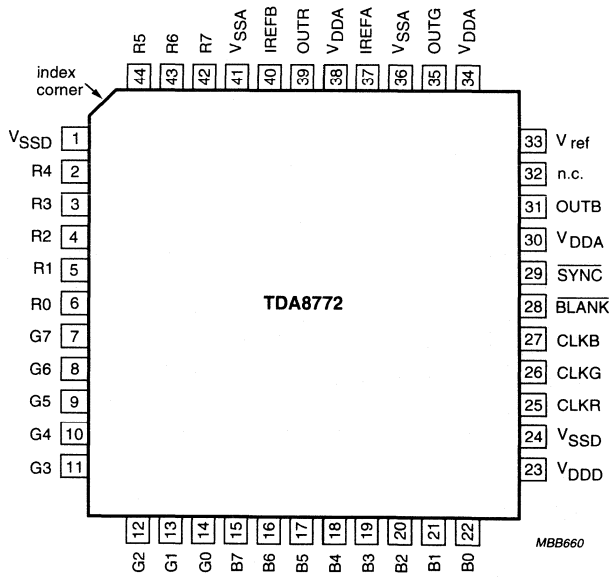


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSD}	1	digital supply ground
R4	2	RED digital input data, bit 4
R3	3	RED digital input data, bit 3
R2	4	RED digital input data, bit 2
R1	5	RED digital input data, bit 1
R0	6	RED digital input data, bit 0 (LSB)
G7	7	GREEN digital input data, bit 7 (MSB)
G6	8	GREEN digital input data, bit 6
G5	9	GREEN digital input data, bit 5
G4	10	GREEN digital input data, bit 4
G3	11	GREEN digital input data, bit 3
G2	12	GREEN digital input data, bit 2
G1	13	GREEN digital input data, bit 1
G0	14	GREEN digital input data, bit 0 (LSB)
B7	15	BLUE digital input data, bit 7 (MSB)
B6	16	BLUE digital input data, bit 6
B5	17	BLUE digital input data, bit 5

SYMBOL	PIN	DESCRIPTION
B4	18	BLUE digital input data, bit 4
B3	19	BLUE digital input data, bit 3
B2	20	BLUE digital input data, bit 2
B1	21	BLUE digital input data, bit 1
B0	22	BLUE digital input data, bit 0 (LSB)
V_{DDD}	23	digital supply voltage
V_{SSD}	24	digital supply ground
CLKR	25	RED clock input
CLKG	26	GREEN clock input
CLKB	27	BLUE clock input
$\overline{BLANK}$	28	composite blank control input (active LOW)
$\overline{SYNC}$	29	composite sync control input; for GREEN channel only (active LOW)
V_{DDA}	30	analog supply voltage
OUTB	31	BLUE analog output
n.c.	32	not connected
V_{ref}	33	decoupling input for reference voltage
V_{DDA}	34	analog supply voltage
OUTG	35	GREEN analog output
V_{SSA}	36	analog supply ground
IREFA	37	reference current input for internal reference
V_{DDA}	38	analog supply voltage
OUTR	39	RED analog output
IREFB	40	reference current for output buffers
V_{SSA}	41	analog supply ground
R7	42	RED digital input data, bit 7 (MSB)
R6	43	RED digital input data, bit 6
R5	44	RED digital input data, bit 5

LIMITING VALUES (TDA8772G-35 and TDA8772G-85)

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage range	−0.5	7.0	V
V_{DDD}	digital supply voltage range	−0.5	7.0	V
V_{DDA} - V_{DDD}	supply voltage differences	−1.0	1.0	V
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
T_j	junction temperature	−	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	75 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

TDA8772G-35 and TDA8772G-85 unless otherwise specified
$V_{DDA} = V_{DDD}$ =4.5 V to 5.5 V; V_{SSA} and V_{SSD} shorted together; $V_{DDA} - V_{DDD}$ = −0.5 V to +0.5 V; T_{amb} = 0 °C to +70 °C; unless otherwise specified (typical values measured at $V_{DDA} = V_{DDD}$ = 5 V and T_{amb} = 25 °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	R7-R0, G7-G0, B7-B0 = logic 0	–	33	–	mA
I_{DDD}	digital supply current					
	TDA8772G-35		–	7	–	mA
	TDA8772G-85		–	16	–	mA
Inputs						
CLOCK INPUTS (PINS 25, 26 AND 27)						
V_{IL}	LOW level input voltage		0	–	tbf	V
V_{IH}	HIGH level input voltage		tbf	–	V_{DDD}	V
$\overline{BLANK}$, $\overline{SYNC}$ INPUTS (PINS 28 AND 29; ACTIVE LOW)						
V_{IL}	LOW level input voltage		0	–	tbf	V
V_{IH}	HIGH level input voltage		tbf	–	V_{DDD}	V
R,G,B DIGITAL INPUTS (PINS 42-44, 2-22)						
V_{IL}	LOW level input voltage		0	–	tbf	V
V_{IH}	HIGH level input voltage		tbf	–	V_{DDD}	V
IREFA INTERNAL REFERENCE SUPPLY CURRENT (PIN 37)						
I_I	input current		–	0.2	–	mA
IREFB OUTPUT BUFFER SUPPLY CURRENT (PIN 40)						
I_I	input current		–	0.6	–	mA
Timing (see Fig.3)						
f_{CLK}	maximum clock frequency					
	TDA8772G-35		35	–	–	MHz
	TDA8772G-85		85	–	–	MHz
k_{CLK}	clock duty factor		40	–	60	%
t_r	clock rise time		–	tbf	–	ns
t_f	clock fall time		–	tbf	–	ns
$t_{SU;DAT}$	input data set-up time		–	tbf	–	ns
$t_{HD;DAT}$	input data hold time		–	tbf	–	ns
Voltage reference (pin 33, referenced to V_{SSA})						
V_{ref}	output voltage reference		tbf	1.2	tbf	V

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
OUTB, OUTR, OUTG ANALOG OUTPUTS (PINS 31, 39 AND 35, REFERENCED TO V_{SSA}) FOR 75 Ω LOAD; SEE TABLES 1 AND 2						
FSR	full-scale output voltage range		tbf	1.0	tbf	V
V_{os}	offset of analog voltage output		tbf	0.8	tbf	V
$V_{OUT(max)}$	maximum output voltage	data inputs = logic 1; note 1	tbf	1.8	tbf	V
$V_{OUT(min)}$	minimum output voltage	data inputs = logic 0; note 1	tbf	0.8	tbf	V
B	–3 dB analog output bandwidth		–	20	–	MHz
Z_L	output load impedance		–	75	–	Ω
Transfer function						
ILE	integral linearity error	f_{CLK} = 10 MHz	–	–	±1/2	LSB
DLE	differential linearity error	f_{CLK} = 10 MHz	–	–	±1/2	LSB
CT	crosstalk DAC to DAC		–	–45	–	dB
	DAC to DAC matching		–	2	–	%
Switching characteristics (for 75 Ω output load; see Fig.4)						
t_{pd}	propagation delay time	1 LSB input to output	–	tbf	–	ns
t_{s1}	settling time	10% to 90% full-scale change	–	5	–	ns
t_{s2}	settling time	to ±1 LSB	–	tbf	–	ns
Output transients (glitches)						
V_g	area for 1 LSB change		–	tbf	–	LSB.ns

Note to the characteristics

1. V_{OUT} is directly proportional to V_{ref}.

Table 1 Input coding and DAC output voltages

BINARY INPUT DATA (SYNC = BLANK = 0)	CODE	DAC OUTPUT VOLTAGES OUTB, OUTR, OUTG Z_L = 75 Ω
0000 0000	0	0.804
0000 0001	1	0.808
....	.	..
1000 0000	128	1.308
....	.	..
1111 1110	254	1.796
1111 1111	255	1.800

Table 2 Input coding and DAC output voltages

BINARY INPUT DATA	$\overline{\text{SYNC}}$ (pin 29)	$\overline{\text{BLANK}}$ (pin 28)	DAC OUTPUT VOLTAGES	
			OUTG (pin 35)	OUTR/B (pin 39, 31)
....	x	1	..	..
....	1	0	0.804 (code 72 level)	0.804 (code 72 level
....	0	0	0.500 (code 0 level)	

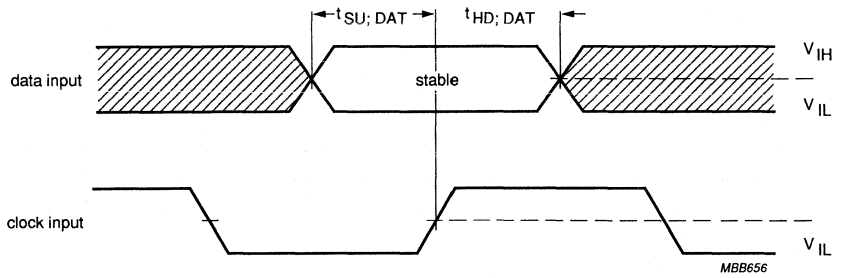


Fig.3 Input timing.

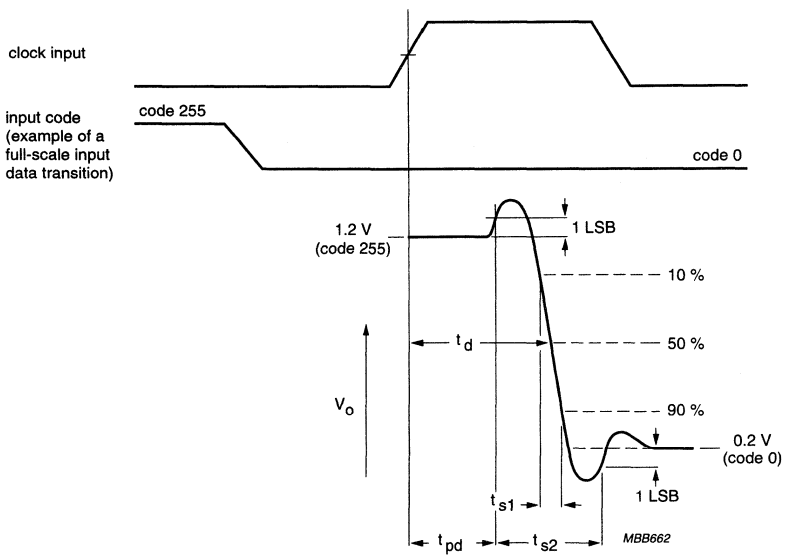


Fig.4 Switching timing.

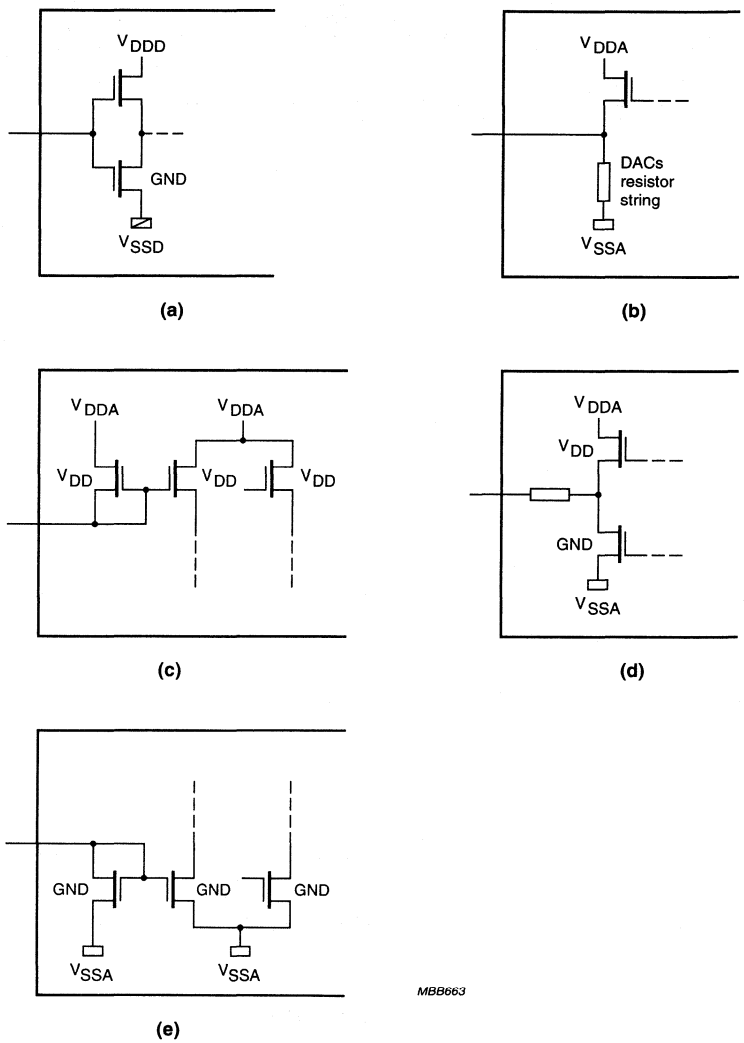


Fig.5 Internal circuitry (a) digital inputs; pins 2-22, 42-44 (b) V_{ref}; pin 33 (c) IREFA; pin 37 (d) OUTR, G, B; pins 39, 35, 31 (e) IREFB; pin 40

APPLICATION INFORMATION

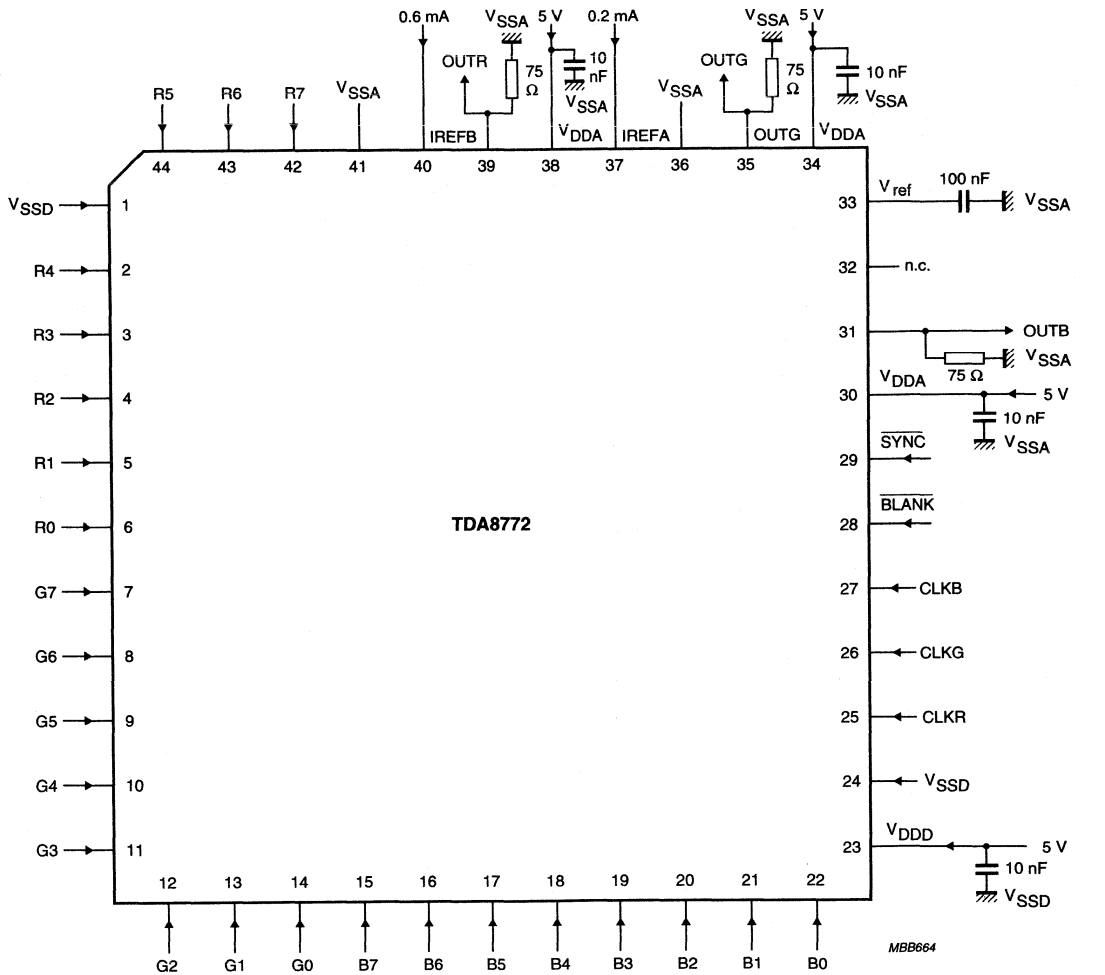
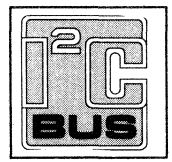


Fig.6 Application diagram.

Notes to Fig.6

1. Analog and digital supplies should be separated and decoupled.
2. Supplies are not connected internally; also applicable to grounds.
3. Pin 32 should be connected to V_{DDA}.

Programmable deflection controller TDA9150



FEATURES

General

- 6.75, 13.5 and 27 MHz clock frequency
- Few external components
- Synchronous logic
- I²C-bus controlled
- Easy interfacing
- Low power
- ESD protection
- Two-level sandcastle pulse

Vertical deflection

- Self-adaptive 16-bit precision vertical scan
- DC coupled deflection to prevent picture bounce
- S-correction can be preset
- S-correction setting independent of the field frequency
- Differential output for high DC stability
- Current source outputs for high EMC immunity

East-West correction

- DC coupled EW correction to prevent picture bounce
- 2nd and 4th order geometry correction can be preset
- Trapezium correction
- Geometry correction settings are independent of field frequency
- Self adaptive Bult generator prevents ringing of the horizontal deflection
- Current source output for high EMC immunity

Horizontal deflection

- φ 2 loop with low jitter
- Internal loop filter
- Dual slicer horizontal flyback input
- Soft start by I²C-bus
- Flash detector with automatic soft restart
- over-voltage protection with restart by I²C-bus

EHT correction

- Input selection between aquadag or EHT bleeder
- Internal filter

General description

The TDA9150 is a programmable deflection controller contained in a 20-pin DIL package and constructed using BIMOS technology. This high performance synchronization and DC deflection processor has been especially designed for use in both digital and analog based TV receivers and monitors, and serves horizontal and vertical deflection functions for all TV standards. The TDA9150 uses a line-locked clock at 6.75, 13.5 or 27 MHz, depending on the line frequency and application, and requires only a few external components. The device is self-adaptive for a number of functions and is fully programmable via the I²C-bus.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9150	20	DIL	plastic	SOT146

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	f_{CLK} = 6.75 MHz	–	22	–	mA
P_{tot}	total power dissipation		–	175	–	mW
T_{amb}	operating ambient temperature range		−25	–	+70	°C
Inputs						
V_{14}	line-locked clock (LLC) logic level		–	TTL	–	V
V_{13}	horizontal sync (H_A) logic level		–	TTL	–	V
V_{12}	vertical sync (V_A) logic level		–	TTL	–	V
V_5	line-locked clock select (LLCS) logic level	note 1	–	CMOS 5 V	–	V
V_{18}	serial clock (SCL) logic level		–	CMOS 5 V	–	V
V_{17}	serial data (SDA) input logic level		–	CMOS 5 V	–	V
V_1	horizontal flyback (HFB) phase slice level	FBL = 0 FBL = 1	– –	4.0 1.3	– –	V V
V_1	horizontal flyback (HFB) blanking slice level		–	100	–	mV
V_3	over-voltage protection (PROT) detection level		–	4.0	–	V
V_7	EHT flash detection level		–	550	–	mV
Outputs						
V_{20}	horizontal output (HOUT) voltage (open drain)	I_{20} = 10 mA	–	–	0.5	V
$I_{11}/I_{10(p-p)}$	vertical differential ($VOUT_{A, B}$) output current (peak-to-peak value)	vertical amplitude = 100%; I_8 = −100 µA	–	1000	–	µA
$V_{10.11}$	vertical output voltage range		0	–	3.9	V
$I_{6(peak)}$	EW (EWOUT) total output current (peak value)	I_8 = −100 µA	–	500	–	µA
V_6	EW (EWOUT) output voltage range		1.0	–	5.5	V
SANDCASTLE OUTPUT LEVELS (DSC)						
V_{BL}	base level		–	0.5	–	V
V_{HV}	horizontal and vertical blanking level		–	2.5	–	V
V_{clamp}	video clamp level		–	4.5	–	V

Note to the quick reference data

1. Hard wired to V_{SS} or V_{CC} is highly recommended.

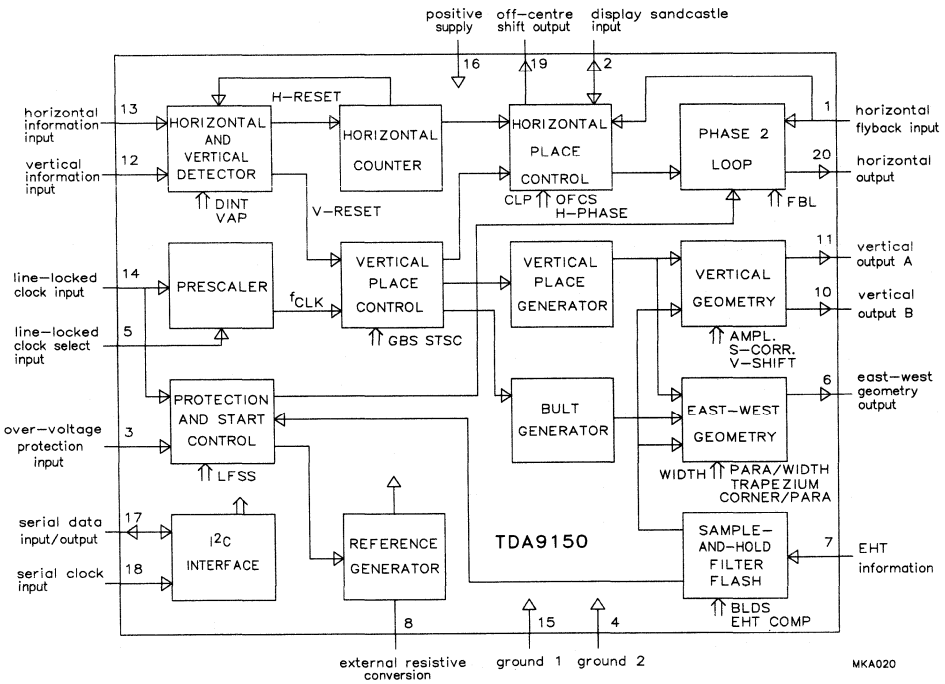


Fig.1 Block diagram.

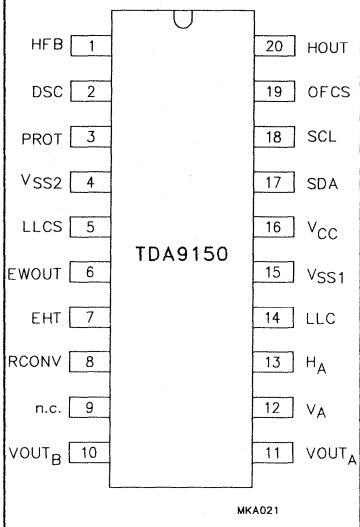


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
HFB	1	horizontal flyback input
DSC	2	display sandcastle input/output
PROT	3	over-voltage protection input
V_{SS2}	4	ground 2
LLCS	5	line-locked clock select input
EWOUT	6	east-west geometry output
EHT	7	EHT information
RCONV	8	external resistive conversion
n.c.	9	not connected
$VOUT_B$	10	vertical output B
$VOUT_A$	11	vertical output A
V_A	12	vertical information input
H_A	13	horizontal information input
LLC	14	line-locked clock input
V_{SS1}	15	ground 1
V_{CC}	16	positive supply input
SDA	17	serial data input/output
SCL	18	serial clock input
OFCS	19	off-centre shift output
HOUT	20	horizontal output

Functional description

Input signals (pins 12, 13, 14, 17 and 18)

The TDA9150 requires three signals for minimum operation (apart from the supply). These signals are the line-locked clock (LLC) and the two I²C-bus signals (SDA and SCL). Without the LLC the device will not operate because the internal synchronous logic uses the LLC as the system clock.
I²C-bus transmissions are required to enable the device to perform its required tasks. Once started the IC will use the H_A and V_A for synchronization. If the LLC is not present the outputs will be switched off and all operations discarded (if the LLC is not present the line drive will be inhibited within 2 µs and the vertical and EW output current will drop to zero within 100 µs). The SDA and SCL inputs meet the I²C specification, the other three inputs are TTL compatible.
The LLC frequency can be divided by two internally by connecting LLCS (pin 5) to ground thereby enabling the prescaler.
The LLC timing is given in the characteristics.

I²C-bus commands

Slave address:
8C HEX = 1000110X BIN

READ MODE

The format of the status byte is;
PON PROT 0 0 0 0 0 0

Where;

PON is the status bit for power-on-reset and after power failure

logic 1 — after the first POR and after power failure. Also set to 1 after a severe voltage dip that may have disturbed the various settings.

logic 0 — after a successful read of the status byte.

PROT is the over-voltage detection e.g. for the scaled EHT

logic 1 — if the input voltage rises above the reference value of 4 V. This results also in a reset of LFSS which terminates the deflection. A restart is achieved with an I²C-bus command i.e. by writing a logic 1 to LFSS (deflection will not start as long as the PROT bit is still logic 1; a read action must first be performed).

logic 0 — after a successful read of the status byte.

Note: A read action is considered successful when an End Of Data signal has been detected (i.e. no master acknowledge).

Table 1 Write mode: subaddress and data byte format

FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
vertical amplitude	00	X	X	A5	A4	A3	A2	A1	A0
vertical S-correction	01	X	X	A5	A4	A3	A2	A1	A0
vertical start scan	02	X	X	A5	A4	A3	A2	A1	A0
vertical off-centre shift	03	X	*	*	*	X	A2	A1	A0
EW trapezium correction	03	X	A6	A5	A4	X	*	*	*
EW width/width ratio	04	X	X	A5	A4	A3	A2	A1	A0
EW parabola/width ratio	05	X	X	A5	A4	A3	A2	A1	A0
EW corner/parabola ratio	06	X	X	A5	A4	A3	A2	A1	A0
EHT compensation	07	X	X	A5	A4	A3	A2	A1	A0
horizontal phase	08	X	X	A5	A4	A3	A2	A1	A0
horizontal off-centre shift	09	X	X	A5	A4	A3	A2	A1	A0
clamp shift	0A	X	X	X	X	X	A2	A1	A0
control	0B	X	X	FBL	VAP	BLDS	LFSS	DINT	GBS

Where: X = don't care; * = data bit used in another function

Table 2 Control bits

CONTROL BIT	LOGIC	FUNCTION
LFSS	0	line stop: becomes 0 after a HIGH on PON or PROT
	1	line start enable: the soft start mechanism is now activated
DINT	0	de-interlace ON: the V_A pulse is sampled with the detected rising edge of H_A
	1	de-interlace OFF: the V_A pulse is sampled with the system clock and the detected rising edge is used as vertical reset
BLDS	0	aquadag selected
	1	bleeder selected
GBS	0	guardband 16/12 lines: becomes 0 after power-on
	1	guardband 48/12 lines
VAP	0	positive $V_A$edge detection
	1	negative $V_A$edge detection
FBL	0	horizontal flyback slicing level = 4 V
	1	horizontal flyback slicing level = 1.3 V

Table 3 Clock frequency control bit (pin 5)

CONTROL BIT	LOGIC	FUNCTION
LLCS	0	prescaler ON: the internal clock frequency $f_{CLK} = f_{LLC}/2$
	1	prescaler OFF: (default by internal pull-up resistor). The internal clock frequency $f_{CLK} = f_{LLC}$

Note to Table 3

Switching of the prescaler is only allowed when LFSS is LOW. It is highly recommended to hard wire LLCS to V_{SS} or V_{CC}.

Active switching may damage the output power transistor due to the changing HOUT pulse. This may cause very high currents and huge flyback pulses. The permitted combinations of LLC and the prescaler are given in table 4.

Table 4 Line duration with prescaler

LLC (MHz)	ON (µs)	OFF (µs)
6.75	*	64
13.5	64	32
27	32	*

Where: * = not allowed combination.

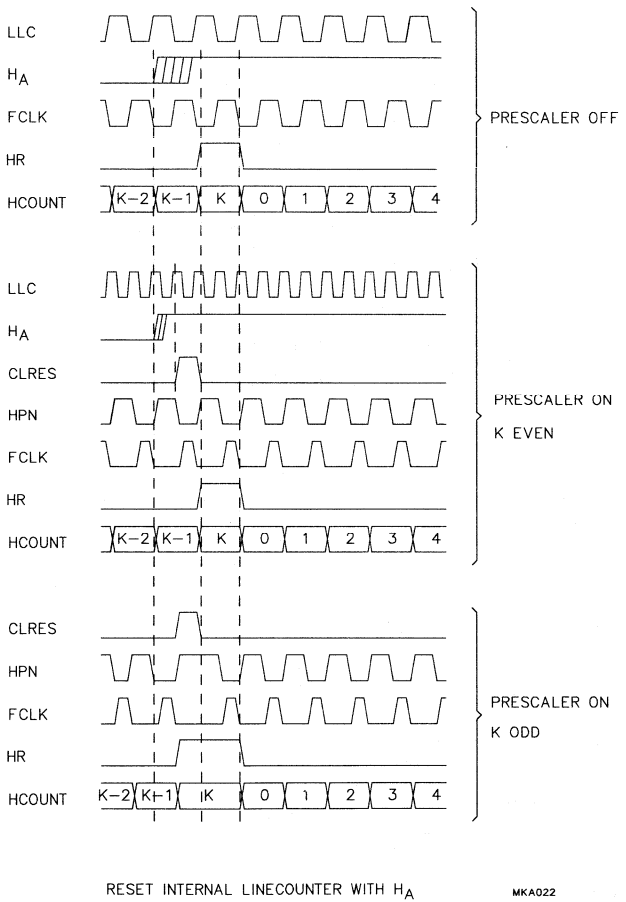


Fig.3 Timing relations between LLC, H_A and line counter.

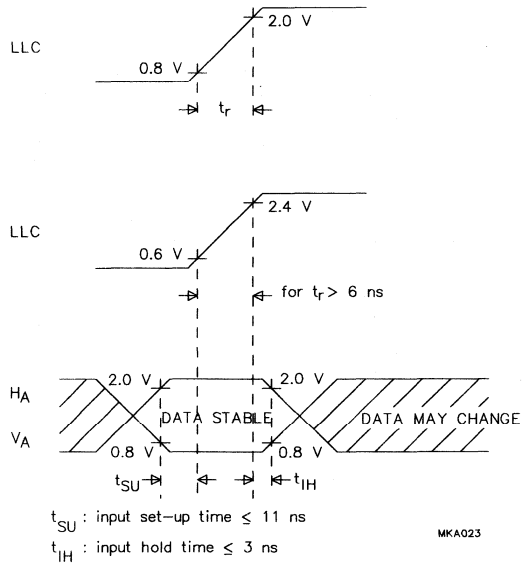


Fig.4 Timing requirements for LLC, H_A and V_A.

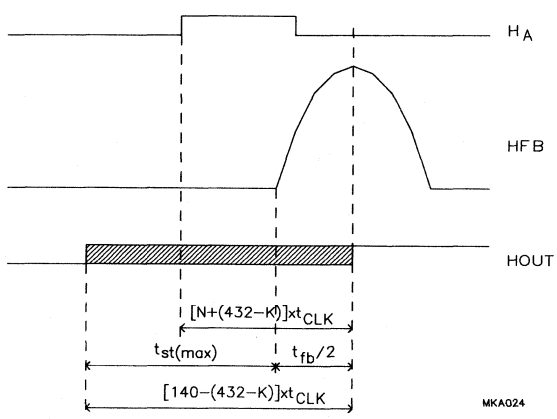


Fig.5 Horizontal phase and HOUT control range.

Horizontal part (pins 1, 2, 13, 19 and 20)

Synchronization pulse

The H_A input (pin 13) is a TTL-compatible ESD protected CMOS input. Pulses at this input have to fulfil the timing requirements as illustrated in Fig.4. For proper detection the minimum pulse width for both the HIGH and LOW period is 2 internal clock periods.

Flyback input pulse

The HFB input (pin 1) is an ESD protected CMOS input. The delay of the centre of the flyback pulse to the leading edge of the H_A pulse can be set via the I²C-bus with the horizontal phase byte (subaddress 08) as illustrated in Fig.5. The resolution is 6-bit.

Output pulse

The HOUT pulse (pin 20) is an ESD protected open-drain NMOS output. The duty factor for this output is typically 55/45 (conducting/non-conducting) during normal operation. A soft start causes the duty factor to increase linearly from 0 to 55% over a period of 400 lines in 400 steps.

Off-centre shift

The OFCS output (pin 19) is an ESD protected push-pull CMOS output which is driven by a pulse-width modulated DAC.
By using a suitable interface, the output signal can be used for off-centre shift correction in the horizontal output stage. This correction is required for HDTV tubes with a 16 x 9 aspect ratio and is useful for high performance flat square tubes to obtain the required horizontal linearity. For applications where off-centre correction is not required, the output can be used as an auxiliary DAC. The OFCS signal is phase-locked with the line frequency. The off-centre shift can be set via the I²C-bus, subaddress 09, with a 6-bit resolution as illustrated in Fig.6.

Sandcastle

The DSC input/output (pin 2) acts as a sandcastle generating output and a guard sensing input. As an output it provides 2 levels (apart from the base level), one for the horizontal and vertical blanking and the other for the video clamp. As an input it acts as a current sensor during the blanking interval for guard detection.

Clamp pulse

The clamp pulse width is 21 internal clock periods. The shift, w.r.t. H_A can be varied from 35 to 49 clock periods in 7 steps via the I²C-bus, clamp shift byte subaddress 0A, as illustrated in Fig.7

Horizontal blanking

The start of the horizontal blanking pulse is minimum 38 and maximum 41 clock periods before the centre of the flyback pulse, depending on the f_{CLK}/f_H ratio 'K' [according to 41–(432–K)].
When the horizontal blanking pulse finishes is determined by the trailing edge of the HFB pulse at the horizontal blanking slicing level coincidence, as illustrated in Fig.8.

Vertical blanking

The vertical blanking pulse starts two internal clock pulses after the rising edge of the V_A pulse. During this interval a small guard pulse, generated during flyback by the vertical power output stage, must be inserted. Stop vertical blanking is effected at the end of the blanking interval only when the guard pulse is present (see Vertical guard).

The start scan setting determines the end of vertical blanking with a 6-bit resolution in steps of one line via the I²C-bus subaddress 02, (see Figs 9 and 10).

Vertical guard

In the vertical blanking interval a small unblanking pulse is inserted. This pulse must be filled-in by a blanking pulse or guard pulse from the vertical power output stage which was generated during the flyback period. In this condition the sandcastle output acts as guard detection input and requires a minimum 500 µA input current. This current is sensed during the unblanking period. Vertical blanking is only stopped at the end of the blanking interval when the inserted pulse is present. In this way the picture tube is protected against damage in case of missing or malfunctioning vertical deflection.

Vertical part (pins 6, 8, 10, 11 and 12)

Synchronization pulse

The V_A input (pin 12) is a TTL-compatible ESD protected CMOS input. Pulses at this input have to fulfil the timing requirements as illustrated in Fig.4. For proper detection the minimum pulse width for both the HIGH and LOW period is 2 internal clock periods.

Vertical place generator

The vertical start-scan data (subaddress 02) determines the vertical placement in the total range of 64 x 432 clock periods, in 63 steps. The maximum number of synchronized lines per scan is 910 with an equivalent field frequency of 17.2 or 34.4 Hz for f_H = 15625 or 31250 Hz respectively.
The minimum number of

synchronized lines per scan is 200 with an equivalent field frequency of 78 or 156 Hz for f_H = 15625 or 31250 Hz respectively.
If the V_A pulse is not present, the number of lines per scan will increase to 910.2. If the LLC is not present the vertical blanking will start within 2 µs.
Amplitude control is automatic, with a setting time of 1 to 2 new fields and an accuracy of either 16/12 or 48/12 lines depending on the value of the GBS bit

Differences in the number of lines per field, as can occur in TXT or in multi-head VTR, will not affect the amplitude setting providing the differences are less than the value selected with GBS. This is called amplitude control guardband. The difference sequence and the difference sequence length are not important.

De-interlace

With De-interlace ON, the V_A pulse is sampled with the detected rising edge of the H_A pulse. The duration of the V_A pulse must, therefore, be sufficient to enable the H_A pulse to coincide, in this case an active time of minimum of half a line (see Fig.11).
With De-interlace OFF, the V_A pulse is sampled with the system clock. The rising edge is used as the vertical reset.

Vertical geometry processing

The vertical geometry processing is DC-coupled and therefore independent of field frequency. The resistive conversion (pin 8) sets the reference current for both the vertical and EW geometry processing. A useful range is 50 to 100 µA, the recommended value is 100 µA.

Vertical outputs

The vertical outputs (pins 10 and 11) together form a differential current output and are ESD protected. The vertical amplitude can be varied over the range 80 to 120% in 63 steps via the I²C-bus (subaddress 00). Vertical S-correction is also applied to these outputs and can be set from 0 to 16% by subaddress 01 with 6-bit resolution.
The vertical off-centre shift (OFCS) shifts the vertical deflection current zero crossing with respect to the EW parabola bottom. The control range is –2 to +2% in 7 steps set by the least significant nibble at subaddress 03.

EW geometry processing

The EW geometry processing is DC-coupled and therefore independent of field frequency. The resistive conversion (pin 8) sets the reference current for both the vertical and EW geometry processing. The EW output is an ESD-protected single-ended current output.
The EW width/width ratio can be set from 100 to 80% in 63 steps via subaddress 04 and the EW parabola/width ratio from 0 to 20% via subaddress 05. The EW corner/EW parabola ratio has a control range of –46 to 0% in 63 steps via subaddress 06.
The EW trapezium correction can be set from –4 to +4% in 7 steps via the most significant nibble at subaddress 03

Bult generator

The Bult generator makes the EW waveform continuous (see Fig.18).

EHT compensation (pin 7)

The EHT input is an ESD protected MOS input which permits scan amplitude modulation should the EHT supply be non-perfect. For correct tracking of the vertical and horizontal deflection the gain of the EW output stage, given by the ratio R_{conv}_EW/R_{conv}, must be $V_{scan}/(20 \times V_{ref})$ (see Fig.12).
The input for EHT compensation can be derived from an EHT bleeder or from the picture tubes aquadag (subaddress 0B, bit BLDS). EHT compensation can be set via subaddress 07 in 63 steps allowing a scan modulation range from –10 to +9.7%. When the EHT input voltage drops below 0.55 V the outputs will be inhibited and an automatic restart will be performed.

Over-voltage protection (pin 3)

The over-voltage protection input is an ESD protected MOS input.
The input voltage can be the scaled EHT and has the following characteristics:

If the protection voltage is less than 4 V do nothing
If the protection voltage is greater than 4 V stop line drive

Restart by I²C-bus command:

1. perform read action to clear the PROT bit
2. write the LFSS bit

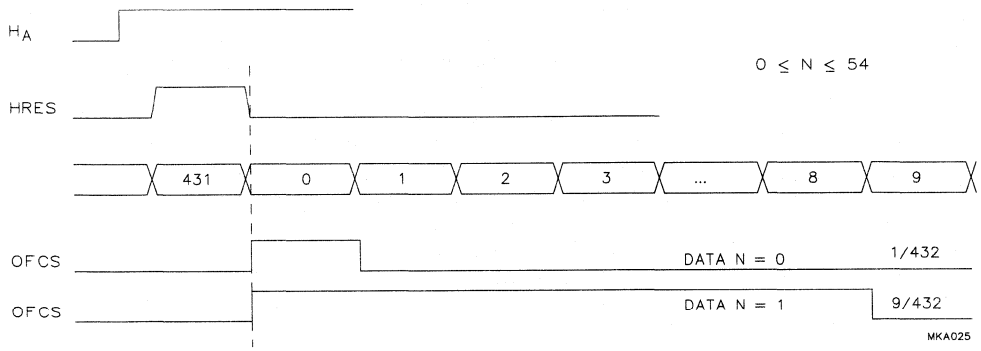


Fig.6 OFCS duty factor.

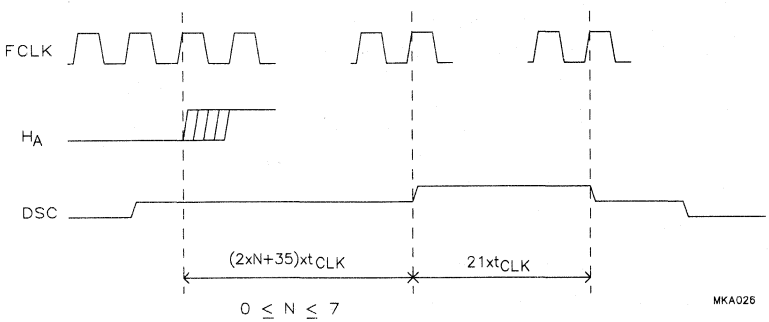


Fig.7 DSC clamp pulse.

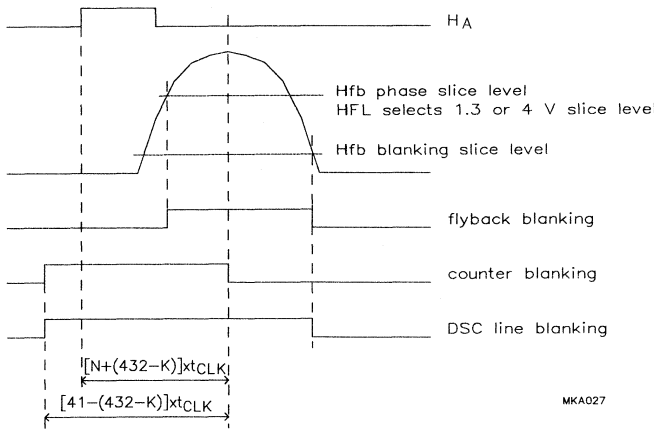


Fig.8 DSC line blanking.

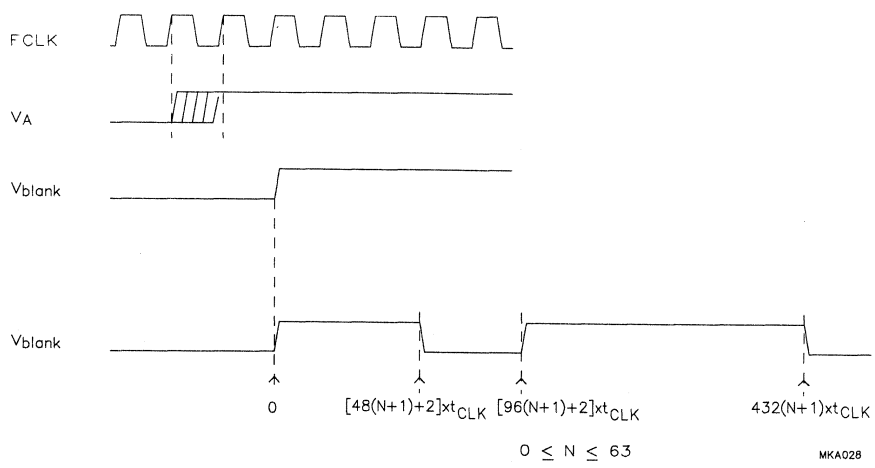


Fig.9 DSC vertical blanking with unblanking.

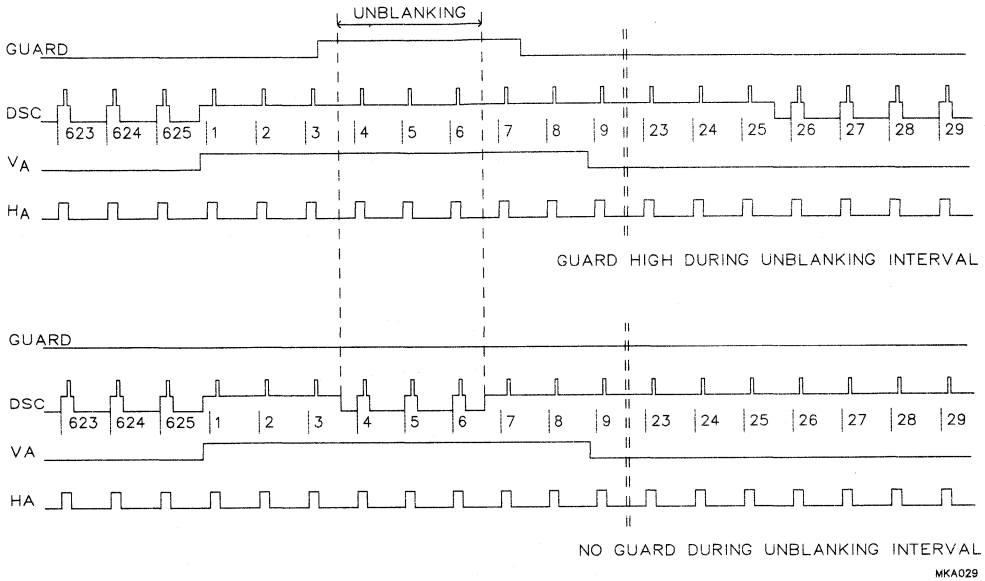


Fig.10 DSC with guard interval.

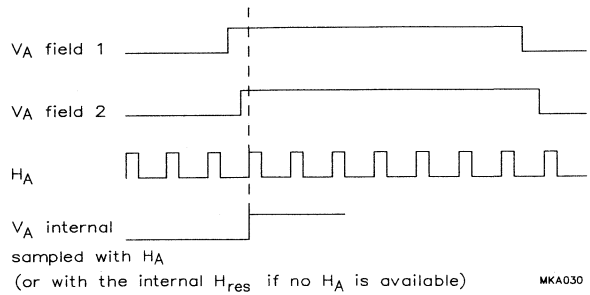


Fig.11 De-interlace timing.

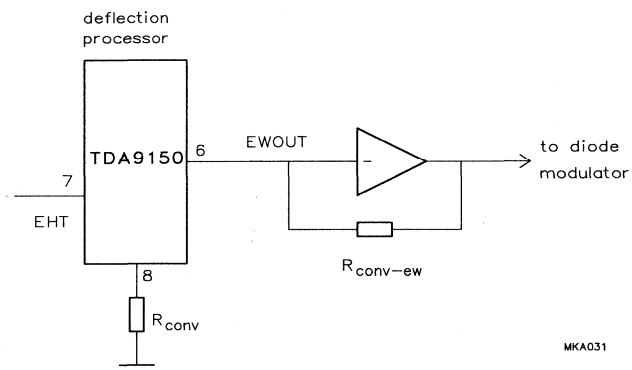


Fig.12 Explanation of R_{conv}–EW/R_{conv} ratio.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	positive supply voltage		−0.5	8.8	V
I_{CC}	supply current		−10	50	mA
P_{tot}	total power dissipation		−	500	mW
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	operating ambient temperature range		−25	+70	°C
V_{supply}	voltage supplied to pins 1 to 3, 5 to 8, 10 to 14 and 17 to 20		−0.5	V_{CC}+0.5	V
$I_{I/O}$	current in or out of any pin except pins 4, 15 and 16		−20	+20	mA

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	70 K/W

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; V_{SS1} = V_{SS2} = 0 V; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	note 1; f_{CLK} = 6.75 MHz	17	22	28	mA
P_{tot}	total power dissipation		−	175	−	mW
SDA and SCL (pins 17 and 18)						
V_{17}	SDA input voltage		0	−	5.5	V
V_{IL}	LOW level input voltage (pin 17)		−	−	1.5	V
V_{IH}	HIGH level input voltage (pin 17)		3.5	−	−	V
I_{IL}	LOW level input current (pin 17)	$V_{17} = V_{SS1}$	−	−	−10	µA
I_{IH}	HIGH level input current (pin 17)	$V_{17} = V_{CC}$	−	−	10	µA
V_{OL}	LOW level output voltage (pin 17)	I_{IL} = 3 mA	−	−	0.4	V
V_{18}	SCL input voltage		0	−	5.5	V
V_{IL}	LOW level input voltage (pin 18)		−	−	1.5	V
V_{IH}	HIGH level input voltage (pin 18)		3.5	−	−	V
I_{IL}	LOW level input current (pin 18)	$V_{18} = V_{SS1}$	−	−	−10	µA
I_{IH}	HIGH level input current (pin 18)	$V_{18} = V_{CC}$	−	−	10	µA
Line locked clock and Line locked clock select (pins 14 and 5)						
V_{IL}	LOW level input voltage (pin 14)		−	−	0.8	V
V_{IH}	HIGH level input voltage (pin 14)		2.0	−	−	V
I_{14}	input current	V_{14} = < 5.5 V	−	−	±10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r, t_f	rise and fall times		0	–	$t_{LLC}/2$	ns
	duty factor	note 2; LLCS = 0	40	50	60	%
		LLCS = 1	25	50	75	%
TIMING (PRESCALER ON) ($F_{CLK} = F_{LLC}/2$) WHERE F_{CLK} = INTERNAL CLOCK						
f_{LLC}	line-locked clock frequency		12.4	–	29.2	MHz
		f_{LLC}/f_H; H locked	856	864	865	
		f_{LLC}/f_H; H unlocked	–	866	–	
K	line-locked clock frequency ratio	f_{CLK}/f_H; H locked	428	432	432.5	
		f_{CLK}/f_H; H unlocked	–	433	–	
TIMING (PRESCALER OFF) ($F_{CLK} = F_{LLC}$) WHERE F_{CLK} = INTERNAL CLOCK						
f_{LLC}	line-locked clock frequency		6.2	–	14.6	MHz
		f_{LLC}/f_H; H locked	428	432	432	
		f_{LLC}/f_H; H unlocked	–	433	–	
K	line-locked clock frequency ratio	f_{CLK}/f_H; H locked	428	432	432	
		f_{CLK}/f_H; H unlocked	–	433	–	
V_5	LLCS input voltage		0	–	8.8	V
V_{IL}	LOW level input voltage (pin 5)		–	–	1.5	V
V_{IH}	HIGH level input voltage (pin 5)		3.5	–	–	V
I_{IL}	LOW level input current (pin 5)	$V_5 = V_{SS1}$	–	–	–150	µA
I_{IH}	HIGH level input current (pin 5)	$V_5 = V_{CC}$	–	–	100	µA
Horizontal part						
INPUT SIGNALS						
H_A (pin 13)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_I	input current	V_{13} = 5.5 V	–	–	±10	µA
t_r; t_f	rise and fall times		0	–	$t_{LLC}/2$	ns
t_{WH}	pulse width HIGH		2	–	–	t_{CLK}
t_{WL}	pulse width LOW		2	–	–	t_{CLK}
HFB (pin 1)						
V_{PS1}	phase slice level	FBL = 0	3.8	4.0	4.2	V
V_{PH2}	phase slice level	FBL = 1	1.1	1.3	1.5	V
V_{blank}	blanking slice level		0	0.1	0.2	V
I_1	input current		–	–	±10	µA
Horizontal phase (delay centre flyback pulse to leading edge of H_A; where N = horizontal phase data)						
CR	control range		0	N	N+(432–K)	t_{CLK}
	number of steps		–	63	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OUTPUT SIGNALS						
HOUT (pin 20)						
V_{20}	output voltage	$I_{20} = 0$	0	–	V_{CC}	V
V_{OL}	LOW level output voltage	$I_{20} = 10$ mA	–	–	0.5	V
I_I	input current	output OFF	–	–	±10	µA
	duty factor	normal operation	54.5	55.5	56.5	%
Soft start (duty factor controlled line drive)						
t_W	initial pulse width soft start		–	–	1.5	%
CR	control range		0	–	56.5	%
t_{ss}	soft start time		250	400	600	lines
Switch-off time to the centre of the flyback pulse						
CR	control range		0	–	140–(432–K)	t_{CLK}
Φ	control sensitivity (loop gain)		400	1000	–	µs/µs
f_G/f_H	unity gain frequency ratio		–	0.15	–	
t_{pj}	phase jitter with respect to LLC		–	–	5	ns
PSRR	power supply rejection ratio		tbf	–	–	µs/V
HORIZONTAL OFF-CENTRE SHIFT (PIN 19) (N = OFF-CENTRE SHIFT DATA)						
V_{19}	output voltage		0	–	V_{CC}	V
V_{OL}	LOW level output voltage	$I_{19} = 2$ mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	$I_{19} = -2$ mA	V_{CC}–0.5	–	–	V
	maximum duty factor	N < 54	1/K	(8N+1)/K	425/K	%
	duty factor	N ≥ 54	–	1	–	%
	number of steps		–	54	–	
SANDCASTLE (PIN 2)						
DSC output voltage						
V_{clamp}	video clamp voltage		4.0	4.5	5.0	V
V_{blank}	horizontal and vertical blanking level		2.0	2.5	3.0	V
V_{base}	base level		0	0.5	1.0	V
I_2	output current		–1.0	–	0.35	mA
		guard detected	0.8	–	2.5	mA
t_r; t_f	rise and fall times		–	60	–	ns
Clamp pulse (N = clamp pulse shift data)						
t_W	clamp pulse width		–	21	–	t_{CLK}
t_{clamp}	clamp pulse shift w.r.t H_A		35	2N+35	49	t_{CLK}
	number of steps		–	7	–	
t_{start}	start of horizontal blanking before middle of flyback pulse		38	41–(432–K)	41	t_{CLK} x 432

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical blanking width (N = vertical start–scan data)						
CR	control range		1	N+1	64	t_{CLK}
		K = 432	1	–	64	lines
	number of steps		–	63	–	
Guard detection (N = vertical start–scan data)						
t_{start}	start interval w.r.t V_A		48(N+1)+2	–	–	t_{CLK}
t_{stop}	stop interval w.r.t V_A		96(N+1)+2	–	–	t_{CLK}
Vertical section						
INPUT SIGNALS (PIN 12) (V_A)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{12}	input current	V_{12} < 5.5 V	–	–	±10	μA
t_r; t_f	rise and fall times		0	–	$t_{LLC}/2$	t_{CLK}
t_{WH}	pulse width HIGH		2	–	–	t_{CLK}
t_{WL}	pulse width LOW		2	–	–	t_{CLK}
t_{WH}	pulse width HIGH	de-interlace mode	0.5	–	–	t_{line}
t_{WL}	pulse width LOW	de-interlace mode	0.5	–	–	t_{line}
VERTICAL PLACE GENERATOR (N = VERTICAL START–SCAN DATA)						
CR	control range		1	N+1	64	t_{CLK} x 432
		K = 432	1	–	64	lines
	number of steps		–	63	–	
$Lines_{max}$	maximum number of synchronized lines per scan		–	910	–	lines/scan
f_{eq}	equivalent field frequency at 910 lines/scan	f_H = 15625 Hz	–	17.2	–	Hz
		f_H = 31250 Hz	–	34.4	–	Hz
$Lines_{min}$	minimum number of synchronized lines per scan		–	200	–	lines/scan
f_{eq}	equivalent field frequency at 200 lines/scan	f_H = 15625 Hz	–	78	–	Hz
		f_H = 31250 Hz	–	156	–	Hz
CA	amplitude control		–	automatic	–	
CA_g	amplitude control guardband	GBS = 0	–	16/12	–	lines
		GBS = 1	–	48/12	–	lines
	setting time		1	1.5	2	fields

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL GEOMETRY PROCESSING						
$I_{diff(p-p)}$	vertical output differential current (peak-to-peak value)	I_8 = −100 µA	0.96	1.0	1.04	mA
D/ΔT	drift over temperature range		–	10^{-4}	–	
	amplitude error due to S-correction setting		–	tbf	–	%
I_{bias}	vertical output signal bias current		–	−300	–	µA
I_{os}	vertical output offset current		–	–	tbf	µA
OS/ΔT	offset over temperature range		–	–	tbf	µA/K
$V_{10, 11}$	vertical output voltage range		0	–	3.9	V
CMRR	common mode rejection ratio		–	tbf	–	dB
LE	linearity error		–	0.2	2.0	%
Vertical amplitude (N = vertical amplitude data)						
CR	control range		80	–	120	%
	number of steps		–	63	–	
Vertical S-correction (N = S-correction data)						
CR	control range		0	–	16	%
	number of steps		–	63	–	
Vertical shift						
CR	control range		−2	–	+2	%
	number of steps		–	7	–	
EW OUTPUT (PIN 6)						
V_6	output voltage range		0.5	–	5.5	V
I_6	output current range	I_8 = −100 µA	0	–	1000	µA
EW width/width ratio						
CR	control range		100	–	80	%
I_{eq}	equivalent output current		0	–	400	µA
	number of steps		–	63	–	
EW parabola/width ratio						
CR	control range		0	–	20	%
I_{eq}	equivalent output current	width = 100% width = 80%	0 0	– –	400 320	µA µA
	number of steps		–	63	–	
EW corner/EW parabola ratio (note 3)						
CR	control range		−46	–	0	%
I_{eq}	equivalent output current	width = 100% width = 80%	0 0	– –	184 147	µA µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	number of steps		–	63	–	
EW corner/EW parabola ratio (note 3)						
CR	control range		–46	–	0	%
I_{eq}	equivalent output current	width = 100% width = 80%	0 0	– –	184 147	µA µA
	number of steps		–	63	–	
EW trapezium correction						
	EW trapezium/width ratio		–4	–	+4	%
	number of steps		–	7	–	
EHT INPUT (PIN 7)						
V_{ref}	reference voltage	BLDS = 1 BLDS = 0	– –	3.9 V_{CC}	– –	V V
V_I	input voltage range w.r.t V_{ref}	BLDS = 1	–20	–	+20	%
V_I	input voltage range w.r.t V_{CC}	BLDS = 0	–	0	$-2V_{ref}$	V
m_{scan}	scan modulation range		–10	0	–9.7	
m_{GC}	modulation gain control		0	–	1	
	number of steps		–	63	–	
V_7	flash detection level		–	550	–	mV
H	flash detection level hysteresis		400	–	–	mV
I_7	input current		–	–	±100	nA
RCONV INPUT (PIN 8)						
V_O	output voltage		3.7	3.9	4.1	V
I_8	current range		–50	–100	–100	µA
PROT INPUT (PIN 3)						
V_I	input voltage		0	–	V_{CC}	V
V_3	voltage detection level		3.8	4.0	4.2	V
I_I	input current		–	–	±10	µA

Notes to the characteristics

1. When f_{CLK} = 13.5 MHz, an increase of 10 mA in supply current should be expected.
2. When the prescaler is ON, one in two LLC HIGH periods is omitted.
3. The value of –46% corresponds with data 3F Hex and implies maximum 4th order.

TEST AND APPLICATION INFORMATION

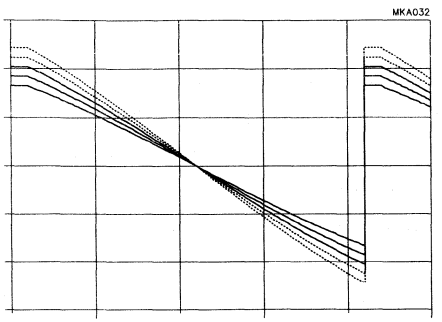


Fig.13 Control range amplitude.

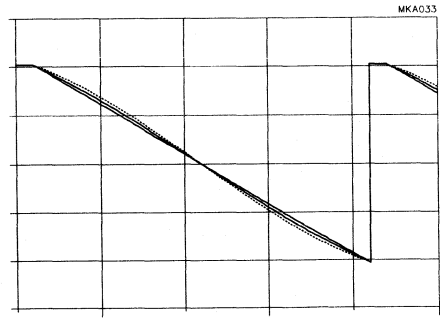


Fig.14 Control range S-correction.

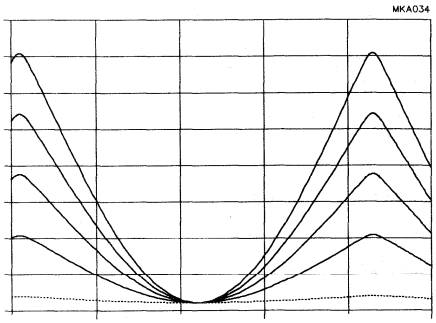


Fig.15 Control range EW parabola/width ratio.

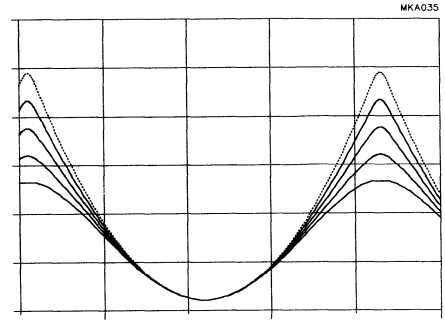


Fig.16 Control range EW corner/EW parabola ratio.

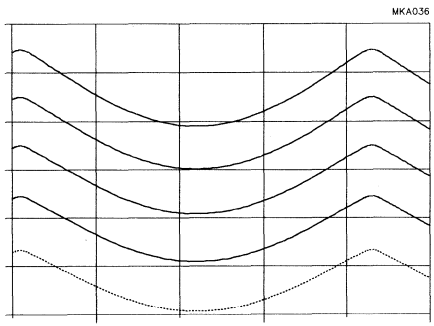


Fig.17 Control range EW width.

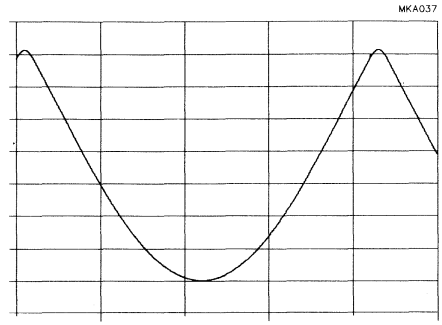
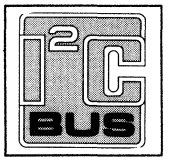


Fig.18 The BULT makes the EW waveform continuous.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Programmable deflection controller TDA9151



FEATURES

General

- 6.75, 13.5 and 27 MHz clock frequency
- Few external components
- Synchronous logic
- I²C-bus controlled
- Easy interfacing
- Low power
- ESD protection
- Two-level sandcastle pulse

Vertical deflection

- 16-bit precision vertical scan
- Self adaptive or programmable fixed slope mode
- DC coupled deflection to prevent picture bounce
- Programmable vertical expansion in the fixed slope mode
- S-correction can be preset
- S-correction setting independent of the field frequency
- Differential output for high DC stability
- Current source outputs for high EMC immunity

East-West correction

- DC coupled EW correction to prevent picture bounce
- 2nd and 4th order geometry correction can be preset
- Trapezium correction
- Geometry correction settings are independent of field frequency
- Self adaptive Bult generator prevents ringing of the horizontal deflection
- Current source output for high EMC immunity

Horizontal deflection

- φ 2 loop with low jitter
- Internal loop filter
- Dual slicer horizontal flyback input
- Soft start by I²C-bus
- Flash detector with automatic soft restart
- over-voltage protection with restart by I²C-bus

EHT correction

- Input selection between aquadag or EHT bleeder
- Internal filter

GENERAL DESCRIPTION

The TDA9151 is a programmable deflection controller contained in a 20-pin DIL package and constructed using BIMOS technology. This high performance synchronization and DC deflection processor has been especially designed for use in both digital and analog based TV receivers and monitors, and serves horizontal and vertical deflection functions for all TV standards. The TDA9151 uses a line-locked clock at 6.75, 13.5 or 27 MHz, depending on the line frequency and application, and requires only a few external components. The device can be programmed in a self adaptive mode or in a programmable fixed slope mode. Selection of these modes and a large number of other functions is fully programmable via the I²C-bus.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9151	20	DIL	plastic	SOT146

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	f_{CLK} = 6.75 MHz	–	22	–	mA
P_{tot}	total power dissipation		–	175	–	mW
T_{amb}	operating ambient temperature range		−25	–	+70	°C
Inputs						
V_{14}	line-locked clock (LLC) logic level		–	TTL	–	V
V_{13}	horizontal sync (H_A) logic level		–	TTL	–	V
V_{12}	vertical sync (V_A) logic level		–	TTL	–	V
V_5	line-locked clock select (LLCS) logic level	note 1	–	CMOS 5 V	–	V
V_{18}	serial clock (SCL) logic level		–	CMOS 5 V	–	V
V_{17}	serial data input (SDA) logic level		–	CMOS 5 V	–	V
V_1	horizontal flyback (HFB) phase slice level	FBL = 0 FBL = 1	– –	4.0 1.3	– –	V V
V_1	horizontal flyback (HFB) blanking slice level		–	100	–	mV
V_3	over-voltage protection (PROT) detection level		–	4.0	–	V
V_7	EHT flash detection level		–	550	–	mV
Outputs						
V_{20}	horizontal output (HOUT) voltage (open drain)	I_{20} = 10 mA	–	–	0.5	V
$I_{11}/I_{10(p-p)}$	vertical differential ($VOUT_{A, B}$) output current (peak-to-peak value)	vertical amplitude = 100%; I_8 = −100 µA	–	1000	–	µA
$V_{10,11}$	vertical output voltage range		0	–	3.9	V
$I_{6(peak)}$	EW (EWOUT) total output current (peak value)	I_8 = −100 µA	–	500	–	µA
V_6	EW (EWOUT) output voltage range		1.0	–	5.5	V
SANDCASTLE OUTPUT LEVELS (DSC)						
V_{BL}	base level		–	0.5	–	V
V_{HV}	horizontal and vertical blanking level		–	2.5	–	V
V_{clamp}	video clamp level		–	4.5	–	V

Note to the quick reference data

1. Hard wired to V_{SS} or V_{CC} is highly recommended.

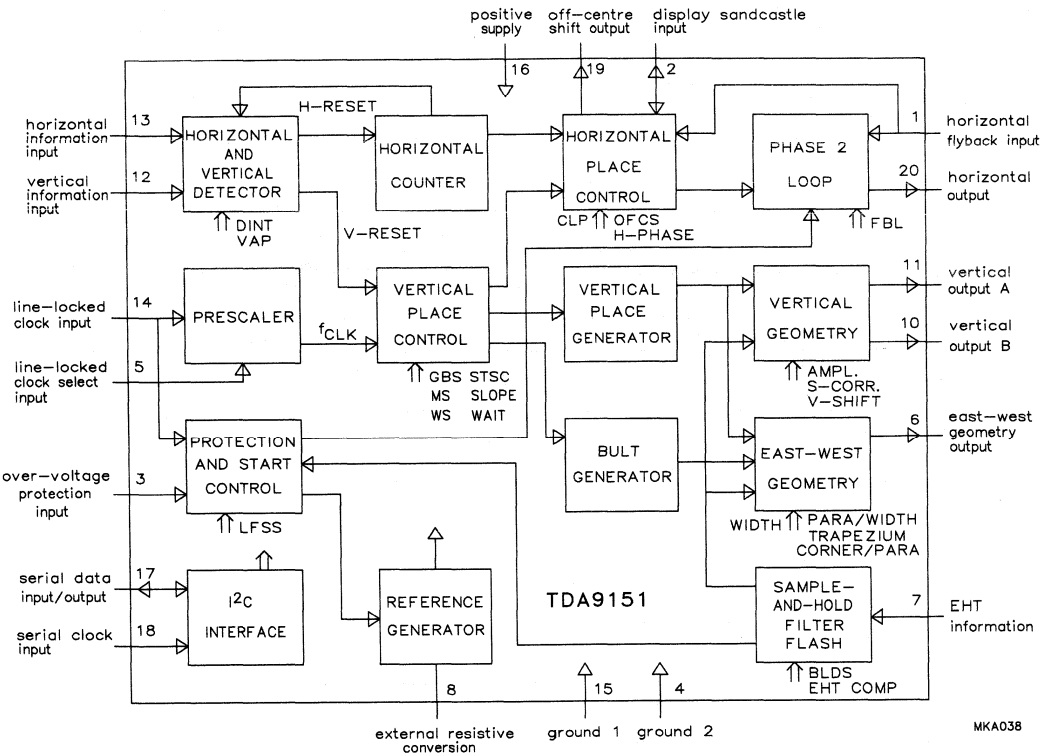


Fig.1 Block diagram.

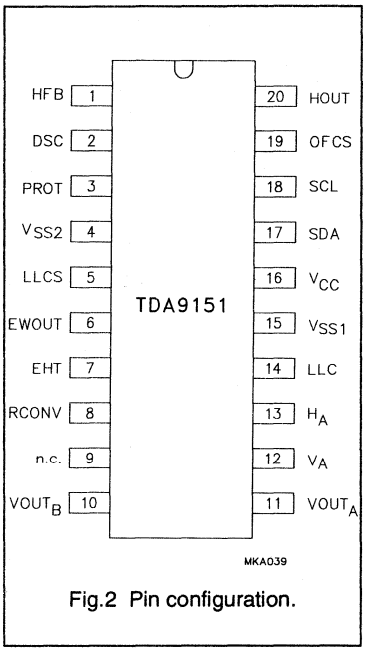


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
HFB	1	horizontal flyback input
DSC	2	display sandcastle input/output
PROT	3	over-voltage protection input
V_{SS2}	4	ground 2
LLCS	5	line-locked clock select input
EWOUT	6	east-west geometry output
EHT	7	EHT information
RCONV	8	external resistive conversion
n.c.	9	not connected
$VOUT_B$	10	vertical output B
$VOUT_A$	11	vertical output A
V_A	12	vertical information input
H_A	13	horizontal information input
LLC	14	line-locked clock input
V_{SS1}	15	ground 1
V_{CC}	16	positive supply input
SDA	17	serial data input/output
SCL	18	serial clock input
OFCS	19	off-centre shift output
HOUT	20	horizontal output

FUNCTIONAL DESCRIPTION

Input signals (pins 12, 13, 14, 17 and 18)

The TDA9151 requires three signals for minimum operation (apart from the supply). These signals are the line-locked clock (LLC) and the two I²C-bus signals (SDA and SCL). Without the LLC the device will not operate because the internal synchronous logic uses the LLC as the system clock.

I²C-bus transmissions are required to enable the device to perform its required tasks. Once started the IC will use the H_A and V_A for synchronization. If the LLC is not present the outputs will be switched off and all operations discarded (if the LLC is not present the line drive will be inhibited within 2 µs and the vertical and EW output current will drop to zero within 100 µs). The SDA and SCL inputs meet the I²C specification, the other three inputs are TTL compatible.

The LLC frequency can be divided by two internally by connecting LLCS (pin 5) to ground thereby enabling the prescaler.

The LLC timing is given in the characteristics.

I²C-bus commands

Slave address:
8C HEX = 1000110X BIN

READ MODE

The format of the status byte is;
PON PROT 0 0 0 0 0 0

Where;

PON is the status bit for power-on-reset and after power failure

logic 1 after the first POR and after power failure. Also set to 1 after a severe voltage dip that may have disturbed the various settings.

logic 0 after a successful read of the status byte.

PROT is the over-voltage detection for the scaled EHT

logic 1 if the input voltage rises above the reference value of 4 V. This results also in a reset of LFSS which terminates the deflection. A restart is achieved with an I²C-bus command i.e. by writing a logic 1 to LFSS (deflection will not start as long as the PROT bit is still logic 1; a read action must first be performed).

logic 0 after a successful read of the status byte.

Note: A read action is considered successful when an End Of Data signal has been detected (i.e. no master acknowledge).

Table 1 Write mode: subaddress and data byte format

FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
vertical amplitude	00	X	X	A5	A4	A3	A2	A1	A0
vertical S-correction	01	X	X	A5	A4	A3	A2	A1	A0
vertical start scan	02	X	X	A5	A4	A3	A2	A1	A0
vertical off-centre shift	03	X	*	*	*	X	A2	A1	A0
EW trapezium correction	03	X	A6	A5	A4	X	*	*	*
EW width/width ratio	04	X	X	A5	A4	A3	A2	A1	A0
EW parabola/width ratio	05	X	X	A5	A4	A3	A2	A1	A0
EW corner/parabola ratio	06	X	X	A5	A4	A3	A2	A1	A0
EHT compensation	07	X	X	A5	A4	A3	A2	A1	A0
horizontal phase	08	X	X	A5	A4	A3	A2	A1	A0
horizontal off-centre shift	09	X	X	A5	A4	A3	A2	A1	A0
clamp shift	0A	X	X	X	X	X	A2	A1	A0
control	0B	MS	WS	FBL	VAP	BLDS	LFSS	DINT	GBS
vertical slope MSB	0C	A7	A6	A5	A4	A3	A2	A1	A0
vertical slope LSB	0D	A7	A6	A5	A4	A3	A2	A1	A0
vertical wait	0E	A7	A6	A5	A4	A3	A2	A1	A0

Where: X = don't care; * = data bit used in another function

Table 2 Control bits

CONTROL BIT	LOGIC	FUNCTION
LFSS	0	line stop: becomes 0 after a HIGH on PON or PROT
	1	line start enable: the soft start mechanism is now activated
DINT	0	de-interlace ON: the V_A pulse is sampled with the detected rising edge of H_A
	1	de-interlace OFF: the V_A pulse is sampled with the system clock and the detected rising edge is used as vertical reset
BLDS	0	aquadag selected
	1	bleeder selected
GBS	0	guardband 16/12 lines: becomes 0 after power-on
	1	guardband 48/12 lines
VAP	0	positive $V_A$edge detection
	1	negative $V_A$edge detection
FBL	0	horizontal flyback slicing level = 4 V
	1	horizontal flyback slicing level = 1.3 V
WS	0	no wait state
	1	programmable wait state (only in constant slope mode MS = 1)
MS	0	adaptive mode with guardband amplitude control
	1	constant slope mode (programmable)

Table 3 Clock frequency control bit (pin 5)

CONTROL BIT	LOGIC	FUNCTION
LLCS	0	prescaler ON: the internal clock frequency $f_{CLK} = f_{LLC}/2$
	1	prescaler OFF: (default by internal pull-up resistor). The internal clock frequency $f_{CLK} = f_{LLC}$

Note to Table 3

Switching of the prescaler is only allowed when LFSS is LOW. It is highly recommended to hard wire LLCS to V_{SS} or V_{CC}.

Active switching may damage the output power transistor due to the changing HOUT pulse. This may cause very high currents and huge flyback pulses. The permitted combinations of LLC and the prescaler are given in table 4.

Table 4 Line duration with prescaler

LLC (MHz)	ON (µs)	OFF (µs)
6.75	*	64
13.5	64	32
27	32	*

Where: * = not allowed combination.

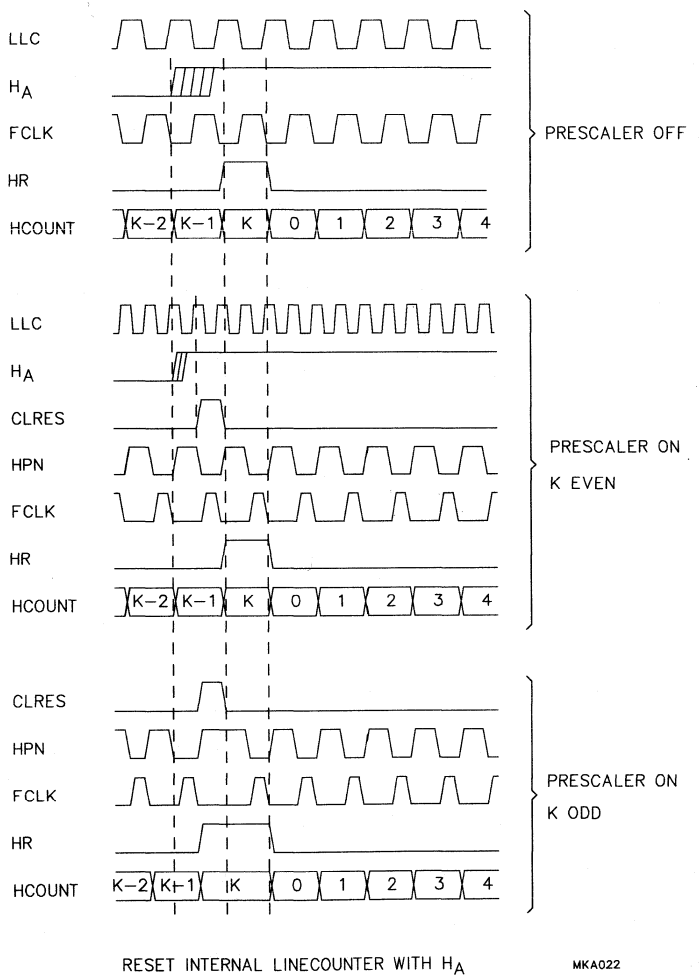


Fig.3 Timing relations between LLC, H_A and line counter.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

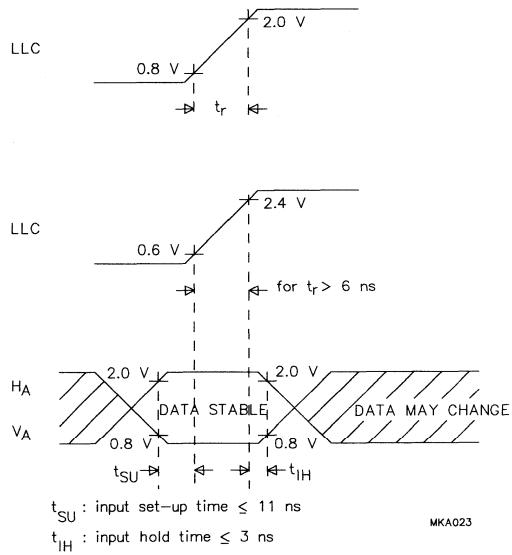


Fig.4 Timing requirements for LLC, H_A and V_A.

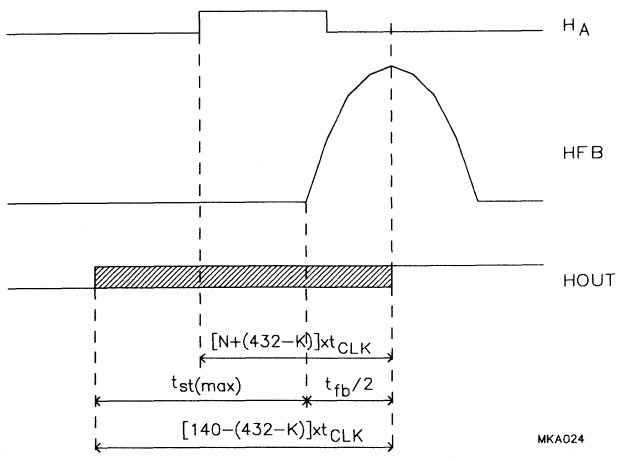


Fig.5 Horizontal phase and HOUT control range.

Horizontal part (pins 1, 2, 13, 19 and 20)

SYNCHRONIZATION PULSE

The H_A input (pin 13) is a TTL-compatible ESD protected CMOS input. Pulses at this input have to fulfil the timing requirements as illustrated in Fig.4. For proper detection the minimum pulse width for both the HIGH and LOW period is 2 internal clock periods.

FLYBACK INPUT PULSE

The HFB input (pin 1) is an ESD protected CMOS input. The delay of the centre of the flyback pulse to the leading edge of the H_A pulse can be set via the I²C-bus with the horizontal phase byte (subaddress 08), as illustrated in Fig.5. The resolution is 6-bit.

OUTPUT PULSE

The HOUT pulse (pin 20) is an ESD protected open-drain NMOS output. The duty factor for this output is typically 55/45 (conducting/non-conducting) during normal operation. A soft start causes the duty factor to increase linearly from 0 to 55% over a period of 400 lines in 400 steps.

OFF-CENTRE SHIFT

The OFCS output (pin 19) is an ESD protected push-pull CMOS output which is driven by a pulse-width modulated DAC.
By using a suitable interface, the output signal can be used for off-centre shift correction in the horizontal output stage. This correction is required for HDTV tubes with a 16 x 9 aspect ratio and is useful for high performance flat square tubes to obtain the required horizontal linearity. For applications where off-centre correction is not required, the output can be used as an auxiliary DAC. The OFCS signal is phase-locked with the line frequency. The off-centre shift can be set via the I²C-bus, subaddress 09, with a 6-bit resolution as illustrated in Fig.6.

SANDCASTLE

The DSC input/output (pin 2) acts as a sandcastle generating output and a guard sensing input. As an output it provides 2 levels (apart from the base level), one for the horizontal and vertical blanking and the other for the video clamp. As an input it acts as a current sensor during the blanking interval for guard detection.

Clamp pulse

The clamp pulse width is 21 internal clock periods. The shift, w.r.t. H_A can be varied from 35 to 49 clock periods in 7 steps via the I²C-bus, clamp shift byte subaddress 0A, as illustrated in Fig.7

Horizontal blanking

The start of the horizontal blanking pulse is minimum 38 and maximum 41 clock periods before the centre of the flyback pulse, depending on the f_{CLK}/f_H ratio 'K' [according to 41–(432–K)].
When the horizontal blanking pulse finishes is determined by the trailing edge of the HFB pulse at the horizontal blanking slicing level coincidence, as illustrated in Fig.8.

Vertical blanking

The vertical blanking pulse starts two internal clock pulses after the rising edge of the V_A pulse. During this interval a small guard pulse, generated during flyback by the vertical power output stage, must be inserted. Stop vertical blanking is effected at the end of the blanking interval only when the guard pulse is present (see Vertical guard).

The start scan setting determines the end of vertical blanking with a 6-bit resolution in steps of one line via the I²C-bus subaddress 02, (see Figs 9 and 10).

Vertical guard

In the vertical blanking interval a small unblanking pulse is inserted. This pulse must be filled-in by a blanking pulse or guard pulse from the vertical power output stage which was generated during the flyback period. In this condition the sandcastle output acts as guard detection input and requires a minimum 500 µA input current. This current is sensed during the unblanking period. Vertical blanking is only stopped at the end of the blanking interval when the inserted pulse is present. In this way the picture tube is protected against damage in case of missing or malfunctioning vertical deflection.

Vertical part (pins 6, 8, 10, 11 and 12)

Synchronization pulse

The V_A input (pin 12) is a TTL-compatible ESD protected CMOS input. Pulses at this input have to fulfil the timing requirements as illustrated in Fig.4. For proper detection the minimum pulse width for both the HIGH and LOW period is 2 internal clock periods.

VERTICAL PLACE GENERATOR

An overview of the various modes of operation of the vertical place generator is illustrated in Fig.11.

VERTICAL PLACE GENERATOR IN ADAPTIVE MODE (MS = 0)

The vertical start-scan data (subaddress 02) determines the vertical placement in the total range of 64 x 432 clock periods, in 63

steps. The maximum number of synchronized lines per scan is 910 with an equivalent field frequency of 17.2 or 34.4 Hz for f_H = 15625 or 31250 Hz respectively.
The minimum number of synchronized lines per scan is 200 with an equivalent field frequency of 78 or 156 Hz for f_H = 15625 or 31250 Hz respectively.
If the V_A pulse is not present, the number of lines per scan will increase to 910.2. If the LLC is not present the vertical blanking will start within 2 µs.
Amplitude control is automatic, with a setting time of 1 to 2 new fields and an accuracy of either 16/12 or 48/12 lines depending on the value of the GBS bit

Differences in the number of lines per field, as can occur in TXT or in multi-head VTR, will not affect the amplitude setting providing the differences are less than the value selected with GBS. This is called amplitude control guardband. The difference sequence and the difference sequence length are not important.

Vertical place generator in constant slope mode (MS = 1)

In this mode the slope can be programmed directly with a two byte value on subaddress 0C (MSB) and 0D (LSB). When the actual number of lines is greater than the programmed number of lines, the circuit will enter the stop condition causing the differential vertical output current to drop to zero.
The programmed value for the slope is the required number of lines multiplied by 72. The programming limits are; minimum 200 x 72 and maximum 910 x 72.
A vertical expansion is obtained with a combination of slope data and a programmable wait status, at subaddress 0E. The wait status is selected with control bit MS and can only be activated in the constant slope mode. The wait state is an 8-bit value, programmable from 0 to 255. The actual wait state is one line longer than the programmed value.
If blanking is applied during stop and wait status the differential output current will drop to zero.

De-interlace

With De-interlace ON, the V_A pulse is sampled with the detected rising edge of the H_A pulse. The duration of the V_A pulse must, therefore, be sufficient to enable the H_A pulse to coincide, in this case an active time of minimum of half a line (see Fig.12).
With De-interlace OFF, the V_A pulse is sampled with the system clock. The rising edge is used as the vertical reset.

Vertical geometry processing

The vertical geometry processing is DC-coupled and therefore independent of field frequency. The resistive conversion (pin 8) sets the reference current for both the vertical and EW geometry processing. A useful range is 50 to 100 µA, the recommended value is 100 µA.

Vertical outputs

The vertical outputs (pins 10 and 11) together form a differential current output and are ESD protected. The vertical amplitude can be varied over the range 80 to 120% in 63 steps via the I²C-bus (subaddress 00). Vertical S-correction is also applied to these outputs and can be set from 0 to 16% by subaddress 01 with 6-bit resolution.
The vertical off-centre shift (OFCS) shifts the vertical deflection current zero crossing with respect to the EW parabola bottom. The control range is –2 to +2% in 7 steps set by the least significant nibble at subaddress 03.

EW geometry processing

The EW geometry processing is DC-coupled and therefore independent of field frequency. The resistive conversion (pin 8) sets the reference current for both the vertical and EW geometry processing. The EW output is an ESD-protected single-ended current output.
The EW width/width ratio can be set from 100 to 80% in 63 steps via subaddress 04 and the EW parabola/width ratio from 0 to 20% via subaddress 05. The EW corner/EW parabola ratio has a control range of –46 to 0% in 63 steps via subaddress 06.
The EW trapezium correction can be set from –4 to +4% in 7 steps via the most significant nibble at subaddress 03

Bult generator

The Bult generator makes the EW waveform continuous (see Fig.19).

EHT compensation (pin 7)

The EHT input is an ESD protected MOS input which permits scan amplitude modulation should the EHT supply be non-perfect. For correct tracking of the vertical and horizontal deflection the gain of the EW output stage, given by the ratio R_{conv}–EW/R_{conv}, must be $V_{scan}/20 \times V_{ref}$ (see Fig.13). The input for EHT compensation can be derived from an EHT bleeder or from the picture tubes aquadag (subaddress 0B, bit BLDS). EHT compensation can be set via subaddress 07 in 63 steps allowing a scan modulation range from –10 to +9.7%. When the EHT input voltage drops below 0.55 V the outputs will be inhibited and an automatic restart will be performed.

Over-voltage protection (pin 3)

The PROT input is an ESD protected MOS input.
The input voltage can be the scaled EHT and has the following characteristics:

If the protection voltage is less than 4 V do nothing
If the protection voltage is greater than 4 V stop line drive

Restart by I²C-bus command:

1. perform read action to clear the PROT bit
2. write the LFSS bit

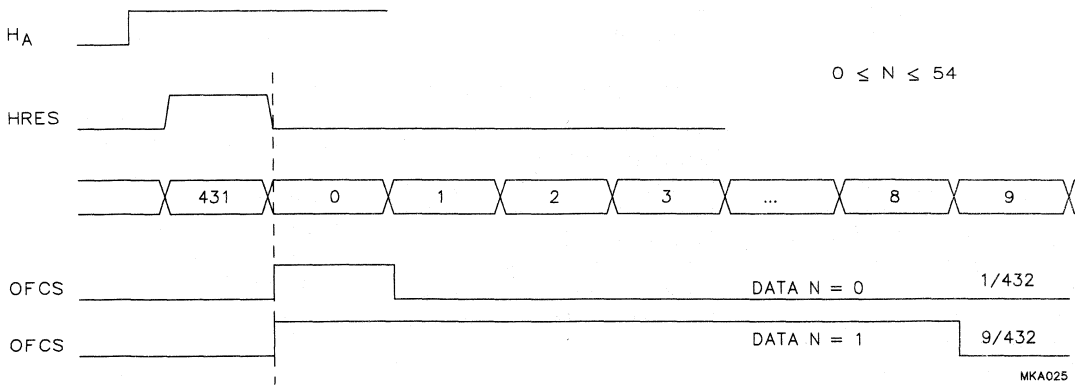


Fig.6 OFCS duty factor.

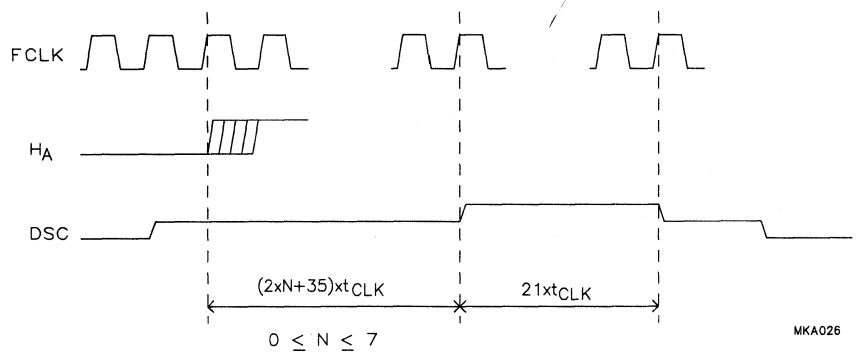


Fig.7 DSC clamp pulse.

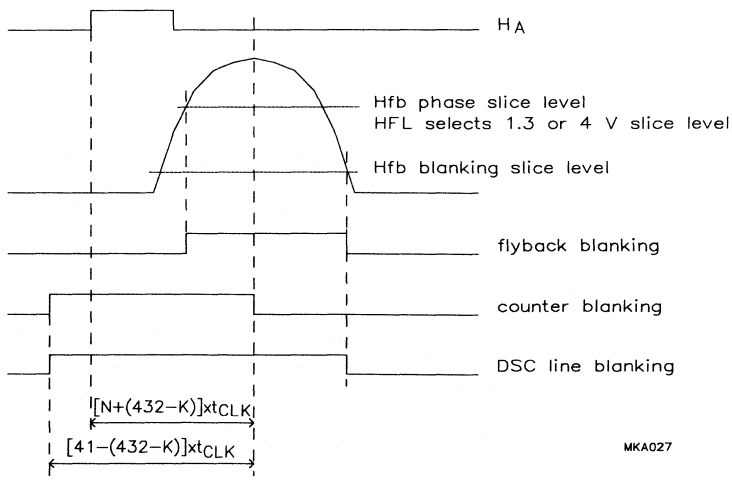


Fig.8 DSC line blanking.

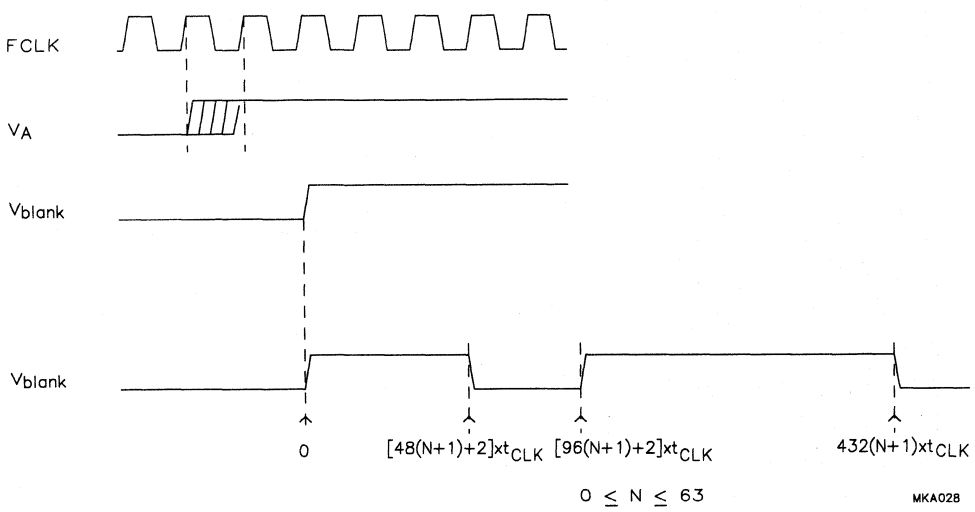


Fig.9 DSC vertical blanking with unblanking.

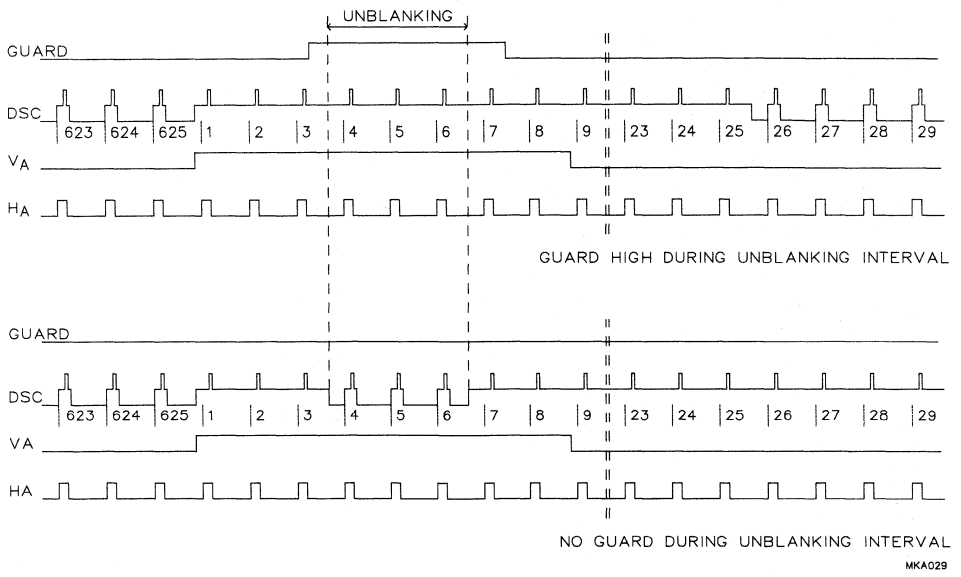


Fig.10 DSC with guard interval.

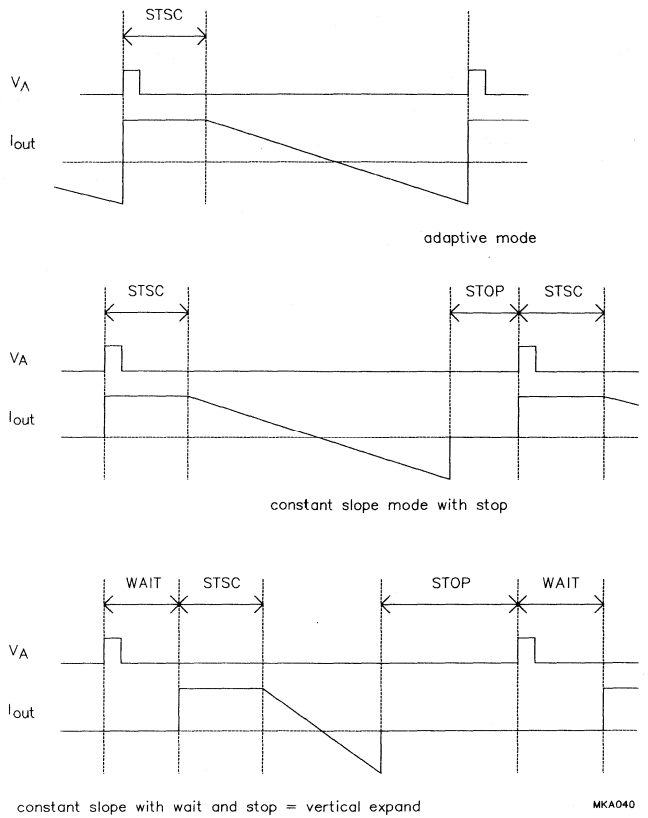


Fig.11 Vertical deflection operating modes.

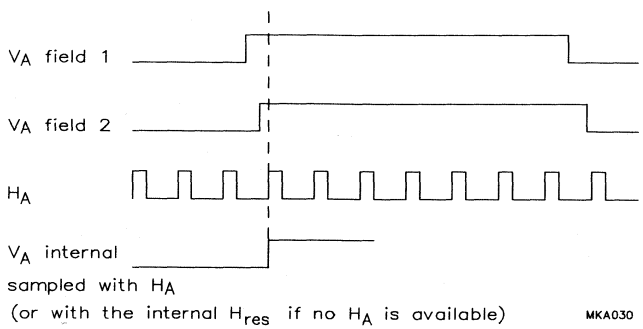


Fig.12 De-interlace timing.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	positive supply voltage		−0.5	8.8	V
I_{CC}	supply current		−10	50	mA
P_{tot}	total power dissipation		−	500	mW
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	operating ambient temperature range		−25	+70	°C
V_{supply}	voltage supplied to pins 1 to 3, 5 to 8, 10 to 14 and 17 to 20		−0.5	V_{CC}+0.5	V
$I_{I/O}$	current in or out of any pin except pins 4, 15 and 16		−20	+20	mA

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	70 K/W

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; V_{SS1} = V_{SS2} = 0 V; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	note 1; f_{CLK} = 6.75 MHz	17	22	28	mA
P_{tot}	total power dissipation		−	175	−	mW
SDA and SCL (pins 17 and 18)						
V_{17}	SDA input voltage		0	−	5.5	V
V_{IL}	LOW level input voltage (pin 17)		−	−	1.5	V
V_{IH}	HIGH level input voltage (pin 17)		3.5	−	−	V
I_{IL}	LOW level input current (pin 17)	$V_{17} = V_{SS1}$	−	−	−10	µA
I_{IH}	HIGH level input current (pin 17)	$V_{17} = V_{CC}$	−	−	10	µA
V_{OL}	LOW level output voltage (pin 17)	I_{IL} = 3 mA	−	−	0.4	V
V_{18}	SCL input voltage		0	−	5.5	V
V_{IL}	LOW level input voltage (pin 18)		−	−	1.5	V
V_{IH}	HIGH level input voltage (pin 18)		3.5	−	−	V
I_{IL}	LOW level input current (pin 18)	$V_{18} = V_{SS1}$	−	−	−10	µA
I_{IH}	HIGH level input current (pin 18)	$V_{18} = V_{CC}$	−	−	10	µA
Line locked clock and Line locked clock select (pins 14 and 5)						
V_{IL}	LOW level input voltage (pin 14)		−	−	0.8	V
V_{IH}	HIGH level input voltage (pin 14)		2.0	−	−	V
I_{14}	input current	V_{14} = < 5.5 V	−	−	±10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r, t_f	rise and fall times		0	–	$t_{LLC}/2$	ns
	duty factor	note 2; LLCS = 0	40	50	60	%
		LLCS = 1	25	50	75	%
TIMING (PRESCALER ON) ($F_{CLK} = F_{LLC}/2$) WHERE F_{CLK} = INTERNAL CLOCK						
f_{LLC}	line-locked clock frequency		12.4	–	29.2	MHz
		f_{LLC}/f_H; H locked	856	864	865	
		f_{LLC}/f_H; H unlocked	–	866	–	
K	line-locked clock frequency ratio	f_{CLK}/f_H; H locked	428	432	432.5	
		f_{CLK}/f_H; H unlocked	–	433	–	
TIMING (PRESCALER OFF) ($F_{CLK} = F_{LLC}$) WHERE F_{CLK} = INTERNAL CLOCK						
f_{LLC}	line-locked clock frequency		6.2	–	14.6	MHz
		f_{LLC}/f_H; H locked	428	432	432	
		f_{LLC}/f_H; H unlocked	–	433	–	
K	line-locked clock frequency ratio	f_{CLK}/f_H; H locked	428	432	432	
		f_{CLK}/f_H; H unlocked	–	433	–	
V_5	LLCS input voltage		0	–	8.8	V
V_{IL}	LOW level input voltage (pin 5)		–	–	1.5	V
V_{IH}	HIGH level input voltage (pin 5)		3.5	–	–	V
I_{IL}	LOW level input current (pin 5)	$V_5 = V_{SS1}$	–	–	–150	µA
I_{IH}	HIGH level input current (pin 5)	$V_5 = V_{CC}$	–	–	100	µA
Horizontal part						
INPUT SIGNALS						
H_A (pin 13)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_I	input current	V_{13} = 5.5 V	–	–	±10	µA
t_r; t_f	rise and fall times		0	–	$t_{LLC}/2$	ns
t_{WH}	pulse width HIGH		2	–	–	t_{CLK}
t_{WL}	pulse width LOW		2	–	–	t_{CLK}
HFB (pin 1)						
V_{PS1}	phase slice level	FBL = 0	3.8	4.0	4.2	V
V_{PH2}	phase slice level	FBL = 1	1.1	1.3	1.5	V
V_{blank}	blanking slice level		0	0.1	0.2	V
I_1	input current		–	–	±10	µA
Horizontal phase (delay centre flyback pulse to leading edge of H_A; where N = horizontal phase data)						
CR	control range		0	N	N+(432–K)	t_{CLK}
	number of steps		–	63	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OUTPUT SIGNALS						
HOUT (pin 20)						
V_{20}	output voltage	I_{20} = 0	0	–	V_{CC}	V
V_{OL}	LOW level output voltage	I_{20} = 10 mA	–	–	0.5	V
I_I	input current	output OFF	–	–	±10	µA
	duty factor	normal operation	54.5	55.5	56.5	%
Soft start (duty factor controlled line drive)						
t_W	initial pulse width soft start		–	–	1.5	%
CR	control range		0	–	56.5	%
t_{ss}	soft start time		250	400	600	lines
Switch-off time to the centre of the flyback pulse						
CR	control range		0	–	140–(432–K)	t_{CLK}
Φ	control sensitivity (loop gain)		400	1000	–	µs/µs
f_G/f_H	unity gain frequency ratio		–	0.15	–	
t_{pj}	phase jitter with respect to LLC		–	–	5	ns
PSRR	power supply rejection ratio		tbf	–	–	µs/V
HORIZONTAL OFF-CENTRE SHIFT (PIN 19) (N = OFF-CENTRE SHIFT DATA)						
V_{19}	output voltage		0	–	V_{CC}	V
V_{OL}	LOW level output voltage	I_{19} = 2 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{19} = –2 mA	V_{CC}–0.5	–	–	V
	maximum duty factor	N < 54	1/K	(8N+1)/K	425/K	%
	duty factor	N ≥ 54	–	1	–	%
	number of steps		–	54	–	
SANDCASTLE (PIN 2)						
DSC output voltage						
V_{clamp}	video clamp voltage		4.0	4.5	5.0	V
V_{blank}	horizontal and vertical blanking level		2.0	2.5	3.0	V
V_{base}	base level		0	0.5	1.0	V
I_2	output current		–1.0	–	0.35	mA
		guard detected	0.8	–	2.5	mA
t_r; t_f	rise and fall times		–	60	–	ns
Clamp pulse (N = clamp pulse shift data)						
t_W	clamp pulse width		–	21	–	t_{CLK}
t_{clamp}	clamp pulse shift w.r.t H_A		35	2N+35	49	t_{CLK}
	number of steps		–	7	–	
t_{start}	start of horizontal blanking before middle of flyback pulse		38	41–(432–K)	41	t_{CLK}

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical blanking width (N = vertical start–scan data)						
CR	control range		1	N+1	64	t_{CLK} x 432
		K = 432	1	–	64	lines
	number of steps		–	63	–	
Guard detection (N = vertical start–scan data)						
t_{start}	start interval w.r.t V_A	no wait	48(N+1)+2	–	–	t_{CLK}
t_{stop}	stop interval w.r.t V_A	no wait	96(N+1)+2	–	–	t_{CLK}
Vertical section						
INPUT SIGNALS (PIN 12) (V_A)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{12}	input current	V_{12} < 5.5 V	–	–	±10	µA
t_r; t_f	rise and fall times		0	–	$t_{LLC}/2$	t_{CLK}
t_{WH}	pulse width HIGH		2	–	–	t_{CLK}
t_{WL}	pulse width LOW		2	–	–	t_{CLK}
t_{WH}	pulse width HIGH	de-interlace mode	0.5	–	–	t_{line}
t_{WL}	pulse width LOW	de-interlace mode	0.5	–	–	t_{line}
VERTICAL PLACE GENERATOR IN ADAPTIVE SLOPE MODE (N = VERTICAL START–SCAN DATA)						
CR	control range		1	N+1	64	t_{CLK} x 432
		K = 432	1	–	64	lines
	number of steps		–	63	–	
$Lines_{max}$	maximum number of synchronized lines per scan		–	910	–	lines/scan
f_{eq}	equivalent field frequency at 910 lines/scan	f_H = 15625 Hz	–	17.2	–	Hz
		f_H = 31250 Hz	–	34.4	–	Hz
$Lines_{min}$	minimum number of synchronized lines per scan		–	200	–	lines/scan
f_{eq}	equivalent field frequency at 200 lines/scan	f_H = 15625 Hz	–	78	–	Hz
		f_H = 31250 Hz	–	156	–	Hz
CA	amplitude control		–	automatic	–	
CA_g	amplitude control guardband	GBS = 0	–	16/12	–	lines
		GBS = 1	–	48/12	–	lines
	setting time		1	1.5	2	newfields

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL PLACE GENERATOR IN CONSTANT SLOPE MODE (N = VERTICAL WAIT DATA)						
CR	control range		1	N+1	256	t_{CLK} x 432
		K = 432	1	–	256	lines
	number of steps		–	255	–	
	programmable slope		200	–	910	lines/scan
	programmable slope data	2 byte instruction; number of lines x 72	200 x 72	–	910 x 72	lines
VERTICAL GEOMETRY PROCESSING						
$I_{diff(p-p)}$	vertical output differential current (peak-to-peak value)	I_8 = –100 µA	0.96	1.0	1.04	mA
D/ΔT	drift over temperature range		–	10^{-4}	–	
	amplitude error due to S-correction setting		–	tbf	–	%
I_{bias}	vertical output signal bias current		–	–300	–	µA
I_{os}	vertical output offset current		–	–	tbf	µA
OS/ΔT	offset over temperature range		–	–	tbf	µA/K
$V_{10, 11}$	vertical output voltage range		0	–	3.9	V
CMRR	common mode rejection ratio		–	tbf	–	dB
LE	linearity error		–	0.2	2.0	%
Vertical amplitude (N = vertical amplitude data)						
CR	control range		80	–	120	%
	number of steps		–	63	–	
Vertical S-correction (N = S-correction data)						
CR	control range		0	–	16	%
	number of steps		–	63	–	
Vertical shift						
CR	control range		–2	–	+2	%
	number of steps		–	7	–	
EW OUTPUT (PIN 6)						
V_6	output voltage range		0.5	–	5.5	V
I_6	output current range	I_8 = –100 µA	0	–	1000	µA
EW width/width ratio						
CR	control range		100	–	80	%
I_{eq}	equivalent output current		0	–	400	µA
	number of steps		–	63	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EW parabola/width ratio						
CR	control range		0	–	20	%
I_{eq}	equivalent output current	width = 100%	0	–	400	µA
		width = 80%	0	–	320	µA
	number of steps		–	63	–	
EW corner/EW parabola ratio (note 3)						
CR	control range		–46	–	0	%
I_{eq}	equivalent output current	width = 100%	0	–	184	µA
		width = 80%	0	–	147	µA
	number of steps		–	63	–	
EW trapezium correction						
	EW trapezium/width ratio		–4	–	+4	%
	number of steps		–	7	–	
EHT INPUT (PIN 7)						
V_{ref}	reference voltage	BLDS = 1	–	3.9	–	V
		BLDS = 0	–	V_{CC}	–	V
V_I	input voltage range w.r.t V_{ref}	BLDS = 1	–20	–	+20	%
V_I	input voltage range w.r.t V_{CC}	BLDS = 0	–	0	$-2V_{ref}$	V
m_{scan}	scan modulation range		–10	0	+9.7	%
m_{GC}	modulation gain control		0	–	1	
	number of steps		–	63	–	
V_7	flash detection level		–	550	–	mV
H	flash detection level hysteresis		400	–	–	mV
I_7	input current		–	–	±100	nA
RCONV INPUT (PIN 8)						
V_O	output voltage		3.7	3.9	4.1	V
I_8	current range		–50	–100	–100	µA
PROT INPUT (PIN 3)						
V_I	input voltage		0	–	V_{CC}	V
V_3	voltage detection level		3.8	4.0	4.2	V
I_I	input current		–	–	±10	µA

Notes to the characteristics

1. When f_{CLK} = 13.5 MHz, an increase of 10 mA in supply current should be expected.
2. When the prescaler is ON, one in two LLC HIGH periods is omitted.
3. The value of –46% corresponds with data 3F Hex and implies maximum 4th order.

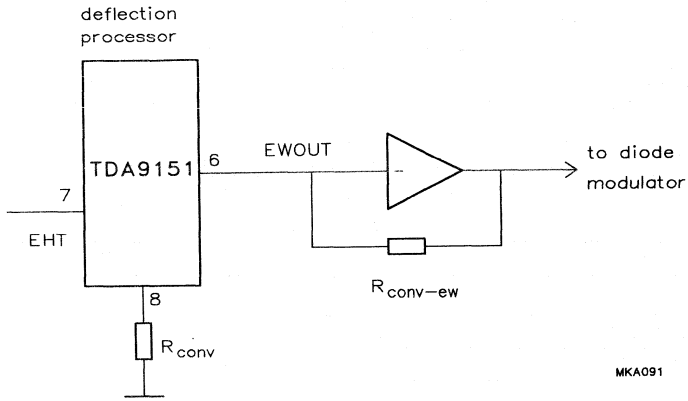


Fig.13 Explanation of R_{conv_EW}/R_{conv} ratio.

TEST AND APPLICATION INFORMATION

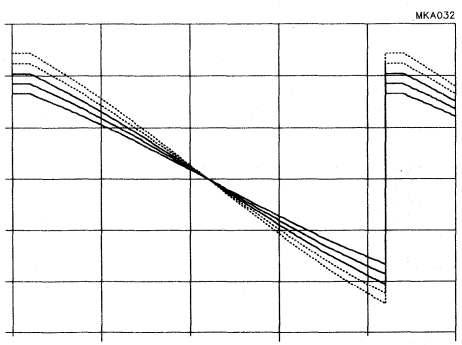


Fig.14 Control range amplitude.

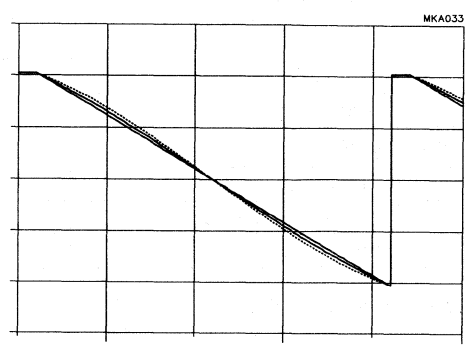


Fig.15 Control range S-correction.

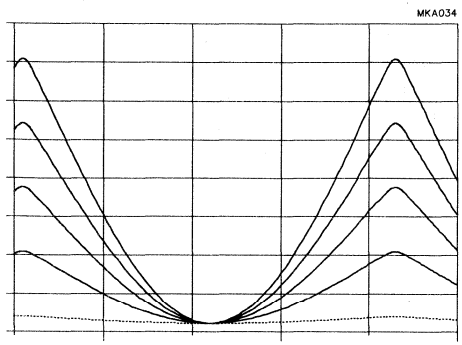


Fig.16 Control range EW parabola/width ratio.

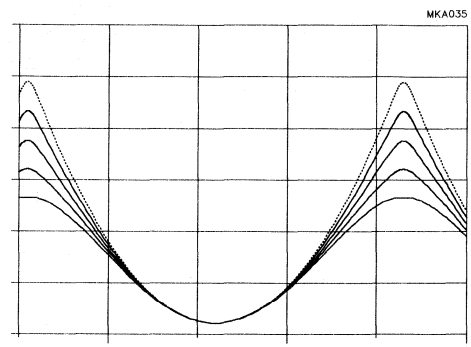


Fig.17 Control range EW corner/EW parabola ratio.

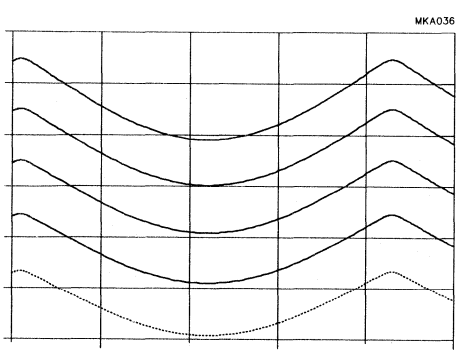


Fig.18 Control range EW width.

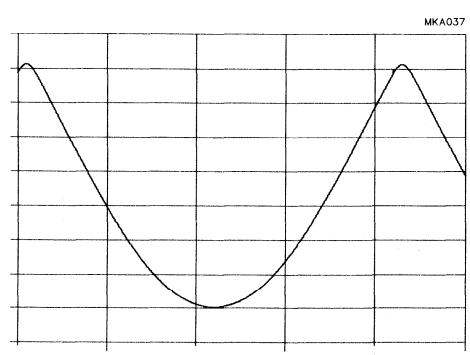


Fig.19 The BULT makes the EW waveform continuous.

PAL/NTSC/SECAM decoder/sync processor

TDA9160

FEATURES

- Multistandard PAL, NTSC and SECAM
- I²C-bus controlled
- I²C-bus addresses can be selected by hardware
- Alignment free
- Few external components
- Designed for use with baseband delay lines
- Integrated video filters
- Horizontal and vertical drive output
- East-West correction drive output
- Two CVBS inputs
- S-VHS input
- Vertical divider system
- H_A synchronization pulse
- Two level sandcastle pulse

GENERAL DESCRIPTION

The TDA9160 is an I²C-bus controlled, alignment-free PAL/NTSC/SECAM decoder/processor. The device contains horizontal and vertical drive outputs and an east-west correction drive circuit. The TDA9160 has been designed for use with baseband chrominance delay lines and DC-coupled vertical and east-west output circuits.
The device has three inputs, two for CVBS and one for S-VHS. The main signal is available at the luminance and colour difference outputs and, also, at the TXT output (unprocessed). The signal at the PIP output can be selected independently from the main signal.
The circuit provides a drive pulse for the horizontal output stage, a differential sawtooth current for the vertical output stage and an east-west drive current for the EW output stage. These signals can be used to provide geometry correction of the picture. A two level sandcastle pulse and an H_A pulse are made available for synchronization purposes.
The I²C-bus address of the TDA9160 can be programmed by hardware.

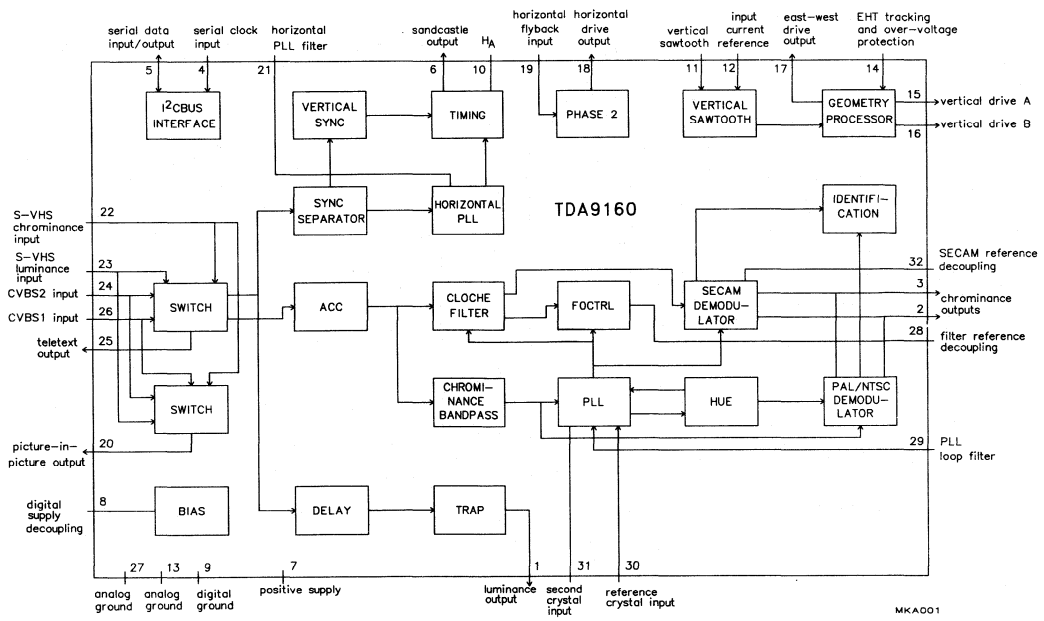


Fig.1 Block diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		–	50	–	mA
$V_{24,26(p-p)}$	CVBS input voltage (peak-to-peak value)		–	1.0	–	V
$V_{23(p-p)}$	S-VHS luminance input voltage (peak-to-peak value)		–	1.0	–	V
$V_{22(p-p)}$	S-VHS chrominance burst input voltage (peak-to-peak value)		–	0.3	–	V
$V_{1(p-p)}$	luminance output voltage (peak-to-peak value)		–	0.45	–	V
$V_{25(p-p)}$	teletext output voltage (peak-to-peak value)		–	1.0	–	V
$V_{2(p-p)}$	chrominance output voltage –(R-Y) (peak-to-peak value)	PAL/NTSC	–	525	–	mV
$V_{2(p-p)}$	chrominance output voltage –(R-Y) (peak-to-peak value)	SECAM	–	1.05	–	V
$V_{3(p-p)}$	chrominance output voltage –(B-Y) (peak-to-peak value)	PAL/NTSC	–	665	–	mV
$V_{3(p-p)}$	chrominance output voltage –(B-Y) (peak-to-peak value)	SECAM	–	1.33	–	V
V_{10}	H_A output voltage		–	5.0	–	V
$I_{15,16(p-p)}$	vertical drive output current (peak-to-peak value)		–	1	–	mA
I_{18}	horizontal drive output current		–	–	10	mA
I_{17}	EW drive output current		–	–	0.9	mA
V_6	sandcastle clamping voltage level		–	4.5	–	V
V_6	sandcastle blanking voltage level		–	2.5	–	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9160	32	SDIL	plastic	SOT232

PAL/NTSC/SECAM decoder/sync processor

TDA9160

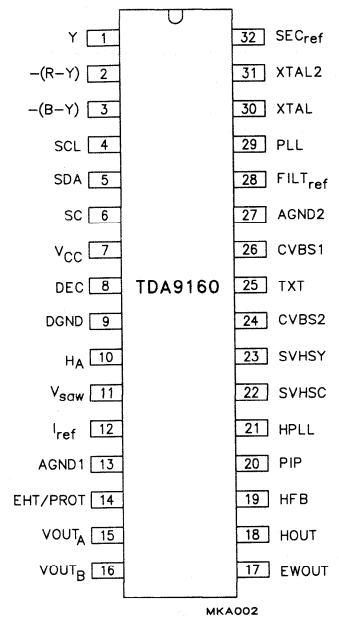


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
Y	1	luminance output
−(R-Y)	2	chrominance output
−(B-Y)	3	chrominance output
SCL	4	serial clock input
SDA	5	serial data input/output
SC	6	sandcastle output
V_{CC}	7	positive supply input
DEC	8	positive supply decoupling
DGND	9	digital ground
H_A	10	horizontal acquisition synchronization pulse
V_{saw}	11	vertical sawtooth
I_{ref}	12	input current reference
AGND1	13	analog ground
EHT/PROT	14	EHT tracking and over-voltage protection
$VOUT_A$	15	vertical drive output A
$VOUT_B$	16	vertical drive output B
EWOUT	17	east-west drive output
HOUT	18	horizontal drive output
HFB	19	horizontal flyback input
PIP	20	picture-in-picture output
HPLL	21	horizontal PLL filter
SVHSC	22	S-VHS chrominance input
SVHSY	23	S-VHS luminance input
CVBS2	24	CVBS2 input
TXT	25	teletext output
CVBS1	26	CVBS1 input
AGND2	27	analog ground
$FILT_{ref}$	28	filter reference decoupling
PLL	29	colour PLL filter
XTAL	30	reference crystal input
XTAL2	31	second crystal input
SEC_{ref}	32	SECAM reference decoupling

FUNCTIONAL DESCRIPTION

The TDA9160 is an I²C-bus controlled, alignment free PAL/NTSC/SECAM colour decoder/sync processor/deflection controller which has been designed for use with baseband chrominance delay lines.
In the standard operating mode the I²C-bus address is 8A . If the TXT output is connected to the positive rail the address will change to 8E

The standards which the TDA9160 can decode are dependent on the choice of external crystals. If a 4.4 MHz and a 3.6 MHz crystal are used then SECAM, PAL 4.4/3.6 and NTSC 4.4/3.6 can be decoded. If two 3.6 MHz crystals are used then only PAL 3.6 and NTSC 3.6 can be decoded. Which 3.6 MHz standards can be decoded is dependent on the exact frequencies of the crystal. In an application where not all standards are required only one crystal is sufficient (in this instance the crystal must be connected to the reference crystal input (pin 30)). If a 4.4 MHz crystal is used it must always be connected to pin 30. Both crystals are used to provide a reference for the filters and the horizontal PLL, however, only the reference crystal is used to provide a reference for the SECAM demodulator.
To enable the calibrating circuits to be adjusted exactly two bits from the I²C-bus address are used to indicate which crystals are connected to the IC.

The standard identification circuit is a digital circuit without external components; the search loop is illustrated in Fig.3.

The decoder (via the I²C-bus) can be forced to decode either SECAM or PAL/NTSC (but not PAL or NTSC). Crystal selection can also be forced. Information, concerning which standard and which crystal have been selected and whether the colour killer is ON or OFF is provided by the read out. Using the forced-mode does not affect the search loop, it does, however, prevent the decoder from reaching or staying in an unwanted state. The identification circuit skips impossible standards (e.g. SECAM when no 4.4 MHz crystal is fitted) and illegal standards (e.g. forced mode). To reduce the risk of wrong identification PAL has priority over SECAM (only line identification is used for SECAM).

The TDA9160 has two CVBS inputs and one S-VHS input which can be selected via the I²C-bus. The input selector can also be switched to enable CVBS2 to be processed, providing that there is no S-VHS signal present at the input. If the input selector is set to CVBS2 it will switch to S-VHS if an S-VHS sync pulse is detected at the luminance input. The S-VHS detector output can be read via the I²C-bus.
If the voltage at either the S-VHS luminance or the chrominance input (pins 22 and 23) exceeds +5.5 V the IC will revert to test mode.

The TDA9160 also provides outputs for picture-in-picture and teletext (PIP pin 20 and TXT pin 25). The decoder input signal can be switched directly to the TXT output. The PIP output signal can be selected independently from the TXT output. If S-VHS is selected at the TXT output only the luminance signal will be present; if S-VHS is selected at the PIP output then the luminance and chrominance signals will be added.

All filters, including the luminance delay line, are an integral part of the IC. The filters are gyrator-capacitor type filters. The resonant frequency of the filters is controlled by a circuit that uses the active crystal to tune the SECAM Cloche filter during the vertical flyback time. The remaining filters and the delay line are matched to this filter. The filters can be switched to either 4.43 MHz, 4.28 MHz or 3.58 MHz irrespective of the frequency of the active crystal. The switching is controlled by the identification circuit.

The S-VHS luminance signal does not pass through the notch filter to preserve bandwidth. The luminance delay line delivers the Y signal to the output 40 ns after the –(R-Y) and –(B-Y) signals. This compensates for the delay of the external chrominance delay lines.

The PAL/NTSC demodulator employs an oscillator that can operate with either crystal (3.6 or 4.4 MHz). If the I²C-bus indicates that only one crystal is connected it will always connect to the crystal at the reference input (pin 30).

The Hue signal, which is adjustable via the I²C-bus, is gated during the burst for NTSC signals.

The SECAM demodulator is an auto-calibrating PLL demodulator which has two references. The reference crystal, to force the PLL to the desired free-running frequency and the bandgap reference, to obtain the correct absolute value of the output signal. The VCO of the PLL is calibrated during each vertical flyback period, when the reference crystal is active. When the second crystal is active the VCO is not calibrated. During this time the frequency of the VCO is kept constant by applying a constant voltage to its control input. If the reference crystal is not 4.4 MHz the decoder will not produce the correct SECAM signals.

The main part of the sync circuit is a 432 x f_H (6.75 MHz) oscillator the

frequency of which is divided by 432 to lock the phase 1 loop to the incoming signal. The time constant of the loop can be forced by the I²C-bus (fast or slow). If required the IC can select the time constant, depending on the noise content of the input signal and whether the loop is phase locked or not (medium or slow). The free-running frequency of the oscillator is determined by a digital control circuit that is locked to the active crystal.

When a power-on-reset pulse is detected the frequency of the oscillator is switched to a frequency greater than 6.75 MHz to protect the horizontal output transistor. The oscillator frequency is reset to 6.75 MHz when the crystal indication bits have been loaded into the IC. To ensure that this procedure does not fail it is absolutely necessary to send subaddress 00 before subaddress 01. Subaddress 00 contains the crystal indication bits, when subaddress 01 is received the line oscillator calibration will be initiated. The calibration is terminated when the oscillator frequency reaches 6.75 MHz. The oscillator is again calibrated when an out-of-lock condition with the input signal is realised by the coincidence detector. Again the calibration will be terminated when the oscillator frequency reaches 6.75 MHz.
The phase 1 loop can be opened using the I²C-bus. This is to facilitate On Screen Display (OSD) information. If there is no input signal or a very noisy input signal the phase 1 loop can be opened to provide a stable line frequency and thus a stable picture.

The sync part provides an H_A pulse that is coupled to the processed CVBS signal.

The horizontal drive signal can be switched off via the I²C-bus (standby mode). The horizontal drive is also switched off when the over-voltage protection circuit trips or when a POR is detected. Should either of these two conditions occur the IC will return to the normal operating mode when the appropriate command is received via the I²C-bus. The duty cycle of the horizontal drive signal is increased from 2%, at start-up, to a constant value of 55% in approximately 300 lines. The two-level sandcastle pulse provides a combined horizontal and vertical blanking signal and a clamping pulse coupled to the display section of the TV.

The vertical sawtooth generator drives the geometry processing circuits which provide control for the horizontal shift, EW width, EW parabola/width ratio, EW corner/parabola ratio, trapezium correction, vertical slope, vertical shift, vertical amplitude and the S-correction. All of these control functions can be set via the I²C-bus. The geometry processor has a differential current output for the vertical drive signal and a single-ended output for the EW drive. Both the vertical drive and the EW drive outputs can be modulated for EHT compensation. The EHT compensation pin (pin 14) can also be used for over-voltage protection. De-interlace of the vertical output can be set via the I²C-bus.

The vertical divider system has a fully integrated vertical sync separator. The divider can accommodate both 50 and 60 Hz systems; it can either locate the field frequency automatically or it can be forced to the desired system via the I²C-bus. A block diagram of the vertical divider system is illustrated in Fig.4. The divider system operates at 432 times the horizontal line frequency. The line counter receives enable pulses at twice the line frequency, thereby counting two lines per pulse.
A state diagram of the controller is illustrated in Fig.5. Because it is symmetrical only the right hand part will be described.

Depending on the previously found field frequency, the controller will be in one of the 'count' states. When the line counter has counted 488 pulses (i.e. 244 lines of the video input signal) the controller will move to the next state depending on the output of the norm counter. This can be either NORM, NEAR-NORM or NO-NORM depending on the position of the vertical sync pulse in the previous fields. When the counter is in the NORM state it generates the vertical sync pulse (VSP) automatically and then, when the line counter is at LC = 626, moves to the WAIT state. In this condition it waits for the next pulse of the double line frequency signal and then moves to the COUNT state of the current field frequency. When the controller returns to the COUNT state the line counter will be reset half a line after the start of the vertical sync pulse of the video input signal.
When the controller is in the NEAR-NORM state it will move to the COUNT state if it detects the vertical sync pulse within the NEAR-NORM window (i.e. $622 < LC < 628$). If no vertical sync pulse is detected, the controller will move back to the COUNT state when the line counter reaches LC = 628. The line counter will then be reset.
When the controller is in the NO-NORM state it will move to the COUNT state when it detects a vertical sync pulse and reset the line counter. If a sync pulse is not detected before LC = 722 (if the

phase loop is locked in forced mode) it will move to the COUNT state and reset the line counter. If the phase loop is not locked the controller will move back to the COUNT state when LC = 628. The forced mode option keeps the controller in either the left-hand side (60 Hz) or the right-hand side (50 Hz) of the state diagram.

Figure 6 illustrates the state diagram of the 'norm' counter which is an up/down counter that counts up if it finds a vertical sync pulse within the selected window. In the NEAR-NORM and NORM states the first correct vertical sync pulse after one or more incorrect vertical sync pulses is processed as an incorrect pulse. This procedure prevents the system from staying in the NEAR-NORM or NORM state if the vertical sync pulse is correct in the first field and incorrect in the second field. If no vertical sync pulse is found in the selected window this will always result in a down pulse for the 'norm' counter.

Figure 7 illustrates the timing of the display sandcastle (DSC) and the reset pulse of the vertical sawtooth with respect to the input signal.

I²C-bus protocol

If the TXT output is connected to the positive supply the address will change from 8A to 8E.

Valid subaddresses = 00 to 0F
Auto-increment mode available for subaddresses.

Subaddress 00 must always be sent before subaddress 01 in order to protect the horizontal output transistor.

Table 1 Slave address (8A)

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	0	0	1	X	1	X

Table 2 Inputs

SUBADDRESS	MSB							LSB
00	INA	INB	INC	IND	FOA	FOB	XA	XB
01	FORF	FORS	DL	STB	POC	FM	SAF	FRQF
02	–	–	HU5	HU4	HU3	HU2	HU1	HU0
03	–	–	HS5	HS4	HS3	HS2	HS1	HS0
04	–	–	EW5	EW4	EW3	EW2	EW1	EW0
05	–	–	PW5	PW4	PW3	PW2	PW1	PW0
06	–	–	CP5	CP4	CP3	CP2	CP1	CP0
07	–	–	TC5	TC4	TC3	TC2	TC1	TC0
08	–	–	VS5	CS4	VS3	VS2	VS1	VS0
09	–	–	VA5	VA4	VA3	VA2	VA1	VA0
0A	–	–	SC5	SC4	SC3	SC2	SC1	SC0
0B	SBL	–	VSH5	VSH4	VSH3	VSH2	VSH1	VSH0

Table 3 Outputs

ADDRESS	POR	FSI	STS	SL	PROT	SAK	SBK	FRQ

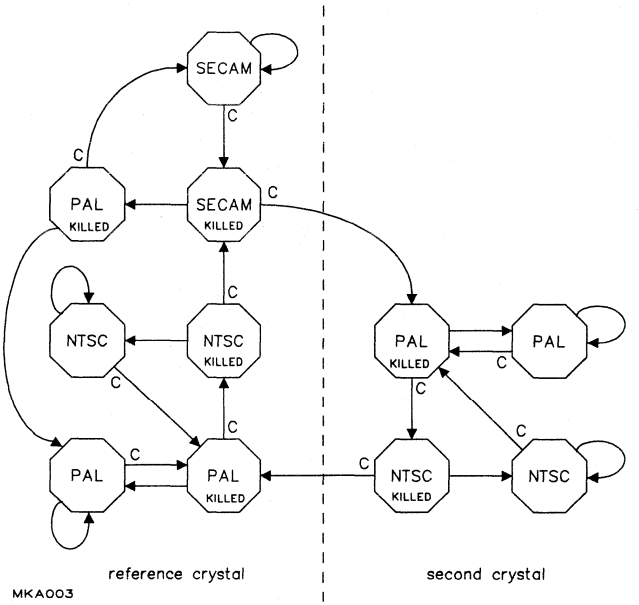


Fig.3 Search loop of the identification circuit.

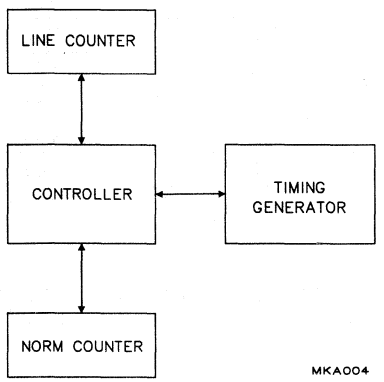


Fig.4 Block diagram of the vertical divider system.

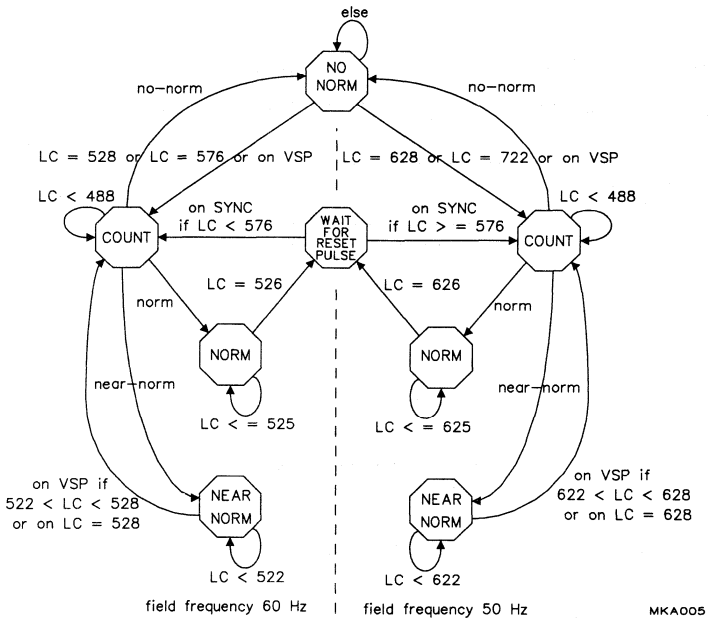


Fig.5 State diagram of the vertical divider system.

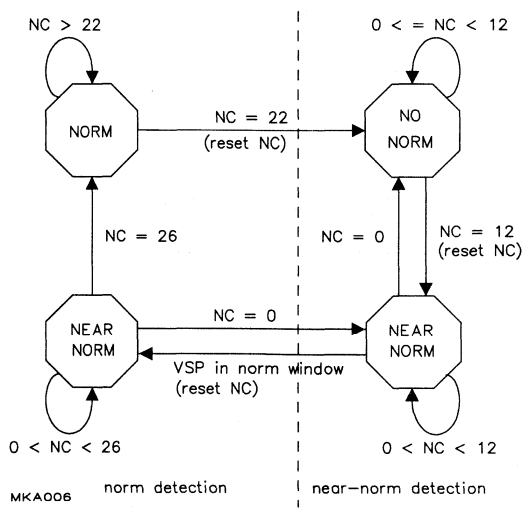


Fig.6 State diagram of the 'norm' counter.

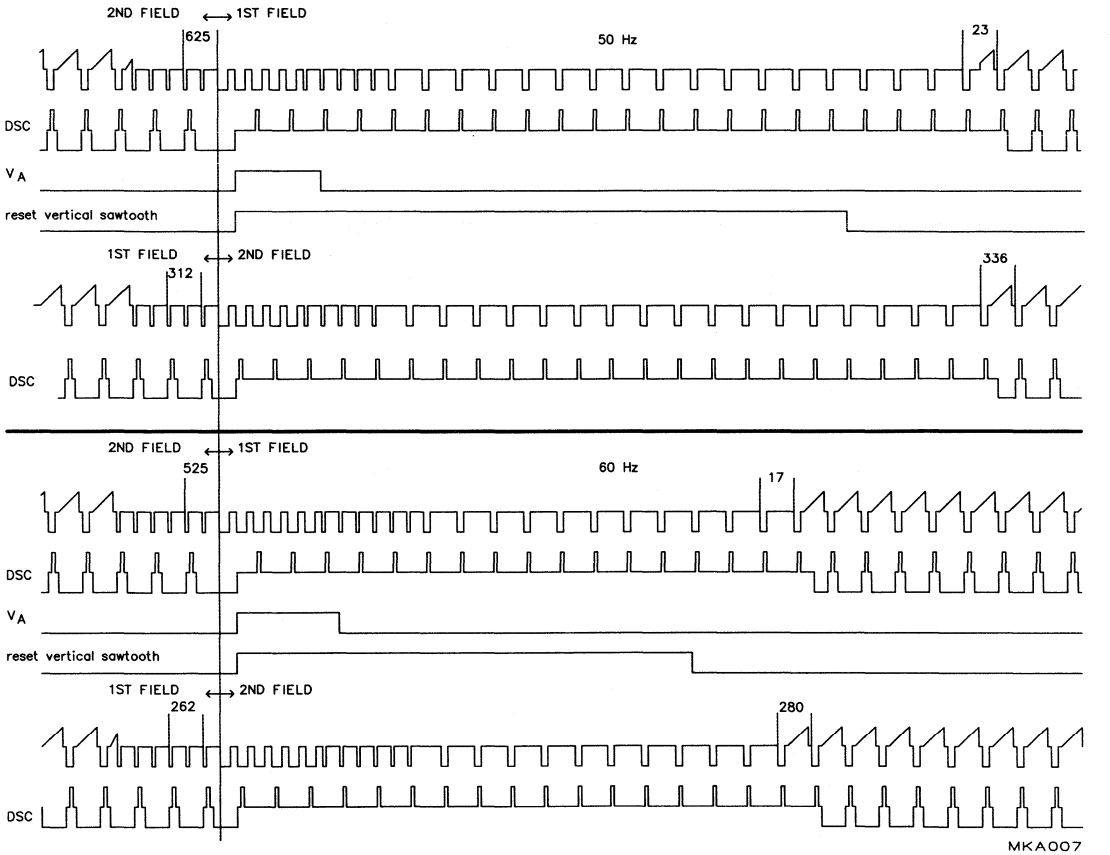


Fig.7 Field timing diagram.

INPUT SIGNALS

Table 4 Source select 1

INA	INB	DECODER AND TXT
0	0	CVBS1
0	1	CVBS2
1	0	S-VHS
1	1	S-VHS (CVBS2)

Table 5 Source select 2

INC	IND	DECODER AND TXT
0	0	CVBS1
0	1	CVBS2
1	0	S-VHS
1	1	S-VHS (CVBS2)

Table 6 Phase time constant

FOA	FOB	MODE
0	0	auto
0	1	slow
1	–	fast

Table 7 XTAL indication

XA	XB	CRYSTAL
0	0	2 x 3.6 MHz
0	1	1 x 3.6 MHz
1	0	1 x 4.4 MHz
1	1	3.6 and 4.4 MHz

Table 8 Forced field frequency

FORF	FORS	FIELD FREQUENCY
0	0	auto
0	1	60 Hz
1	0	50 Hz
1	1	auto

Table 9 Interlace

DL	CONDITION
0	interlace
1	de-interlace

Table 10 Standby

STB	CONDITION
0	standby
1	normal mode

Table 11 Phase loop control

POC	CONDITION
0	phi one loop closed
1	phi one loop open

Table 12 Forced standard

ADD	LOGIC	CONDITION
FM	0	auto search
	1	forced mode
SAF	0	PAL/NTSC
	1	SECAM
FRQF	0	second crystal
	1	reference crystal

Table 13 Service blanking

SBL	CONDITION
0	service blanking OFF
1	service blanking ON

Note to table 12

If XA and XB indicate that only one crystal is connected to the IC and FM and FRQF force it to use the second crystal the colour will be switched off.

Table 14 Other input signals

FUNCTION	ADDRESS	DIGITAL NUMBER
hue	HU5 to HU0	000000 = –45° 111111 = +45°
horizontal shift	HS5 to HS0	000000 = –2.2 µs 111111 = +2.2 µs
EW width	EW5 to EW0	000000 = 80% 111111 = 100%
EW parabola/width	PW5 to PW0	000000 = 0% 111111 = 24%
EW corner/parabola	CP5 to CP0	000000 = 0% 111111 = –44%
EW trapezium	TC5 to TC0	000000 = –4% 111111 = +4%
vertical slope	VS5 to VS0	000000 = –14% 111111 = +14%
vertical amplitude	VA5 to VA0	000000 = –80% 111111 = +120%
S correction	SC5 to SC0	000000 = 0% 111111 = 20%
vertical shift	VSH5 to VSH0	000000 = –4% 111111 = +4%

Table 15 Standard read-out

SAK	SBK	FRQ	STANDARD
0	0	0	PAL, second crystal
0	0	1	PAL, reference crystal
0	1	0	NTSC, second crystal
0	1	1	NTSC, reference crystal
1	0	0	not used
1	0	1	SECAM, reference crystal
1	1	0	colour off
1	1	1	clolour off

INPUT SIGNALS

Table 16 Power-on-reset

POR	CONDITION
0	normal mode
1	power-down mode

Table 17 Field frequency indication

FSI	CONDITION
0	50 Hz
1	60 Hz

Table 18 S-VHS status

STS	CONDITION
0	no signal at input
1	signal at input

Table 19 Phase lock indication

SL	CONDITION
0	not locked
1	locked

Table 20 Over-voltage protection

PROT	CONDITION
0	no over-voltage detected
1	over-voltage detected

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	positive supply voltage		–	8.8	V
I_{CC}	supply current		–	70	mA
P_{tot}	total power dissipation		–	–	W
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−10	+65	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	t.b.f.

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		–	50	–	mA
P_{tot}	total power dissipation		–	400	–	mW
Input switch						
CVBS1 AND CVBS2 INPUTS (PINS 26 AND 24)						
$V_{26,24(p\text{-}p)}$	input voltage (peak-to-peak value)		–	1.0	1.43	V
Z_I	input impedance		60	–	–	kΩ
S-VHS Y INPUT (PIN 23)						
$V_{23(p\text{-}p)}$	input voltage (peak-to-peak value)		–	1.0	1.43	V
Z_I	input impedance		60	–	–	kΩ
S-VHS CHROMINANCE INPUT (PIN 22)						
$V_{22(p\text{-}p)}$	input voltage (peak-to-peak value)	burst	–	0.3	1.43	V
Z_I	input impedance		60	–	–	kΩ
LUMINANCE OUTPUT (PIN 1)						
$V_{1(p\text{-}p)}$	output voltage (peak-to-peak value)		–	450	–	mV
Z_O	output impedance		–	–	500	Ω
V_O	top sync level		–	2.1	–	V
S/N	signal-to-noise ratio		–	tbf	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SUPP	suppression of unselected inputs		50	–	–	dB
TXT AND PIP OUTPUTS (PINS 25 AND 20)						
$V_{20.25(p-p)}$	output voltage (peak-to-peak value)		–	1.0	–	V
Z_O	output impedance		–	–	500	Ω
V_O	top sync level	TXT output	–	1.8	–	V
		PIP output	–	2.8	–	V
SUPP	suppression of unselected inputs	f = 0 to 5 MHz; PIP output	50	–	–	dB
SUPP	suppression of unselected inputs	f = 0 to 5 MHz; TXT output	35	–	–	dB
Bias generator						
V_8	digital supply voltage		–	5.0	–	V
V_{12}	DC voltage		–	3.9	–	V
Subcarrier regeneration						
$V_{ACC(p-p)}$	burst amplitude within ACC range (peak-to-peak value)		25	–	500	mV
CR	catching range	note 1	500	–	–	Hz
φ	phase shift for 400 Hz deviation		–	–	5	deg
TC	temperature coefficient of oscillator		–	tbf	–	Hz/K
Z_I	input impedance	reference crystal input	–	1.0	–	kΩ
		second crystal input	–	1.5	–	kΩ
V_{dep}	supply voltage dependency		–	tbf	–	V
Demodulators						
Δ2/Δ3	change of –(R-Y) and –(B-Y) signals over the ACC range		–	–	1	dB
	ratio of –(R-Y) and –(B-Y) signals		–	1.27	–	
TC	temperature coefficient of –(R-Y) and –(B-Y) amplitude		–	tbf	–	Hz/K
	spread of –(R-Y) and –(B-Y) ratio between standards		–1	–	+1	dB
V_2	output level of –(R-Y) during blanking		–	2.0	–	V
V_3	output level of –(B-Y) during blanking		–	2.0	–	V
B	bandwidth	at –3 dB	–	1	–	MHz
Z_O	output impedance		–	–	500	Ω
V_{dep}	supply voltage dependency		–	tbf	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL/NTSC DEMODULATOR						
$V_{2(p-p)}$	–(R-Y) output voltage (peak-to-peak value)	standard colour bar	–	525	–	mV
$V_{3(p-p)}$	–(B-Y) output voltage (peak-to-peak value)	standard colour bar	–	665	–	mV
α	crosstalk between –(R-Y) and –(B-Y)		–	tbf	–	dB
$V_{2.3(p-p)}$	8.8 MHz residue (peak-to-peak value)	both outputs	–	–	15	mV
$V_{2.3(p-p)}$	7.2 MHz residue (peak-to-peak value)	both outputs	–	–	20	mV
S/N	signal-to-noise ratio		46	–	–	dB
PAL DEMODULATOR						
$V_{R(p-p)}$	H/2 ripple (peak-to-peak value)		–	–	50	mV
S/N	signal-to-noise ratio		46	–	–	dB
NTSC DEMODULATOR						
φ	hue phase shift		–45	–	+45	deg
SECAM DEMODULATOR						
$V_{2(p-p)}$	–(R-Y) output voltage (peak-to-peak value)	standard colour bar	–	1.05	–	mV
$V_{3(p-p)}$	–(B-Y) output voltage (peak-to-peak value)	standard colour bar	–	1.33	–	mV
f_{OS}	black level offset		–	–	7	kHz
S/N	signal-to-noise ratio		–	43	–	dB
$V_{res(p-p)}$	7.8 to 9.4 MHz residue (peak-to-peak value)		–	–	30	mV
f_{pole}	pole frequency of deemphasis		77	85	93	kHz
	ratio of pole and zero frequency		–	3	–	
V_{cal}	calibration voltage		3.0	4.0	5.0	V
NL	non linearity		–	–	3	%
Filters						
V_{tune}	tuning voltage		1.5	3.0	6.0	V
Luminance delay						
t_d	delay time	PAL/NTSC/BW	–	430	–	ns
t_d	delay time	SECAM	–	480	–	ns
Luminance trap						
f_o	notch frequency	f_{sc} = 3.6 MHz f_{sc} = 4.4 MHz SECAM S-VHS/BW; not active	3.53 4.37 4.23	3.58 4.43 4.29	3.63 4.49 4.35	MHz MHz MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B	bandwidth at –3 dB	f_{SC} = 3.6 MHz	–	2.8	–	MHz
		f_{SC} = 4.4 MHz	–	3.4	–	MHz
		SECAM	–	3.3	–	MHz
SUPP	subcarrier suppression		26	–	–	dB
CHROMINANCE BANDPASS						
f_{res}	resonant frequency	f_{SC} = 3.6 MHz	–	3.58	–	MHz
		f_{SC} = 4.4 MHz	–	4.43	–	MHz
B	bandwidth at –3 dB	f_{SC} = 3.6 MHz	–	1.6	–	MHz
		f_{SC} = 4.4 MHz	–	2	–	MHz
Cloche filter						
f_{res}	resonant frequency	SECAM	4.26	4.29	4.31	MHz
B	bandwidth	at –3 dB; SECAM	241	268	295	kHz
Sync input						
V_{22}	sync pulse amplitude	CVBS 1/2; S-VHS input	50	300	600	mV
	slicing level		–	50	–	%
t_d	delay of sync pulse due to internal filter		0.2	0.3	0.4	µs
S/N	noise detector threshold level		–	20	–	dB
H	hysteresis		–	3	–	dB
t_d	delay between video signal and internally separated vertical sync pulse		12	18.5	27	µs
Horizontal section						
H_A OUTPUT (PIN 10)						
V_{OH}	output voltage HIGH		2.4	5.0	5.5	V
V_{OL}	output voltage LOW		–	0.3	0.6	V
I_{sink}	sink current		2	–	–	mA
I_{source}	source current		2	–	–	mA
t_W	pulse width	32 clock cycles	–	4.7	–	µs
t_d	delay between middle of horizontal sync pulse and middle of H_A	note 2	0.3	0.45	0.6	µs
FIRST LOOP						
Δf	frequency deviation when not locked		–	–	1.5	%
SVRR	supply voltage ripple rejection		–	tbf	–	V
TC	temperature coefficient		–	tbf	–	Hz/°C
f_{CR}	catching range		625	–	–	Hz
f_{HR}	holding range		–	–	1400	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ϕ	static phase shift		–	–	0.1	µs/kHz
SECOND LOOP						
φ	control sensitivity		300	–	–	µs/µs
t_{CR}	control range of the positive going edge of horizontal drive to flyback	HS = 00; note 4	13.5	–	–	µs
t_d	delay between second loop reference and mid-sync of processed video		–	3	–	µs
HORIZONTAL SHIFT						
SR	horizontal shift range	63 steps	–2.2	–	+2.2	µs
HORIZONTAL DRIVE OUTPUT (PIN 18)						
R_{18}	output resistance	on-state	–	–	50	Ω
I_{18}	output current		–	–	10	mA
	duty cycle of output current		–	55	–	%
HORIZONTAL FLYBACK INPUT (PIN 19)						
V_{HB}	switching level for horizontal blanking		–	0.3	–	V
$V_{\varphi 2}$	switching level for phase two loop		–	3.8	–	V
V_{19}	maximum input voltage		–	–	V_{CC}	V
Z_I	input impedance		10	–	–	MΩ
Soft start						
CR	duty cycle control range		2	–	55	%
	soft start time		200	300	500	lines
Vertical section (note 3)						
VERTICAL OSCILLATOR						
f_{fr}	free running frequency	divider ratio 628	–	50	–	Hz
f_{LR}	frequency locking range		43	–	64	Hz
LR	divider locking range		488	625	722	
VERTICAL SAWTOOTH (PIN 11)						
$V_{11(P-P)}$	voltage amplitude level (peak-to-peak value)	VS = 1F; C = 100 nF; R = 39 kΩ	–	3.5	–	V
I_{dis}	discharge current		–	1	–	mA
I_{charge}	charge current set by external resistor	f = 50 Hz; VS = 1F	–	19	–	µA
CR	vertical slope control range	63 steps	–14	–	+14	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL DRIVE OUTPUTS (PINS 15 AND 16)						
$I_{diff(p-p)}$	differential output current (peak-to-peak value)	VA = 1F	–	1	–	mA
$I_{15,16}$	common mode current		–	400	–	µA
V_O	output voltage range		0	–	4.0	V
EHT TRACKING AND OVER-VOLTAGE PROTECTION (PIN 14)						
TR	tracking range		1.2	–	2.8	V
SMR	scan modulation range		–6	–	+6	%
α	sensitivity		–	7.5	–	%/V
V_{14}	over-voltage protection detection level		–	3.9	–	V
DE-INTERLACE						
	first field delay		–	0.5H	–	
Sandcastle (pin 6)						
V_6	zero level		0	0.5	1.0	V
I_{sink}	sink current		0.5	–	–	mA
HORIZONTAL AND VERTICAL BLANKING						
V_{bl}	blanking voltage level		2.0	2.5	3.0	V
I_{source}	source current		0.5	–	–	mA
I_{ext}	external current required to force the output to the blanking level		1	–	3	mA
CLAMPING PULSE						
V_{clamp}	clamping voltage level		4.0	4.5	5.0	V
I_{source}	source current		0.5	–	–	mA
t_W	pulse width	PAL (17 LLC pulses) SECAM (24 LLC pulses)	– –	2.5 3.6	– –	µs µs
t_d	delay between mid sync of input and start of clamping pulse		3.6	3.7	3.8	µs
Geometry processing (note 3)						
EW WIDTH						
CR	control range	63 steps	100	–	80	%
I_{eq}	equivalent EW output current		0	–	400	µA
V_O	EW output voltage range		1.0	–	8.0	V
I_O	EW output current range		0	–	900	µA
EW PARABOLA/WIDTH						
CR	control range	63 steps	0	–	24	%
I_{eq}	equivalent EW output current	EW = 3F	0	–	480	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EW CORNER/PARABOLA						
CR	control range	63 steps	−44	−	0	%
I_{eq}	equivalent EW output current	EW = 3F; PW = 3F	−210	−	0	μA
EW TRAPEZIUM						
CR	control range	63 steps	−4	−	+4	%
I_{eq}	equivalent EW output current		−80	−	+80	μA
EW EHT TRACKING						
TR	tracking range		1.2	−	2.8	V
SMR	scan modulation range		−6	−	+6	%
I_{eq}	equivalent output current		+120	−	−120	μA
φ	sensitivity		−	−7.5	−	%/V
VERTICAL AMPLITUDE						
CR	control range	63 steps; SC = 00 63 steps; SC = 3F	80 86	− −	120 112	% %
I_{eq}	equivalent differential vertical drive output current	SC = 00	800	−	1200	μA
VERTICAL SHIFT						
CR	control range	63 steps	−4	−	+4	%
I_{eq}	equivalent differential vertical drive output current		−40	−	+40	μA
S CORRECTION						
CR	control range	63 steps	0	−	20	%

Notes to the characteristics

1. All oscillator specifications are measured with the Philips crystal series 4322 143/144. The spurious response of the reference crystal must be less than −7 dB with respect to the fundamental frequency for a damping resistance of 1 kΩ. The spurious response of the second crystal must be less than −7 dB with respect to the fundamental frequency for a damping resistance of 1.5 kΩ.
2. This delay is caused by the low pass filter at the sync separator input.
3. All values are valid for a reference current of 100 μA (R_C = 39 kΩ).
4. Valid for flyback pulse width of 12 μs at the switching level of the phase 2 loop.

QUALITY SPECIFICATION

Quality level according to URV 4-2-59/601.

SYMBOL	PARAMETER	RANGE A	RANGE B	UNIT
ESD	protection circuit specification (note 1)	2000	500	V
		100	200	pF
		1500	0	Ω

Test and application information

EW output stage

In order to obtain the correct tracking of the vertical and horizontal EHT correction, the EW output stage should be configured as illustrated in figure 8.

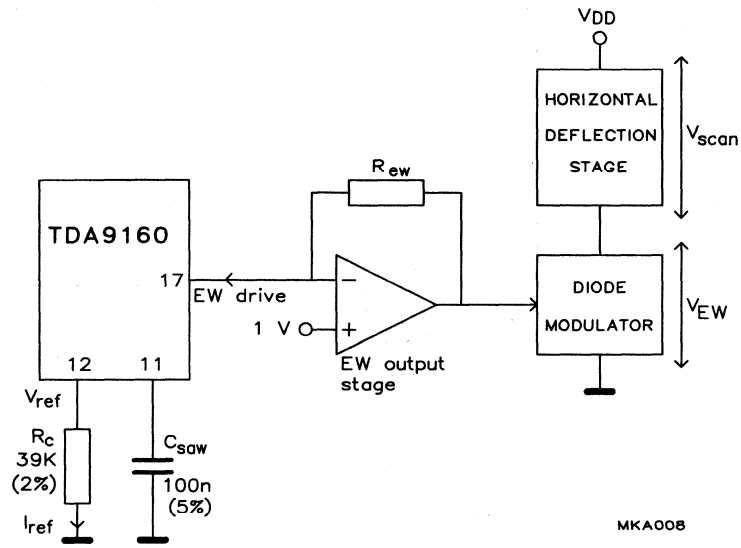


Fig.8 Configuration of the EW output stage.

Note to Fig.8

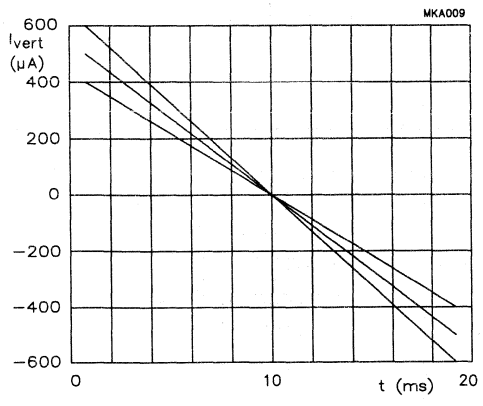
Resistor R_{ew} determines the gain of the EW output stage. Resistor R_c sets the reference current for both the vertical sawtooth generator and the geometry processor. The preferred value of R_c = 39 kΩ results in a reference current of 100 µA (V_{ref} = 3.9 V).
The value of R_{ew} is given in the following equation:

$$R_{ew} = R_c \times \frac{V_{scan}}{(18 \times V_{ref})}$$

Example: If V_{ref} = 3.9 kΩ, R_c = 39 kΩ and V_{scan} = 120 V then R_{ew} = 68 kΩ

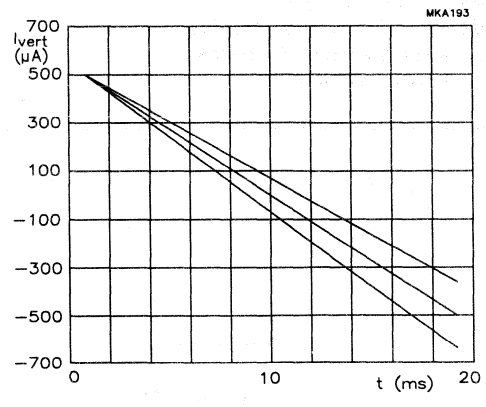
Control ranges of geometry control parameters

Typical case curves (R_C = 39 kΩ; C_{saw} = 100 nF)



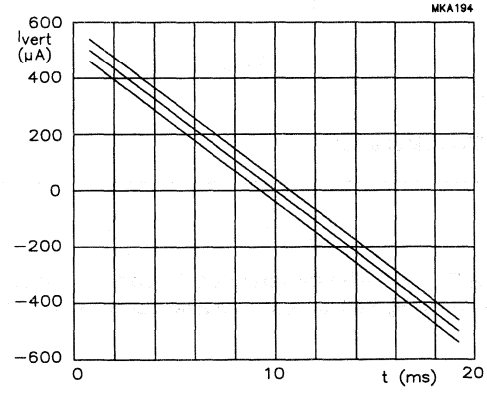
VA = 0, 31 and 63; VSH = 31; SC = 0

Fig.9 Control range of vertical amplitude.



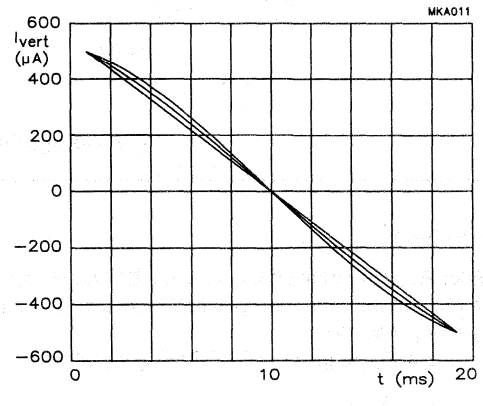
VA = 31; VS = 0, 31 and 63; VSH = 31; SC = 0

Fig.10 Control range of vertical slope.



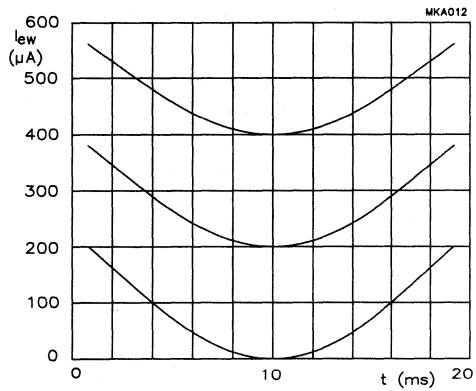
VA = 31; VSH = 0, 31 and 63; SC = 0

Fig.11 Control range of vertical shift.



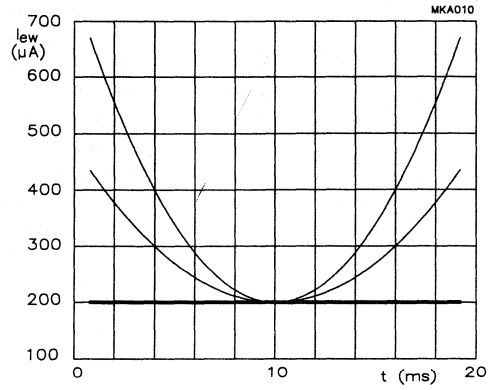
SC = 0, 31 and 63; VA = 31; VSH = 31. The picture height does not change with the setting of S correction for nominal setting of vertical amplitude (VA = 31).

Fig.12 Control range of S correction.



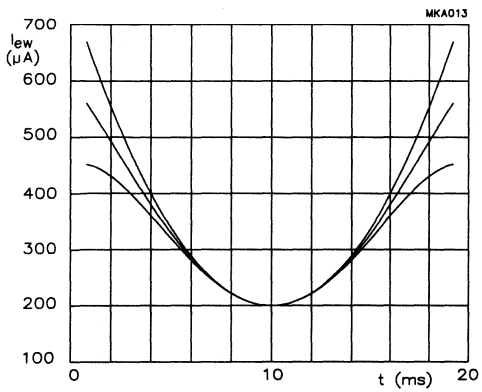
EW = 0, 31 and 63; PW = 31; CP = 31

Fig.13 Control range of EW width.



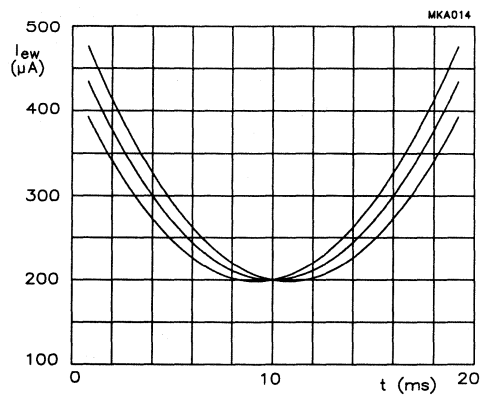
EW = 0, 31 and 63; PW = 31; CP = 31

Fig.14 Control range of EW parabola/width ratio.



CP = 0, 31 and 63; EW = 31; PW = 63

Fig.15 Control range of EW corner/parabola ratio.



TC = 0, 31 and 63; EW = 31; PW = 31; CP = 0

Fig.16 Control range of EW trapezium correction.

Adjustment of geometry control parameters

The deflection processor of the TDA9160 offers nine control parameters for picture alignment:

- S-correctiion, vertical amplitude, vertical slope and vertrical shift for the vertical picture alignment
- Horizontal shift, EW width, EW parabola/width, EW corner/parabola and EW trapezium correction for the horizontal picture alignment

The required values for the settings of S-correction, EW parabola/width ratio and EW corner/parabola ratio are determined for a particular combination of picture tube type, vertical output stage and EW output stage. These parameters can be preset via the I²C-bus and do not require any additional adjustment. The remainder of the parameters are preset to the mid value of their control range (i.e. 1F), or to values that have obtained from previous TV set adjustments.
After the vertical S-correction has been preset the vertical picture alignment could, in theory, be completed by positioning the top of the picture using the vertical amplitude adjustment and the bottom of the picture using the vertical slope adjustment (see note). It can be shown, however, that without compensation offsets in the external vertical output stage or in the picture tube would result in a certain linearity error especially with picture tubes that need large S-correction. The total linearity error is in first order approximation proportional to the offset and to the square of the required S-correction. A vertical shift control is available for offset compensation.
For adjustmen of the vertical shift, independent of the vertical slope, a special vertical shift alignment is provided. This mode is entered by setting the SBL bit HIGH. In this mode the –(R-Y) and –(B-Y) outputs are blanked during the second half of the picture. The first line in which the colours are blanked must be positioned in the middle of the screen.
The necessity to use the vertical shift alignment depends on the expected offsets in the vertical output stage and picture tube, on the required value of the S-correction and on the demands upon the vertical linearity. If the vertical shift alignment is not used VSH should be set to its mid value (i.e. VSH = 1F).
The actual factory adjustments of the picture consist of the following steps:

- The vertical shift is adjusted as previously described (if required).
- The top of the picture is positioned by adjusting the vertical amplitude and the bottom of the picture by adjusting the vertical slope
- The picture is positioned in the horizontal direction by adjusting the EW width and horizontal shift
- The left and right hand sides of the picture are aligned in parallel by adjusting the EW trapezium correction (if required).

Note

The value of the vertical slope determines the charge current of the vertical sawtooth capacitor (C_{saw} as shown in Fig.8) and thus the amplitude of the sawtooth voltage at pin 11. This voltage serves as the input voltage for the geometry processor. Consequently the setting of the vertical slope will affect both the vertical and EW output currents.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

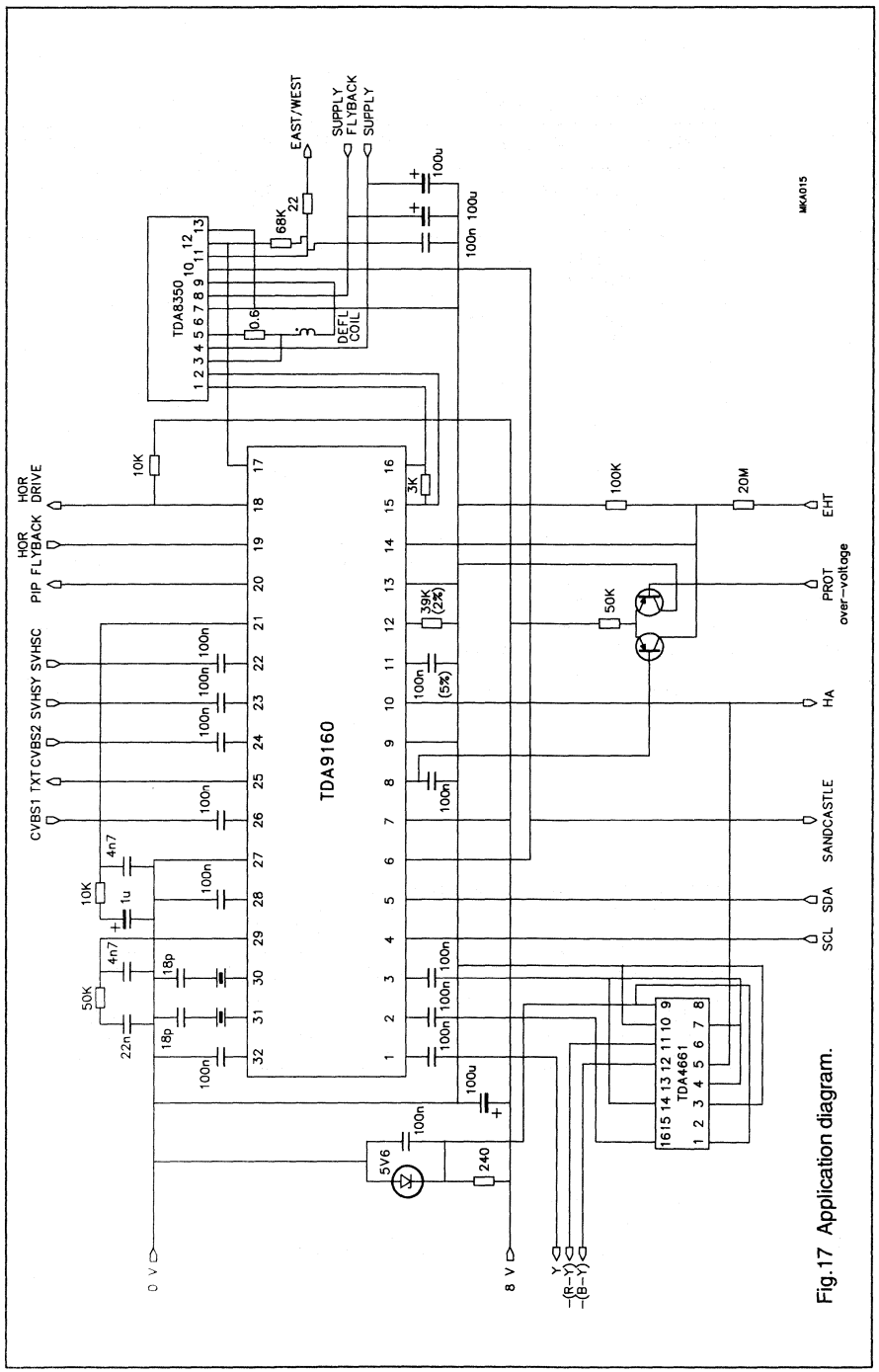


Fig.17 Application diagram.

Notes to figure 17

1. Pins 31 and 32 are sensitive to leakage current.
2. The analog and digital ground currents should be well separated.
3. The decoupling capacitor connected between pins 8 and 9 must be placed as close to the IC as possible.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 91

TDA9820

Multistandard / dual channel TV FM intercarrier sound demodulator

FEATURES

- Multistandard application for sound standards M, B/G, I, D/K
- Two alignment-free PLL FM demodulators
- Four-input source selector for one of the two FM demodulators
- Automatic second sound carrier mute
- Mono and dual channel application
- Low power consumption
- Few external components

GENERAL DESCRIPTION

The TDA9820 is a monolithic, integrated, multistandard TV FM intercarrier sound demodulator for all FM standards. The circuit contains two separate FM demodulators using Phase-Locked Loop (PLL) reference frequency generation. The circuit has a minimum number of external components.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
I_M	peak output current (pin 8 and pin 7)		–	–	± 1.5	mA
P_{tot}	power dissipation	V_P = 5 V	–	–	150	mW
(S+N)/N	signal-to-noise ratio (pin 8 and pin 7)	CCIR 468-3	64	68	–	dB
$\alpha_{8/7}$	crosstalk attenuation	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection (pin 7 and pin 8)	V_{RR} < 200 mV; f = 70 Hz	–	20	–	dB
T_{amb}	operating ambient temperature range		0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9820	16	DIL	plastic	SOT38
TDA9820T	16	DIL	plastic	SOT162A

Multistandard / dual channel TV FM intercarrier sound demodulator

TDA9820

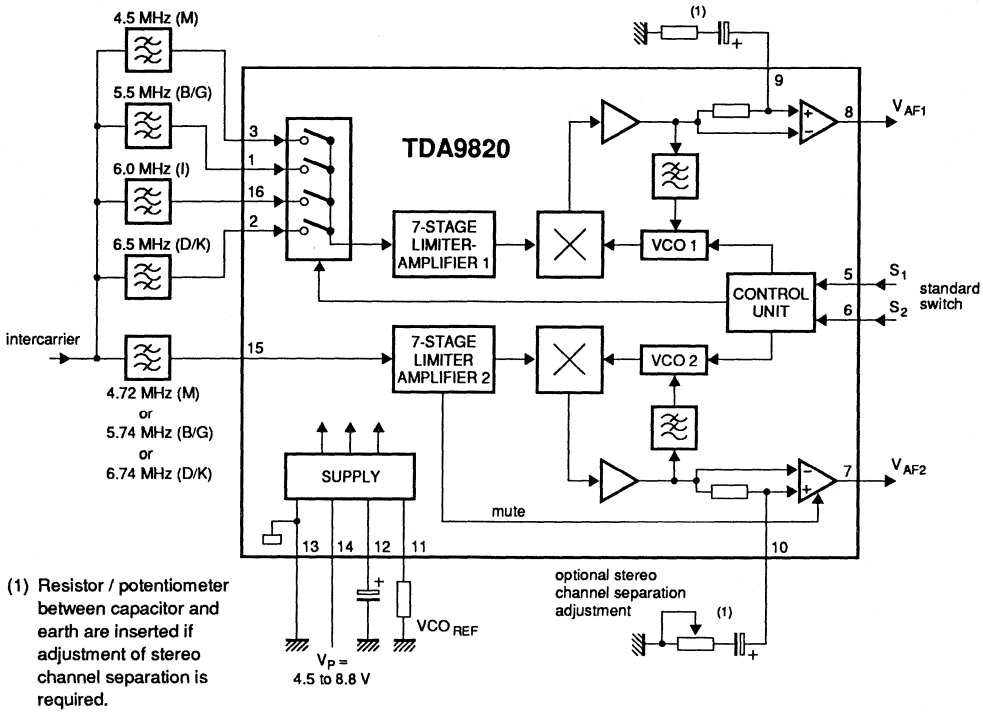


Fig.1 Block diagram.

Multistandard / dual channel TV FM intercarrier sound demodulator

TDA9820

PINNING

SYMBOL	PIN	DESCRIPTION
$IN_{1(B/G)}$	1	first intercarrier input at 5.5 MHz
$IN_{1(D/K)}$	2	first intercarrier input at 6.5 MHz
$IN_{1(M)}$	3	first intercarrier input at 4.5 MHz
n.c.	4	not connected
S_1	5	standard switch bit 1
S_2	6	standard switch bit 2
V_{AF2}	7	second audio output voltage
V_{AF1}	8	first audio output voltage
C_1	9	decoupling capacitor
C_2	10	decoupling capacitor
VCO_{REF}	11	VCO reference
C_{STAB}	12	supply voltage stabilization
GND	13	ground
V_P	14	supply voltage
IN_2	15	second intercarrier input
$IN_{1(I)}$	16	first intercarrier input at 6.0 MHz

PIN CONFIGURATION

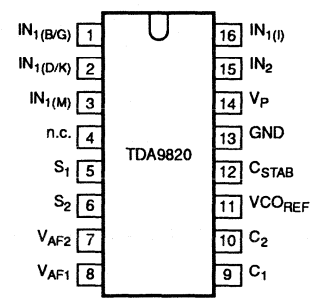


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The complete circuit consists of two separate channels , each consisting of a limiter-amplifier, FM demodulator and AF amplifier. Circuit operation is as follows (see Fig.1):

Source selector

The intercarrier signal is fed through external ceramic bandpass filters which are tuned to the sound carrier frequencies.
One of the four filtered sound carriers from pins 1, 2, 3 or 16 is fed to limiter-amplifier 1 via the appropriate electronic switch in the source selector. The electronic switch of the sound carrier is selected by the control unit (see Logic Table).
The second sound carrier of the intercarrier signal is directly fed from pin 15 to limiter-amplifier 2.

FM demodulators

Each limiter amplifier is AC-coupled into an FM demodulator. The FM demodulator PLLs ensures that the demodulators are alignment-free. The FM demodulator outputs are amplified to 500 mV_{RMS}. High amplification and DC error signals of the PLLs, which are superimposed on the FM demodulator outputs, require DC de-coupling at pin 9 and pin 10 of the AF amplifier inputs.

Stereo channel separation adjustment (optional)

Optimal stereo channel separation is achieved by adjusting V_{AF1} (pin 8) and V_{AF2} (pin 7) as followes:
a) V_{AF1} by a resistor in series with the DC de-coupling capacitor at pin 9
b) V_{AF2} by a variable resistor in series with the DC de-coupling capacitor on pin 10 to the same voltage as V_{AF1} .

Second sound carrier mute

The output of the second FM demodulator is muted when the signal level (signal and/or noise) at pin 15 is less than typically 0.5 mV_{RMS}. This avoids an incorrect stereo or dual sound identification when a mono signal is transmitted. Therefore, with a mono transmission, there is no audio output at pin 7. When the signal level at pin 15 is greater than typically 1.0 mV_{RMS} mute is switched off.

Control unit

The control unit selects the required sound standard according to the voltages on pin 5 and pin 6. The control unit performs the following:
(a) selects the free-running frequencies of VCO1 and VCO2
(b) switches the source selector (the four possible combinations are shown in Table 1).

Multistandard / dual channel TV FM intercarrier sound demodulator

TDA9820

Table 1 Logic Table

STANDARD	S1 (pin 5)	S2 (pin 6)	FREQUENCY VCO1	FREQUENCY VCO2	SOURCE SELECTOR CONNECTION
B/G	1	1	5.5 MHz	5.74 MHz	pin 1
M	1	0	4.5 MHz	4.72 MHz	pin 3
I	0	1	6.0 MHz	OFF	pin 16
D/K	0	0	6.5 MHz	6.74 MHz	pin 2

Note to Table 1

In columns S1 and S2:
0 = LOW
1 = HIGH.

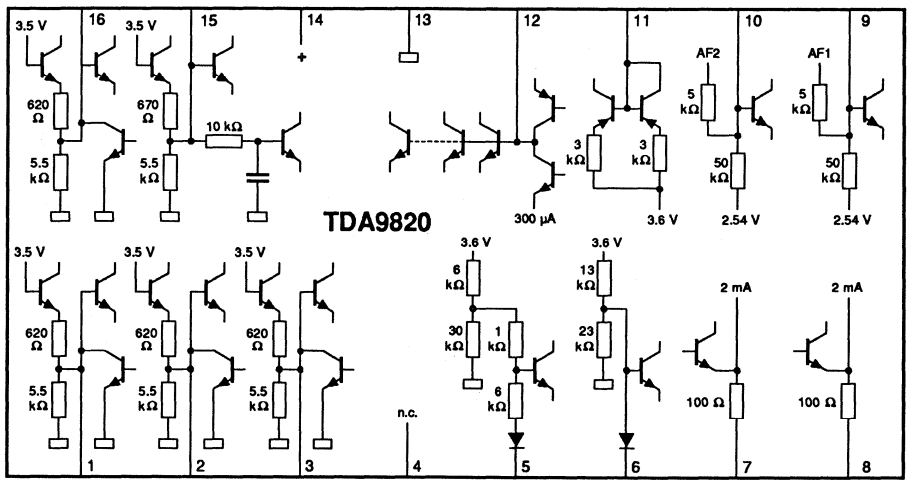


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range (pin 14)	−0.5	9.0	V
V_i	input signal (pins 1, 2, 3, 15 and 16)	−0.5	5.0	V
V_{adj}	adjustment voltage (pin 9 and pin 10)	−0.5	V_P + 0.5	V
T_{stg}	storage temperature range	−25	+ 125	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
P_{tot}	total power dissipation	−	150	mW

CHARACTERISTICS

All voltages are measured to GND (pin 13); V_P = 5.0 V; Δf_i = ± 50 kHz; f_{mod} = 1 kHz; $V_{1,2,3,16/15(rms)}$ = 10 mV; T_{amb} = 25 °C; measured in test circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
Source selector and limiter-amplifier 1 (pins 1, 2, 3 and 16)						
V_I	DC input voltage	input activated	–	2.55	–	V
		input not activated	–	–	0.1	V
R_I	input resistance	input activated	480	600	720	Ω
		input not activated	–	–	100	Ω
$V_{i(rms)}$	input signal (RMS value)	(S+N)/N = 40 dB	–	100	250	μV
	allowed input signal (RMS value)		200	–	–	mV
α_i	crosstalk attenuation	not activated input to activated input	–	50	–	dB
Limiter-amplifier 2						
V_{15}	DC input voltage		–	2.55	–	V
$V_{15(rms)}$	input signal (RMS value)	(S+N)/N = 40 dB; note 1	–	150	250	μV
	input signal for mute off (RMS value)		0.7	1.0	1.5	mV
	allowed input signal (RMS value)		200	–	–	mV
R_{15}	input resistance		480	600	720	Ω
δ	hysteresis of level detector		–	12	–	dB
PLL FM demodulators VCO1 and VCO2						
f_{VCO1}	free-running frequencies	R_{11} = 27 kΩ see Table 1	– – – –	4.5 5.5 6.0 6.5	– – – –	MHz MHz MHz MHz
f_{VCO2}	free-running frequencies	R_{11} = 27 kΩ see Table 1	– – –	4.72 5.74 6.74	– – –	MHz MHz MHz
$\Delta f_{VCO1/2}$	free-running frequency spread		–	–	± 10	%
	drift of free-running frequencies	0 to 70 °C	–	500	–	kHz
	shift of free-running frequencies	4.5 V < V_P < 8.8 V	–	200	–	kHz
	adjustment range of free-running frequencies	resistance at pin 11	± 1	–	–	MHz
R_{11}	adjustment resistance for free-running frequencies (pin 11)		15	22	29	kΩ
S	steepness of free-running frequency adjustment	resistance at pin 11	–	–200	–	kHz/kΩ
Δf1	catching range of PLLs		± 1.4	± 1.9	–	MHz
Δf2	holding range of PLLs		± 2.0	± 3.0	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output amplifiers AF1 (pin 8) and AF2 (pin 7)						
V_o	DC output voltage (pin 8 and pin7)		–	2.15	–	V
$V_{o(rms)}$	output signal (pin 8 and pin7) (RMS value)		–	0.5	–	V
		clipping level	1.2	–	–	V
I_M	AC output peak current (pin 8 and pin7)		–	–	± 1.5	mA
I_o	DC output current (pin 8 and pin7)		–	–	–2.0	mA
$\Delta V_o/V_o$	absolute drift of AF output signals	0 to 70 °C	–	0.7	–	dB
$\Delta V_o/\Delta V_o$	relative drift of AF output signals	0 to 70 °C	–	0.2	–	dB
$V_{AF(1-2)}$	difference between output signals (pin 8 and pin7)	with 50 µs de-emphasis	–	± 0.3	± 1.0	dB
R_o	output resistance (pin 8 and pin7)		–	100	–	Ω
R_s	series resistor for optional crosstalk adjustment (pin 9 and pin 10)	$V_{AF(1-2)}$ = ± 1.5 dB	–	1.1	–	kΩ
THD	distortion (pin 8 and pin7)	with 50 µs de-emphasis	–	0.1	0.3	%
α_{AM}	AM suppression of AF1/2 (pin 8 and pin7)	with 50 µs de-emphasis; m = 0.3; Δfi = ± 50 kHz; f_{AM} = 1 kHz	46	66	–	dB
(S+N)/N	signal-to-noise ratio (pin 8 and pin7)	with 50 µs de-emphasis; CCIR 468-3	64	68	–	dB
AF_{resp}	AF frequency response (pin 8 and pin 7)	$\Delta V_{AF1/2}$ = –3 dB	0.02	–	200	kHz
$AM_{res(rms)}$	residual sound carrier signal and harmonics (RMS value) (pins 8, 7)		–	50	–	mV
$\alpha_{8/7}$	crosstalk attenuation between AF outputs	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection	V_{RR} < 200 mV; f = 70 Hz	–	20	–	dB
Control unit (see Table 1)						
$V_{5,6}$	voltage for 'low'		0	–	0.8	V
$I_{5,6}$	input current	$0 < V_{5,6} < 0.8$	–	–180	–250	µA
$R_{5,6}$	allowed resistance to ground	$0 < V_{5,6} < 0.8$ ('low')	–	–	3.0	kΩ
V_5	voltage for HIGH (note 2)		2.2	–	V_P	V
V_6	voltage for HIGH (note 2)		1.8	–	V_P	V
$I_{5,6}$	input current	$V_{5,6} = V_P$	–	–	10	µA

Notes to the characteristics

1. The input signal at pin 15 can only be measured when mute is disabled. This is achieved by inserting a resistor of 2.7 kΩ between pin 15 and ground. Under this condition the input impedance is 490 Ω.
2. An open pin (n.c.) is interpreted as HIGH.

Multistandard / dual channel TV FM intercarrier sound demodulator

TDA9820

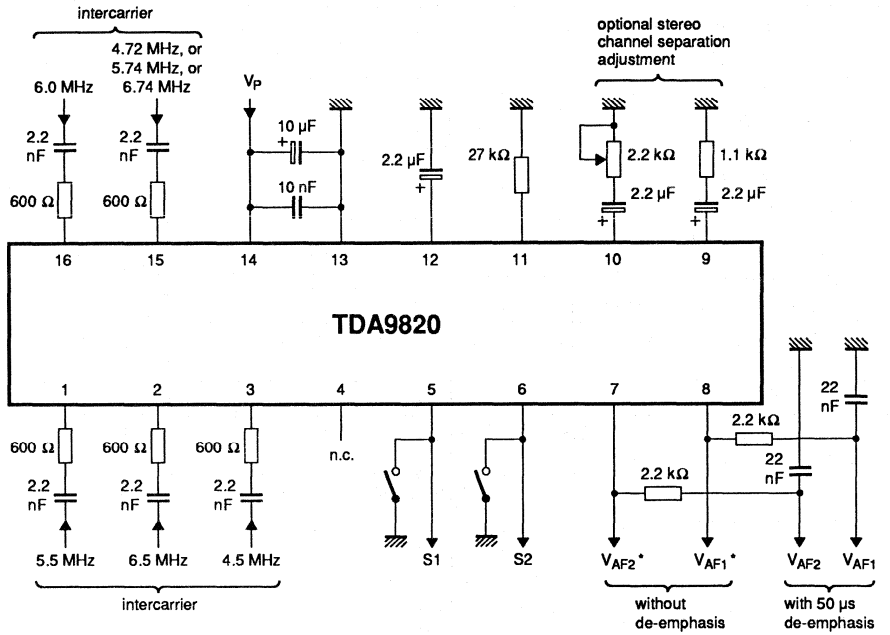


Fig.4 Test circuit.

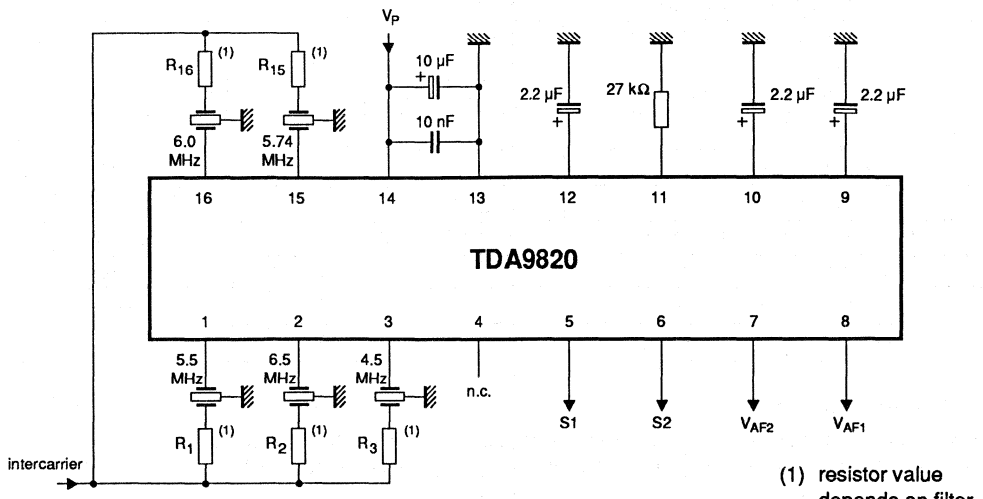


Fig.5 Application circuit.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1991

TDA9821

Dual channel TV FM intercarrier sound demodulator

FEATURES

- Two alignment-free PLL FM demodulators
- Automatic second sound carrier mute
- Mono and dual channel application
- Low power consumption
- Few external components

GENERAL DESCRIPTION

The TDA9821 is a monolithic, integrated, TV FM intercarrier sound demodulator for all FM standards. The circuit contains two separate FM demodulators using Phase-Locked Loop (PLL) reference frequency generation. The circuit has a minimum number of external components.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
I_M	peak output current (pin 8 and pin 7)		–	–	± 1.5	mA
P_{tot}	power dissipation	V_P = 5 V	–	–	150	mW
(S+N)/N	signal-to-noise ratio (pin 8 and pin 7)	CCIR 468-3	64	68	–	dB
$\alpha_{8/7}$	crosstalk attenuation	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection (pin 7 and pin 8)	V_{RR} < 200 mV; f = 70 Hz	–	20	–	dB
T_{amb}	operating ambient temperature range		0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9821	16	DIL	plastic	SOT38

Dual channel TV FM intercarrier sound demodulator

TDA9821

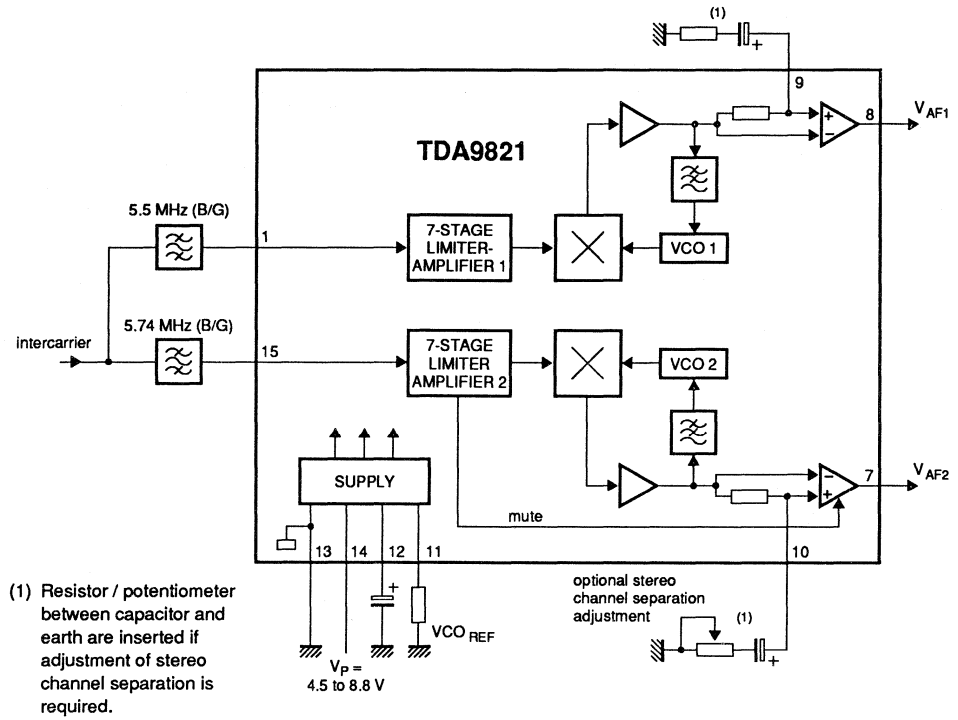


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The complete circuit consists of two separate channels , each consisting of a limiter-amplifier, FM demodulator and AF amplifier. Circuit operation is as follows (see Fig.1):

FM demodulators

The intercarrier signal is fed through external ceramic bandpass filters which are tuned to the sound carrier frequencies.

Each limiter amplifier is AC-coupled into an FM demodulator. The FM demodulator PLLs ensure that the demodulators are alignment-free. The FM demodulator outputs are amplified to 500 mV_{RMS}. The high amplification and DC error signals of the PLLs, which are superimposed on the FM demodulator outputs, require DC de-coupling at pin 9 and pin 10 of the AF amplifier inputs.

Stereo channel separation adjustment (optional)

Optimal stereo channel separation is achieved by adjusting V_{AF1} (pin 8) and V_{AF2} (pin 7) as follows:

a) V_{AF1} by a resistor in series with the DC de-coupling capacitor at pin 9

b) V_{AF2} by a variable resistor in series with the DC de-coupling capacitor on pin 10 to the same voltage as V_{AF1} .

Normally stereo channel separation is adjusted in the stereo decoder for the B/G standard.

Second sound carrier mute

The output of the second FM demodulator is muted when the signal level (signal and/or noise) at pin 15 is less than typically 0.5 mV_{RMS}. This avoids an incorrect stereo or dual sound identification when a mono signal is transmitted. Therefore, with a mono transmission, there is no audio output at pin 7. When the signal level at pin 15 is greater than typically 1.0 mV_{RMS} mute is switched off.

Dual channel TV FM intercarrier sound demodulator

TDA9821

PINNING

SYMBOL	PIN	DESCRIPTION
$IN_{1(B/G)}$	1	first intercarrier input at 5.5 MHz
n.c.	2	not connected
n.c.	3	
n.c.	4	
n.c.	5	
n.c.	6	
V_{AF2}	7	second audio output voltage
V_{AF1}	8	first audio output voltage
C_1	9	decoupling capacitor
C_2	10	decoupling capacitor
VCO_{REF}	11	VCO reference
C_{STAB}	12	supply voltage stabilization
GND	13	ground
V_P	14	supply voltage
$IN_{2(B/G)}$	15	second intercarrier input
n.c.	16	not connected

PIN CONFIGURATION

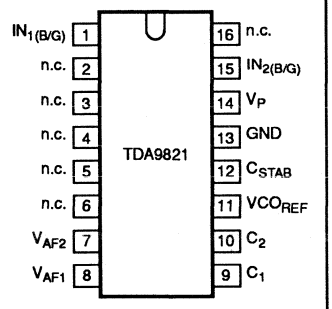


Fig.2 Pin configuration.

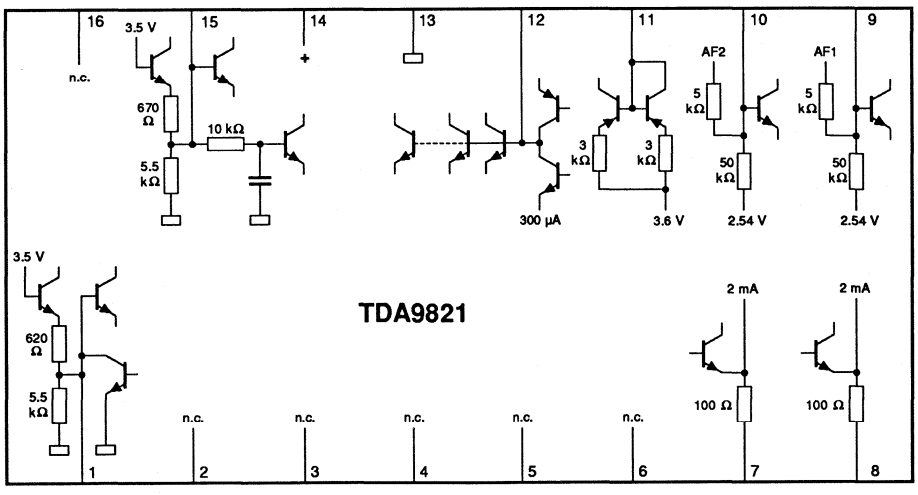


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage range (pin 14)	–0.5	9.0	V
V_i	input signal (pin 1 and pin 15)	–0.5	5.0	V
V_{adj}	adjusting voltage (pin 9 and pin 10)	–0.5	V_P + 0.5	V
T_{stg}	storage temperature range	–25	+ 125	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
P_{tot}	total power dissipation	–	150	mW

CHARACTERISTICS

All voltages are measured to GND (pin 13); V_P = 5.0 V; Δf_i = ± 50 kHz; f_{mod} = 1 kHz; $V_{1/15(rms)}$ = 10 mV; T_{amb} = 25 °C;measured in test circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
Limiter-amplifier 1						
V_1	DC input voltage		–	2.55	–	V
R_1	input resistance		480	600	720	Ω
$V_{1(rms)}$	input signal(RMS value)	(S+N)/N = 40 dB	–	100	250	µV
	allowed input signal (RMS value)		200	–	–	mV
Limiter-amplifier 2						
V_{15}	DC input voltage		–	2.55	–	V
$V_{15(rms)}$	input signal (RMS value)	(S+N)/N = 40 dB; note 1	–	150	250	µV
	input signal for mute off (RMS value)		0.7	1.0	1.5	mV
	allowed input signal (RMS value)		200	–	–	mV
ΔV_{15}	mute hysteresis		–	12	–	dB
R_{15}	input resistance		480	600	720	Ω
PLL FM demodulators VCO1 and VCO2						
f_{VCO1}	free-running frequency	R_{11} = 27 kΩ	–	5.5	–	MHz
f_{VCO2}	free-running frequency	R_{11} = 27 kΩ	–	5.74	–	MHz
$\Delta f_{VCO1/2}$	free-running frequency spread		–	–	± 10	%
	drift of free-running frequencies	0 to 70 °C	–	500	–	kHz
	shift of free-running frequencies	4.5 V < V_P < 8.8 V	–	200	–	kHz
	adjustment range of free-running frequencies	resistance at pin 11	± 1	–	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PLL FM demodulators VCO1 and VCO2 (continued)						
R_{11}	adjustment resistance for free-running frequencies (pin 11)		15	22	29	kΩ
S	steepness of free-running frequency adjustment	R_{11} = 27 kΩ	–	–200	–	kHz/kΩ
Δf1	catching range of PLLs		± 1.4	± 1.9	–	MHz
Δf2	holding range of PLLs		± 2.0	± 3.0	–	MHz
Output amplifiers AF1 (pin 8) and AF2 (pin 7) and overall performance						
V_o	DC output voltage (pin 8 and pin7)		–	2.15	–	V
$V_{o(rms)}$	output signal (pin 8 and pin7) (RMS value)		–	0.5	–	V
		clipping level	1.2	–	–	V
I_M	AC output peak current (pin 8 and pin7)		–	–	± 1.5	mA
I_o	DC output current (pin 8 and pin7)		–	–	–2.0	mA
$\Delta V_o/V_o$	absolute drift of AF output signals	0 to 70 °C	–	0.7	–	dB
	relative drift of AF output signals	0 to 70 °C	–	0.2	–	dB
$V_{AF(1-2)}$	difference between output signals (pin 8 and pin7)	with 50 μs de-emphasis	–	± 0.3	± 1.0	dB
R_o	output resistance (pin 8 and pin7)		–	100	–	Ω
R_s	series resistor for optional crosstalk adjustment at pin 9	$V_{AF(1-2)}$ = ± 1.5 dB	–	1.1	–	kΩ
	at pin 10		–	1.1	2.2	kΩ
THD	total harmonic distortion at pin 8	with 50 μs de-emphasis	–	0.1	0.3	%
	at pin 7		–	0.25	0.5	%
α_{AM}	AM suppression of AF1/2 (pin 8 and pin7)	with 50 μs de-emphasis; m = 0.3; Δf_i = ± 50 kHz; f_{AM} = 1 kHz	46	66	–	dB
(S+N)/N	signal-to-noise ratio (pin 8 and pin7)	with 50 μs de-emphasis; CCIR 468-3	64	68	–	dB
AF_{resp}	AF frequency response (pin 8 and pin 7)	$\Delta V_{AF1/2}$ = –3 dB	0.02	–	200	kHz
$AM_{res(rms)}$	residual sound carrier signal and harmonics (RMS value) (pins 8, 7)		–	50	–	mV
$\alpha_{8/7}$	crosstalk attenuation between AF outputs	f = 50 to 12.500 Hz	–	70	–	dB
RR	supply voltage ripple rejection	V_{RR} < 200 mV; f = 70 Hz	–	20	–	dB

Note to the characteristics

1. The input signal at pin 15 can only be measured when mute is disabled. This is achieved by inserting a resistor of 2.7 kΩ between pin 15 and ground. Under this condition the input impedance is 490 Ω.

Dual channel TV FM intercarrier sound demodulator

TDA9821

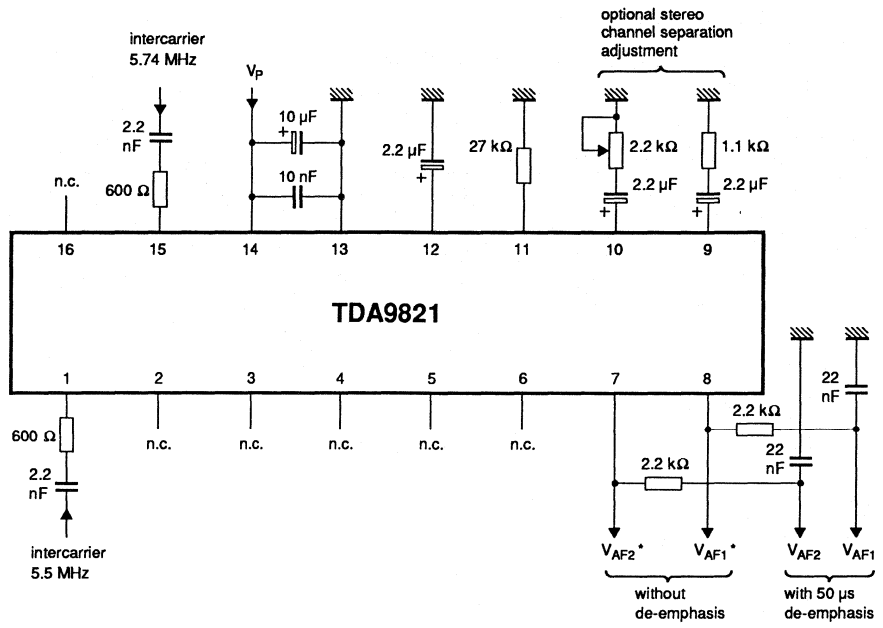


Fig.4 Test circuit.

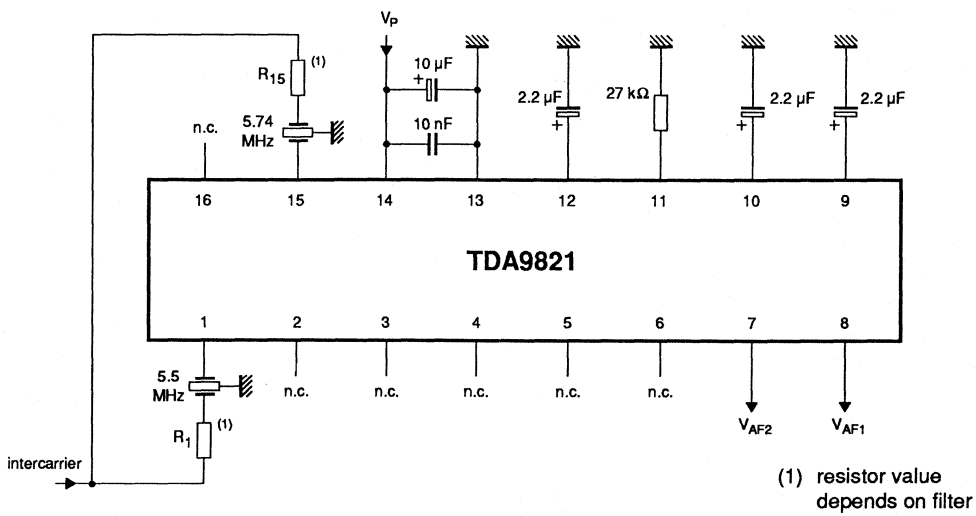


Fig.5 Application circuit.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1992

TDA9830

TV sound AM-demodulator and audio source switch

FEATURES

- Adjustment free wideband synchronous AM demodulator
- Audio source-mute switch (low noise)
- Audio level according EN50049
- 5 to 8 V power supply or 12 V alternative
- Low power consumption

GENERAL DESCRIPTION

The TDA9830, a monolithic integrated circuit, is designed for AM-sound demodulation used in L- and L'-standard. The IC provides an audio source selector and a mute switch.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{14}	positive supply voltage	4.5	5.0	8.8	V
V_{11}	supply voltage (alternative)	10.8	12.0	13.2	V
$I_{14,11}$	supply current	24	30	36	mA
V_{1-16}	IF sensitivity (RMS value) (for –3 dB AF-signal)	–	60	100	µV
G_V	gain control range	60	66	–	dB
V_6	AF output signal (m = 54%) (RMS value)	400	500	600	mV
V_6	S/N ratio acc. CCIR468-3 (IF-signal 10 mV_{RMS})	47	53	–	dB
$V_{7,9}$	AF input signal (for THD < 1.5%) (RMS value)	–	–	1.2	V
V_8	crosstalk and mute attenuation	80	90	–	dB
T_{amb}	operating ambient temperature range	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9830	16	DIL	plastic	SOT38

TV sound AM-demodulator and audio source switch

TDA9830

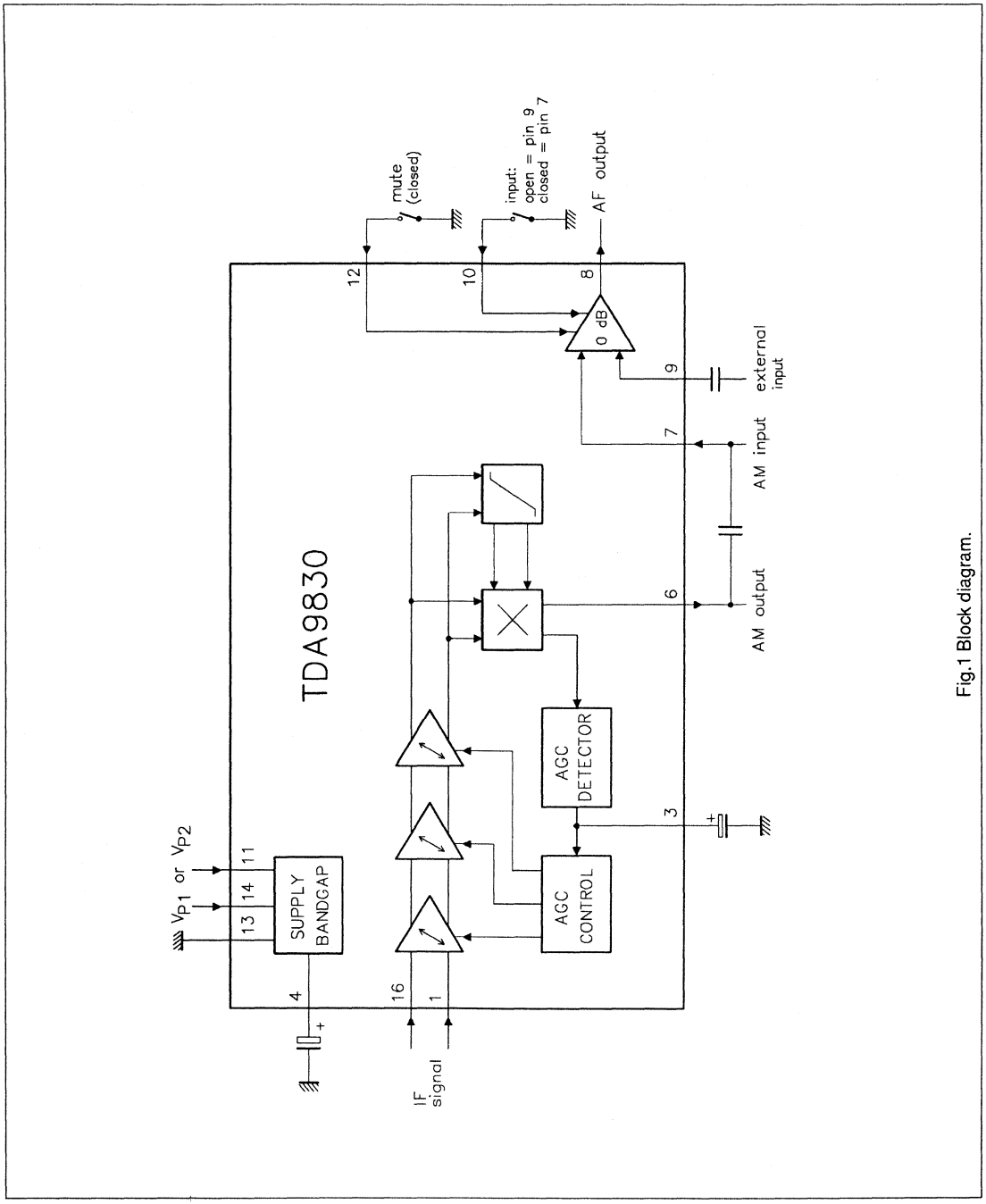


Fig.1 Block diagram.

TV sound AM-demodulator and audio source switch

TDA9830

PINNING

SYMBOL	PIN	DESCRIPTION
IFIN	1	sound IF differential input signal
n.c.	2	not connected
C_{AGC}	3	AGC capacitor
C_{REF}	4	REF voltage filtering capacitor
n.c.	5	not connected
AMOUT	6	AM demodulator output
AMIN	7	input signal (from AM) to audio switch
AFOUT	8	output signal from audio switch
EXTIN	9	input signal (from external) to audio switch
SWITCH	10	switch input select control
V_{p2}	11	supply voltage +12 V (alternative)
MUTE	12	mute control
GND	13	ground (0 V)
V_{p1}	14	supply voltage +5 to +8 V
n.c.	15	not connected
IFIN	16	sound IF differential input signal

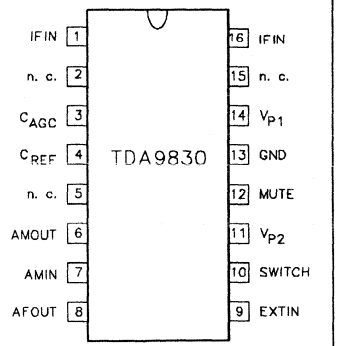


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Sound IF input

The sound IF amplifier consists of three AC-coupled differential amplifier stages each with approximately 20 dB gain. At the output of each stage is a multiplier for gain controlling (→ current distribution gain control). The overall control range is approximately -6 to +60 dB and the frequency response (-3 dB) of the IF amplifier is approximately 6 to 70 MHz. The steepness of gain control is approximately 10 mV/dB.

IF AGC

The automatic gain control voltage to maintain the AM demodulator output signal at a constant level is generated by a mean level detector. This AGC-detector charges and discharges the capacitor at pin 3 controlled by the output signal of the AM-demodulator compared to an internal reference voltage. The maximum charge/discharge current is approximately 5 μA. This value in combination with the value of the AGC capacitor and the AGC steepness determines the lower cut-off audio frequency and the THD-figure at low modulation frequency of the whole AM-demodulator. Therefore a large time constant has to be choosen which leads to slow AGC reaction at IF level charge. To speed up the AGC in case of IF signal jump from low to high level, there is an additional comparator built in, which can provide additional discharge current from the AGC capacitor up to 5 mA in a case of overloading the AM demodulator by the internal IF signal.

AM-demodulator

The IF amplifier output signal is fed to a limiting amplifier (two stages) and to a multiplier circuit. However the limiter output signal (which is not longer AM modulated) is also fed to the multiplier, which provides AM demodulation (in phase demodulation). After lowpass filtering ($f_g \approx 400$ kHz) for carrier rejection and buffering, the demodulator output signal is present on pin 6. The AM demodulator operates over a wide frequency range, so that in combination with the frequency response of the IF amplifier applications in a frequency range from approximately 6 MHz up to 70 MHz are possible.

Audio switch

This circuit is an operational amplifier with three input stages and internal feedback network determining gain (0 dB) and frequency response ($f_g \approx 700$ kHz). Two of the input stages are connected to pin 7 and pin 9, the third input stage to an internal reference voltage. Controlled by the switching pins 10 and 12, one of the three input stages can be activated and a choice made between two different AF signals or mute state. The selected signal is present at pin 8. The decoupling capacitors at the input pins are needed, because the internally generated bias voltage for the input stages must not be influenced by the application in order to avoid DC-plop in case of switching.

The AM demodulator output is designed to provide almost the same DC voltage as the input bias voltage of the audio switch. But there may be spread between both voltages. Therefore it is possible to connect pin 6 directly to pin 7 (without a decoupling capacitor), but in this event the DC-plop for switching can increase up to 100 mV.

Reference circuit

This circuit is a band gap stabilizer in combination with a voltage regulation amplifier, which provides an internal reference voltage of about 3.6 V nearly independant from supply voltage and temperature. This reference voltage is filtered by the capacitor at pin 4 in order to reduce noise. It is used as a reference to generate all important voltages and currents of the circuit.

For application in 12 V power supply concepts, there is an internal voltage divider in combination with a Darlington transistor in order to reduce the supply voltage for all IC function blocks to approximately 6 V. This is necessary because of use of modern high frequency IC technology, where most of the used integrated components are only allowed to operate at maximum 9 V supply voltage.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{14-13}	supply voltage V_{P1}	-0.5	8.9	V
V_{11-13}	supply voltage V_{P2}	-0.5	13.3	V
$V_{10,12-13}$	switching voltage	-0.5	V_P + 0.5	V
T_{amb}	operating ambient temperature range	0	+70	°C
T_{stg}	storage temperature	-25	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	74 K/W

CHARACTERISTICS

V_{P1} = 5.0 V at pin 14; T_{amb} = +25 °C; sound carrier f_{SC} = 32.4 MHz modulated with f = 1 kHz and modulation depth m = 54%. IF input signal (sound carrier): V_{1-16} = 10 mV_{RMS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{14-13}	positive supply voltage V_{P1}	note 1	4.5	5.0	8.8	V
V_{11-13}	positive supply voltage V_{P2}	note 1	10.8	12.0	13.2	V
I_{11}/I_{14}	current consumption		24	30	36	mA
IF amplifier and gain control						
R_{1-16}	input resistance		1.75	2.2	2.65	kΩ
C_{1-16}	input capacitance		1.0	1.5	2.2	pF
V_{1-16}	minimum IF input signal (RMS value)	note 2	–	60	100	μV
V_{1-16}	maximum IF input signal (RMS value)	note 3	70	120	–	mV
G_V	gain control range		60	66	–	dB
I_3	maximum AGC charging/discharging current		3.5	5	7	μA
I_3	fast AGC discharging current		–	–	5	mA
V_3-V_{13}	gain control voltage (G_{min}-G_{max})		1.5	–	2.8	V
B	–3 dB IF bandwidth	upper cut-off frequency	50	70	–	MHz
		lower cut-off frequency	–	6	10	MHz
$V_{1/16-13}$	DC potential		–	1.7	–	V
AM-Demodulator						
V_{6-13}	AF output signal (RMS value)		400	500	600	mV
B	–3 dB AF bandwidth	upper cut-off frequency	100	–	–	kHz
		lower cut-off frequency; note 7	–	–	20	Hz
V_{6-13}	THD		–	0.8	2	%
V_{6-13}	S/N (weighted acc. CCIR 468-3)		47	53	–	dB
V_{6-13}	DC potential		2.00	2.15	2.30	V
R_6	output resistance (emitter follower with 0.5 mA bias current)		–	300	–	Ω
I_{6abs}	allowable AC output current		–	–	0.3	mA
$-I_6$	allowable DC output current		–	–	0.5	mA
Audio-switch						
$V_{7,9-13}$	AF-input-signal for THD < 1.5% (RMS value)		–	–	1.2	V
V_{8-13}	S/N ratio of audio switch (in accordance with CCIR 468-3)	reference signal at pin 7/9 is 0.5V_{RMS}	70	80	–	dB
B	–3 dB AF bandwidth	upper limit	100	–	–	kHz
V_{8-13}	THD at 1 V_{RMS} input signal at pin 7 or 9		–	0.1	1.0	%
V_{8-13}	crosstalk and mute attenuation	20 Hz to 20 kHz	80	90	–	dB
$V_{7,8,9-13}$	DC-potential		2.00	2.15	2.30	V
$R_{7,9-13}$	input resistance		40	50	60	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$G_{7,9-8}$	gain of audio switch		-0.5	0	+0.5	dB
V_{10-13}	audio switching voltage to activate pin 7		0	–	0.8	V
V_{10-13}	audio switching voltage to activate pin 9	note 4	1.5	–	V_P	V
V_{12-13}	input voltage for MUTE-ON		0	–	0.8	V
	input voltage for MUTE-OFF	note 4	1.5	–	V_P	V
$-I_{10,12}$	output current of switching-pins at $V_{10,12-13} = 0$ V		110	145	185	μA
V_{8-13}	DC-plop at AF output pin with switching from internal to external audio signal or to mute-state or vice-versa	note 5	–	5	10	mV
R_8	output resistance		70	100	150	Ω
Ripple rejection note 6						
RR	AF signal output: $\alpha_{RR} = V_{ripple}$ on V_P / V_{ripple} on V_{out}		26	30	–	dB
	AF signal output with AF signal from external source		40	44	–	dB

Notes to the characteristics

1. In the power supply voltage range V_{P1} = 5.0 V up to 8.0 V the performance will not change essentially. With power supply from V_{P2} = 12.0 V the performance will be comparable with the performance at V_{P1} = 5.0 V up to 8.0 V.
   The unused power supply pin must be not connected.
2. Start of gain control (low IF input signal) at –3 dB AF signal reduction at pin 6.
3. End of gain control (high IF input signal) at +1 dB AF signal expansion at pin 6.
4. This state is also valid for pin left open.
5. If a DC-plop of about maximum 100 mV is acceptable when switching from internal to external audio-signal or from internal to mute state or vice-versa, the capacitor between pin 6 and 7 can be omitted and pin 6 can be connected to pin 7.
6. Measured with V_{ripple} = 200 $mV_{(p-p)}$ at 70 Hz superimposed on supply voltage V_P.
7. Dependent on value of AGC capacitor.

TV sound AM-demodulator and audio source switch

TDA9830

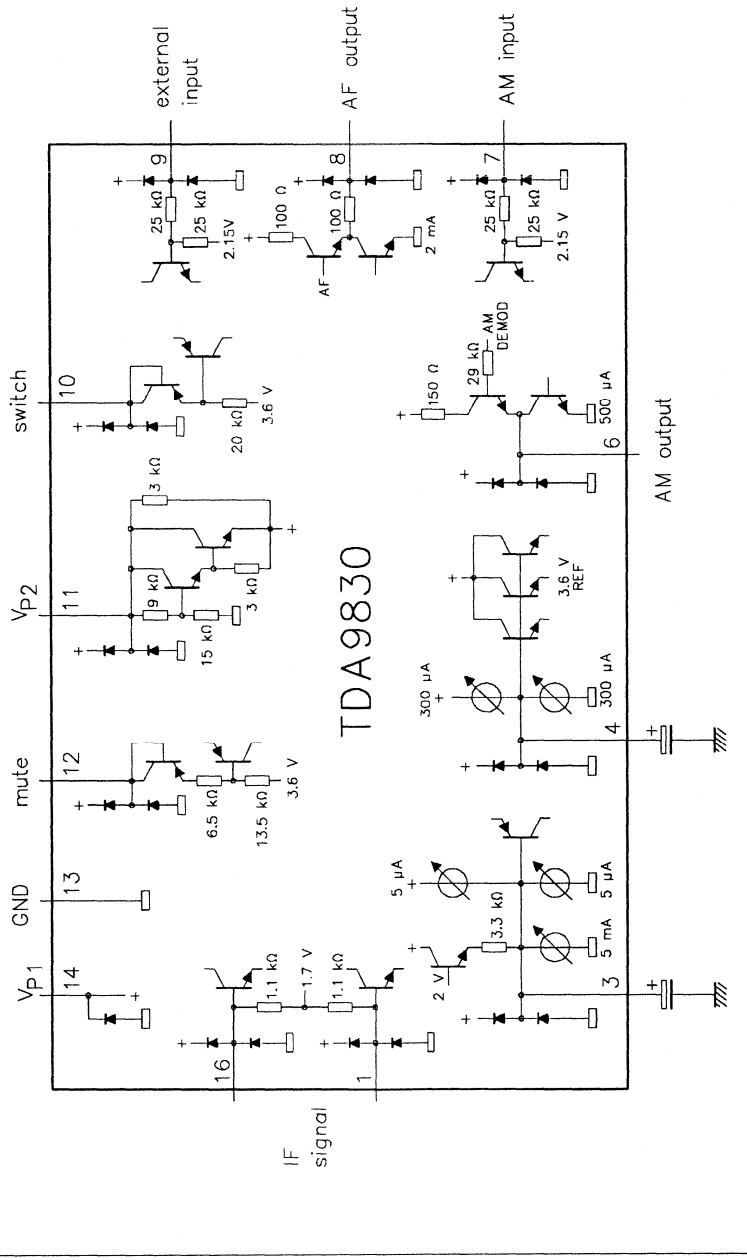


Fig.3 Internal circuits.

TV sound AM-demodulator and audio source switch

TDA9830

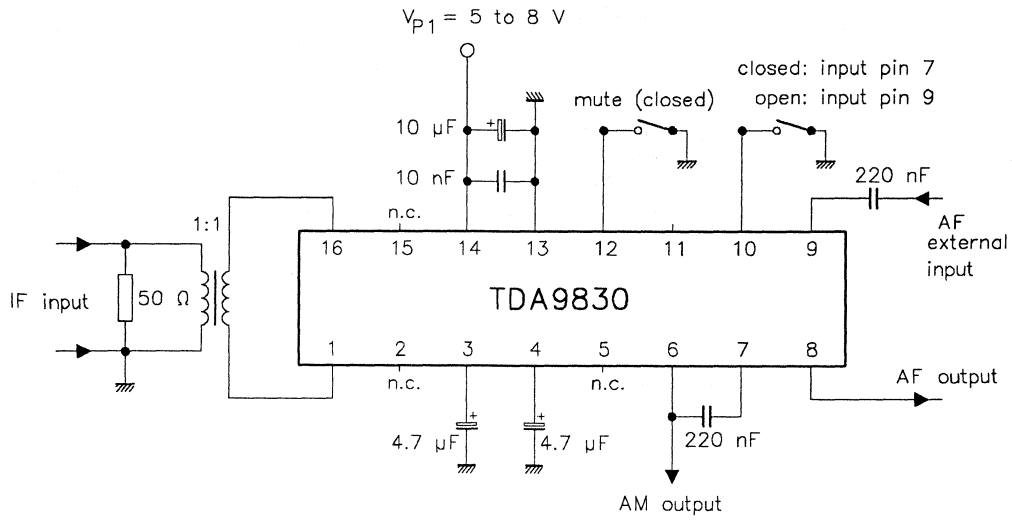


Fig.4(a) Test circuit 5 to 8 V supply.

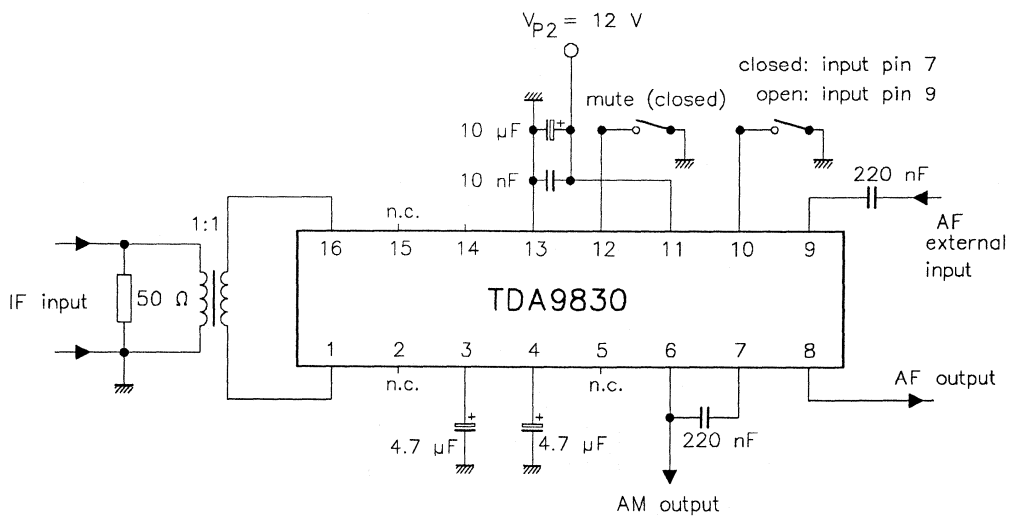


Fig.4(b) Test circuit 12 V supply.

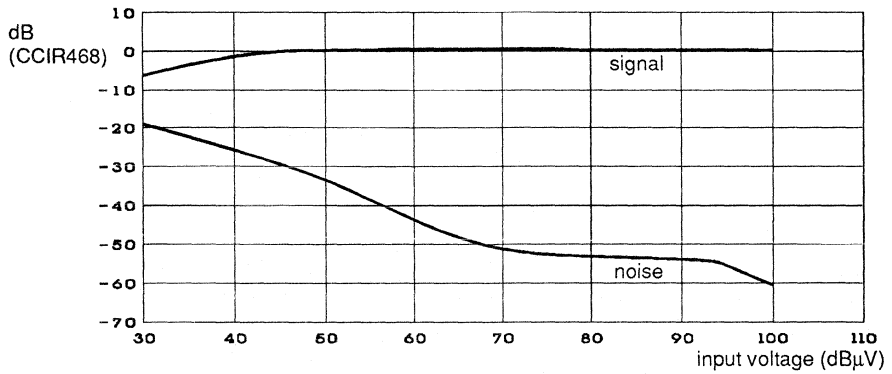


Fig.5 S/N figure as a function of the IF input signal.

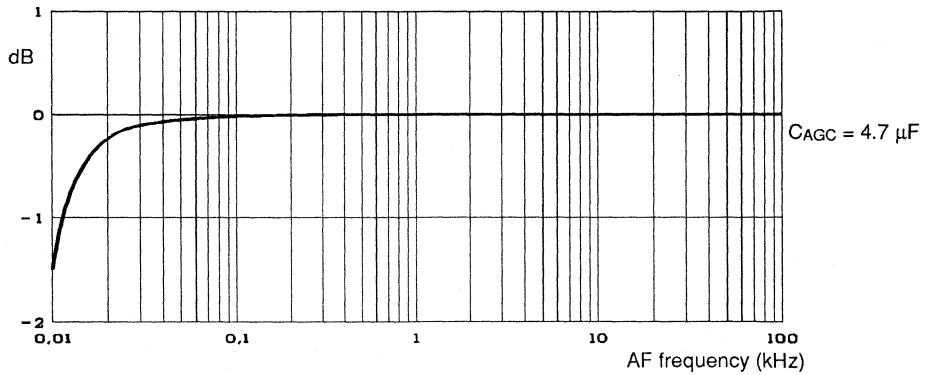


Fig.6(a) Frequency response at pin 6.

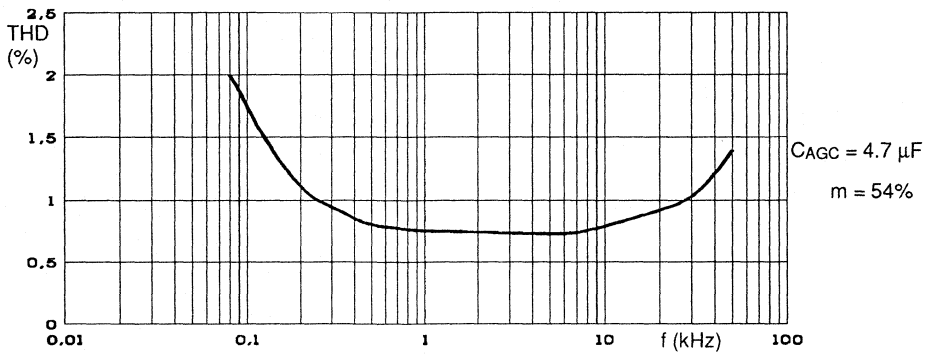


Fig.6(b) THD at pin 6.

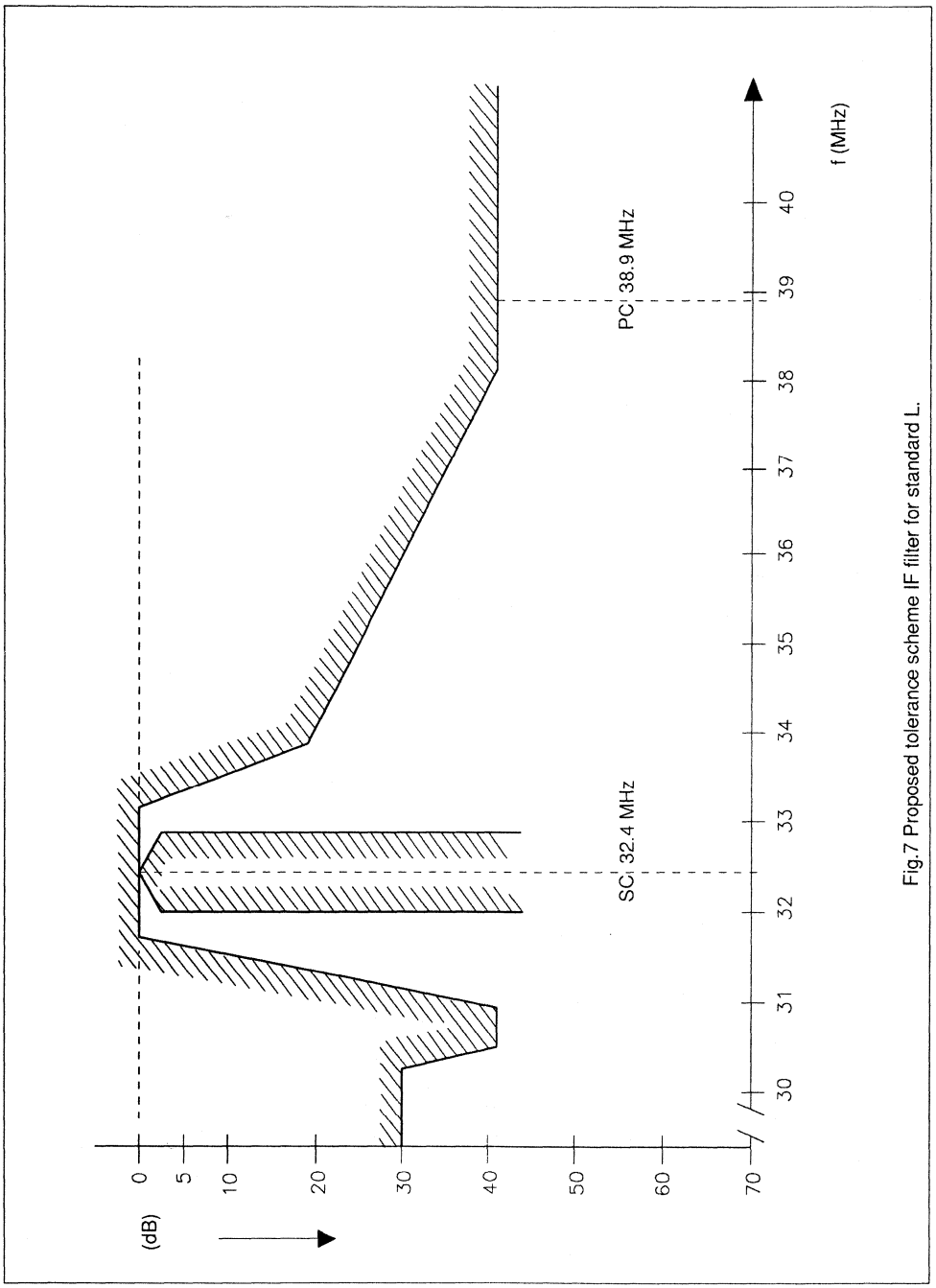


Fig.7 Proposed tolerance scheme IF filter for standard L.

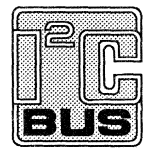
With an IF filter according to this proposal, the video buzz suppression on the audio output is better than 50 dB (in accordance with CCIR468-3, m = 54%) for the worst case video modulation with 6 kHz sinewave black-to-white.

Philips Semiconductors

Data sheet	
status	Objective specification
date of issue	June 1991

TDA9840

Stereo/dual sound processor with digital identification



FEATURES

- Level and stereo matrix adjustment possible via the I²C-bus
- Two additional AF inputs for NICAM and AM sound
- Outputs for MAIN and SCART
- AF input and AF output signals selectable via the I²C-bus
- Pilot frequency regeneration for mixer by digital PLL
- Demodulation of sound identification (117 and 274 Hz) by digital PLL and digital integration
- Information for identified transmission mode readable via the I²C-bus
- Supply voltage 5 to 8 V

GENERAL DESCRIPTION

The TDA9840 is a stereo/dual sound processor for TV and VTR sets. Its digital identification ensures safe operation by using internal digital PLL filter technique with extremely small bandwidth (switching time maximum 2 s).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 18)	4.5	5	8.8	V
I_P	supply current	-	15	-	mA
V_i	input signal (RMS value)	-	500	-	mV
V_o	output signal (RMS value)	-	1	-	V
G_v	total signal gain	5	6	7	dB
ΔG_v	stereo control range for $V_{i\,1}$ (0.1 dB steps) level control range for $V_{i\,2}$ (0.5 dB steps)	 - -	+2.5 −2.4 +2.5 −2.0	- - - -	dB dB dB dB
$V_{i\,pil}$	input sensivity of pilot frequency	5	-	-	mV
t_{sw}	switching time for change to any mode	0.6	-	2	s
S/N(W)	weighted signal-to-noise ratio	72	-	-	dB
THD	total harmonic distortion	-	0.2	-	%
T_{amb}	operating ambient temperature	0	-	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9840	20	DIL	plastic	SOT146
TDA9840T	20	mini-pack	plastic	SOT163A

Stereo/dual sound processor with digital identification

TDA9840

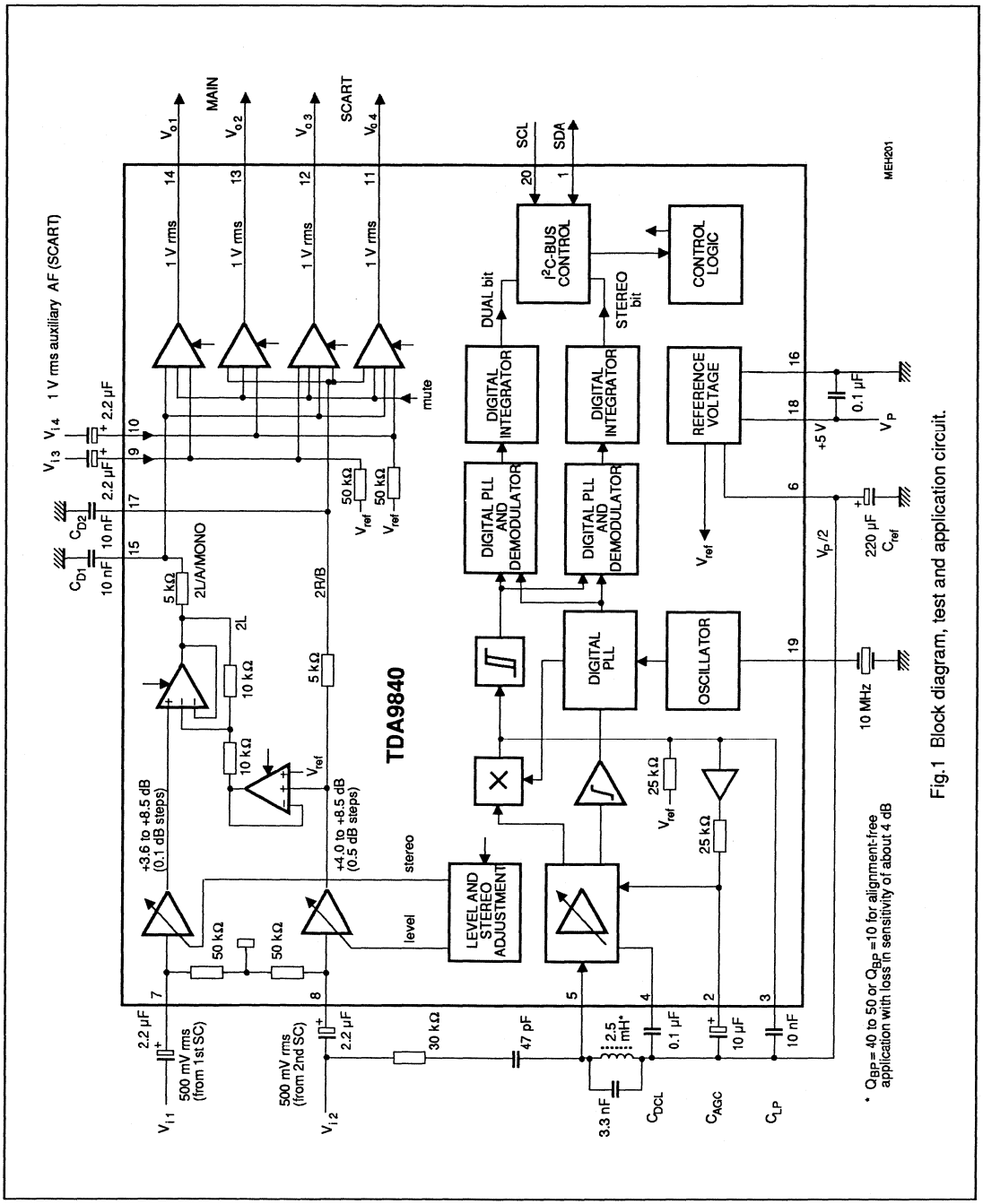


Fig.1 Block diagram, test and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus data line
C_{AGC}	2	AGC capacitor of pilot frequency amplifier
C_{LP}	3	low-pass capacitor
C_{DCL}	4	DC loop capacitor
$V_{i\,pil}$	5	pilot frequency input
C_{ref}	6	capacitor of reference voltage (V_P/2)
$V_{i\,1}$	7	AF input 1 signal (from 1st sound carrier)
$V_{i\,2}$	8	AF input 2 signal (from 2nd sound carrier)
$V_{i\,3}$	9	AF input 3 signal (additional input)
$V_{i\,4}$	10	AF input 4 signal (additional input)
$V_{o\,4}$	11	AF output 4 signal
$V_{o\,3}$	12	AF output 3 signal
$V_{o\,2}$	13	AF output 2 signal
$V_{o\,1}$	14	AF output 1 signal
C_{D1}	15	50 µs de-emphasis capacitor of channel 1
GND	16	ground (0 V)
C_{D2}	17	50 µs de-emphasis capacitor of channel 2
V_P	18	supply voltage (+5 to +8 V)
XTAL	19	10 MHz crystal
SCL	20	I²C-bus clock line

PIN CONFIGURATION

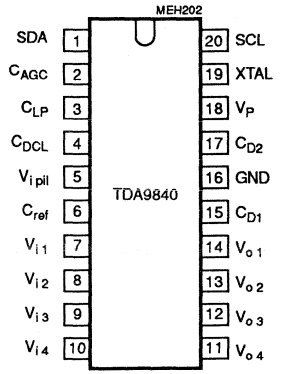


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

AF signal handling

AF input signals for pins 7 and 8 are coming from the FM demodulators. The information of the 1st sound carrier corresponds with AF input 1 (pin 7). The circuit contains a level controller (pin 8) and a stereo controller (pin 7) to correct spreads in signals of the previous demodulators.These controls by the customer are achieved via the I²C-bus (Tables 4 and 5); final bytes are stored in a memory. Normally the gain is 6 dB to provide 1 V rms output signals for 0.5 V rms input signals. Stereo de-matrixing uses the wellknown technique of two operational amplifiers to switch and add the AF signals.
De-emphasis of 50 µs is performed by two low-pass filters (internal 5 kΩ; external 10 nF on pins 15 and 17).

Four source selectors with 0 dB gain, composed of rail-to-rail amplifiers, are controlled via the I²C-bus. Switching plop and distortion are minimized, random noise is considerably reduced. Selections can be made for different modes as there are STEREO, DUAL, MONO and AUX sound (Table 3).

Stereo/dual sound identification

The pilot signal of 54.7 kHz is coupled by means of a high-pass to the input pin 5. The external LC bandpass should have a Q-factor of about 40 to 50 to ensure the highest identification sensitivity. By using a fixed coil to save the alignment, a Q-factor of about 10 is proposed. This may cause a loss in sensitivity of about 4 to 5 dB.
A digital PLL regenerates the pilot carrier, which is used in the synchronous AM demodulator to get the identification signal. The identification signal is internally filtered by a low-pass (pin 3).

AGC voltage integration is achieved by an internal 25 kΩ resistor and an external capacitor (pin 2).

The identification signal is shaped in a Schmitt-trigger, provided that the signal is higher than the threshold. Smaller signals are suppressed, as a measure against mis-identification caused by spurious components in the signal.

The identification stages are digital PLL circuits with digital synchronous demodulators followed by digital integrator stages. The generated HIGH-levels are loaded into the status register to be read via the I^2C-bus. Automatically switching of AF modes is not provided.

The 10 MHz crystal oscillator provides the reference clock frequency. The corresponding detection bandwidth for the pilot carrier signal is larger than ±50 Hz to ensure the identification, if the pilot frequency is drifting due to the transmitter.

I^2C-bus transmission

The circuit is a slave transmitter to read the status byte with information of transmitted mode and power-on reset (Table 1). It is slave receiver to switch the mode and to adjust at first the AF level and then the stereo balance (Tables 2 to 5).

Subaddresses 00 to 03 (hex) increment automatically. For subaddress 01 there is no register, but the data byte (of 01 subaddress) is acknowledged.

Power-on reset sets all register bits to zero, the PONRES bit of the status byte is set to one.

After a power-on reset, the microcontroller has to write the contents of the registers once more.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)	0	8.8	V
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling for all pins	-	±500*	V
		-	±4**	kV

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

** Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; $V_{i\ AF}$ = 0.5 V rms; $V_{o\ AF}$ = 1 V rms; f = 1 kHz; $V_{i\ pil}$ = 16 mV rms; f_{pil} = 54.6875 kHz (identification frequencies: STEREO = 117.48 Hz; DUAL = 274.1 Hz); 50 µs pre-emphasis and measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 18)		4.5	5	8.8	V
I_P	supply current		-	15	-	mA
V_{ref}	reference voltage range (pin 6)		-	$V_P/2$	-	V
V_n	DC voltage on input and output pins 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 and 17		-	$V_P/2$	-	V
AF inputs (pins 7 and 8)						
V_i	nominal input signal (RMS value)		-	500	-	mV
$\Delta V_{i\ 1}$	stereo control range	on pin 7 only	+2.4 −2.3	+2.5 −2.4	+2.6 −2.5	dB dB
	nominal step	maximum 49 steps	-	0.1	-	dB
$\Delta V_{i\ 2}$	level control range	on pin 8 only	- -	+2.5 −2.0	- -	dB dB
	nominal step	maximum 9 steps	-	0.5	-	dB
R_i	input resistance		-	50	-	kΩ
R_{deem}	internal de-emphasis resistor	Fig.4	4.25	5.0	5.75	kΩ
	resistore tolerance		-	-	±15	%
Additional AF inputs (pins 9 and 10)						
V_i	input signal (RMS value)	nominal	-	1	-	V
R_i	input resistance		-	50	-	kΩ
AF outputs (pins 11, 12, 13 and 14)						
V_o	nominal output signal (RMS value)	THD ≤ 0.5 %	-	1	-	V
R_o	output resistance		-	500	-	Ω
C_L	load capacitor on output		-	-	1.5	nF
G_v	signal gain	$G = V_o / V_i$; note 1	5	6	7	dB
B	frequency response (bandwidth)	f = 40 to 15000 Hz; note 2	-	-	±0.5	dB
THD	total harmonic distortion	note 1	-	0.2	0.3	%
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3 (quasi-peak)	72	-	-	dB
α_{cr}	crosstalk attenuation for	notes 1 and 3				
	DUAL	$R_S \leq 1$ kΩ	70	75	-	-dB
	STEREO	$R_S \leq 1$ kΩ	30	40	-	-dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{mute}	mute attenuation	$R_S \leq 1$ kΩ; note 1	76	80	-	dB
ΔV_{DC}	offset voltage on outputs between any two modes	after switching	-	-	±10	mV
RR	ripple rejection	f = 70 Hz; Fig.3	50	-	-	dB
α_{SCL}	crosstalk from I²C-bus		tbf	-	-	dB
10 MHz crystal oscillator (pin 19)						
f_o	series resonant frequency of crystal	$C_L = \infty$	9.995	10.008	10.021	MHz
$\Delta f/f_{o\ typ}$	spread of oscillator frequency		-	-	±2000	10^{-6}
R_S	series resistance of crystal		-	60	-	Ω
C_{19}	input capacitance		-	tbf	-	pF
Pilot processing						
$V_{i\ pil}$	pilot input sensitivity on pin 5 (RMS value)	unmodulated	5	-	-	mV
m	modulation depth	AM	25	50	75	%
Δf_{pil}	pilot PLL pull-in range	f_o = 10.008	-	-	±300	Hz
R_5	input resistance		-	tbf	-	kΩ
ΔG_v	signal gain control range (AGC)		-	tbf	-	dB
V_2	AGC voltage range		-	tbf	-	V
f_{LP}	low-pass response (pin 3)	–3 dB	450	600	750	Hz
R_3	output resistance		19	25	31	kΩ
Q_L	quality factor of resonant circuit	high sensitivity	40	-	50	
	with fixed coil	sensitivity loss 4 to 5 dB	-	10	-	
Identification (internal functions)						
V_i	identification sensitivity (pin 5)	note 4	-	28	-	dB/μV
S/N	pilot carrier-to-noise ratio for start of identification (pin 5)	1.1 kHz bandwidth	-	0	-	dB
H	hysteresis		-	-	3	dB
f_{det}	pull-in range of identification PLL	STEREO	-	-	±0.38	Hz
		DUAL	-	-	±0.69	Hz
t_{det}	pull-in time of identification PLL		-	-	1	s
f_{ident}	identification window width	STEREO	-	-	1.88	Hz
		DUAL	-	-	2.24	Hz
t_{integr}	integrator time constant		-	-	1	s
t_{ident}	total identification time		0.6	-	2	s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus, SDA and SCL (pins 1 and 20)						
$V_{1, 20}$	input voltage HIGH-level		3	-	V_P	V
	input voltage LOW-level		0	-	1.5	V
$I_{1, 20}$	input current		-	-	±10	µA
V_{ACK}	output voltage at acknowledge (pin 1)	I_1 = –3 mA	-	-	0.4	V

Notes to the characteristics

1. V_o = 1 V RMS; f = 1 kHz; input controlling amplifiers with ΔG_v = 0 dB
2. without de-emphasis capacitors with respect to nominal gain
3. In DUAL mode: signal A into channel B, signal B into channel A.
   In STEREO mode: signal R into left channel, signal L = 0
4. EMF on pin 5 with R_S = 75 Ω (2T/20T/W, 100% video modulation); VC/SC1 = 13 dB; VC/SC2 = 20 dB; Δf ≤ 70 kHz; THD ≤ 3%, AF bandwidth ≤ 20 kHz.

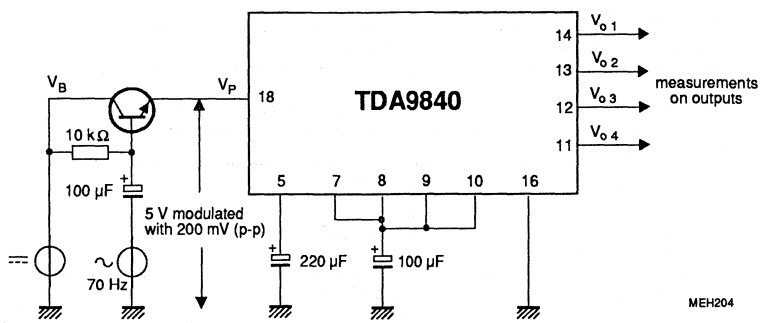


Fig.3 Test circuit for measurement of ripple rejection.

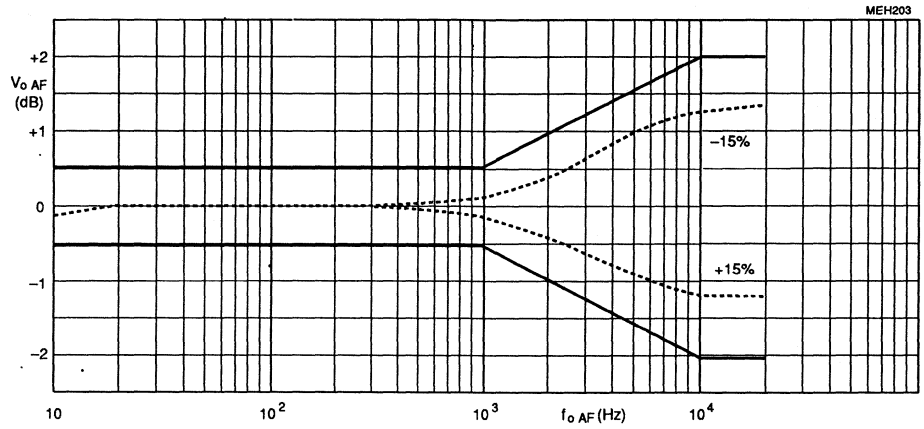


Fig.4 Tolerance scheme of AF frequency response. De-emphasis with C = 10 nF and R = 5 kΩ (±15%).

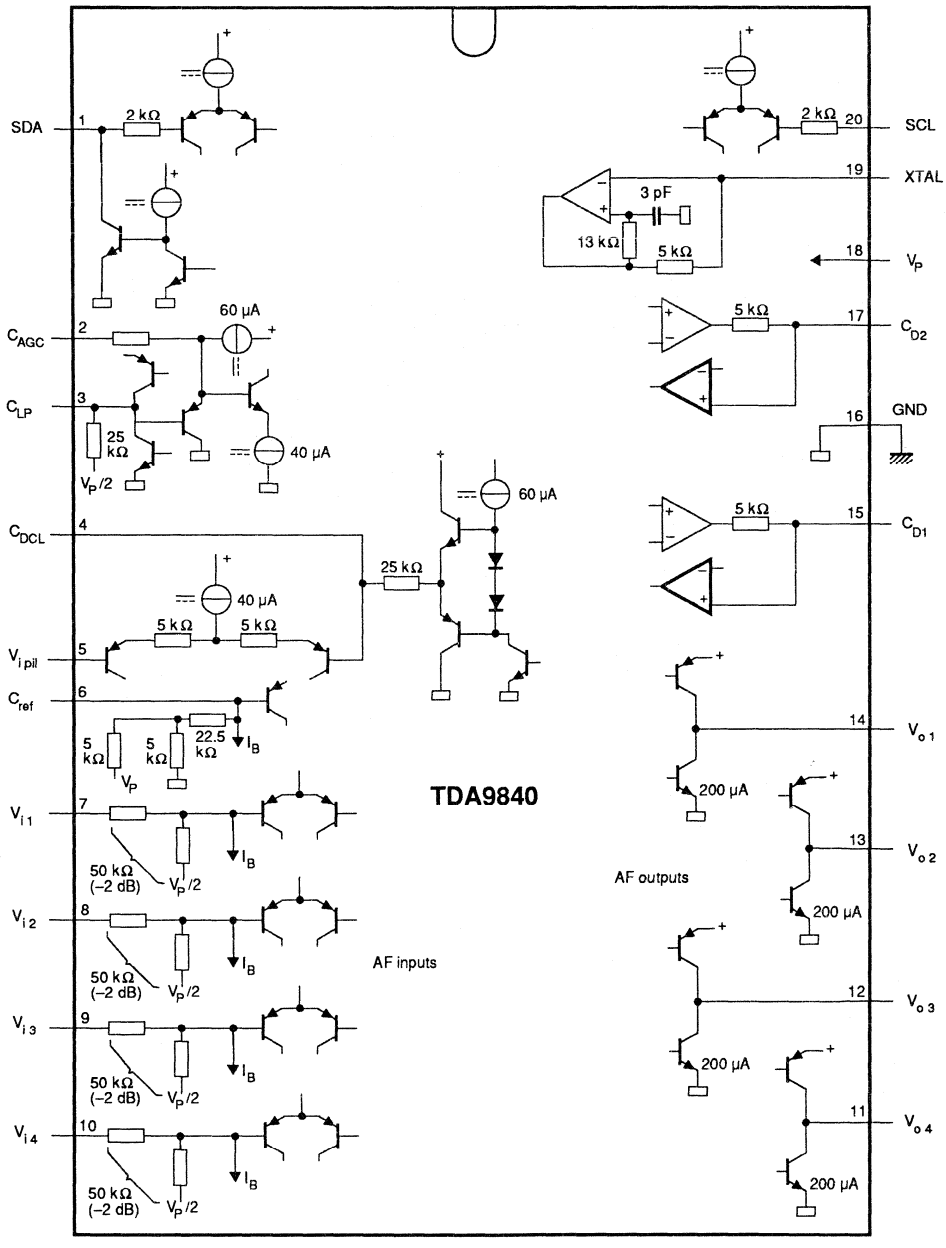


Fig.5 Internal circuit.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S = start condition
SLAVE ADDRESS = **1000 010X**
A = acknowledge, generated by the slave
SUBADDRESS = subadress byte, see Table 1
DATA = data byte, see Table 1
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read status (the circuit is slave transmitter)

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; SUBADDRESS/DATA to read the status byte (X = 1 in the address byte)

FUNCTION	SLAVE ADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
status byte	1 0 0 0 0 1 0 1	PONRES	ST	DS	0	0	0	0	0

Function of the bits:

PONRES = 0 after successful reading the status register by the microcontroller
PONRES = 1 after power-on reset or after supply breakdown

ST	DS	
0	0	= MONO sound identified
0	1	= DUAL sound identified
1	0	= STEREO sound identified
1	1	= incorrect identification

Table 2 I²C-bus; SUBADDRESS/DATA for writing (X = 0 in the address byte)

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
switching	0 0 0 0 0 0 0 0	0	SW6	SW5	SW4	SW3	SW2	SW1	SW0
without function*	0 0 0 0 0 0 0 1	0	0	0	0	0	0	0	0
level adjust	0 0 0 0 0 0 1 0	0	0	0	0	LV3	LV2	LV1	LV0
stereo adjust	0 0 0 0 0 0 1 1	0	0	ST5	ST4	ST3	ST2	ST1	ST0

Function of the bits:
SW6 to SW0 input and output AF selection, Table 3
LV3 to LV0 level adjustment, Table 4
ST5 to ST0 stereo adjustment, Table 5
* this byte is acknowledged by the TDA 9840

Table 3 Data byte to select AF inputs and AF outputs (subaddress 00)

input/output pin	mode	input signal ST/DS V_{i1} 7	V_{i2} 8	AUX V_{i3} 9	V_{i4} 10	output signal MAIN V_{o1} 14	V_{o1} 13	SCART V_{o1} 12	V_{o1} 11	DATA D7	D6	D5	D4	D3	D2	D1	D0	HEX
sound mute		-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	00
MONO	M	M	-	-	-	M	M	M	M	0	0	0	1	0	0	0	0	10
STEREO	ST	L*	R	-	-	L*	L*	L*	L*	0	0	0	1	0	0	0	0	10
	ST	L*	R	-	-	L	R	L	R	0	0	1	0	1	0	1	0	2A
DUAL	DS	A	B	-	-	A	B	A	A	0	0	0	1	0	0	1	0	12
DUAL	DS	A	B	-	-	A	B	A	B	0	0	0	1	1	0	1	0	1A
DUAL	DS	A	B	-	-	A	B	B	A	0	0	0	1	0	1	1	0	16
DUAL	DS	A	B	-	-	A	B	B	B	0	0	0	1	1	1	1	0	1E
AUX	AUX	-	-	C	D	C	D	C	D	0	1	1	1	1	0	1	0	7A

R = right
L = left
L* = (L + R)/2
A and B = STEREO/DUAL sound
C = AM sound (standard L)
D = auxiliary sound

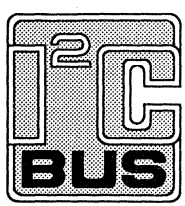
Table 4 Data byte to select level adjustment (subaddress 02)

ΔG_v (dB)	DATA D7	D6	D5	D4	D3	D2	D1	D0	HEX
+2.5	0	0	0	0	1	1	0	1	0D
+2.0	0	0	0	0	1	1	0	0	0C
+1.5	0	0	0	0	1	0	1	1	0B
+1.0	0	0	0	0	1	0	1	0	0A
+0.5	0	0	0	0	1	0	0	1	09
0	0	0	0	0	0	0	0	0	00
−0.5	0	0	0	0	0	0	0	1	01
−1.0	0	0	0	0	0	0	1	0	02
−1.5	0	0	0	0	0	0	1	1	03
−2.0	0	0	0	0	0	1	0	0	04

Table 5 Data byte to select stereo adjustment (subaddress 03)

ΔG_v (dB)	DATA D7	D6	D5	D4	D3	D2	D1	D0	HEX
+2.5	0	0	1	1	1	0	0	1	39
+2.4	0	0	1	1	1	0	0	0	38
+2.3	0	0	1	1	0	1	1	1	37
+2.2	0	0	1	1	0	1	1	0	36
+2.1	0	0	1	1	0	1	0	1	35
+2.0	0	0	1	1	0	1	0	0	34
+1.9	0	0	1	1	0	0	1	1	33
+1.8	0	0	1	1	0	0	1	0	32
+1.7	0	0	1	1	0	0	0	1	31
+1.6	0	0	1	1	0	0	0	0	30
+1.5	0	0	1	0	1	1	1	1	2F
+1.4	0	0	1	0	1	1	1	0	2E
+1.3	0	0	1	0	1	1	0	1	2D
+1.2	0	0	1	0	1	1	0	0	2C
+1.1	0	0	1	0	1	0	1	1	2B
+1.0	0	0	1	0	1	0	1	0	2A
+0.9	0	0	1	0	1	0	0	1	29
+0.8	0	0	1	0	1	0	0	0	28
+0.7	0	0	1	0	0	1	1	1	27
+0.6	0	0	1	0	0	1	1	0	26
+0.5	0	0	1	0	0	1	0	1	25
+0.4	0	0	1	0	0	1	0	0	24
+0.3	0	0	1	0	0	0	1	1	23
+0.2	0	0	1	0	0	0	1	0	22
+0.1	0	0	1	0	0	0	0	1	21
0	0	0	0	0	0	0	0	0	00

ΔG_v (dB)	DATA D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	0	0	0	0	0	00
–0.1	0	0	0	0	0	0	0	1	01
–0.2	0	0	0	0	0	0	1	0	02
–0.3	0	0	0	0	0	0	1	1	03
–0.4	0	0	0	0	0	1	0	0	04
–0.5	0	0	0	0	0	1	0	1	05
–0.6	0	0	0	0	0	1	1	0	06
–0.7	0	0	0	0	0	1	1	1	07
–0.8	0	0	0	0	1	0	0	0	08
–0.9	0	0	0	0	1	0	0	1	09
–1.0	0	0	0	0	1	0	1	0	0A
–1.1	0	0	0	0	1	0	1	1	0B
–1.2	0	0	0	0	1	1	0	0	0C
–1.3	0	0	0	0	1	1	0	1	0D
–1.4	0	0	0	0	1	1	1	0	0E
–1.5	0	0	0	0	1	1	1	1	0F
–1.6	0	0	0	1	0	0	0	0	10
–1.7	0	0	0	1	0	0	0	1	11
–1.8	0	0	0	1	0	0	1	0	12
–1.9	0	0	0	1	0	0	1	1	13
–2.0	0	0	0	1	0	1	0	0	14
–2.1	0	0	0	1	0	1	0	1	15
–2.2	0	0	0	1	0	1	1	0	16
–2.3	0	0	0	1	0	1	1	1	17
–2.4	0	0	0	1	1	0	0	0	18



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Data sheet	
status	Preliminary specification
date of issue	November 1990

TDE8712D

8-bit video digital-to-analog converter

FEATURES

- 8-bit resolution
- Conversion rate up to 50 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation (250 mW typical)
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Test and measurement
- Telecommunications
- Radar/sonar
- Image processing

DESCRIPTION

The TDE8712D is a monolithic bipolar 8-bit digital-to-analog converter (DAC) for professional video and other applications. The operating temperature range is -55 °C to +125 °C. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 50 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDE8712D	16	CERDIP	ceramic	SOT74

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
V_{OUT} – $\overline{V_{OUT}}$	full-scale analog output voltage (peak-to-peak value)	Z_L = 10 kΩ	–1.45	–1.60	–1.75	V
		Z_L = 75 Ω	–0.72	–0.80	–0.88	V
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
f_{CLK}	maximum conversion rate		50	-	-	MHz
B	–3 dB bandwidth	f_{CLK} = 50 MHz	-	150	-	MHz
P_{tot}	total power dissipation		-	250	340	mW

Notes to the Quick Reference Data

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.

2. The analog output voltages (V_{OUT} and $\overline{V_{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.

3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

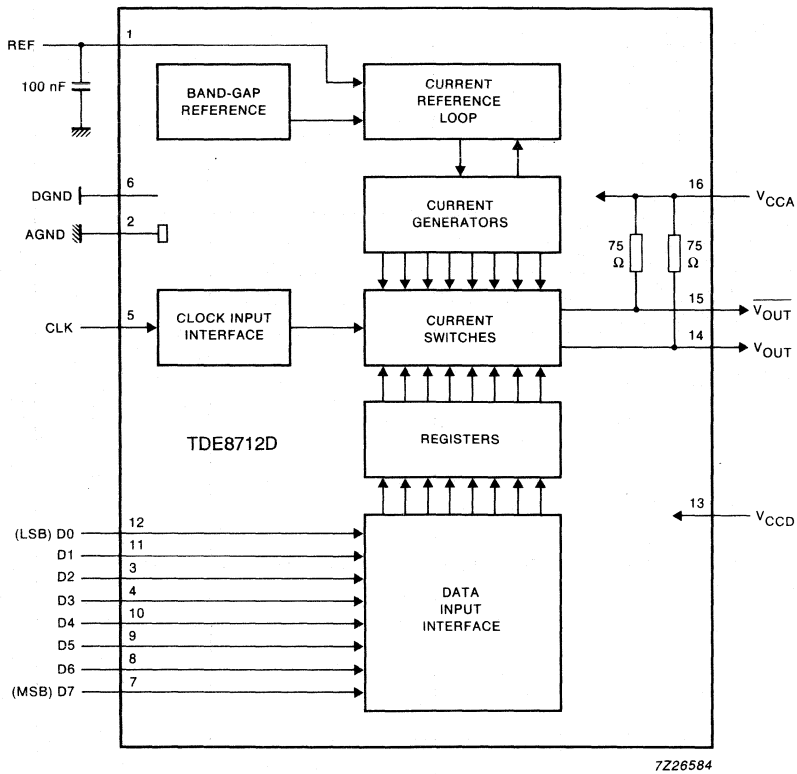


Fig.1 Block diagram.

8-bit video digital-to-analog converter TDE8712D

PIN CONFIGURATION

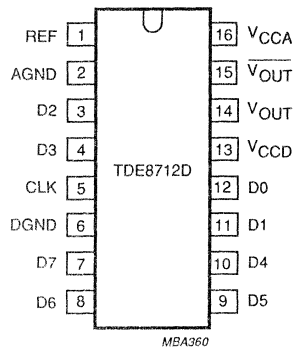


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input, bit 2
D3	4	data input, bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input, bit 7
D6	8	data input, bit 6
D5	9	data input, bit 5
D4	10	data input, bit 4
D1	11	data input, bit 1
D0	12	data input, bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$\overline{V_{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+ 7.0	V
V_{CCD}	digital supply voltage range	−0.3	+ 7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differential	−0.5	+ 0.5	V
AGND − DGND	ground voltage differential	−0.1	+ 0.1	V
V_I	input voltage range (pins 3 to 5 and 7 to 12)	−0.3	V_{CCD}	V
I_{OUT}	total output current range (pin 14)	−5	+ 26	mA
$\overline{I_{OUT}}$	total output current range (pin 15)	−5	+ 26	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−55	+125	°C
T_j	junction temperature	-	+175	°C

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT74	112	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2 = 4.75$ V to 5.25 V; $V_{CCD} = V_{13} - V_6 = 4.75$ V to 5.25 V; $V_{CCA} - V_{CCD} = -0.25$ V to +0.25 V; V_{REF} decoupled to AGND by a 100 nF capacitor; $T_{amb} = -55$ °C to +125 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
AGND – DGND	ground voltage differential		–0.1	-	0.1	V
Inputs DIGITAL INPUTS (D7 - D0) AND CLOCK INPUT (CLK)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	-	–0.3	–0.4	mA
I_{IH}	input current HIGH	$V_I = 2.7$ V	-	0.01	20	µA
f_{CLK}	maximum clock frequency		50	-	-	MHz
Outputs (note 2; referenced to V_{CCA})						
$V_{OUT} - \overline{V_{OUT}}$	full-scale analog output voltages (peak- to-peak value)	$Z_L = 10$ kΩ	–1.45	–1.61	–1.75	V
		$Z_L = 75$ Ω	–0.72	–0.80	–0.88	V
V_{offset}	analog offset output voltage	code = 0	-	–3	–25	mV
ΔV_{OUT}	full-scale analog output voltage temperature coefficient		-	-	200	µV/K
ΔV_{offset}	analog offset output voltage temperature coefficient		-	-	20	µV/k
B	–3 dB bandwidth	note 3; $f_{CLK} = 50$ MHz	-	150	-	MHz
G_d	differential gain		-	0.6	-	%
ϕd	differential phase		-	1	-	deg
Z_o	output impedance		-	75	-	Ω
Transfer function ($f_{CLK} = 50$ MHz)						
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
Switching characteristics (fCLK = 50 MHz; notes 4 and 5; see Figs 3,4 and 5)						
$t_{SU;DAT}$	data set-up time		–0.3	-	-	ns
$t_{HD;DAT}$	data hold time		2	-	-	ns
t_{PD}	propagation delay time		-	-	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	-	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	-	6.5	8.0	ns
t_d	input to 50% output delay time		-	3.0	5.0	ns
Output transients (glitches; $f_{CLK} = 50$ MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	-	-	30	ns

Notes to the characteristics

1. D0 to D7 connected to V_{CCD}, CLK connected to DGND.

2. The analog output voltages (V_{OUT} and $\overline{V_{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.

3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $\overline{V_{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data are latched at the rising-edge of the clock. The output voltage remains stable (independent of input data variations) during the high level of the clock (CLK = HIGH). During LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages, see Fig.5).

5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising-edge of the clock and still be recognized. The data hold time ($t_{HD;\ DAT}$) is the minimum period following the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising-edge of the clock and still be recognized.

6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling-edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of offset voltage)

		DAC OUTPUT VOLTAGES			
CODE	**BINARY INPUT DATA (D7 - D0)**	Z_L = 10 kΩ	Z_L = 75 Ω		
		$\overline{V_{OUT}}$ (V)	V_{OUT} (V)	$\overline{V_{OUT}}$ (V)	V_{OUT} (V)
0	000 000 00	0	–1.6	0	–0.8
1	000 000 01	–0.006	–1.594	–0.003	–0.797
.	. . . . .	.	.	.	.
128	100 000 00	–0.8	–0.8	–0.4	–0.4
.	. . . . .	.	.	.	.
254	111 111 10	–1.594	–0.006	–0.797	–0.003
255	111 111 11	–1.6	0	–0.8	0

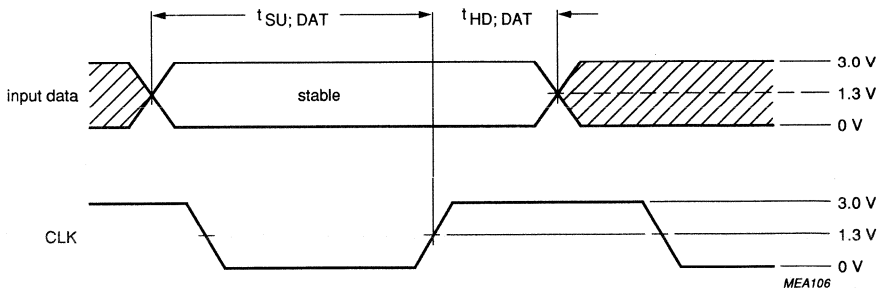


Fig.3 Data set-up and hold times.

Note to Fig.3

The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns, after the first rising-edge of the clock ($t_{SU;\ DAT}$ is negative; –0.3 ns). Data must be held at least 2 ns after the rising-edge ($t_{HD;\ DAT}$ = +2 ns).

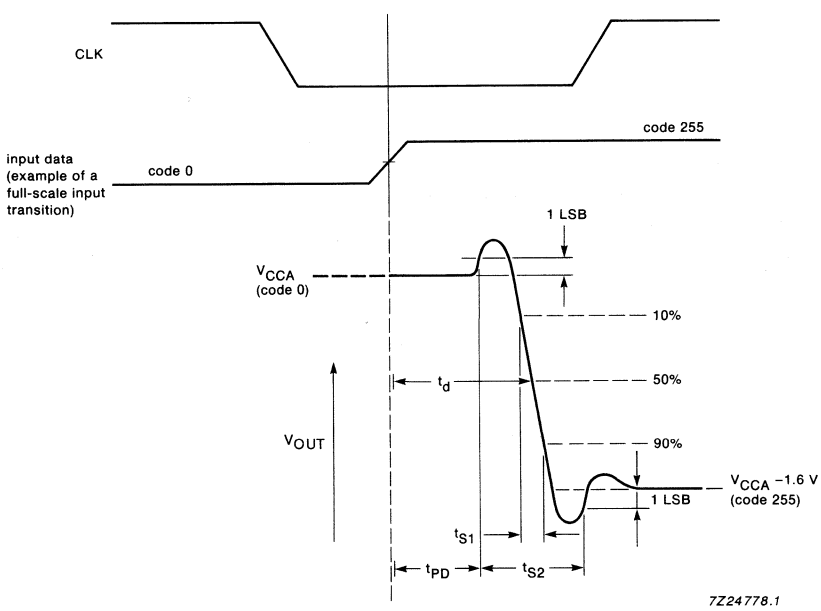


Fig.4 Switching characteristics.

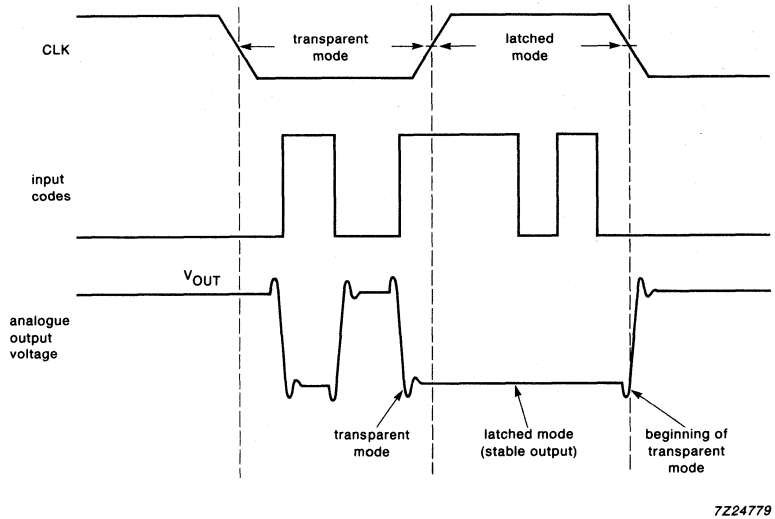


Fig.5 Latched and transparent mode.

Note to Fig.5

During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable, regardless of any changes at the input. A change of input data during the latched mode will be seen on the falling-edge of the clock (beginning of the transparent mode).

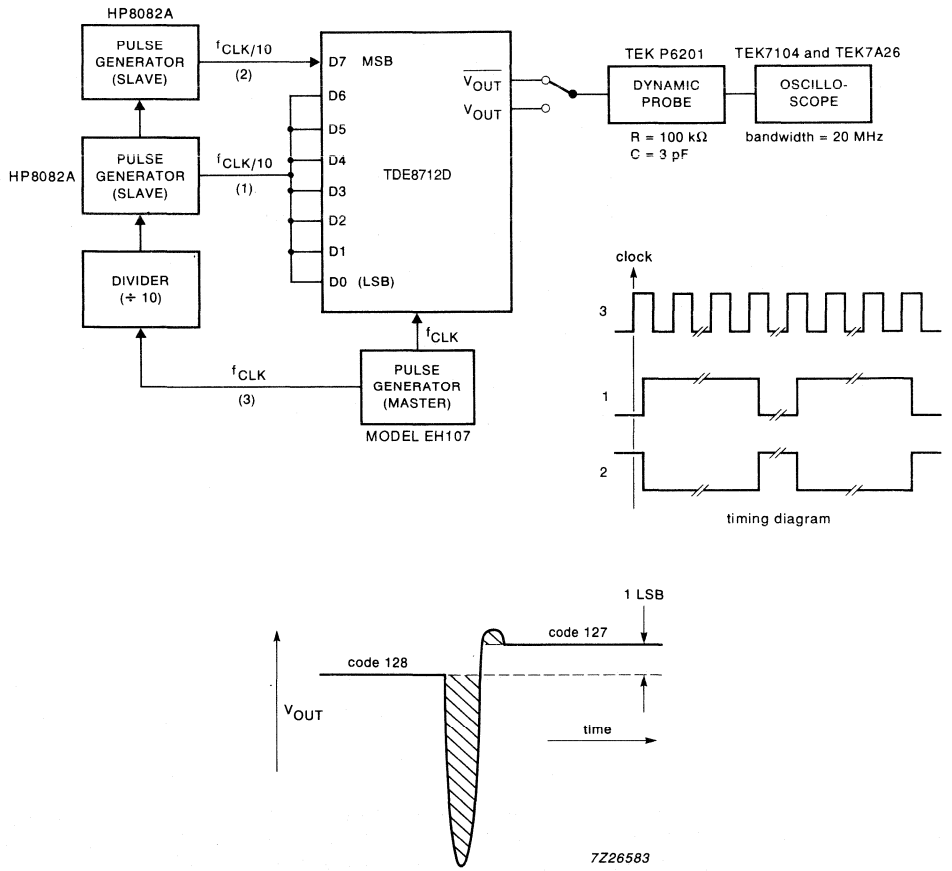


Fig.6 Glitch energy measurement.

Note to Fig.6

The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

INTERNAL PIN CONFIGURATIONS

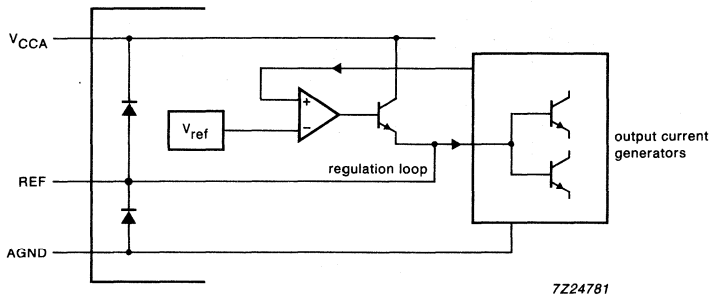


Fig.7 Reference voltage generator decoupling.

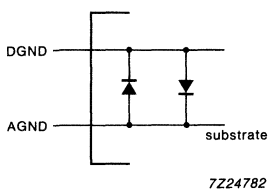


Fig.8 AGND and DGND.

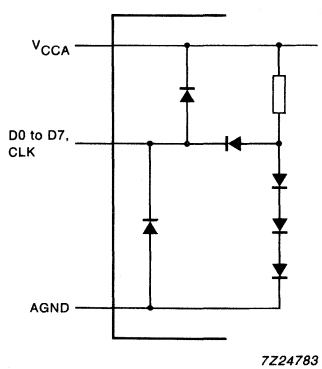


Fig.9 D7 to D0 and CLK.

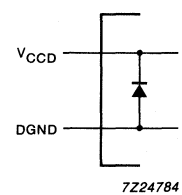


Fig.10 Digital supply.

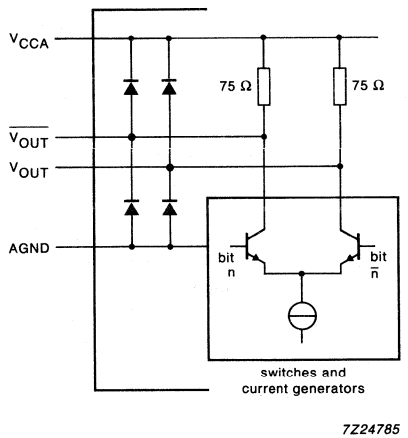


Fig.11 Analog outputs.

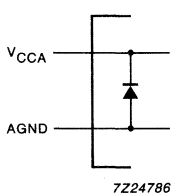


Fig.12 Analog supply.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

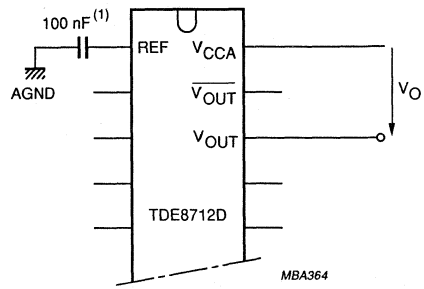


Fig.13 Analog output voltage without external load ($V_O = -\overline{V_{OUT}}$; see Table 1, Z_L = 10 kΩ).

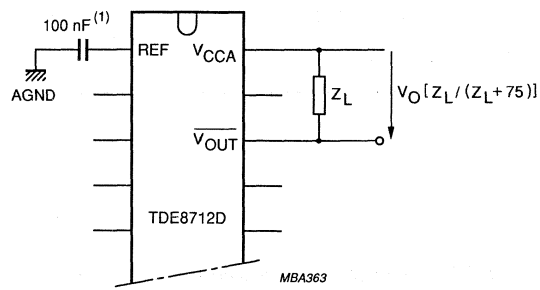


Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).

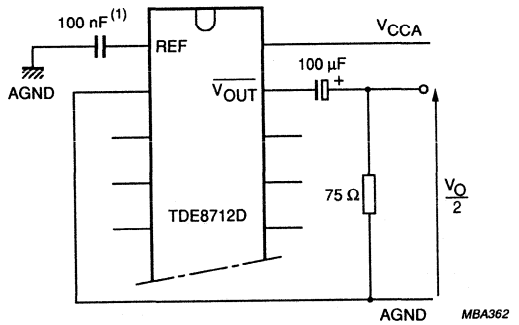


Fig.15 Analog output with AGND as reference.

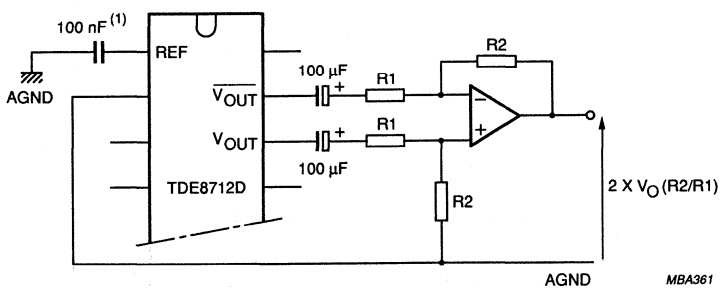


Fig.16 Differential mode (improved supply voltage ripple rejection).

Notes to Figs 13, 14, 15 and 16

1. This is a recommended value for decoupling pin 1.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	November 1990

TDE8715D

8-bit high-speed analog-to-digital converter

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 50 MHz clock frequency)
- ECL (10KH family) compatible digital inputs and outputs
- Overflow/underflow ECL output
- Low-level AC clock input signal allowed
- Power dissipation only 325 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - video data digitizing
  - radar pulse analysis
  - transient signal analysis
  - high energy physics research
  - $\Sigma\Delta$ modulators
  - medical imaging

DESCRIPTION

The TDE8715D is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. The operating temperature range is 55 °C up to 125 °C It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are 10 KH ECL compatible.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDE8715D	18	DIL	ceramic (cerdip)	SOT 133BH3

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		–4.95	–5.2	–5.45	V
V_{EED}	digital supply voltage		–4.95	–5.2	–5.45	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	see note	-	52	60	mA
ILE	DC integral linearity error		-	±0.4	±0.75	LSB
DLE	DC differential linearity error		-	±0.25	±0.5	LSB
EB	effective bits (f_i = 4.43 MHz)	f_{CLK} = 50 MHz	-	7.2	-	bits
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
T_{amb}	operating ambient temperature range		–55	-	+125	°C
P_{tot}	total power dissipation	see note	-	325	425	mW

Note to the Quick Reference Data

All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

8-bit high-speed analog-to-digital converter TDE8715D

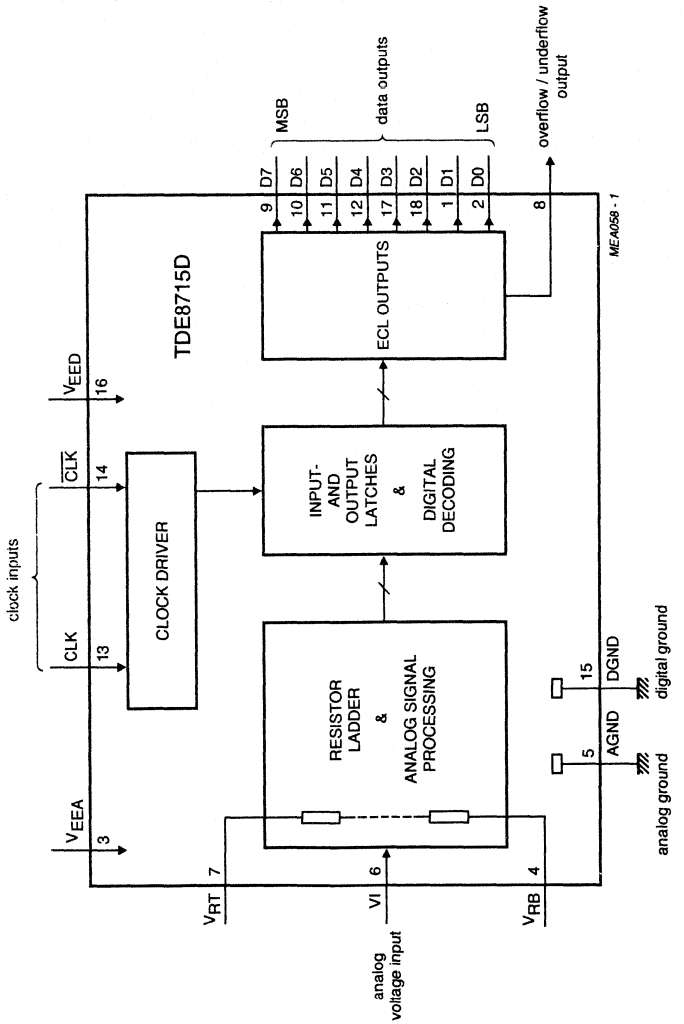


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter TDE8715D

PIN CONFIGURATION

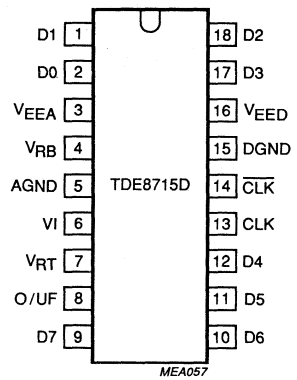


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
V_{EEA}	3	analog negative supply voltage (–5.2 V)
V_{RB}	4	reference voltage bottom input
AGND	5	analog ground
VI	6	analog voltage input
V_{RT}	7	reference voltage top input
O/UF	8	overflow/underflow data output
D7	9	data output, bit 7(MSB)
D6	10	data output, bit 6
D5	11	data output, bit 5
D4	12	data output, bit 4
CLK	13	clock input
$\overline{CLK}$	14	complementary clock input
DGND	15	digital ground
V_{EED}	16	digital negative supply voltage (–5.2 V)
D3	17	data output, bit 3
D2	18	data output, bit 2

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage range		−7	0.3	V
V_{EED}	digital supply voltage range		−7	0.3	V
V_{VI}	input voltage range		−7	0.3	V
$V_{\overline{CLK}}$/ V_{CLK}	AC input voltage for switching (peak-to-peak value)	see note	-	2.0	V
I_O	output current		−15	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		-55	+125	°C
T_j	junction temperature		-	+175	°C

Note to the Ratings

The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- When driving the CLK input with a ECL signal only (Asymmetrical drive modes) , it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT133BH3	+75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{EEA} = V_3 - V_5 = -4.95$ V to -5.45 V; $V_{EED} = V_{16} - V_{15} = -4.95$ V to -5.45 V; AGND and DGND shorted together; $T_{amb} = -55$ °C to +125 °C; unless otherwise specified (typical values measured at $V_{EEA} = -5.2$V; $V_{EED} = -5.2$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{EEA}	analog supply voltage		–4.95	–5.2	–5.45	V
V_{EED}	digital supply voltage		–4.95	–5.2	–5.45	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	note 5	-	52	60	mA
ΔV_{EE}	supply voltage difference V_{EEA} - V_{EED}		–0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	reference voltage LOW		–3.4	–3.1	–2.8	V
V_{RT}	reference voltage HIGH		–1.0	–0.6	–0.4	V
V_{ref}	differential reference voltage V_{RT}-V_{RB}		2.4	2.5	-	V
I_{ref}	reference current		-	12.6	-	mA
R_{LAD}	resistor ladder		-	200	-	Ω
R_{TLC}	temperature coefficient of the ladder		-	0.24	-	Ω/°C
V_{OB}	voltage offset bottom	note 6	-	317	-	mV
V_{OBTC}	voltage offset bottom temperature coefficient	note 6	-	0.1	-	mV/°C
V_{OT}	voltage offset top	note 6	-	174	-	mV
V_{OTTC}	voltage offset top temperature coefficient	note 6	-	–0.3	-	mV/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs CLOCK INPUT CLK (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	V_{CLK} = −1.77 V	-	−240	-	μA
I_{IH}	input current HIGH	V_{CLK} = −0.88 V	-	−14	-	μA
R_i	input resistance	f_{CLK} = 10 MHz	-	7.0	-	kΩ
		f_{CLK} = 50 MHz	-	3.5	-	kΩ
C_i	input capacitance	f_{CLK} = 10 MHz	-	1.8	-	pF
		f_{CLK} = 50 MHz	-	1.55	-	pF
CLOCK INPUT $\overline{CLK}$ (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	$V_{\overline{CLK}}$ = −1.77 V	-	−140	-	μA
I_{IH}	input current HIGH	$V_{\overline{CLK}}$ = −0.88 V	-	75	-	μA
R_i	input resistance	$f_{\overline{CLK}}$ = 10 MHz	-	9.3	-	kΩ
		$f_{\overline{CLK}}$ = 50 MHz	-	4.5	-	kΩ
C_i	input capacitance	$f_{\overline{CLK}}$ = 10 MHz	-	2.6	-	pF
		$f_{\overline{CLK}}$ = 50 MHz	-	2.4	-	pF
$V_{\underline{CLK}(p\text{-}p)}$ − $V_{CLK(p\text{-}p)}$	AC input voltage for switching (peak-to-peak value)		0.5	0.9	1.1	V
VI (analog input with V_{RB} = −3.1 V and V_{RT} = −0.6 V)						
I_{IL}	input current LOW	data output 00	-	0	-	μA
I_{IH}	input current HIGH	data output FF	-	120	-	μA
R_i	input resistance	f_i = 1 MHz	-	9.4	-	kΩ
C_i	input capacitance	f_i = 1 MHz	-	13.7	20	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs DIGITAL OUTPUTS (D7 - D0 and 0/UF) (Digital 10KH ECL outputs)						
V_{OL}	output voltage LOW	T_{amb} = 25 °C	−1.9	−1.77	−1.65	V
V_{OH}	output voltage HIGH	T_{amb} = 25 °C	−0.96	−0.88	−0.81	V
I_{OL}	output current LOW		-	1.8	4	mA
I_{OH}	output current HIGH		-	1.8	4	mA
Switching characteristics						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	−3 dB bandwidth	note 2	-	20.5	-	MHz
G_d	differential gain	note 3	-	0.3	2.0	%
ϕ_d	differential phase	note 3	-	0.4	1.5	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	0	0	0	dB
F_{even}	even harmonics (full-scale)	f_i = 4.43 MHz	-	−60	-	dB
F_{odd}	odd harmonics (full-scale)	f_i = 4.43 MHz	-	−50	-	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		-	-	±0.75	LSB
DLE	DC differential linearity error		-	-	±0.5	LSB
AILE	AC integral linearity error	note 4	-	±0.75	-	LSB
EB	effective bits f_i = 600 kHz	f_{CLK} = 20 MHz	-	7.8	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 50 MHz	-	7.2	-	bits
EB	effective bits f_i = 7 MHz	f_{CLK} = 50 MHz	-	6.9	-	bits
Timing (note 7; see Fig. 3)						
t_{dS}	sampling delay		-	1	3	ns
t_{HD}	output hold time		3	4	-	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	4	5	8	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	6	7	10	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals imposed on a DC level of –1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.

- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of –1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.

- When driving the CLK input with a ECL signal only (Asymmetrical drive modes) , it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

2. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).

3. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.

4. Full-scale sinewave (f_i = 4.43 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 50 MHz).

5. All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

6. Analog input voltages producing code 00 up to and including FF

- V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C.
- V_{OBTC} (voltage offset bottom temperature coefficient) is the dependence of V_{OB} with temperature.
- V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
- V_{OTTC} (voltage offset top temperature coefficient) is the dependence of V_{OT} with temperature.

7. Output data acquisition

- Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
- Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; V_{RB} = –3.1 V; V_{RT} = –0.6 V and V_{VI} referenced to AGND)

STEP	V_{VI}	O/UF	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
underflow	<–2.789	1	0	0	0	0	0	0	0	0
0	–2.783	0	0	0	0	0	0	0	0	0
1	–2.775	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0
255	–0.774	0	1	1	1	1	1	1	1	1
overflow	>–0.770	1	1	1	1	1	1	1	1	1

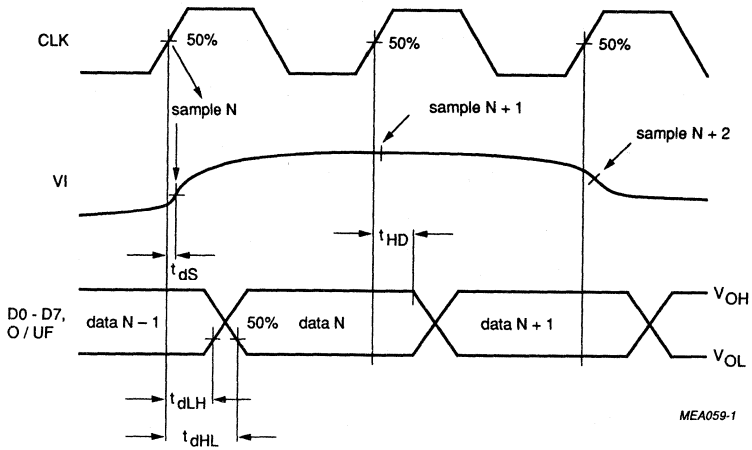


Fig.3 Timing diagram.

INTERNAL PIN CONFIGURATIONS

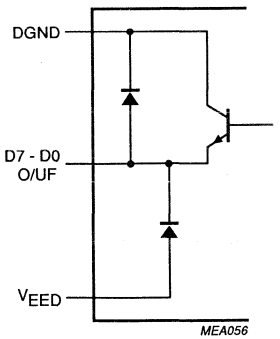


Fig.4 ECL data outputs

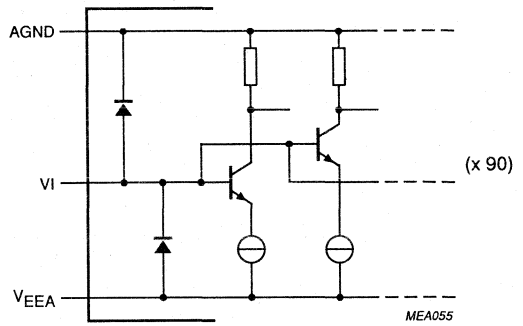


Fig.5 Analog input

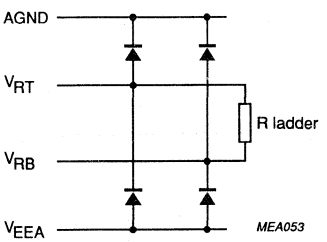


Fig.6 V_{RT} and V_{RB} inputs

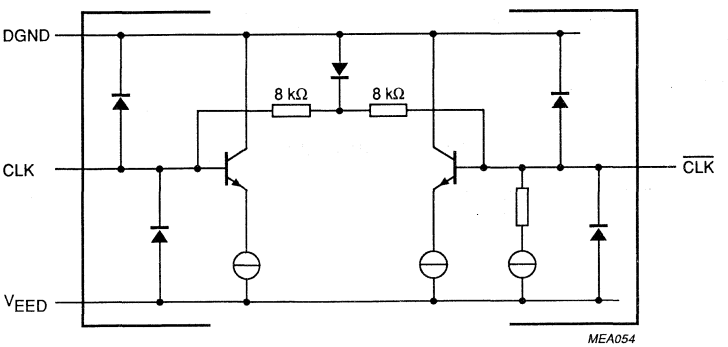


Fig.7 CLK and $\overline{CLK}$ input

APPLICATION INFORMATION

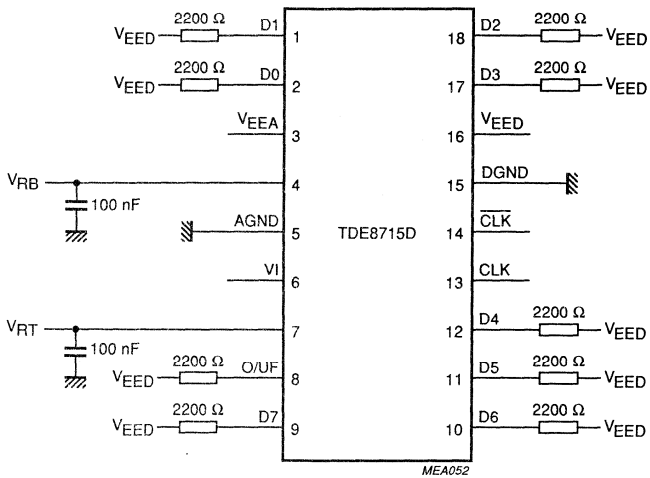


Fig.8 Application diagram.

Notes to Fig.8

- All resistors have a value of 2.2 kΩ; all capacitors have a value of 100 nF
- Analog and digital supplies should be separated and decoupled.
- The external voltage regulator must be build in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.
- $V_{EEA} = V_{EED} = -5.2$ V; $V_{RB} = -3.1$ V; $V_{RT} = -0.6$ V.

CONTROL CIRCUIT FOR SWITCHED-MODE POWER SUPPLY

GENERAL DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g. a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

It has the following features:

- Suited for frequency and duty factor regulation.
- Suited for flyback converters and forward converters.
- Wide frequency range.
- Adjustable input sensitivity.
- Adjustable minimum frequency or maximum duty factor limit.
- Adjustable overcurrent protection limit.
- Supply voltage out-of-range protection.
- Slow-start facility.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom.	14 V
Supply current	I_{CC}	max.	13 mA
Output pulse repetition frequency range	f_o	1 Hz to 100	kHz
Output current LOW	I_{OL}	max.	1 A
Operating ambient temperature range	T_{amb}	−25 to +125	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

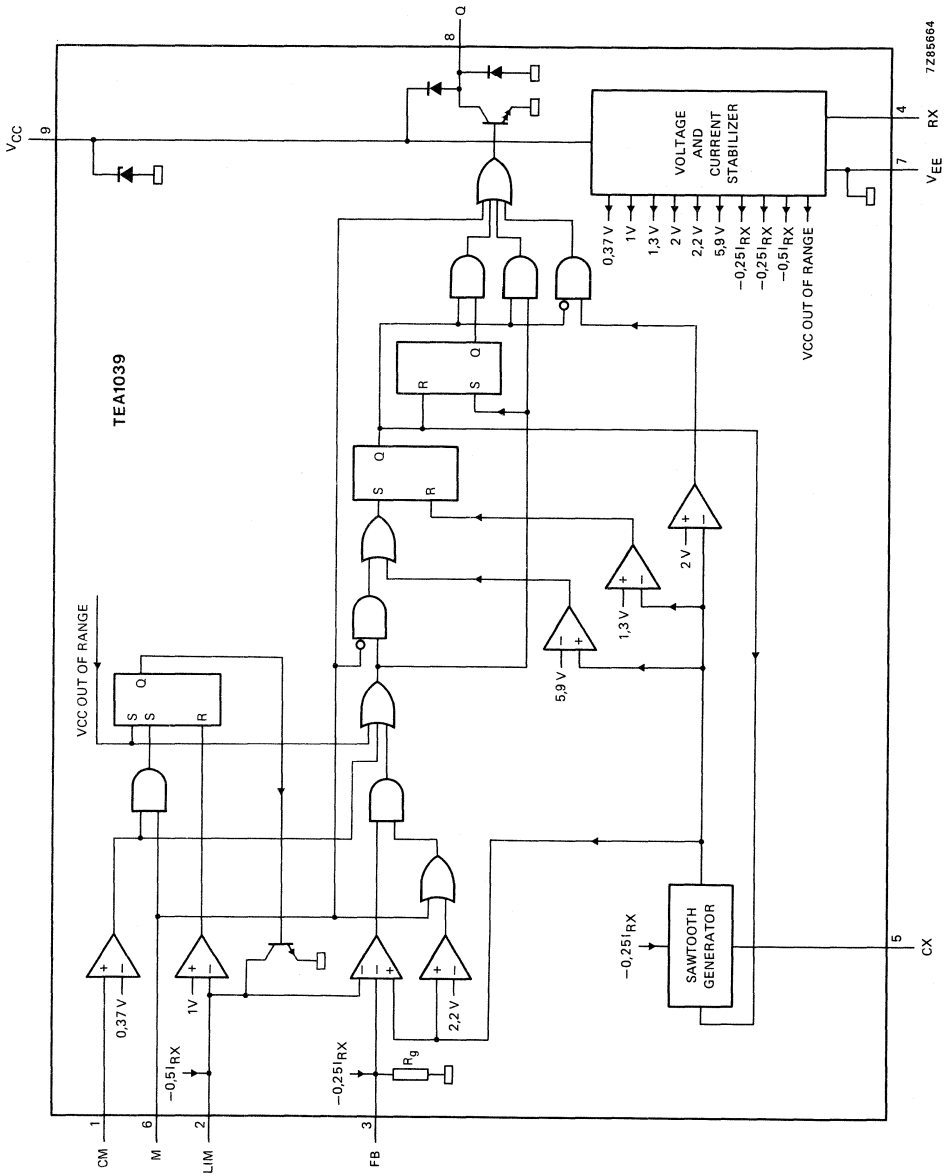


Fig. 1 Block diagram.

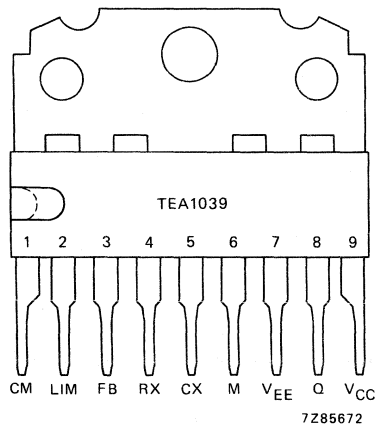


Fig. 2 Pinning diagram.

PINNING

1	CM	overcurrent protection input
2	LIM	limit setting input
3	FB	feedback input
4	RX	external resistor connection
5	CX	external capacitor connection
6	M	mode input
7	V_{EE}	common
8	Q	output
9	V_{CC}	positive supply connection

FUNCTIONAL DESCRIPTION

The TEA1039 produces pulses to drive the transistor in a switched-mode power supply. These pulses may be varied either in frequency (frequency regulation mode) or in width (duty factor regulation mode).

The usual arrangement is such that the transistor in the SMPS is ON when the output of the TEA1039 is HIGH, i.e. when the open-collector output transistor is OFF. The duty factor of the SMPS is the time that the output of the TEA1039 is HIGH divided by the pulse repetition time.

Supply V_{CC} (pin 9)

The circuit is usually supplied from the SMPS that it regulates. It may be supplied either from its primary d.c. voltage or from its output voltage. In the latter case an auxiliary starting supply is necessary.

The circuit has an internal V_{CC} out-of-range protection. In the frequency regulation mode the oscillator is stopped; in the duty factor regulation mode the duty factor is made zero. When the supply voltage returns within its range, the circuit is started with the slow-start procedure.

When the circuit is supplied from the SMPS itself, the out-of-range protection also provides an effective protection against any interruption in the feedback loop.

Mode input M (pin 6)

The circuit works in the frequency regulation mode when the mode input M is connected to ground (V_{EE}, pin 7). In this mode the circuit produces output pulses of a constant width but with a variable pulse repetition time.

The circuit works in the duty factor regulation mode when the mode input M is left open. In this mode the circuit produces output pulses with a variable width but with a constant pulse repetition time.

FUNCTIONAL DESCRIPTION (continued)

Oscillator resistor and capacitor connections RX and CX (pins 4 and 5)

The output pulse repetition frequency is set by an oscillator whose frequency is determined by an external capacitor C5 connected between the CX connection (pin 5) and ground (V_{EE}, pin 7), and an external resistor R_4 connected between the RX connection (pin 4) and ground. The capacitor C5 is charged by an internal current source, whose current level is determined by the resistor R4. In the frequency regulation mode these two external components determine the minimum frequency; in the duty factor regulation mode they determine the working frequency (see Fig. 4). The output pulse repetition frequency varies less than 1% with the supply voltage over the supply voltage range.

In the frequency regulation mode the output is LOW from the start of the cycle until the voltage on the capacitor reaches 2 V. The capacitor is further charged until its voltage reaches the voltage on either the feedback input FB or the limit setting input LIM, provided it has exceeded 2,2 V. As soon as the capacitor voltage reaches 5,9 V the capacitor is discharged rapidly to 1,3 V and a new cycle is initiated (see Figs 5 and 6).

For voltages on the FB and LIM inputs lower than 2,2 V, the capacitor is charged until this voltage is reached; this sets an internal maximum frequency limit.

In the duty factor regulation mode the capacitor is charged from 1,3 V to 5,9 V and discharged again at a constant rate. The output is HIGH until the voltage on the capacitor exceeds the voltage on the feedback input FB; it becomes HIGH again after discharge of the capacitor (see Figs 7 and 8). An internal maximum limit is set to the duty factor of the SMPS by the discharging time of the capacitor.

Feedback input FB (pin 3)

The feedback input compares the input current with an internal current source whose current level is set by the external resistor R4. In the frequency regulation mode, the higher the voltage on the FB input, the longer the external capacitor C5 is charged, and the lower the frequency will be. In the duty factor regulation mode external capacitor C5 is charged and discharged at a constant rate, the voltage on the FB input now determines the moment that the output will become LOW. The higher the voltage on the FB input, the longer the output remains HIGH, and the higher the duty factor of the SMPS.

Limit setting input LIM (pin 2)

In the frequency regulation mode this input sets the minimum frequency, in the duty factor regulation mode it sets the maximum duty factor of the SMPS. The limit is set by an external resistor R2 connected from the LIM input to ground (pin 7) and by an internal current source, whose current level is determined by external resistor R4.

A slow-start procedure is obtained by connecting a capacitor between the LIM input and ground. In the frequency regulation mode the frequency slowly decreases from f_{max} to the working frequency. In the duty factor regulation mode the duty factor slowly increases from zero to the working duty factor.

Overcurrent protection input CM (pin 1)

A voltage on the CM input exceeding 0,37 V causes an immediate termination of the output pulse. In the duty factor regulation mode the circuit starts again with the slow-start procedure.

Output Q (pin 8)

The output is an open-collector n-p-n transistor, only capable of sinking current. It requires an external resistor to drive an n-p-n transistor in the SMPS (see Figs 9 and 10).

The output is protected by two diodes, one to ground and one to the supply.

At high output currents the dissipation in the output transistor may necessitate a heatsink. See the power derating curve (Fig. 3).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, voltage source	V_{CC}	−0,3 to +20	V
Supply current range, current source	I_{CC}	−30 to +30	mA
Input voltage range, all inputs	V_I	−0,3 to +6	V
Input current range, all inputs	I_I	−5 to +5	mA
Output voltage range	V_{8-7}	−0,3 to +20	V
Output current range			
output transistor ON	I_8	0 to 1	A
output transistor OFF	I_8	−100 to + 50	mA
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range (see Fig. 3)	T_{amb}	−25 to +125	°C
Power dissipation (see Fig. 3)	P_{tot}	max. 2	W

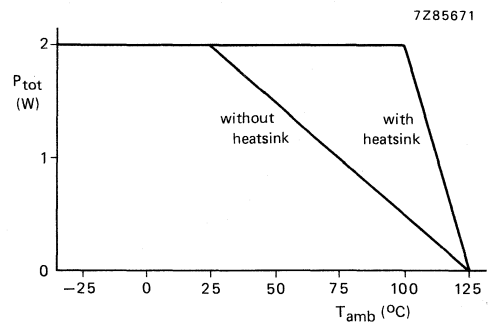


Fig. 3 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 9)					
Supply voltage, operating	V_{CC}	11	14	20	V
Supply current					
at V_{CC} = 11 V	I_{CC}	–	7,5	11	mA
at V_{CC} = 20 V	I_{CC}	–	9	12	mA
variation with temperature	$\frac{\Delta I_{CC}/I_{CC}}{\Delta T}$	–	–0,3	–	%/K
Supply voltage, internally limited					
at I_{CC} = 30 mA	V_{CC}	23,5	–	28,5	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	18	–	mV/K
Low supply threshold voltage	V_{CCmin}	9	10	11	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	–5	–	mV/K
High supply threshold voltage	V_{CCmax}	21	23	24,6	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	10	–	mV/K
Feedback input FB (pin 3)					
Input voltage for duty factor = 0; M input open	V_{3-7}	0	–	0,3	V
Internal reference current	$-I_{FB}$	–	0,5 I_{RX}	–	mA
Internal resistor R_g	R_g	–	130	–	kΩ
Limit setting input LIM (pin 2)					
Threshold voltage	V_{2-7}	–	1	–	V
Internal reference current	$-I_{LIM}$	–	0,25 I_{RX}	–	mA
Overcurrent protection input CM (pin 1)					
Threshold voltage	V_{1-7}	300	370	420	mV
variation with temperature	$\Delta V_{1-7}/\Delta T$	–	0,2	–	mV/K
Propagation delay, CM input to output	t_{PHL}	–	500	–	ns

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.	unit
Oscillator connections RX and CX (pins 4 and 5)					
Voltage at RX connection at $-I_4$ = 0,15 to 1 mA	V_{4-7}	6,2	7,2	8,1	V
variation with temperature	$\Delta V_{4-7}/\Delta T$	–	2,1	–	mV/K
Lower sawtooth level	V_{LS}	–	1,3	–	V
Threshold voltage for output H to L transition in F mode	V_{FT}	–	2	–	V
Threshold voltage for maximum frequency in F mode	V_{FM}	–	2,2	–	V
Higher sawtooth level	V_{HS}	–	5,9	–	V
Internal capacitor charging current, CX connection	$-I_{CX}$	–	0,25 I_{RX}	–	mA
Oscillator frequency (output pulse repetition frequency)	f_o	1	–	10^5	Hz
Minimum frequency in F mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Maximum frequency in F mode, initial deviation	$\Delta f/f$	−20	–	+20	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	−0,16	–	%/K
Output LOW time in F mode, initial deviation	$\Delta t/t$	−25	–	+25	%
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Pulse repetition frequency in D mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Minimum output LOW time in D mode at C_5 = 3,6 nF	t_{OLmin}	–	1	–	μs
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Output Q (pin 8)					
Output voltage LOW at I_8 = 100 mA	V_{8-7}	–	0,8	1,2	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	1,5	–	mV/K
Output voltage LOW at I_8 = 1 A	V_{8-7}	–	1,7	2,1	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	−1,4	–	mV/K

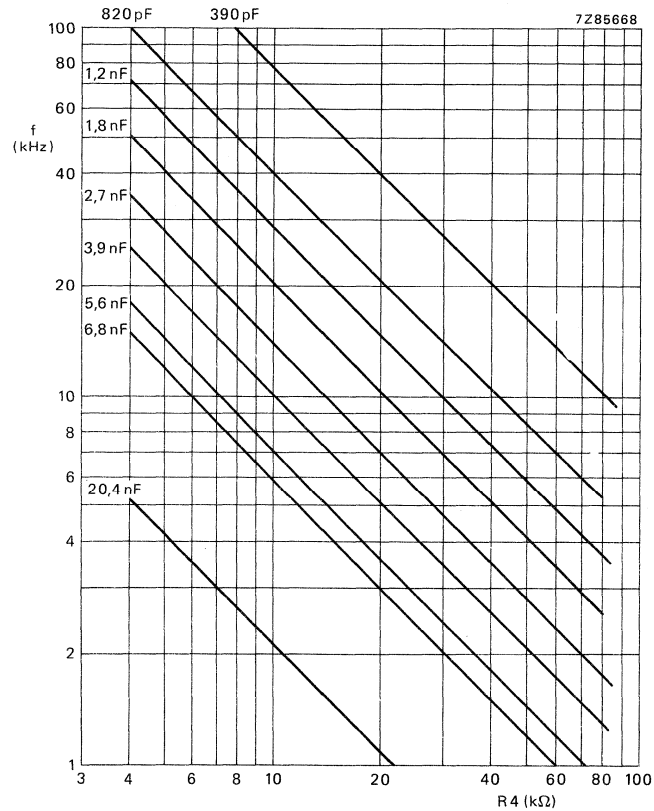


Fig. 4 Minimum pulse repetition frequency in the frequency regulation mode, and working pulse repetition frequency in the duty factor regulation mode, as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

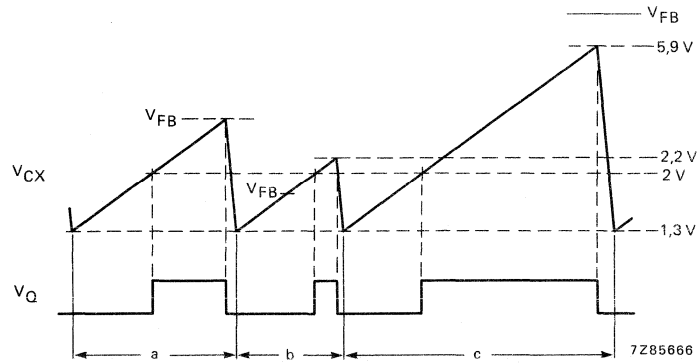


Fig. 5 Timing diagram for the frequency regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for three combinations of input signals. *a:* The voltages on inputs FB or LIM are between 2,2 V and 5,9 V. The circuit is in its normal regulation mode. *b:* The voltage on input FB or input LIM is lower than 2,2 V. The circuit works at its maximum frequency. *c:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit works at its minimum frequency.

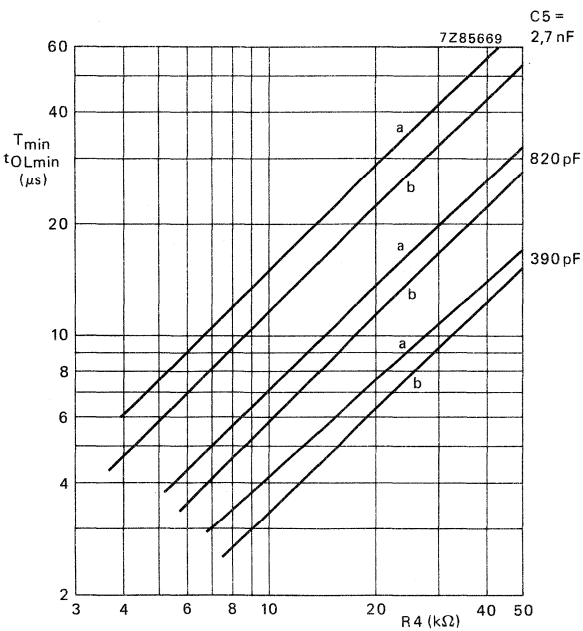


Fig. 6 Minimum output pulse repetition time T_{min} (curves a) and minimum output LOW time t_{OLmin} (curves b) in the frequency regulation mode as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

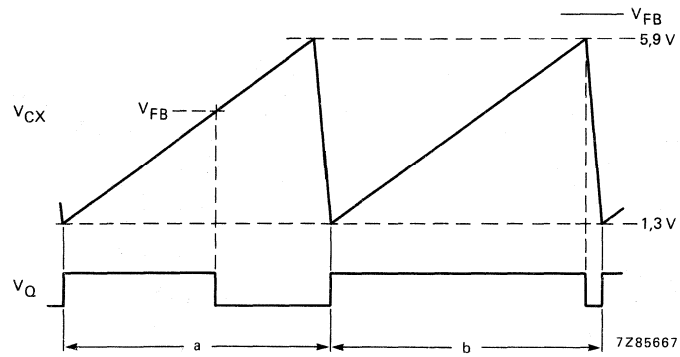


Fig. 7 Timing diagram for the duty factor regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for two combinations of input signals. *a:* The voltages on inputs FB or LIM are below 5,9 V. The circuit is in its normal regulation range. *b:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit produces its minimum output LOW time, giving the maximum duty factor of the SMPS.

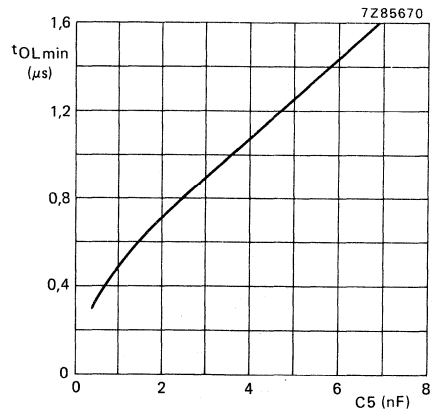


Fig. 8 Minimum output LOW time t_{OLmin} in the duty factor regulation mode as a function of external capacitor C5 connected between CX and ground. In this mode the minimum output LOW time is independent of R4 for values of R4 between 4 kΩ and 80 kΩ.

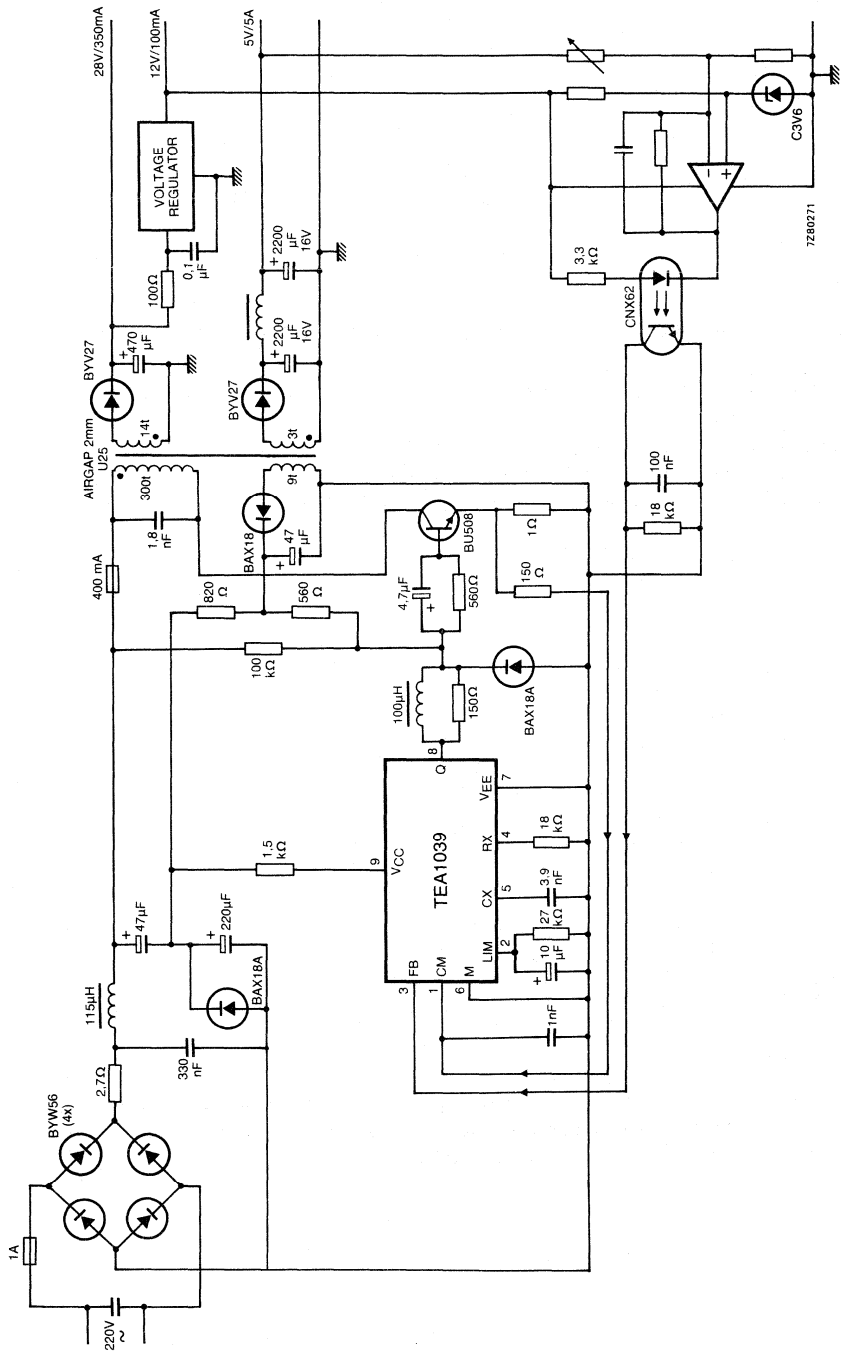


Fig. 9 Typical application of the TEA1039 in a variable-frequency flyback converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

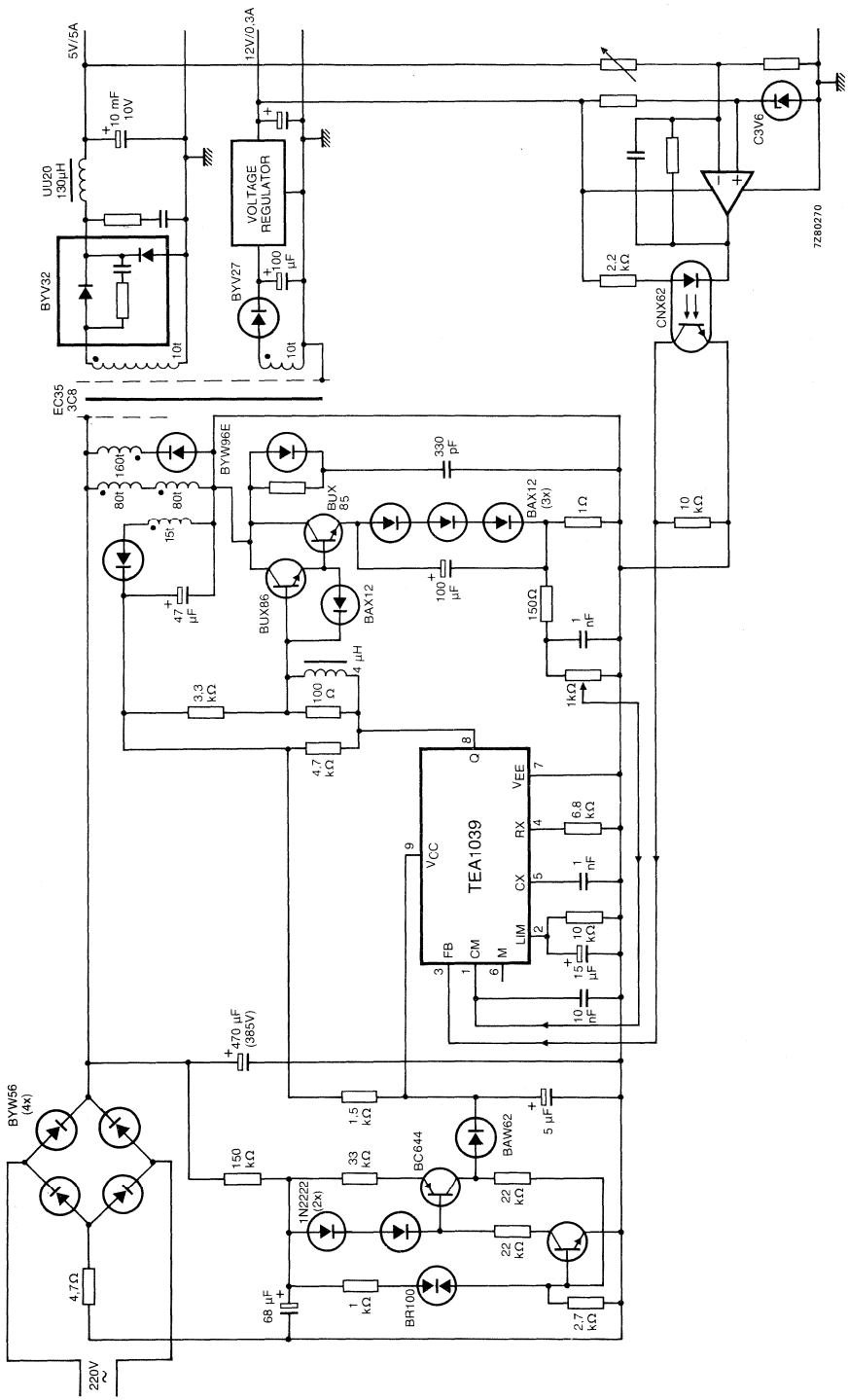


Fig. 10 Typical application of the TEA1039 in a fixed-frequency, variable duty factor forward converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

PLL STEREO DECODER (BTSC SYSTEM)

GENERAL DESCRIPTION

The TEA5582, a 20-pin integrated phase-locked loop (PLL) stereo decoder, is designed primarily for low cost stereo decoding in a low- to medium-line TV. The MUX input (pin 1) is a low impedance current input, the gain of the input amplifier is therefore determined by the external resistor R1 (see Fig.5). All characteristics are measured with R1 = 47 kΩ. The de-emphasis of (L, R) and (L−R) can be chosen by means of external capacitors and resistors. The supply voltage range of the device is from 7 V to 16 V.

Features

- Wide supply voltage range
- Automatic mono/stereo switching (pilot presence detector)
- LED driver for stereo indicator
- Smooth mono/stereo control
- Matrix and two amplifiers for left and right output signals
- A source selector to switch between the MUX signal and an external signal
- Mute circuit for 60 dB muting of the output level
- External de-emphasis control of (L, R) and (L−R)
- 6 dB fixed attenuation of (L−R) with respect to (L+R) prior to matrix
- All pins are protected against Electrostatic Discharge (ESD)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_S	7.0	8.5	16	V
Total current consumption	without LED driver	I_{tot}	–	19	25	mA
Decoder						
Overall gain	mono; R1 = 47 kΩ	$G_o(V_o/V_i)$	4	5.8	7	dB
AF output voltage (RMS value)		$V_{14} = V_{15}$	–	245	–	mV
Total harmonic distortion	V_o = 600 mV	THD	–	0.3	–	%
Output channel unbalance		$\lvert V_{14}/V_{15}\rvert$	–	0.1	–	dB
Channel separation	L = 1; R = 0	α	24	28	–	dB
Source selector						
Suppression of MUX signal	$V_6 \geqslant 2$ V	α	80	90	–	dB
Suppression of external signal	$V_6 \leqslant 0.8$ V	α	56	60	–	dB
Output amplifiers						
Gain output amplifier						
MUX signal		G_v	6.7	7.2	7.7	dB
external signal		G_v	−0.5	0	+0.5	dB
AF output voltage (RMS value)		$V_{11} = V_{10}$	460	560	640	mV
Mute suppression	$V_7 \leqslant 0.8$ V					
MUX signal		α	56	60	–	dB
external signal		α	56	60	–	dB

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

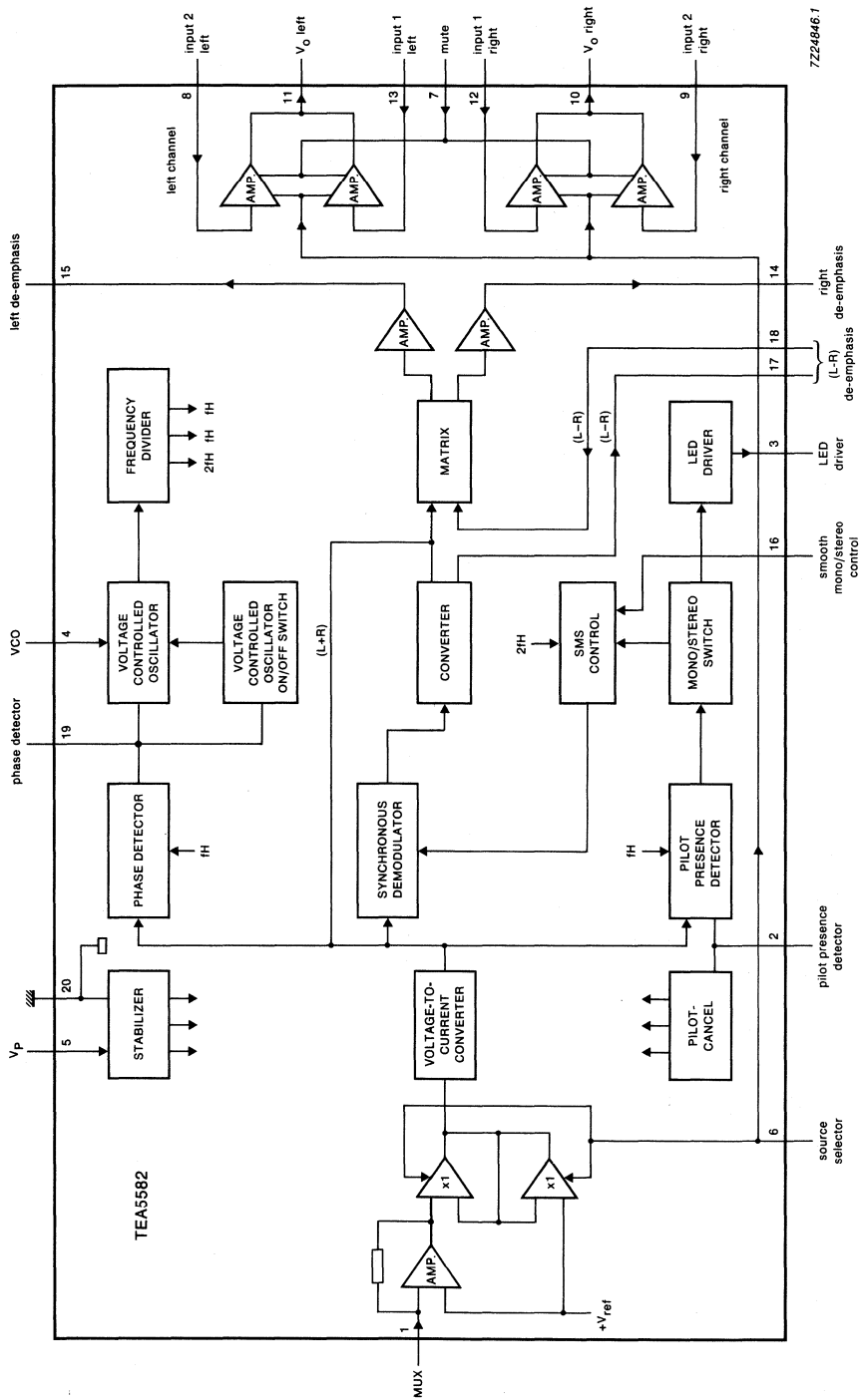


Fig.1 Block diagram.

PINNING

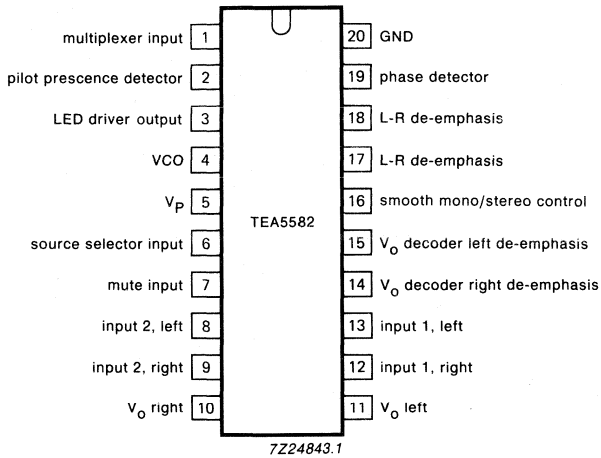


Fig.2 Pinning diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 5)	V_P	–	18	V
LED-driver current (peak value)	I_3	–	75	mA
Total power dissipation	P_{tot}	see Fig.3		
Storage temperature range	T_{stg}	−65	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C
Electrostatic handling *	V_{es}	−2	+2	kV

* ESD withstand voltage is defined by MIL STD 883C (C = 100 pF; R = 1.5 kΩ).

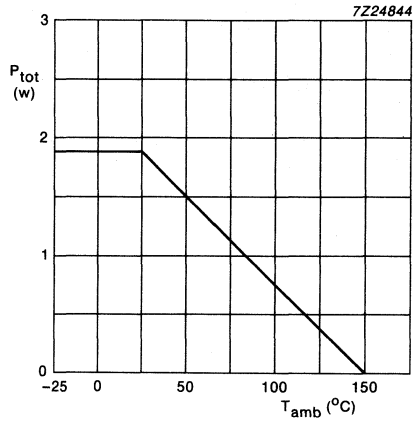


Fig.3 Power derating curve.

DC CHARACTERISTICS

All voltages are with respect to ground (pin 20); all currents are positive into the device; all parameters are measured in the test set-up (see Fig.5) at a nominal supply voltage of V_S = 8.5 V; T_{amb} = 25 °C unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_S	7.0	8.5	16	V
Total current consumption	without LED driver	I_{tot}	–	19	25	mA
Power dissipation		P_{tot}	–	160	–	mW
Voltage						
pin 1		V_1	–	2.1	–	V
pins 8, 9, 10, 11, 12 and 13		V_8-V_{13}	–	4.2	–	V
DC output current						
pins 14 and 15		$-I_{14}$, I_{15}	1.1	1.4	1.8	mA
LED-driver current						
pin 3		I_3	–	–	20	mA
Switch "VCO-OFF" voltage	I_{19} = 50 μA	V_{19}	–	2	–	V
Switch "VCO-OFF" current		I_{19}	50	–	–	μA

AC CHARACTERISTICS

Measured in the test circuit of Fig.5; V_S = 8.5 V; T_{amb} = 25 °C.
AC conditions: (1) input signal (V_i) of 815 mV p-p for L = 1, R = 1 (mono) f_m = 1 kHz (= 80% modulation). (2) MUX input signal (V_i) of 1.2 V p-p for L = 1, R = 0 and no DBX; f_m = 1 kHz (stereo) and V_{pilot} = 200 mV p-p. (3) S1 open, unless specified (without L–R filter); voltage controlled oscillator (VCO) adjusted to 188.8 kHz at V_i = 0 V; values are measured with an external IF roll-off network (–2 dB at 31.5 kHz = $2f_H$) at the input (dashed components RS and CS in Fig.5).
All the above conditions apply unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Overall performance (V_i to V_o)						
Input current (RMS value)		$I_{I(rms)}$	–	–	12	μA
Overall gain	mono; R1 = 47 kΩ	G_o (V_o/V_i)	4	5.8	7	dB
AF output voltage (mono) (RMS value)		$V_{11} = V_{10}$	460	560	640	mV
AF output voltage (mono) (RMS value)		$V_{15} = V_{14}$	–	245	–	mV
Total harmonic distortion	note 1	THD	–	0.3	0.5	%
Output voltage	THD = 1%	$V_{11} = V_{10}$	–	800	–	mV
Output channel unbalance		$\lvert V_{11}/V_{10} \rvert$	–	0.1	1	dB
Channel separation	L = 1; R = 0	α	24	28	–	dB
Signal-to-noise ratio	bandwidth 20 Hz to 16 kHz	S/N	–	76	–	dB
	bandwidth IEC 79 (curve Din A)	S/N	–	82	–	dB
Pilot presence detector	note 2					
Switching to:						
stereo		V_{pilot}	–	40	60	mV
mono		V_{pilot}	15	30	–	mV
hysteresis		ΔV_{pilot}	–	2.5	–	dB
Smooth mono/stereo control (pin 16)	see Fig.4					
Channel separation (α)						
Full stereo	$V_{16} \geqslant 1.25$ V	α	24	28	–	dB
Smooth operation	V_{16} = typ. 1 V	α	–	10	–	dB
Full mono	$V_{16} \leqslant 0.75$ V	α	–	–	1	dB
Attenuation (L–R)			–	6	–	dB

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Carrier and harmonic suppression at the output	note 3					
Pilot signal suppression	f_{pilot} = 15.734 kHz (1 fH)	αfH	32	36	–	dB
Subcarrier suppression f = 2 fH		α2fH	–	60	–	dB
VCO suppression f = 12fH		α12fH	–	75	–	dB
SAP signal suppression (Second Audio Programme) f = 5fH		α5fH	–	60	–	dB
Intermodulation suppression	note 4					
f_m = 8.367 kHz	spurious signal f_s = 1 kHz	α_2	–	60	–	dB
f_m = 10.823 kHz	spurious signal f_s = 1 kHz	α_3	–	70	–	dB
Ripple rejection	f = 120 Hz; V_{ripple} = 100 mV; mono	RR_{120}	–	50	–	dB
VCO						
R adjust (R5)	f_{osc} = 188.808 kHz R7 = 10 kΩ 5% C6 = 820 pF 1%	R_{adj}	0	–	8	kΩ
Capture range	deviation from f_{osc} centre frequency; V_{pilot}=200 mV p-p	$\Delta f/f$	–	4.5	–	%
Temperature coefficient	uncompensated	TC	–	250 x 10^{-6}	–	K^{-1}
Output amplifiers						
Gain MUX signal		G_v	6.7	7.2	7.7	dB
external signal		G_v	–0.5	0	+0.5	dB
Input impedance		Z_i	–	50	–	kΩ
Output impedance		Z_o	–	10	–	Ω
External load impedance		Z_1	10	–	–	kΩ
External load capacitance		Z_1	–	–	1.5	nF
Mute suppression	$V_7 \leqslant 0.8$ V					
MUX signal		α	56	60	–	dB
external signal		α	56	60	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
DC offset voltage at outputs	mute OFF-to-ON	ΔV	–	10	50	mV
	mute ON-to-OFF	ΔV	–	10	50	mV
Source selector (pin 6)						
Suppression of MUX signal	$V_6 \geqslant 2$ V	α	80	90	–	dB
Suppression of external signal	$V_6 \leqslant 0.8$ V	α	56	60	–	dB
Switching level	MUX selected					
voltage		V_{IL}	–	–	0.8	V
current	$V_I = 0.8$ V	I_{IL}	–	10	25	μA
Switching level	external selected					
voltage		V_{IH}	2	–	V_P	V
current	$V_I = V_P$	I_{IH}	–	0.1	1	μA
Muting circuit (pin 7)						
Input voltage	mute ON	V_{IL}	–	–	0.8	V
	mute OFF	V_{IH}	2	–	V_P	V
Input current	mute ON; $V_{IL} = 0.8$ V	$-I_{IL}$	–	10	25	μA
	mute OFF; $V_{IH} = V_P$	I_{IL}	–	0.1	1	μA

DEVELOPMENT DATA

Notes to the characteristics

1. Guaranteed for mono, mono + pilot and stereo.
2. Adjustable.
3. S1 closed; reference: AF output voltage f = 1 kHz (mono).
4. Intermodulation suppression (Beat-Frequency Components (BFC)):

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (2 \times 8.367\text{ kHz}) - fH$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (3 \times 10.823\text{ kHz}) - 2fH$$

measured with 100% modulated input signal: L = R; pilot signal = 200 mV p-p; f_m = 8.367 or 10.823 kHz.

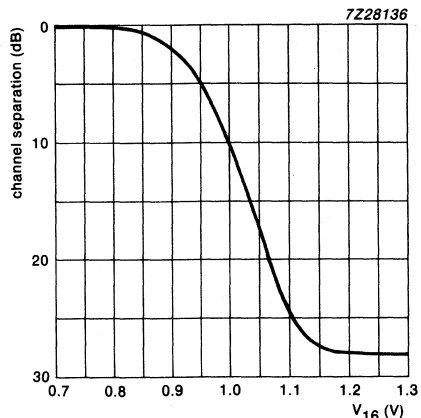


Fig.4 Smooth mono/stereo control.

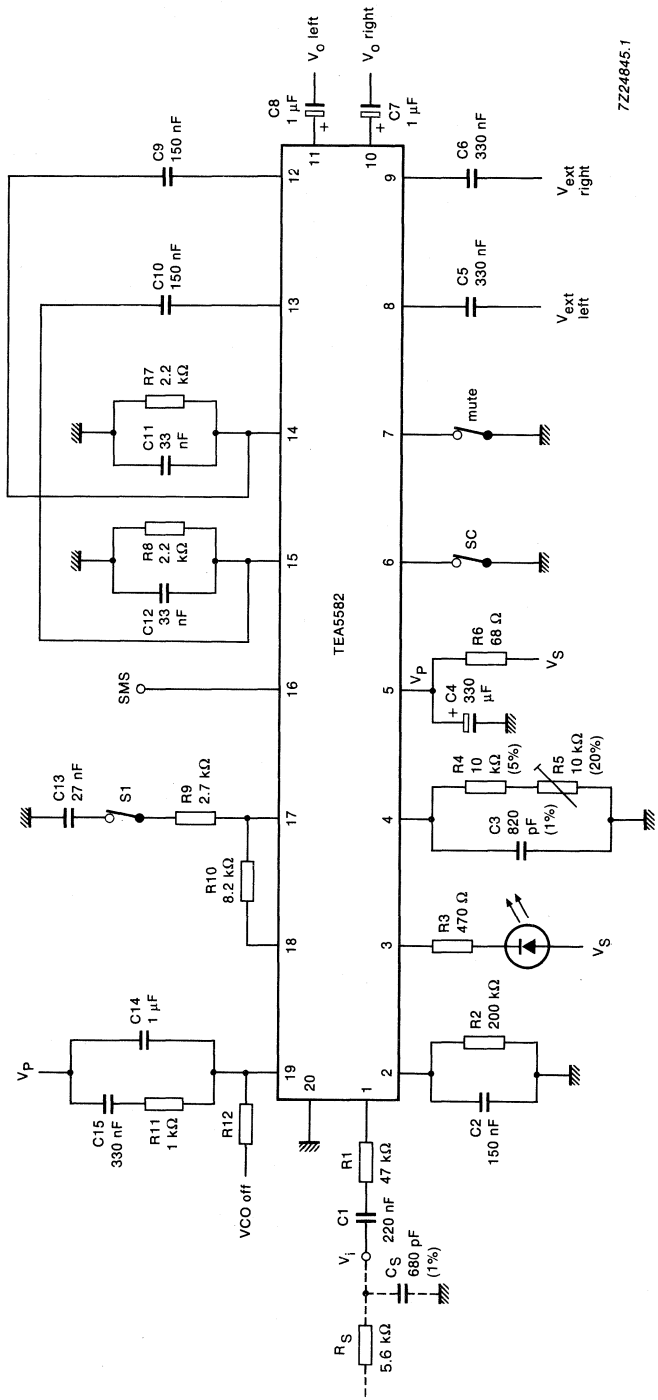


Fig.5 Test and application circuit.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	September 1990

TEA7650H

Video signal processor for CD-video/laser vision

FEATURES

- Modulation Transfer Function correction (MTF) at signal input for both standards
- HF drop out detector
- Data slicer, data output for program information (IEC standards)
- Separation of signals for Electronic Time Base Correction (ETBC)
- Noise reduction with chrominance trap, noise level adjust point
- Dynamic picture insertion and 6 dB video attenuation of main picture
- Bandgap reference voltage output, suitable for CCD delay line

GENERAL DESCRIPTION

Bipolar IC for video signal processing used in CD-Video/LaserVision players.

Standard PAL respectively NTSC output signal (CVBS).

MTF amplifier.

FM-demodulator followed by de-emphasis stage.

PAL/NTSC switch for switching the MTF and de-emphasis.

Drop out detector with drop out switch, also externally switchable.

+5 volt supply, only 325 mW total power dissipation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 12, 30, 47)	-	5	-	V
I_P	total supply current	-	-	65	mA
$V_{i\ (p-p)}$	FM input signal at pin 7 (peak-to-peak value)	50	-	300	mV
$V_{o\ (p-p)}$	CVBS output signal for CCDs (peak sync – peak white, pin 29)	-	850	-	mV
V_{29}	black level voltage (pin 29)	-	1.85	-	V
$V_{i\ (p-p)}$	delayed CVBS input signal for drop out path at pin 27 (peak-to-peak value)	-	700	-	mV
$V_{i\ (p-p)}$	delayed CVBS input signal at pin 31 from ETBC path (peak-to-peak value)	-	600	-	mV
$V_{o\ (p-p)}$	main CVBS output signal at pin 42 (peak-to-peak value)	-	1	-	V
V_{42}	black level voltage (pin 42)	-	2.2	-	V
$V_{o\ (p-p)}$	chrominance output signals at pins 44, 48 (peak-to-peak value)				
	PAL (burst)	-	760	-	mV
	NTSC (burst)	-	725	-	mV
V_{ref}	reference output voltage (pin 41)	-	1.6	-	V

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA7650H	48	QFP48	plastic	SOT196A

Video signal processor for CD-video/laser vision

TEA7650H

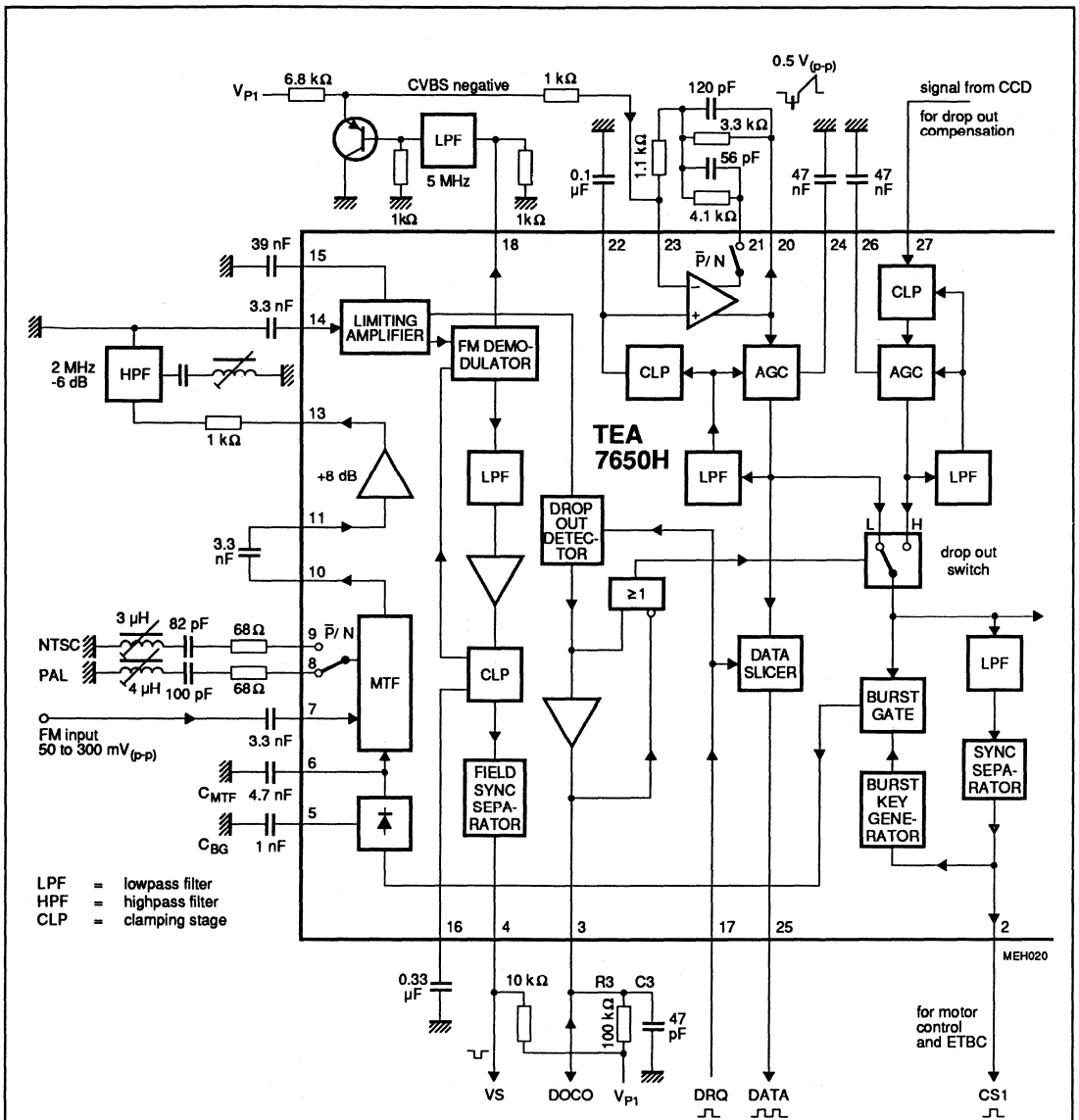


Fig.1(a) Block and test circuit; (continued in Fig.1(b)).

Video signal processor for CD-video/laser vision

TEA7650H

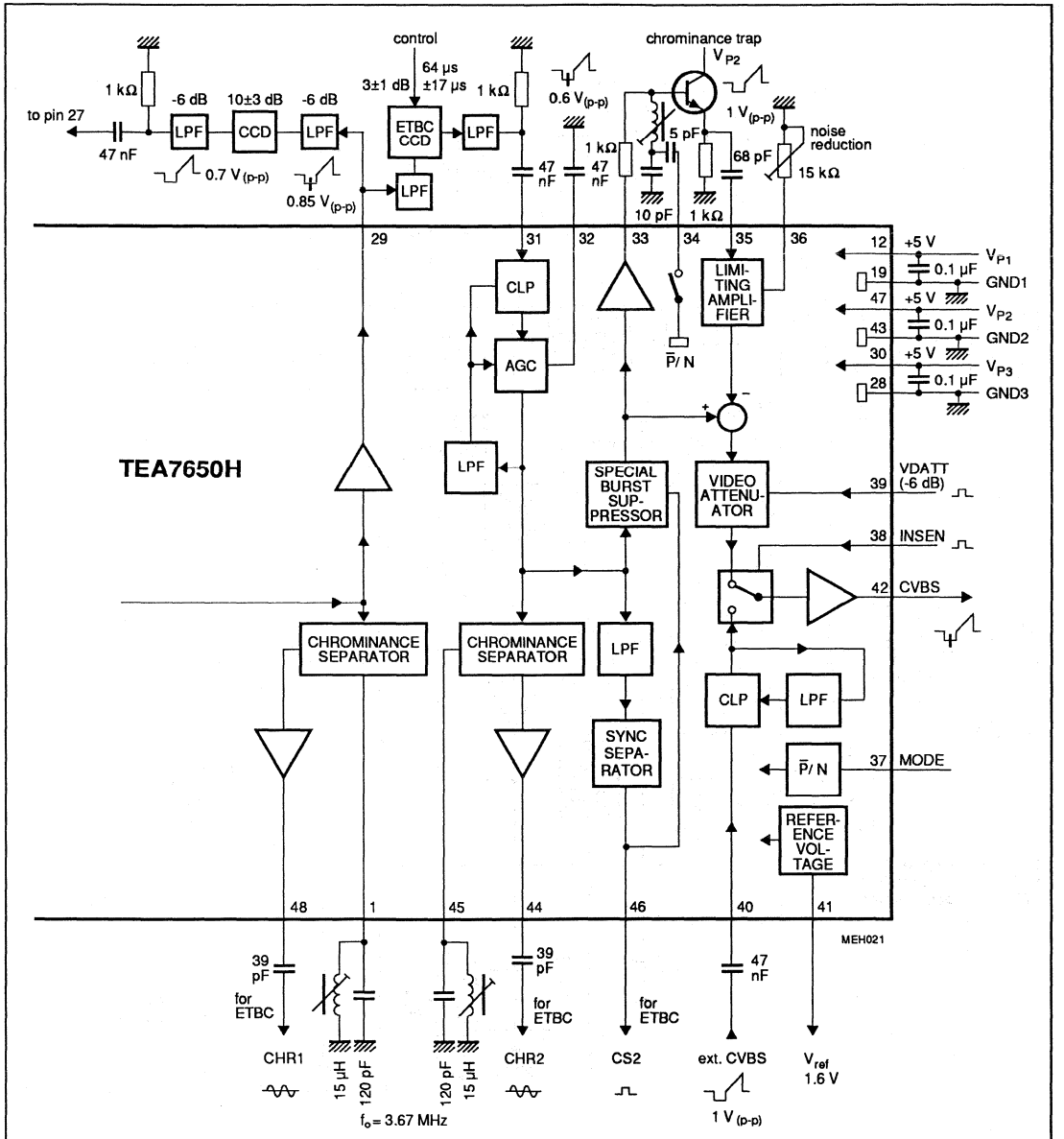


Fig.1(b) Block and test circuit; (continued from Fig.1(a)).

PINNING

SYMBOL	PIN	DESCRIPTION
CRSC1	1	3.67 MHz resonant circuit 1
CS1	2	line synchronization output pulse 1 (composite sync)
DOCO	3	drop out control, input/output for external control
VS	4	field sync output
C_{BG}	5	charging capacitor for burst rectifier
C_{MTF}	6	charging capacitor for MTF control voltage
FM-IN	7	FM input signal from preamplifier
FREF1	8	PAL resonant circuit for the MTF
FREF2	9	NTSC resonant circuit for the MTF
MTFO	10	MTF output signal (corrected FM signal)
AMPIN	11	input for 8 dB amplifier (FM signal)
V_{P1}	12	+5 V supply (referred to pins 6 to 15 and 18)
AMPO	13	output of 8 dB amplifier (FM signal)
LIMIN1	14	limiter amplifier input (FM signal to demodulator)
C_{LIM}	15	capacitor for slicing level control of limiter
C_{DEM}	16	capacitor for clamping level of FM demodulator
DRQ	17	data request input for data at pin 25
DEMO	18	FM demodulator output (CVBS negative)
GND1	19	ground (0 V) for V_{P1}
FBO1	20	feedback output at PAL and NTSC (de-emphasis)
FBO2	21	feedback output, additional at NTSC (de-emphasis)
C_{CVBS}	22	capacitor for clamping of CVBS amplifier
DEEMI	23	de-emphasis input for CVBS from demodulator
C_{AGC1}	24	capacitor for AGC of CVBS amplifier
DATA	25	data output of information code
C_{AGC2}	26	capacitor for AGC of drop out amplifier
PRLIN	27	input signal of preceding line from CCD delay
GND3	28	ground (0 V) for V_{P3}
DOSW	29	drop out switch buffer output (to CCD delay and ETBC)
V_{P3}	30	+5 V supply (referred to pins 5, 17, 20 to 36, 38 to 42)
VIDIN	31	CVBS input signal from ETBC
C_{AGC3}	32	capacitor for AGC of CVBS follower amplifier
VIBUF	33	video signal buffer output to chroma trap circuitry
FTRAP	34	switching output for chroma trap at NTSC
LIMI2	35	limiter amplifier input for noise reduction
NRADJ	36	noise level adjust point (resistor to ground)
MODE	37	standard select input PAL/NTSC (PAL = LOW)
INSEN	38	insertion enable input
VDATT	39	6 dB CVBS attenuation (active HIGH)

SYMBOL	PIN	DESCRIPTION
EXVID	40	external CVBS input for insertion
V_{ref}	41	reference voltage output (1.6 V)
CVBS	42	main CVBS output signal
GND2	43	ground (0 V) for V_{P2}
CHR2	44	chrominance output signal 2
CRSC2	45	3.67 MHz resonant circuit 2
CS2	46	line synchronization pulse 2 (composite sync)
V_{P2}	47	+5 V supply (referred to pins 1 to 4, 16, 37, 43 to 48)
CHR1	48	chrominance output signal 1

PIN CONFIGURATION

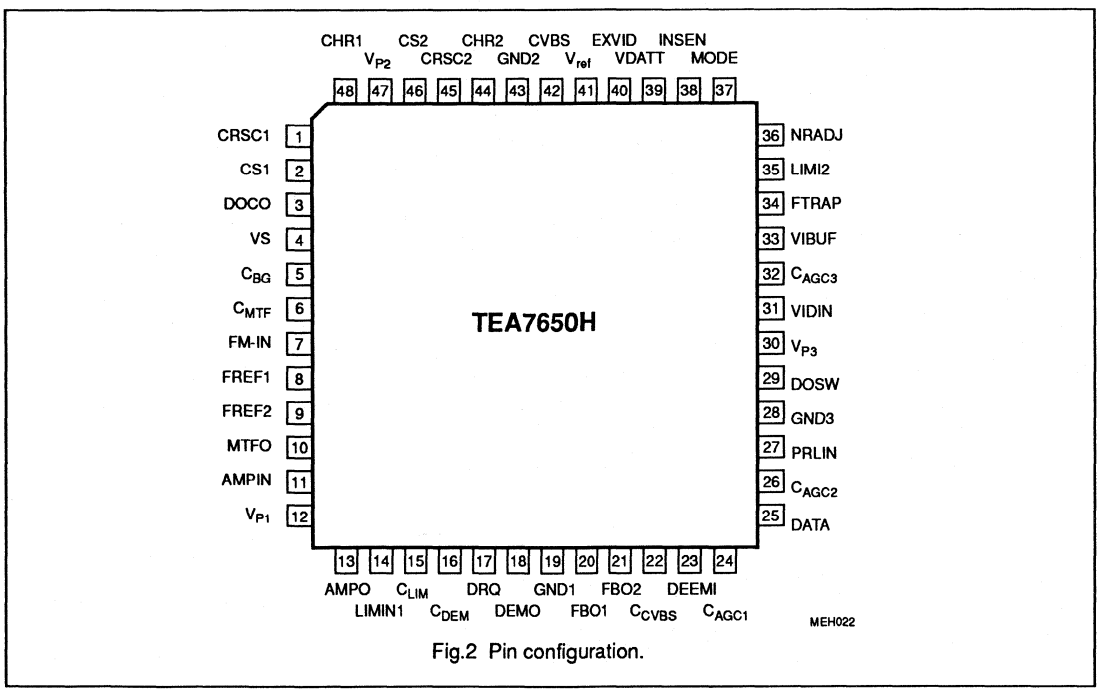


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 1 is the block diagram of the Video Signal Processor (VSP) including the peripherial circuitry for the video signal processing.The pulse-width modulated FM signal from the preamplifier is fed, via a DC blocking capacitor, into the IC (pin 7) at the input to the Modulation Transfer Function (MTF) circuit which corrects for the characteristic of the optical reading system.

MTF correction

Due to the finite diameter of the laser beam spot and the tangential velocity of the track of pits on the disk, the MTF of the optical system acts like a radius-dependent low-pass filter for the FM input signal. Although the video signal can be recovered without correction, the ratio of the amplitudes of the chrominance and luminance signals would not then be the same at the most inner and the most outer part of the disk. This influence of the disk radius is automatically corrected by the Video Signal Processor. The principle of correction is to use the deviation of the demodulated burst signal to generate an error voltage in order to control the frequency selective MTF circuit. The burst measurement operates as follows: A burst-key generator is triggered by the line synchronization pulse (CS1) to generate a burst-key pulse which activates the burst gate and rectifier stage. The signal at the rectifier output (pin 6) is used to control the amplification of the MTF circuit.

The carrier frequency in the PAL standard is different to that in the NTSC standard, therefore two separate resonant circuits are required on pins 8 and 9. They are selected by the PAL/NTSC system selector (pin 37).

The MTF-corrected FM signal at pin 10 is amplified (+8 dB) and fed, via the external filter which removes the audio frequency components from the signal, into the demodulator at pin 14.

Demodulation

The FM signal is first fed into a limiter circuit (pin 14) with automatic slicing level control to suppress the main carier in the demodulated signal. The demodulator has two outputs. The first (internal) clamps the demodulated video signal on peak-sync by controlling the transconductance of the demodulator. The FM signal can now be demodulated during disk start-up, thereby facilitating fast run-in. The second output signal from the demodulator (pin 18) is passed through an external 5 MHz low-pass filter to extract the CVBS signal. The CVBS signal is then fed into the de-emphasis network to compensate for the pre-emphasis of the video signal recorded on the disk.

De-emphasis

The de-emphasis circuit consists of an internal inverting amplifier and an external RC feedback network. Since the pre-emphasis on the disk in the PAL standard is different from that in the NTSC standard, the time constants are switchable. When PAL is selected, the first arm of the feedback network is active, otherwise both operate in parallel.The de-emphasized video signal is fed into an AGC stage (pin 20) where it is clamped on its black level and amplitude-controlled to a constant level. The signal is then fed into the data slicer and the drop out switch.

Data slicer

Coded signals on the video disk are extracted by the data slicer (output pin 25) when the Data Request input is activated (pin 17).

Drop out compensation

The drop out detector (DOD) in the IC is triggered by every positive or negative transition of the FM signal. A drop out is detected when the half-cycle period is outside the limits. Protection against a drop out is achieved by use of a video signal delayed by one line. The signal at the output of the drop out switch is fed out of the IC via a buffer (pin 29) and then through a delaying device (CCD) before being fed back into the IC (pin 27). The delayed video signal appears at the input of an AGC circuit to compensate for gain tolerances of the delay line and avoids the need for an external adjustment. When a drop out is detected, the drop out detector activates the video switch so that the lost information of the line is substituted by the information of the preceding line.

The drop out pulse is also present at pin 3 and can be used for different purposes. This pin can also act as an input to control the drop out switch by an external signal for test purposes.

Time error compensation

In a videodisk player timing errors are caused by deviations of the rotational speed of the motor, imperfections in the disk and unavoidable tolerances in the centering of the disk on the turntable. Track excentricity is the main cause of timing errors.

To minimize timing errors, it is necessary in the first place to keep the rotational speed of the disk as constant as possible. Referring back to the output of the switch in Fig.1, the video signal is also fed into a sync seperator and a chrominance separator with its external resonant circuits tuned to the chrominance subcarrier frequency. The phase of the line synchronization pulses (CS1, pin 2) can be used to control the speed of the turntable motor.

However, with this method it is not possible to obtain an acceptable reduction of timing errors for frequencies of 25 Hz and above. To reduce errors, use is made of an external Electronic Time Base Corrector (ETBC) between pins 27 and 31 which functions as a variable delay line driven by an error signal.

This error signal can be extracted from the output signal CS1 (pin 2), CHR1 (pin 48), CS2 (pin 46) and CHR2 (pin 44).

Since the line sync pulses (CS1) are not suitable to achieve an accurate enough measurement of time difference, use is made of the 3.58 MHz burst signal derived from the chrominance signal CHR1. If the same zero crossing of the burst signal is used in every line, the actual time can be measured with sufficient accuracy.

The CVBS signal leaving the ETBC might still have small timing errors due to residual control error. A second (feedback) loop is therefore required. The CVBS signal is fed into an AGC circuit (pin 31) that compensates for gain tolerances in the ETBC. As in the first loop, the line synchronization pulses (CS2) and the chrominance signal (CHR2) are derived from the CVBS signal by using second sync and chrominance separators. The error signal obtained by comparison in this feedback loop is added to the error signal obtained in the first loop.

Using the burst signal for accurate measurements is a problem in the PAL format due to its alternating phase. A special 3.75 MHz (240 fh) burst has therefore been added to the video signal recorded on the PAL disk. This burst is inserted on the top level of the line sync pulses.

In dual standard applications, the resonant circuits of the chrominance separators (pins 1 and 45) should be tuned to 3.67 MHz to ensure good separation of the special burst or the chrominance subcarrier.

When the timebase-corrected CVBS signal has by-passed the second sync and chrominance separators, it reaches the special burst suppressor which removes the special burst. The signal is then fed into the noise reduction circuit.

Noise reduction

A noise reduction circuit can be used to improve the apparent picture quality of a noisy signal. It operates as follows: First the timebase corrected CVBS signal is buffered (pin 33) and then fed into an external network which removes the chrominance subcarrier and all low-frequency components. It is then fed into a limiter (pin 35) which ensures that only small amplitudes (mainly noise) are removed from the main signal.

The chrominance subcarrier trap is switched to either the PAL subcarrier frequency (4.43 MHz) or the NTSC subcarrier (3.58 MHz) by the PAL/NTSC system selector (pin 37) using the additional small capacitor at pin 34. An external resistor at pin 36 is included so that manufacturers can select their preferred level of noise reduction, or none at all, by grounding the pin.

Picture insertion

The CVBS signal containing the information to be displayed is applied to pin 40. A clamp circuit ensures that the black level of this signal is the same as that of the main signal. Both signals are applied to the insertion switch.

When, for example, a character is to be displayed the 6 dB attenuation (pin 39) is first activated to generate a reduced contrast background area around the character (with respect to the black level so that the original picture is still visible). Next, the insertion switch (pin 38) is activated and the character appears at the output. By switching back to the original picture, the procedure operates in the reverse sequence.

Other examples of the picture insertion facility are displaying a background picture during start-up of the video disk player or the use of picture-in-picture.

A buffer is provided at the CVBS output (pin 42) which delivers a CVBS signal clamped to black level and controlled to a peak-to-peak amplitude of 1 V.

Reference voltage

A reference voltage of 1.6 V is provided by a bandgap circuit. Internally, all control circuits are supplied with this reference voltage. Externally, it can be used for various purposes.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage 1 (pin 12)	0	6	V
V_{P2}	supply voltage 2 (pin 47)	0	6	V
V_{P3}	supply voltage 3 (pin 30)	0	6	V
V_n	voltage on all pins except ground pins	0	V_P	V
P_{tot}	total power dissipation	0	360	mW
T_{stg}	storage temperatur range	–25	+150	°C
T_{amb}	operating ambient temperatur range	0	+70	°C
V_{ESD}	electrostatic handling* for all pins	±400	-	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	92	K/W

CHARACTERISTICS

$V_{P1} = V_{P2} = V_{P3} = 5$ V, $T_{amb} = 25$ °C, measurements taken in Fig.1 ; unless otherwise specified.

Voltages referred to GND1 (pin 19): V_{P1} and voltage at pins 6 to 15, 18
GND2 (pin 43): V_{P2} and voltage at pins 1 to 4, 16, 37, 44 to 48
GND3 (pin 28): V_{P3} and voltage at pins 5, 17, 20 to 36, 38 to 42

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage 1 (pin 12)		4.5	5	5.5	V
V_{P2}	supply voltage 2 (pin 47)		4.5	5	5.5	V
V_{P3}	supply voltage 3 (pin 30)		4.5	5	5.5	V
$I_{12+30+47}$	total supply current		-	-	65	mA
Standard select input (pin 37)						
V_{IL}	input voltage for standard PAL (LOW)		0	-	1	V
V_{IH}	input voltage for standard NTSC (HIGH), alternative measure for standard NTSC	pin connected pin open-circuit	3 -	- -	V_{P2} -	V
I_{IL}	input current (LOW)	V_{37} = 1 V	-	-	–100	µA
I_{IH}	input current (HIGH)	V_{37} = 4 V	-	-	20	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Modulation transfer function MTF (referred to GND1, pin 19)						
$V_{i\ (p-p)}$	FM input signal at pin 7 (peak-to-peak value)		50	-	300	mV
	for proper MTF correction		50	-	200	mV
Z_7	input impedance		-	5	-	kΩ
	MTF control signal					
$I_{(p-p)}$	output current for storage of the burst amplitude at pin 5 (peak-to-peak value)		-	200	-	μA
I_6	burst amplitude integrator, charging current (pin 6)		-	±50	-	μA
g	conductance $g = dI_6 / dV_5$		-	–1	-	mS
	MTF frequency selection (pins 8 and 9)	pin 8 aktive for PAL; pin 9 active for NTSC				
$V_{o\ (p-p)}$	output signal		-	$V_{7\ (p-p)}$	-	mV
Z	output impedance		-	-	10	Ω
$I_{o\ (p-p)}$	output current		-	-	4.5	mA
$V_{o\ (p-p)}$	MTF output signal (pin 10)		-	-	300	mV
Z_{10}	MTF output impedance		-	-	100	Ω
G_v	signal gain	$G_v = V_{10} / V_7$				
G_o	$G_v = G_o + 20 \log G_r (V_6)$		-	0	-	dB
G_r	minimum gain	$V_6 = 0$	-	0	-	dB
	maximum gain	$V_6 = 2.6$ V	-	300Ω/R8	-	
	maximum gain	$V_6 = 2.6$ V	-	300Ω/R9	-	
B	bandwith	–3 dB; $G_r = 0$	15	-	-	MHz
α_{2H}	second harmonic suppression	f = 8 MHz	40	-	-	dB
MTF following amplifier (pins 11 and 13)						
$V_{i\ (p-p)}$	FM input signal at pin 11 (peak-to-peak value)		-	-	300	mV
Z_{11}	intput impedance		10	-	-	kΩ
R_E	internal emitter resistor to ground		-	1.8	-	kΩ
Z_{13}	output impedance (pin 13)		-	-	50	Ω
$I_{o\ (p-p)}$	output current at pin 13 (peak-to-peak value)		-	-	1	mA
G_v	voltage gain (pins 13-11)		-	8	-	dB
B	bandwith (pin 13)	–3 dB	15	-	-	MHz
α_{2H}	second harmonic suppression		40	-	-	dB

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Limiting amplifier for demodulator						
$V_{i\,(p\text{-}p)}$	input signal for proper demodulation at pin 14 (peak-to-peak value)		0.1	-	1	V
Z_{14}	input impedance		10	-	-	kΩ
$I_{(p\text{-}p)}$	charging current of 2nd harmonic control at pin 15 (peak-to-peak value)		-	200	-	μA
FM demodulator with pulswidth-modulated current output ($f = 2\,f_{in}$). Referred to GND1, pin 19						
$I_{(p\text{-}p)}$	output current pulse at pin 18 (peak-to-peak value)		-	−3.2	-	mA
I_{18}	mean (average) DC current	for top sync	-	−1.75	-	mA
Z_{18}	output impedance		30	-	-	kΩ
V_{18}	DC output voltage range		0	-	2	V
S	transconductance	at PAL	-	−210	-	μA/MHz
		at NTSC	-	−185	-	μA/MHz
N	static non-linearity		-	-	10	%
B	bandwidth	±1 dB	5	-	-	MHz
α	main carrier suppression	$V_{14\,(p\text{-}p)} = 100$ mV	35	-	-	dB
$I_{(p\text{-}p)}$	charging current at pin 16 (amplitude storage for top sync, peak-to-peak value)		-	26	-	μA
De-emphasis amplifier (output pin 21 only for NTSC active). Referred to GND3, pin 28						
Z_{23}	input impedance (pin 23)		10	-	-	kΩ
I_{23}	DC input current		-	-	2	μA
$I_{(p\text{-}p)}$	charging current for black clamping capacitor at pin 22 (peak-to-peak value)		-	3	-	μA
$R_{20,\,21}$	output impedance (pins 20 and 21)		-	-	100	Ω
$V_{20,\,21}$	DC output voltage (black level)		-	2.2	-	V
BW_g	gain bandwidth product		40	-	-	MHz
$I_{24\,(p\text{-}p)}$	charging current for AGC capacitor at pin 24 (peak-to-peak value)		-	11	-	μA
Composite sync output CS1 (pin 2; referred to GND2, pin 43)						
V_{oH}	sync output voltage (active HIGH)	$I_2 = -0.5$ mA	4	-	-	V
V_{oL}	sync output voltage (LOW)	$I_2 = 0.5$ mA	-	-	0.4	V
t_d	delay of positive going sync edge		-	-	300	ns
Δt_d	jitter of positive going sync edge		-	-	40	ns
t_r, t_f	rise and fall time	$C_L = 22$ pF	-	-	200	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical sync output (VS), open collector output with 500 Ω internal series resistor, referred to GND2, pin 43						
V_4	sync output voltage active LOW (pin 4)	$I_4 = -0.5$ mA	-	-	0,7	V
t_d	delay time		-	18	-	µs
t_e	elongation time		-	70	-	µs
Drop out processing. (referred to GND3, pin 28)						
f_i	frequency range for no drop out recognition					
f_1	minimum value at PAL		-	5.6	-	MHz
f_2	maximum value at PAL		-	9.7	-	MHz
f_1	minimum value at NTSC		-	6.97	-	MHz
f_2	maximum value at NTSC		-	11.1	-	MHz
t_d	delay time on negative going edge for an abrupt drop out with $f < 0.5\ f_1$ or $f > 1.5\ f_2$		-	-	250	ns
t_e	drop out elongation time	C3 = 47 pF; R3 = 100 kΩ	-	3.5	-	µs
V_3	output voltage during drop out	internal R_S = 500 Ω; $I_3 = -0.5$ mA	-	-	0.7	V
$V_{3\ thr}$	threshold voltage of drop out switch		-	2	-	V
$V_{3\ DO}$	input voltage for forced drop out switching		0		0.7	V
$V_{i\ (p-p)}$	delayed video input signal at pin 27 (peak-to-peak value)	$R_G \leq 1$ kΩ	-	700	-	mV
V_{27}	DC input voltage (black level)		-	2.2	-	V
Z_{27}	input impedance		10	-	-	kΩ
$I_{(p-p)}$	charging current for coupling capacitor at pin 27 (peak-to-peak value)		-	3	-	µA
$I_{(p-p)}$	charging current for AGC of the delayed signal at pin 26 (peak-to-peak value)		-	11	-	µA
Chrominance output for purpose of ETBC, with R_L = 5 kΩ (pin 48) and nominal input signal. Resonant circuit at pin 1 tuned to 4.43 MHz for PAL (3.58 MHz for NTSC). Referred to GND2, pin 43. See previous comment to characteristics.						
$V_{o\ (p-p)}$	burst amplitude (peak-to-peak value) at pin 48	PAL; f = 4.43 MHz	-	760	-	mV
		NTSC; f = 3.58 MHz	-	725	-	mV
Z_{48}	output impedance		-	-	250	Ω
$I_{o\ (p-p)}$	output current (peak-to-peak value)		-	-	700	µA
α_{CR}	crosstalk attenuation from pin 44		32	-	-	dB
R_1	output impedance for resonant circuit		-	1.4	-	kΩ

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Electronic time base control ETBC and CCD delay (external). Referred to GND3, pin 28.						
$V_{o\ (p-p)}$	CVBS output signal of emitter output at pin 29 (peak-to-peak value)	$V_{20\ (p-p)}$= 0.5 V ±3 dB (peak-to-peak value)	-	850	-	mV
	burst amplitude in signal	for PAL	-	230	-	mV
		for NTSC	-	219	-	mV
V_{29}	DC output voltage (black level)		-	1.85	-	V
Z_{29}	output impedance		-	$-V_t / I_{29}$	-	Ω
I_{29}	output current (source)		-	-	–3	mA
S/N	signal-to-noise ratio from pin 7 to pin 29	5 MHz unweighted	50	-	-	dB
$\Delta V_{o\ (p-p)}$	difference of CVBS amplitude (peak-to-peak value)	switching from main to delayed signal; $V_{27\ (p-p)}$ = 0.7 V				
	at pin 29 referred to 0 dB level	0 dB	-		±2	%
	at pin 29 referred to ±4 dB level	±4 dB	-	-	±6	%
α_{CR}	crosstalk attenuation	f = 2 MHz	35	-	-	dB
ΔV_{29}	offset voltage after switching		-	-	10	mV
ΔV_S	spike amplitude at switching (pin 29)	t_S > 50 ns	-	-	15	mV
Chrominance and luminance amplifier (referred to GND3, pin 28).						
$V_{i\ (p-p)}$	delayed CVBS input signal (pin 31)	$R_G \leq 1$ kΩ	-	600	-	mV
V_{31}	DC input voltage (black level)		-	2.2	-	V
Z_{31}	input impedance		10	-	-	kΩ
$I_{(p-p)}$	charging current for coupling capacitor at pin 31 (peak-to-peak value)		-	3	-	µA
$I_{(p-p)}$	charging current for AGC at pin 32 (peak-to-peak value)		-	11	-	µA
Chrominance output for purpose of ETBC, with R_L = 5 kΩ (pin 44) and nominal input signal. Resonant circuit at pin 45 tuned to 4.43 MHz for PAL (3.58 MHz for NTSC). Referred to GND2, pin 43. See previous comment to characteristics.						
$V_{o\ (p-p)}$	burst amplitude (peak-to-peak value) at pins 44 for PAL	f = 4.43 MHz	-	760	-	mV
	for NTSC	f = 3.58 MHz	-	725	-	mV
Z_{44}	output impedance		-	-	250	Ω
$I_{o\ (p-p)}$	output current (peak-to-peak value)		-	-	700	µA
α_{CR}	crosstalk attenuation from pin 48		32	-	-	dB
R_{45}	output impedance for resonant circuit		-	1.4	-	kΩ

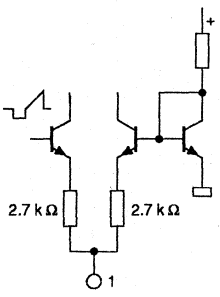
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Luminance noise reduction (referred to GND3, pin 28)						
$V_{(p-p)}$	output signal at pin 33 (peak-to-peak value)	$V_{i(p-p)}$= 0.6 V ±3 dB at pin 31	-	1	-	V
V_{33}	DC output voltage (black level)		-	2.2	-	V
I_E	internal emitter current to ground of emitter follower		-	1	-	mA
Z_{33}	output impedance		-	-	100	Ω
$I_{o(p-p)}$	AC output current at pin 33 (peak-to-peak value)		-	-	1.5	mA
$I_{(p-p)}$	chroma trap switch, active for NTSC input current (peak-to-peak value)		-	-	350	µA
Z_{34}	input impedance (pin 34)		-	-	50	Ω
$V_{i(p-p)}$	limiter amplifier input signal at pin 35 (peak-to-peak value)		-	1	-	V
	input signal for start of limiting		0	-	100	mV
Z_{35}	intput impedance		-	2	-	kΩ
V_{36}	voltage range for limiter control (pin 36)		0.1	-	1.5	V
	voltage for control-off		-	0	-	V
I_{36}	DC output current		-	–100	-	µA
Main CVBS output (referred to GND3, pin 28).						
$V_{o(p-p)}$	CVBS output signal of emitter output at pin 42 (peak-to-peak value)	$V_{i(p-p)}$= 0.6 V ±0 dB at pin 31	-	1	-	V
$\Delta V_{o(p-p)}$	residual variation of output voltage at pin 42 (peak-to-peak value)	$V_{i(p-p)}$= 0.6 V ±3 dB at pin 31	-	-	±3	%
V_{42}	DC output voltage (black level)		-	2.2	-	V
I_E	internal emitter current to ground of emitter follower		-	300	-	µA
Z_{42}	output impedance		-	-	100	Ω
I_o	output source current		-	-	–5	mA
B	video bandwidth	–3 dB	5			MHz
S/N	signal-to-noise ratio from pin 31 to pin 42	5 MHz unweighted	60	-	-	dB
α_{CR}	crosstalk attenuation between main and inserted signal	f = 5 MHz	45	-	-	dB
	differences at output due to switching from main to inserted signal (pin 42)					
α_{burst}	suppression of special burst		35	-	-	dB
ΔV_{42}	offset voltage after switching		-	-	50	mV
ΔV_S	spike amplitude at switching	t_S > 50 ns	-	-	20	mV
ΔV_{VID}	video attenuation for internal signal	V_{39} = HIGH	-	6	-	dB

CHARACTERISTICS (continued)

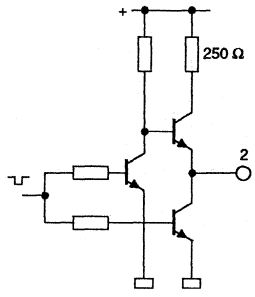
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
External video insertion input and switching control						
$V_{i\,(p\text{-}p)}$	input signal at pin 40 (peak-to-peak value)	$R_G \leq 1$ kΩ	-	1	-	V
V_{40}	DC voltage (black level)		-	2.9	-	V
G_v	voltage gain (pins 42-40)		-	0	-	dB
Z_{40}	intput impedance		10	-	-	kΩ
$I_{(p\text{-}p)}$	charging current at pin 40 (peak-to-peak value)		-	3	-	μA
B	video bandwith	–3 dB	8	-	-	MHz
V_{38}	voltage for insertion-on (HIGH)		3	-	V_P	V
	voltage for insertion-off (LOW)		0	-	1	V
I_{38}	input current (HIGH)	$V_{38} = 4$ V	-	-	2	μA
	input current (LOW)	$V_{38} = 1$ V	-	-	–10	μA
t_d	switchover delay time		-	-	50	ns
V_{39}	voltage for video attenuation-on (HIGH)	–6 dB video	3	-	V_P	V
	voltage for video attenuation-off (LOW)	0 dB video	0	-	1	V
I_{39}	input current (HIGH)	$V_{39} = 4$ V	-	-	2	μA
I_{39}	input current (LOW)	$V_{39} = 1$ V	-	-	–10	μA
t_d	switchover delay time		-	-	100	ns
Data output and data request input (pins 25 and 17)						
V_{25}	output voltage HIGH-level (pin 25)	$I_{25} = -0.5$ mA	3.5	-	-	V
	output voltage LOW-level	$I_{25} = 0.5$ mA	-	-	0.8	V
t_p	duty factor (t_p / T)		-	50	-	%
t_r and t_f	rise and fall time	$C_L = 22$ pF	-	-	150	ns
t_d	delay time		-	-	200	ns
V_{17}	voltage for data request-on (HIGH) at pin 17		3	-	V_P	V
	voltage for data request-off (LOW)		0	-	1	V
I_{17}	input current (HIGH)	$V_{17} = 4$ V	-	-	20	μA
	input current (LOW)	$V_{17} = 1$ V	-	-	–100	μA
t_d	data delay time		-	-	200	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Composite sync output CS2 (referred to GND2, pin 43)						
V_{46}	sync output voltage (active HIGH)	$I_{46} = -0.5$ mA	4	-	-	V
	sync output voltage at pin 46 (LOW)	$I_{46} = 0.5$ mA	-	-	0.4	V
t_d	delay of positive going sync edge		-	-	300	ns
Δt_d	jitter of positive going sync edge		-	-	40	ns
t_r	rise time	$C_{L\,46} = 22$ pF	-	-	150	ns
t_f	fall time	$C_{L\,46} = 22$ pF	--	-	200	ns
Reference output voltage (refered to GND3, pin 28)						
V_{ref}	reference output voltage (pin 41)		-	1.6	-	V
R_{41}	output resistance		-	-	5	kΩ
I_{ref}	output current (used for CCD reference)		-	-	±10	μA
dV_{41}/dV_P	supply voltage dependence		-	-	–20	dB
dV_{41}	dependence of junction temperature	$T_j = 20$ to 120 °C	-	-	±30	mV

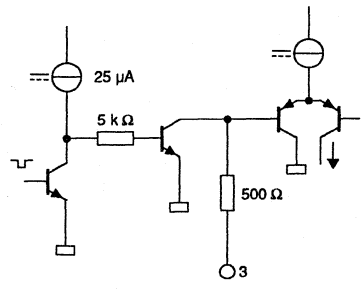
APPLICATION INFORMATION



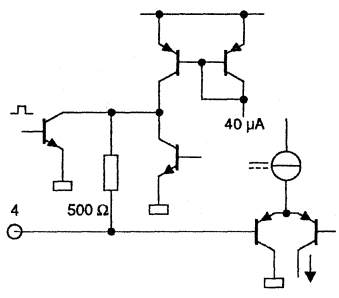
Pins 1 or 45: Frequency selection



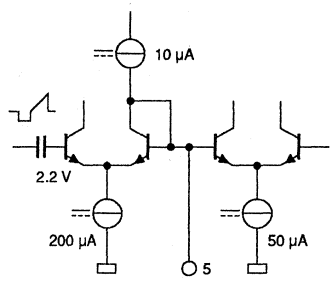
Pin 2: Output of first sync separator



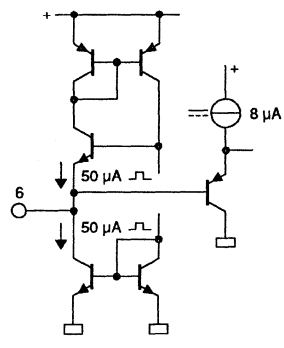
Pin 3: Output of dropout detector



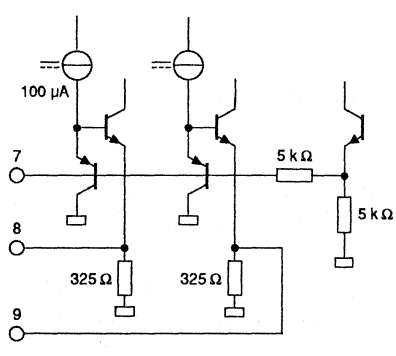
Pin 4: Output of vertical sync separator



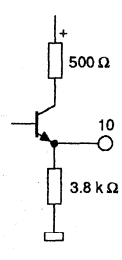
Pin 5: Output of burst rectifier



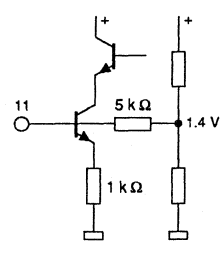
Pin 6: Burst amplitude integrator



Pins 7, 8 or 9: MTF corrector



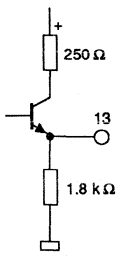
Pin 10: Output of MTF corrector



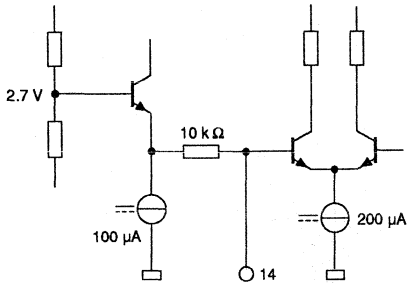
Pin 11: Input of 8 dB amplifier

MEH023

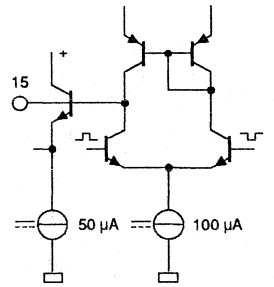
Fig.3(a) Internal circuits; (continued in Fig.4(b)).



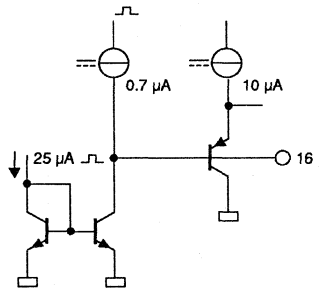
Pin 13: 8 dB amplifier output



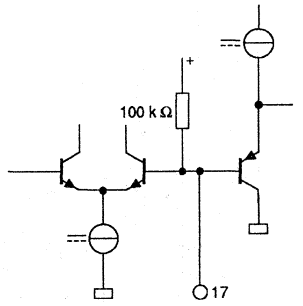
Pin 14: Input of limiter amplifier



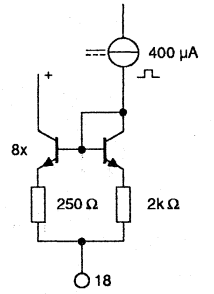
Pin 15: Control input of limiter amplifier



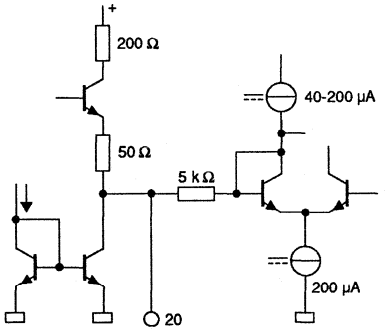
Pin 16: Demodulator control



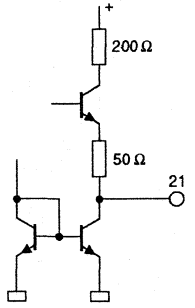
Pin 17: Input data request



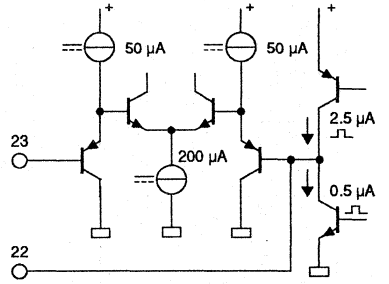
Pin 18: Output of FM-demodulator



Pin 20: De-emphasis amplifier output



Pin 21: De-emphasis amplifier output

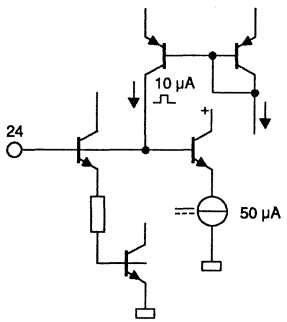


Pins 22 and 23: De-emphasis amplifier inputs

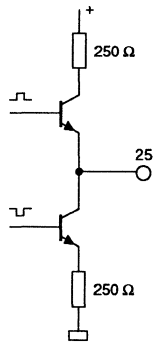
MEH024

Fig.3(b) Internal circuits; (continued from Fig.3(a)).

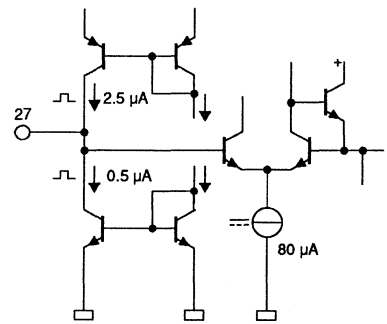
APPLICATION INFORMATION (continued)



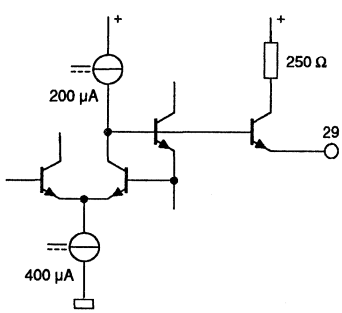
Pins 24, 26 or 32: AGC control input



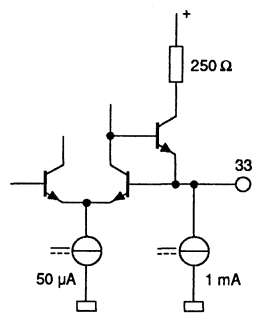
Pin 25: Data slicer output



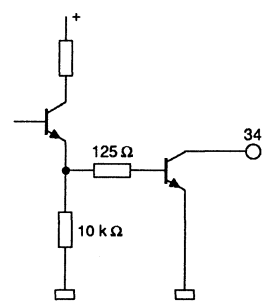
Pins 27 or 31: Video input



Pin 29: Video output



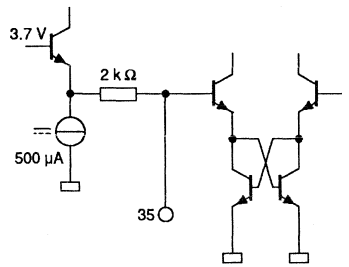
Pin 33: Video output



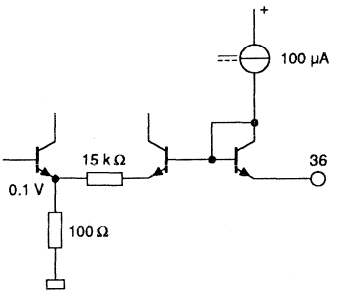
Pin 34: PAL/NTSC switch

MEH025

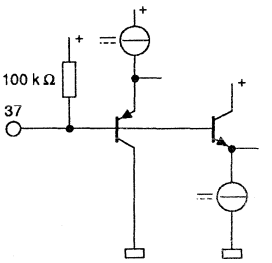
Fig.3(c) Internal circuits; (continued from Fig.3(b)).



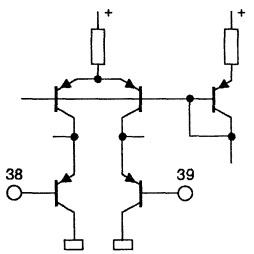
Pin 35: Input of noise reduction circuit



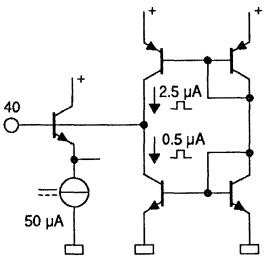
Pin 36: Noise reduction adjust



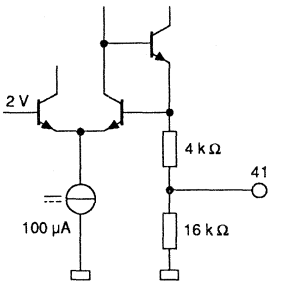
Pin 37: PAL/NTSC select



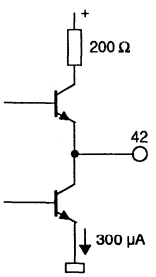
Pins 38 and 39: Insertion and video attenuation inputs



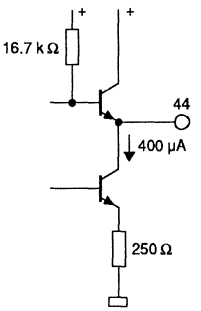
Pin 40: Video input



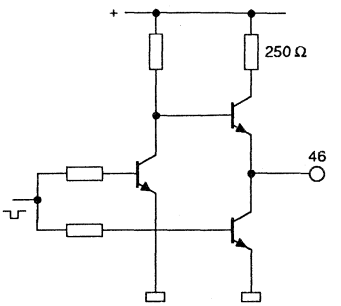
Pin 41: Reference voltage output



Pin 42: Video output



Pins 44 or 48: Chroma output
(Pin 45: Go to pin 1)



Pin 46: Output of second sync separator

MEH026

Fig.3(d) Internal circuits; (continued from Fig.3(c)).

2.5 GHz bi-directional I²C-bus controlled synthesizer

TSA5055T

GENERAL DESCRIPTION

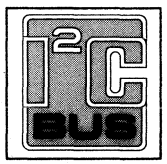
The TSA5055T is a single chip PLL frequency synthesizer designed for satellite TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, program the six output ports and set the charge-pump current. Four of these ports can also be used as input ports (3 general purpose I/O ports, one A/D converter). Digital information concerning these ports can be read out of the TSA5055T on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has one fixed I²C-bus address and 3 programmable addresses, programmed by applying a specific voltage to port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

FEATURES

- Complete 2.5 GHz single-chip system
- Low power 5 V, 60 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- 5-level A/D converter
- Address selection for Picture-In-Picture (PIP), DBS tuner, etc.
- 6 controllable outputs, 4 bi-directional
- Power-down flag
- Available in SOT109A package

APPLICATIONS

- Satellite TV
- High IF cable tuning systems



QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	4.75	5	5.5	V
I_{CC}	supply current	–	60	80	mA
Δf	frequency range	1	–	2.5	GHz
$V_{I\ (RMS)}$	input voltage level (RMS value)				
	1 GHz to 1.8 GHz	50	–	300	mV
	1.8 GHz to 2.6 GHz	70	–	300	mV
f_{XTAL}	crystal oscillator	3.2	4	4.48	MHz
I_O	open–collector output current				
	P7, P6, P5, P4	–	–	10	mA
	output current				
	P3, P0	–	1	–	mA
T_{amb}	operating ambient temperature range	–10	–	70	°C
T_{stg}	storage temperature range	–40	–	125	°C
$R_{th\ j\text{-}a}$	thermal resistance	–	110	–	K/W

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5055T	16	SO	plastic	SOT109A

2.5 GHz bi-directional I²C-bus controlled synthesizer

TSA5055T

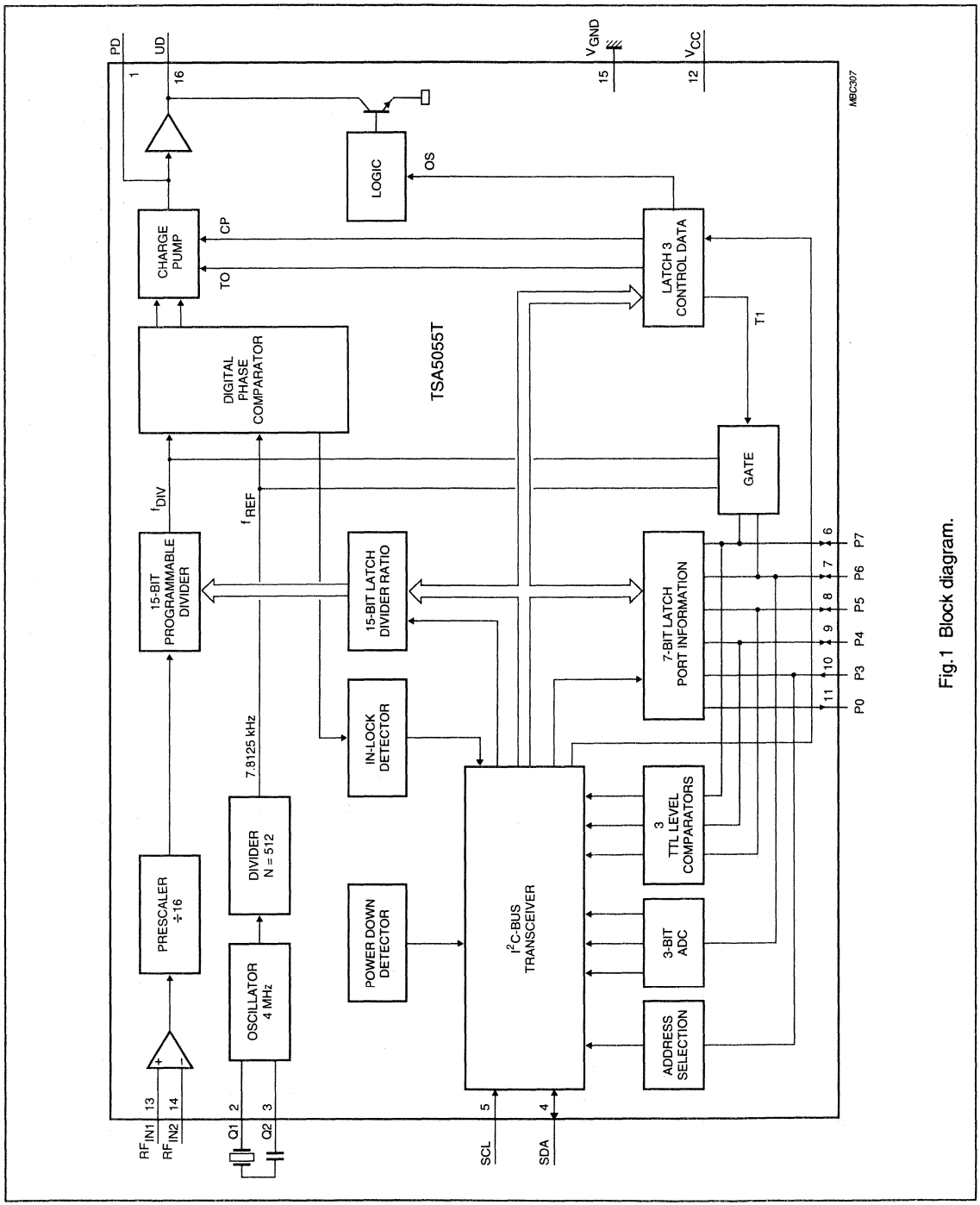


Fig.1 Block diagram.

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6	V
V_{P1}	charge-pump output voltage	−0.3	V_{CC}	V
V_{P2}	crystal (Q1) input voltage	−0.3	V_{CC}	V
V_{P4}	serial data input/output	−0.3	6	V
V_{P5}	serial clock input	−0.3	6	V
V_{P6}	input/output ports P7 - P0	−3	16	V
V_{P13}	prescaler inputs	−0.3	2.5	V
V_{P16}	drive output	−0.3	V_{CC}	V
I_{6L}	output ports P7 - P4 (open collector)	−1	15	mA
I_{4L}	SDA output (open collector)	−1	5	mA
T_{stg}	storage temperature range	−40	125	°C
T_j	junction temperature	−	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	110 K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C, category A (1000 V).

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

2.5 GHz bi-directional I²C-bus controlled synthesizer

TSA5055T

PINNING

SYMBOL	PIN	DESCRIPTION
PD	1	charge-pump output
Q1	2	crystal oscillator input 1
Q2	3	crystal oscillator input 2
SDA	4	serial data input/output
SCL	5	serial clock input
P7	6	port output/input (general purpose)
P6	7	port output/input (A/D converter)
P5	8	port output/input (general purpose)
P4	9	port output/input (general purpose)
P3	10	port output/input (address selection)
P0	11	port output
V_{CC}	12	voltage supply
RF_{IN1}	13	UHF/VHF signal input 1
RF_{IN2}	14	UHF/VHF signal input 2 (decoupled)
GND	15	ground
UD	16	drive output

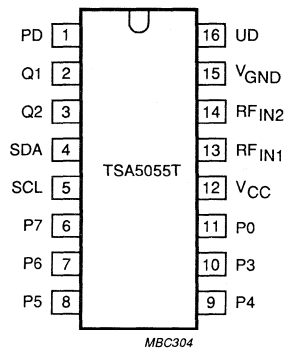


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TSA5055T is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode :
R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the TSA5055T. The bus transceiver has an auto-increment facility that permits the programming of the TSA5055T within one single transmission (address + 4 data bytes).

The TSA5055T can also be partly programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning. At power-on, the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of the UHF/VHF signal is first divided by 16, the step size is 125 kHz. A 3.2 MHz crystal can offer a step size of 100 kHz.

Table 1 Write data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
Output ports control bits	P7	P6	P5	P4	P3	X	X	P0	A	byte 5

MA1, MA0 programmable address bits (see Table 4)

A acknowledge bit

N14 to N0 programmable divider bits

$N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + N0$

CP charge-pump current

CP = 0 50 µA

CP = 1 220 µA

P7 - P4 = 1 open-collector outputs are active

P7 - P0 = 0 outputs are in high impedance state

P3 - P0 = 1 current-limited outputs are active

T1, T0, OS = 0 0 0 normal operation

T1 = 1 P6 = f_{ref}, P7 = f_{DIV}

T0 = 1 3-state charge-pump

OS = 1 operational amplifier output is switched off (varicap drive disable)

X don't care.

READ mode :
R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5055T by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5055T generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.

A second data byte can be read out of the TSA5055T if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs.The TSA5055T will then release the data line to allow the processor to generate a STOP condition. When ports P3 to P7 are used as inputs, they must be programmed in their high-impedance state.

The POR flag (power-on-reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5055T (end of a READ sequence). Control of the loop is made possible with the in-lock flag FL, which indicates (FL = 1) when the loop is phase-locked.

The I2, I1 and I0 bits represent the status of the I/O ports P7, P5 and P4 respectively. A logic '0' indicates a low level and a logic '1' a high level (TTL levels). A built-in 5-level A/D converter is available at I/O port P6. This converter can be used to feed AFC information to the controller from the IF section of the television, as shown in Fig. 3. The relationship between bits A2, A1, A0 and the input voltage at port P6 is given in Table 3.

Table 2 Read data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I1	I1	I0	A2	A1	A0	–	byte 2

POR power-on-reset flag. (POR = 1 on power-on)

FL in-lock flag (FL = 1 when the loop is phase-locked).

I2, I1, I0 digital information for I/O ports P7, P5 and P4 respectively

A2, A1, A0 digital outputs of the 5-level A/D converter. Accuracy is ½ LSB (see Table 3).

MSB is transmitted first.

Address selection (see Table 4)

The module address contains programmable address bits (MA1 and MA0), which offer the possibility of having several synthesizers (up to 3) in one system. The relationship between MA1 and MA0 and the input voltage at port P3 is given in Table 4.

Table 3 A/D converter levels

Voltage applied on port P6	A2	A1	A0
0.6 V_{CC} to V_{CC}	1	0	0
0.45 V_{CC} to 0.6 $_{CC}$	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V_{CC}	0	0	0

Table 4 Address selection

MA1	MA0	Voltage applied on port P3
0	0	0 to 0.1 V_{CC}
0	1	open
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

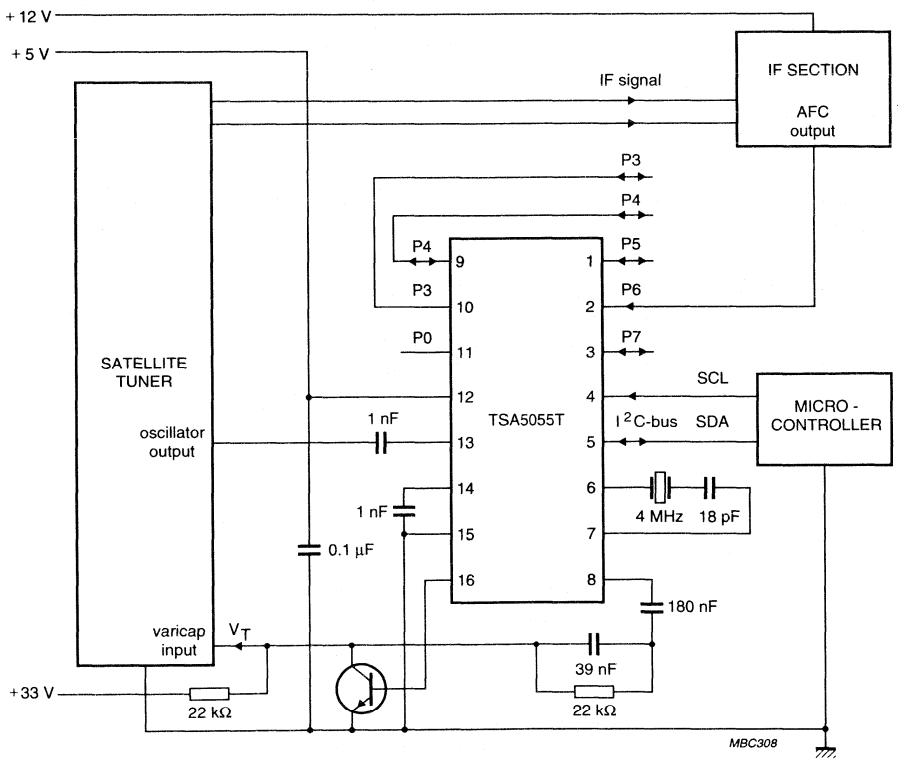


Fig.3 Typical application diagram.

CHARACTERISTICS

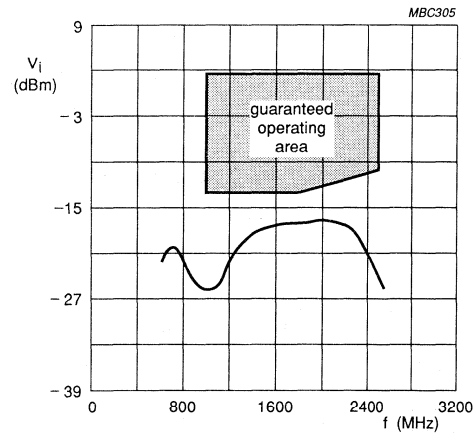
V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage range		4.75	–	5.5	V
T_{amb}	operating ambient temperature range		–10	–	70	°C
f_{RF}	RF input frequency range		1	–	2.5	GHz
N	divider		256	–	32767	
I_{CC}	supply current		–	60	80	mA
f_{XTAL}	crystal oscillator frequency		3.2	4	4.48	MHz
Z_I	input impedance (pin 2)		–480	–400	–320	Ω
$V_{I\ (RMS)}$	input voltage level (RMS value) f = 1 to 1.8 GHz f = 1.8 to 2.5 GHz	V_{CC} = 4.75 to 5.5 V; T_{amb} = –10 to 70 °C see typical sensitivity curve in Fig. 4	 50/–13 70/–10	 – –	 300/2.6 300/2.6	 mV mV
R_I	prescaler input impedance	see Smith chart in Fig. 5	–	50	–	Ω
C_I	input capacitance		–	2	–	pF
Output ports P3, P0 (current limited)						
I_{LO}	leakage current	V_{10H} = 13.5 V	–	–	10	µA
I_{OS}	output sink current	V_{10} = 13.5 V	0.7	1	1.5	mA
Output ports P7 to P4 (open collector) (see note 1)						
I_{LO}	leakage current	V_{6H} = 13.5 V	–	–	10	µA
V_{OL}	output voltage LOW	I_{6L} = 10 mA note 2	–	–	0.7	V
Input ports P6, P3						
I_{IH}	input current HIGH	V_{7H} = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_{7L} = 0	–10	–	–	µA
Input ports P7, P5, P4						
V_{IH}	input voltage HIGH		2.7	–	–	V
V_{IL}	input voltage LOW		–	–	0.8	V
I_{IH}	input current HIGH	V_{6H} = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_{6L} = 0	–10	–	–	µA
Bus inputs SCL, SDA						
V_{IH}	input voltage HIGH		3	–	5.5	V
V_{IL}	input voltage LOW		–	–	1.5	V
I_{IH}	input current HIGH	V_{5H} = 5 V; V_{CC} = 0	–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Bus inputs SCL, SDA						
I_{IL}	input current LOW	V_{5H} = 5 V; V_{CC} = 5 V	–	–	10	µA
		V_{5L} = 0; V_{CC} = 0	−10	–	–	µA
		V_{5L} = 0; V_{CC} = 5 V	−10	–	–	µA
Output SDA (open collector)						
I_{4H}	leakage current	V_{4H} = 5.5 V	–	–	10	µA
V_{4L}	output voltage	I_{4L} = 3 mA	–	–	0.4	V
Charge-pump output PD						
I_{OH}	output current HIGH (absolute value)	CP = 1	90	220	300	µA
I_{OL}	output current LOW (absolute value)	CP = 0	22	50	75	µA
V_O	output voltage	in-lock	1.5	–	2.5	V
I_{1leak}	off-state leakage current	T0 = 1	−5	–	5	nA
Operational amplifier output UD (test mode: T0 = 1)						
V_{16}	output voltage	V_{IL} = 0	–	–	100	mV
	output voltage when switched off	T0 = 1; OS = 1; V_{IL} = 2 V	–	–	250	mV
h_{FE}	operational amplifier current gain $I_{16}/(I_1 - I_{1leak})$	T0 = 1; OS = 0; V_{IL} = 2 V; I_{16} = 10 µA	2000	–	–	

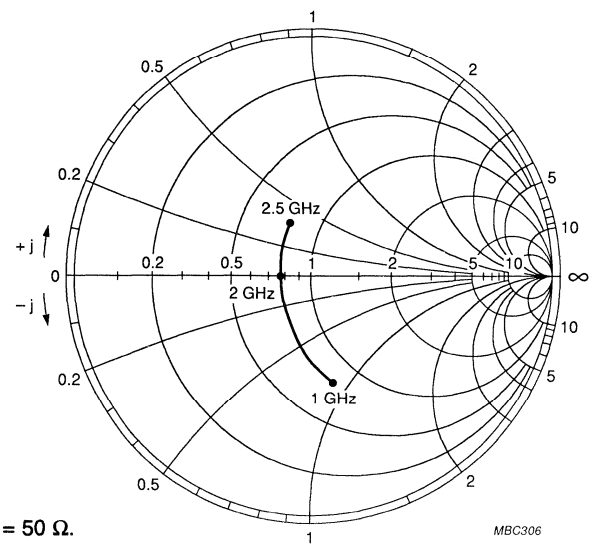
Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with a single open collector active.



V_{CC} = 5 V; T_{amb} = 25 °C.

Fig.4 Prescaler typical input sensitivity curve.



V_{CC} = 5 V; reference value = 50 Ω.

Fig.5 Prescaler Smith chart of typical input impedance.

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm (K_{VCO} / K_O) \times I_{CP} \times (C1 + C2)/(C1 \times C2)$$

where:

K_{VCO} = oscillator slope (Hz/V)

I_{CP} = charge-pump current (A)

K_O = 4×10^6

C1 and C2 = loop filter capacitors.

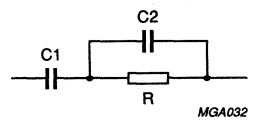


Fig.6 Loop filter.

FLOCK FLAG APPLICATION

- K_{VCO} = 50 MHz/V (UHF band)
- I_{CP} = 220 μA
- C1 = 180 nF
- C2 = 39 nF
- Δf = ±85.8 kHz.

Table 5 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	μs
Time span between the loop losing lock and FL-flag resetting	0	128	μs

1.3 GHz Bidirectional I²C-bus controlled synthesizer

TSA5511

FEATURES

- Complete 1.3 GHz single chip system
- Low power 5 V, 35 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner
- Analog-to-digital converter
- 8 bus controlled ports (5 for TSA5511T), 4 open collector outputs (bi-directional)
- Power-down flag

APPLICATIONS

- TV tuners
- VCR Tuners

DESCRIPTION

The TSA5511 is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the eight output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning those ports can be read out of the TSA5511 on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has one fixed I²C-bus address and 3 programmable addresses, programmed by applying a specific voltage on Port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δf	frequency range	64	–	1300	MHz
V_I	input voltage level				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator	3.2	4	4.48	MHz
I_O	open–collector output current	10	–	–	mA
I_O	current–limited output current	–	1	–	mA
T_{amb}	operating ambient temperature range	–10	–	80	°C
T_{stg}	storage temperature range (IC)	–40	–	150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5511	18	DIL	plastic	SOT102
TSA5511T	16	SO	plastic	SOT109
TSA5511AT	20	SO	plastic	SOT163

1.3 GHz Bidirectional I²C-bus controlled synthesizer

TSA5511

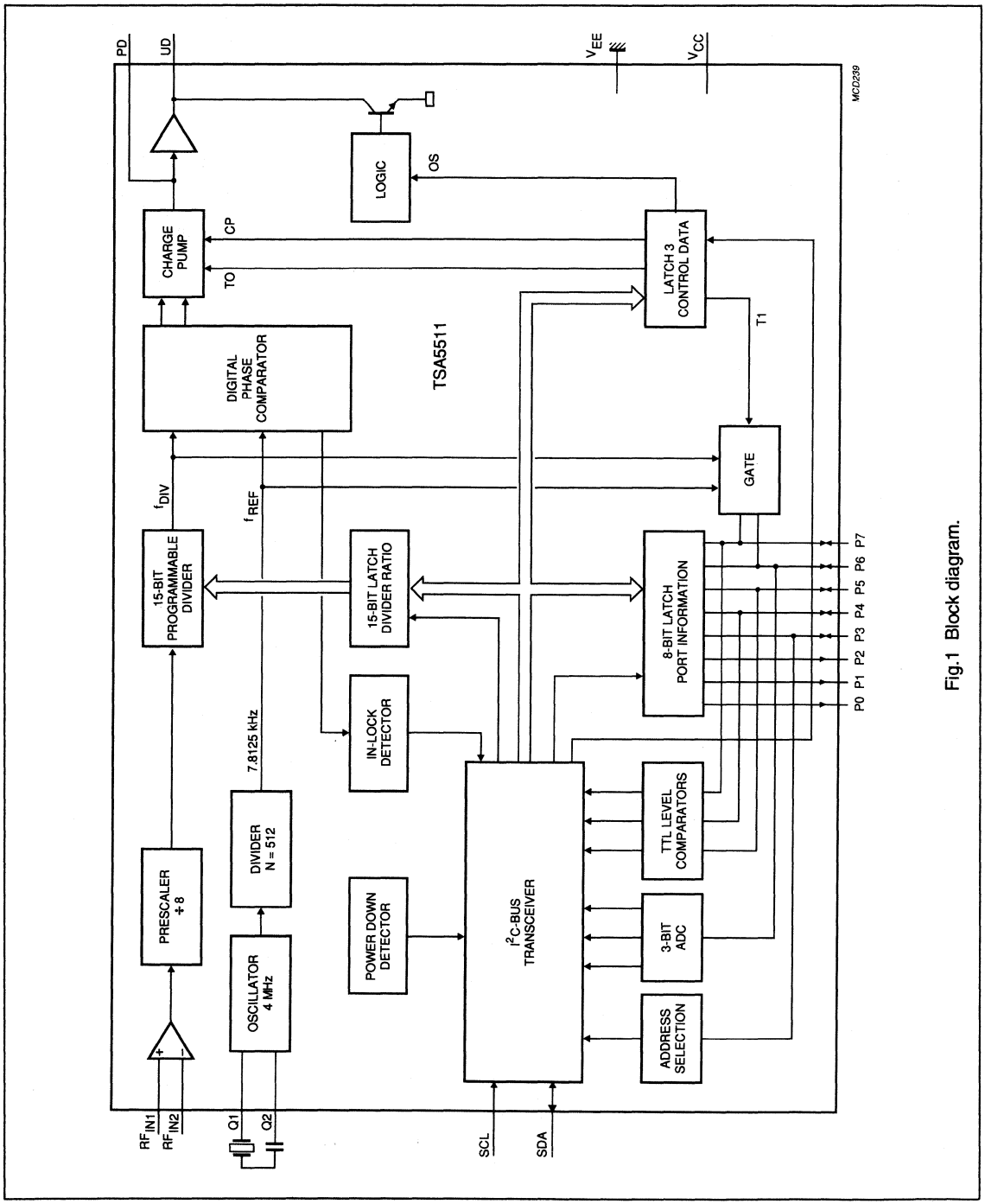


Fig.1 Block diagram.

1.3 GHz Bidirectional I²C-bus controlled synthesizer

TSA5511

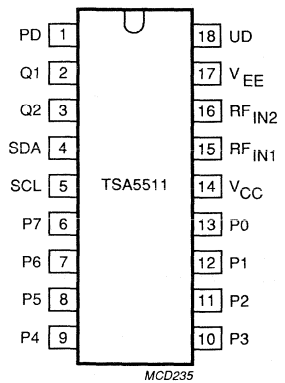


Fig.2 Pin configuration (SOT102).

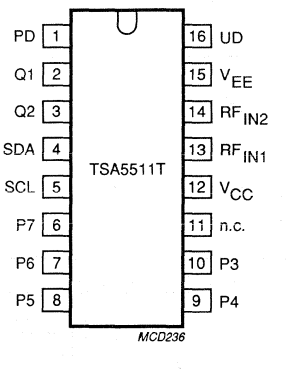


Fig.3 Pin configuration (SOT109).

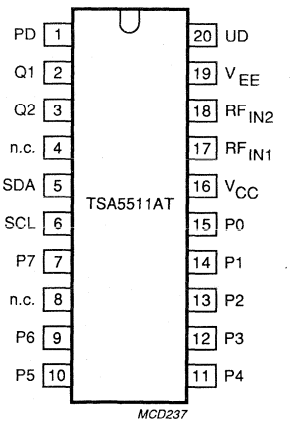


Fig.4 Pin configuration (SOT163).

PINNING

SYMBOL	PIN DIL 18	PIN SO16	PIN SO20	DESCRIPTION
PD	1	1	1	charge-pump output
Q1	2	2	2	crystal oscillator input 1
Q2	3	3	3	crystal oscillator input 2
n.c.			4	not connected
SDA	4	4	5	serial data input/output
SCL	5	5	6	serial clock input
P7	6	6	7	port output/input (general purpose)
n.c.			8	not connected
P6	7	7	9	port output/input for general purpose ADC
P5	8	8	10	port output/input (general purpose)
P4	9	9	11	port output/input (general purpose)
P3	10	10	12	port output/input for address selection
P2	11		13	port output
n.c.		11		not connected
P1	12		14	port output
P0	13		15	port output
V_{CC}	14	12	16	voltage supply
RF_{IN1}	15	13	17	UHF/VHF signal input 1
RF_{IN2}	16	14	18	UHF/VHF signal input 2 (decoupled)
V_{EE}	17	15	19	GND
UD	18	16	20	drive output

FUNCTIONAL DESCRIPTION

The TSA5511 is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode : R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the TSA5511. The bus transceiver has an auto-increment facility which permits the programming of the TSA5511 within one single transmission (address + 4 data bytes).

The TSA5511 can also be partially programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purpose. At power-on the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of UHF/VHF signal is first divided by 8 the step size is 62.5 kHz. A 3.2 MHz crystal can offer step sizes of 50 kHz.

Table 1 Write data format

	MSB							**LSB**		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
Output ports control bits	P7	P6	P5	P4	P3	P2*	P1*	P0*	A	byte 5

note

* not valid for TSA5511T.

MA1, MA0 programmable address bits (see Table 4)

A acknowledge bit

$N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + N0$

CP charge-pump current

CP = 0 50 µA

CP = 1 220 µA

P3 to P0 = 1 limited-current output is active

P7 to P4 = 1 open-collector output is active

P7 to P0 = 0 output are in high impedance state

T1 = 1 P6 = f_{ref}, P7 = f_{DIV}

T0 = 1 3-state charge-pump

OS = 1 operational amplifier output is switched off (varicap drive disable)

FUNCTIONAL DESCRIPTION (continued)

READ mode : R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5511 by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5511 generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.
A second data byte can be read out of the TSA5511 if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs.
The TSA5511 will then release the data line to allow the processor to generate a STOP condition.
When ports P3 to P7 are used as inputs, they must be programmed in their high-impedance state.
The POR flag (power-on-reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5511 (end of a READ sequence).
Control of the loop is made possible with the in-lock flag FL which indicates (FL = 1) when the loop is phase-locked. The bits I2, I1 and I0 represent the status of the I/O ports P7, P5 and P4 respectively. A logic 0 indicates a LOW level and a logic 1 a HIGH level (TTL levels).
A built-in 5-level ADC is available on I/O port P6. This converter can be used to feed AFC information to the controller from the IF section of the television as illustrated in the typical application circuit in Fig. 5. The relationship between bits A2, A1 and A0 and the input voltage on port P6 is given in Table 3.

Table 2 Read data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	–	byte 2

POR	power-on-reset flag. (POR = 1 on power-on)
FL	in-lock flag (FL = 1 when the loop is phase-locked)
I2, I1, I0	digital information for I/O ports P7, P5 and P4 respectively
A2, A1, A0	digital outputs of the 5-level ADC. Accuracy is 1/2 LSB (see Table 3)

MSB is transmitted first.

Address selection

The module address contains programmable address bits (MA1 and MA0) which together with the I/O port P3 offers the possibility of having several synthesizers (up to 3) in one system.
The relationship between MA1 and MA0 and the input voltage I/O port P3 is given in Table 4.

Table 3 A/D converter levels

Voltage applied on the port P6	A2	A1	A0
0.6 V_{CC} to 13.5 V	1	0	0
0.45 V_{CC} to 0.6 V_{CC}	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V	0	0	0

Table 4 Address selection

MA1	MA0	Voltage applied on port P3
0	0	0 to 0.1 V_{CC}
0	1	always valid
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6	V
V_1	charge-pump output voltage	−0.3	V_{CC}	V
V_2	crystal (Q1) input voltage	−0.3	V_{CC}	V
V_4	serial data input/output	−0.3	6	V
V_5	serial clock input	−0.3	6	V
$V_{6\text{-}13}$	P7 to P1 I/O voltage	−0.3	+16	V
V_{15}	prescaler input	−0.3	V_{CC}	V
V_{18}	drive output voltage	−0.3	V_{CC}	V
I_6	P7 to P0 output current (open collector)	−1	15	mA
I_4	SDA output current (open collector)	−1	5	mA
T_{stg}	storage temperature range (IC)	−40	+150	°C
T_j	maximum junction temperature		150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air (DIL18)	-	80	K/W
	from junction to ambient in free air (SO16)	-	110	K/W
	from junction to ambient in free air (SO20)	-	80	K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified
All pin numbers refer to DIL 18 version

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Functional range						
V_{CC}	supply voltage range		4.5	–	5.5	V
T_{amb}	operating ambient temperature range		–10	–	80	°C
f_{CLK}	clock input frequency		64	–	1300	MHz
N	divider		256	–	32767	
I_{CC}	supply current		25	35	50	mA
f_{XTAL}	crystal oscillator		3.2	4	4.48	MHz
Z_I	input impedance (pin 2)		–480	–400	–320	Ω
	input level	V_{CC} = 4.5 V to 5.5 V; T_{amb} = –10 to 80 °C; see typical sensitivity curve in Fig. 6				
	f = 80 to 150 MHz		12/–25	–	300/2.6	mV/dBm
	f = 150 to 1000 MHz		9/–28	–	300/2.6	mV/dBm
	f = 1000 to 1300 MHz		40/–15	–	300/2.6	mV/dBm
R_I	prescaler input resistance see SMITH chart in Fig. 7		–	50	–	Ω
C_I	input capacitance		–	2	–	pF
Output ports (current-limited) P0-P3						
I_{LO}	leakage current	V_{13} = 13.5 V	–	–	10	µA
I_{sink}	output sink current	V_{13} = 12 V	0.7	1.0	1.5	mA
Output ports (open collector) P4-P7 (see note 1)						
I_{LO}	leakage current	V_9 = 13.5 V	–	–	10	µA
V_{OL}	output voltage LOW	I_9 = 10 mA; note 2	–	–	0.7	V
Input P3						
I_{OH}	input current HIGH	V_{OH} = 13.5 V	–	–	10	µA
I_{OL}	input current LOW	V_{OL} = 0 V	–10	–	–	µA
Input ports P4-5, P7						
V_{IL}	input voltage LOW		–	–	0.8	V
V_{IH}	input voltage HIGH		2.7	–	–	V
I_{IH}	input current HIGH	V_6 = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_6 = 0 V	–10	–	–	µA
Input port P6						
I_{IH}	input current HIGH	V_7 = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_7 = 0 V	–10	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA inputs						
V_{IH}	input voltage HIGH		3.0	–	5.5	V
V_{IL}	input voltage LOW		–	–	1.5	V
I_{IH}	input current HIGH	V_5 = 5 V, V_{CC} = 0 V; V_5 = 5 V, V_{CC} = 5 V	– –	– –	10 10	µA µA
I_{IL}	input current LOW	V_5 = 0 V, V_{CC} = 0 V; V_5 = 0 V, V_{CC} = 5 V	–10 –10	– –	– –	µA µA
Output SDA (open collector)						
I_{LO}	leakage current	V_4 = 5.5 V	–	–	10	µA
V_4	output voltage	I_4 = 3 mA	–	–	0.4	V
Charge-pump output PD						
I_{IH}	input current HIGH (absolute value)	CP = 1	90	220	300	µA
I_{IL}	input current LOW (absolute value)	CP = 0	22	50	75	µA
V_O	output voltage	in-lock	1.5	–	2.5	V
I_{1Leak}	off-state leakage current	T0 = 1	–5	–	5	nA
Operational amplifier output UD (test mode : T0 = 1)						
V_{18}	output voltage	V_{IL} = 0 V	–	–	100	mV
V_{18}	output voltage when switched-off	OS = 1; V_{IL} = 2 V	–	–	200	mV
G	operational amplifier current gain; $I_{18}/(I_1 - I_{1leak})$	OS = 0; V_{1L} = 2 V; I_{18} = 10 µA	2000	–	–	

Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with a single open-collector port active.

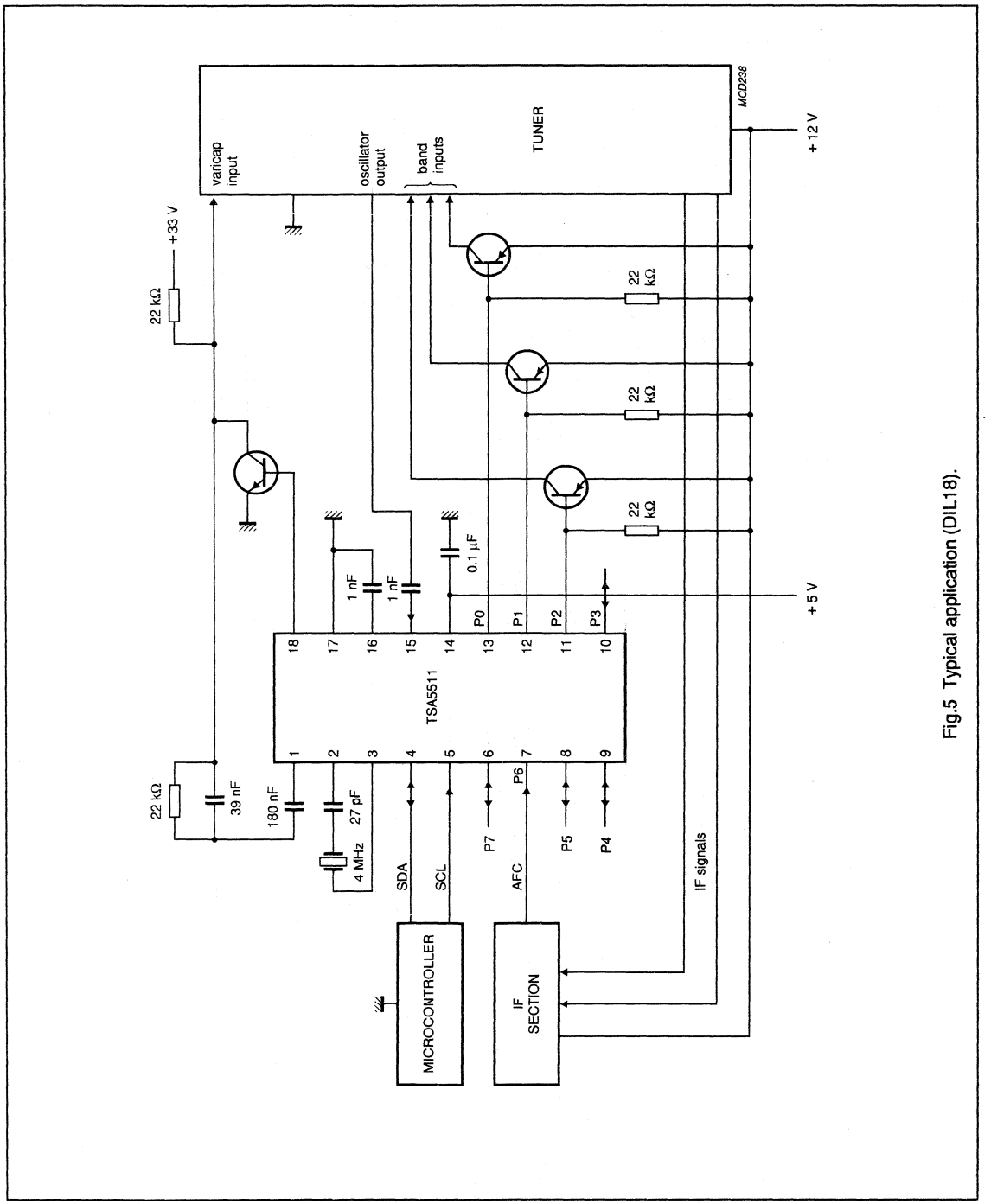


Fig.5 Typical application (DIL18).

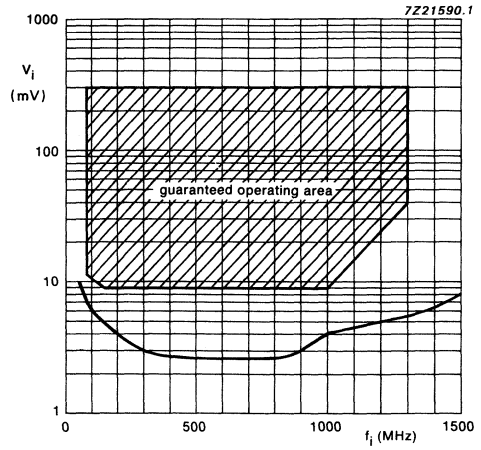


Fig.6 Prescaler typical input sensitivity curve; V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to +80 °C.

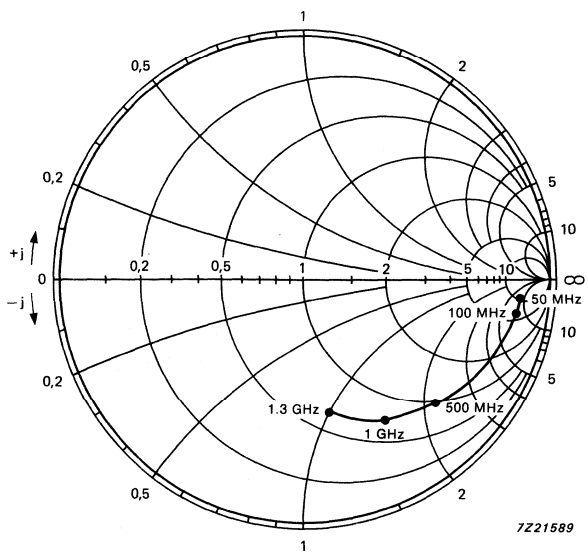


Fig.7 Prescaler Smith chart of typical input impedance; V_{CC} = 5 V; reference value = 50 Ω.

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm (K_{VCO} / K_O) \times I_{CP} \times (C1 + C2)/(C1 \times C2)$$

where:

K_{VCO}	=	oscillator slope (Hz/V)
I_{CP}	=	charge-pump current (A)
K_O	=	4 x 10E6
C1 and C2	=	loop filter capacitors

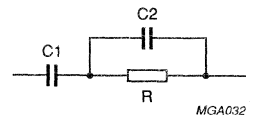


Fig.8 Loop filter.

FLOCK FLAG APPLICATION

- K_{VCO} = 16 MHz/V (UHF band)
- I_{CP} = 220 μA
- C1 = 180 nF
- C2 = 39 nF
- Δf = ± 27.5 kHz.

Table 5 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	μs
Time span between the loop losing lock and FL-flag resetting	0	128	μs

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

1.3 GHz Bidirectional I²C-bus controlled synthesizer

TSA5512

FEATURES

- Complete 1.3 GHz single chip system
- Low power 5 V, 35 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner
- Analog-to-digital converter
- 8 bus controlled ports (6 for TSA5512T), 8 open collector outputs (4 bidirectional)
- Power-down flag

APPLICATIONS

- TV tuners
- VCR Tuners

DESCRIPTION

The TSA5512 is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the eight output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning those ports can be read out of the TSA5512 on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has one fixed I²C-bus address and 3 programmable addresses, programmed by applying a specific voltage on Port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δf	frequency range	64	–	1300	MHz
V_I	input voltage level				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator	3.2	4	4.48	MHz
I_O	open–collector output current	5	–	–	mA
T_{amb}	operating ambient temperature range	–10	–	80	°C
T_{stg}	storage temperature range (IC)	–40	–	150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5512	18	DIL	plastic	SOT102
TSA5512T	16	SO	plastic	SOT109
TSA5512AT	20	SO	plastic	SOT163
TSA5512M	20	SSOP	plastic	SOT266

1.3 GHz Bidirectional I²C-bus controlled synthesizer

TSA5512

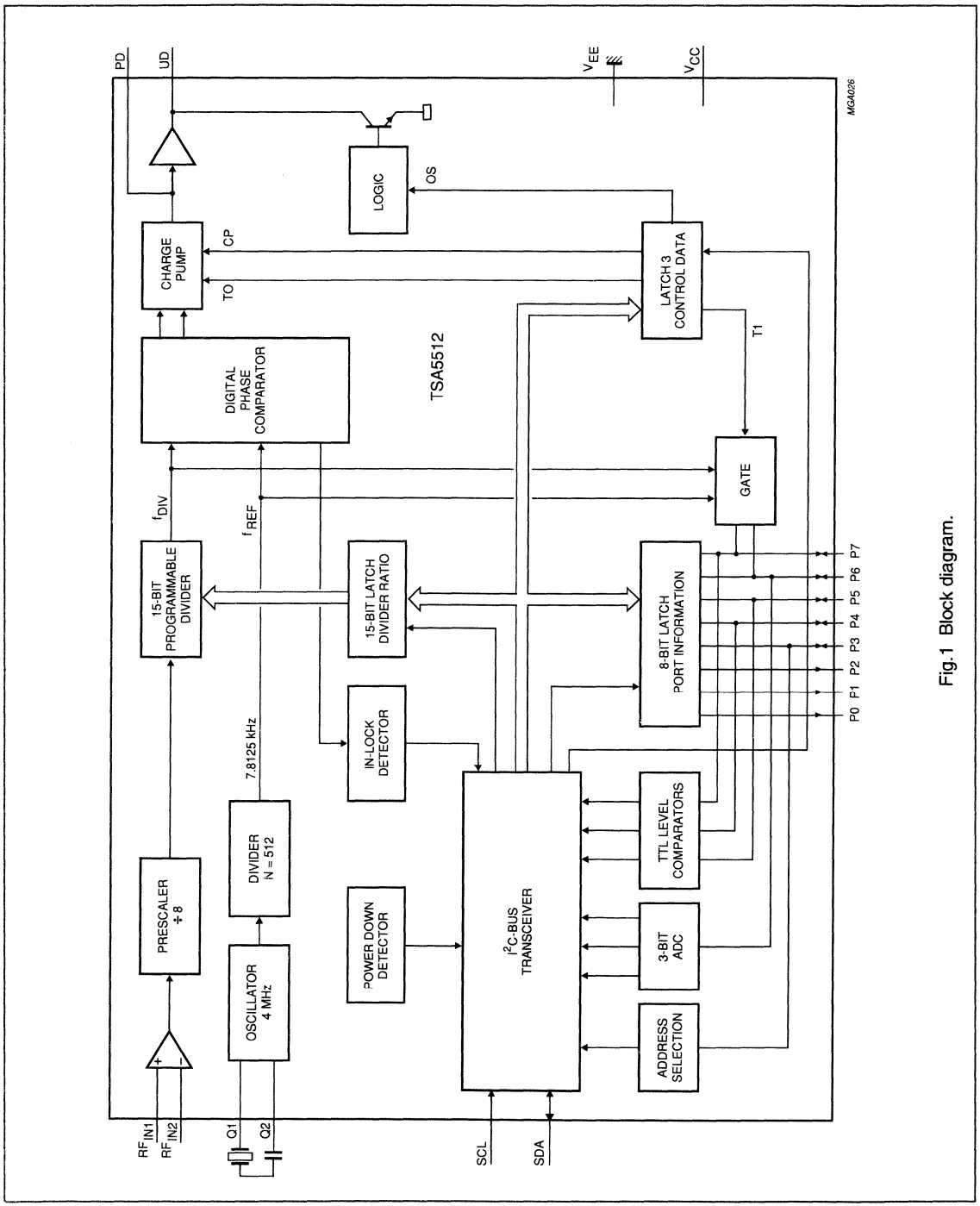


Fig.1 Block diagram.

1.3 GHz Bidirectional I²C-bus controlled synthesizer

TSA5512

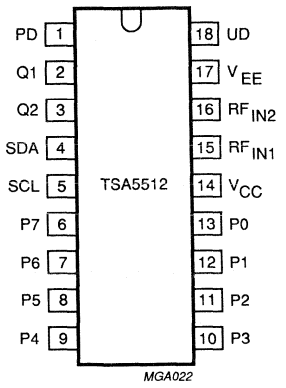


Fig.2 Pin configuration (SOT102).

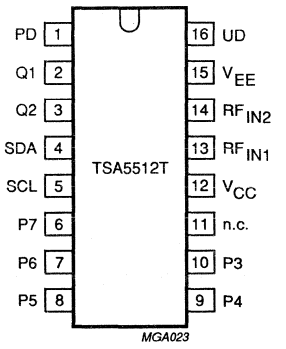


Fig.3 Pin configuration (SOT109).

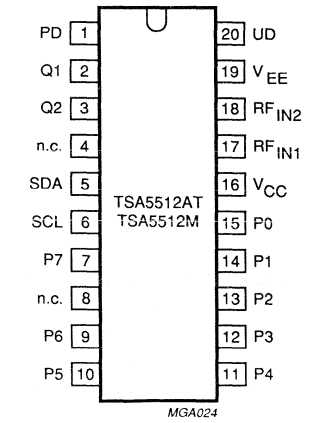


Fig.4 Pin configuration (SOT163/SOT266).

PINNING

SYMBOL	PIN DIL 18	PIN SO16	PIN SO20/SSOP20	DESCRIPTION
PD	1	1	1	charge-pump output
Q1	2	2	2	crystal oscillator input 1
Q2	3	3	3	crystal oscillator input 2
n.c.			4	not connected
SDA	4	4	5	serial data input/output
SCL	5	5	6	serial clock input
P7	6	6	7	port output/input (general purpose)
n.c.			8	not connected
P6	7	7	9	port output/input for general purpose ADC
P5	8	8	10	port output/input (general purpose)
P4	9	9	11	port output/input (general purpose)
P3	10	10	12	port output/input for address selection
P2	11	11	13	port output
P1	12		14	port output
P0	13		15	port output
V_{CC}	14	12	16	voltage supply
RF_{IN1}	15	13	17	UHF/VHF signal input 1
RF_{IN2}	16	14	18	UHF/VHF signal input 2 (decoupled)
V_{EE}	17	15	19	GND
UD	18	16	20	drive output

FUNCTIONAL DESCRIPTION

The TSA5512 is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode : R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the TSA5512. The bus transceiver has an auto-increment facility which permits the programming of the TSA5512 within one single transmission (address + 4 data bytes).

The TSA5512 can also be partially programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purpose. At power-on the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of UHF/VHF signal is first divided by 8 the step size is 62.5 kHz. A 3.2 MHz crystal can offer step sizes of 50 kHz.

Table 1 Write data format

	MSB							**LSB**		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
Output ports control bits	P7	P6	P5	P4	P3	P2	P1*	P0*	A	byte 5

note

* not valid for TSA5512T.

MA1, MA0 programmable address bits (see Table 4)

A acknowledge bit

N14 to N0 programmable divider bits

$N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + N0$

CP charge-pump current

CP = 0 50 µA

CP = 1 220 µA

P7 to P0 = 1 open-collector output is active

P7 to P0 = 0 output are in high impedance state

T1, T0, OS = 0 0 0 normal operation

T1 = 1 P6 = f_{ref}, P7 = f_{DIV}

T0 = 1 3-state charge-pump

OS = 1 operational amplifier output is switched off (varicap drive disable)

FUNCTIONAL DESCRIPTION (continued)

READ mode : R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5512 by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5512 generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.
A second data byte can be read out of the TSA5512 if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs.
The TSA5512 will then release the data line to allow the processor to generate a STOP condition.
When ports P3 to P7 are used as inputs, they must be programmed in their high-impedance state.
The POR flag (power-on-reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5512 (end of a READ sequence).
Control of the loop is made possible with the in-lock flag FL which indicates (FL = 1) when the loop is phase-locked. The bits I2, I1 and I0 represent the status of the I/O ports P7, P5 and P4 respectively. A logic 0 indicates a LOW level and a logic 1 a HIGH level (TTL levels).
A built-in 5-level ADC is available on I/O port P6. This converter can be used to feed AFC information to the controller from the IF section of the television as illustrated in the typical application circuit in Fig.8. The relationship between bits A2, A1 and A0 and the input voltage on port P6 is given in Table 3.

Table 2 Read data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	–	byte 2

POR	power-on-reset flag. (POR = 1 on power-on)
FL	in-lock flag (FL = 1 when the loop is phase-locked)
I2, I1, I0	digital information for I/O ports P7, P5 and P4 respectively
A2, A1, A0	digital outputs of the 5-level ADC. Accuracy is 1/2 LSB (see Table 3)

MSB is transmitted first.

Address selection

The module address contains programmable address bits (MA1 and MA0) which together with the I/O port P3 offers the possibility of having several synthesizers (up to 3) in one system.
The relationship between MA1 and MA0 and the input voltage I/O port P3 is given in Table 4.

Table 3 A/D converter levels

Voltage applied on the port P6	A2	A1	A0
0.6 V_{CC} to 13.5 V	1	0	0
0.45 V_{CC} to 0.6 V_{CC}	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V	0	0	0

Table 4 Address selection

MA1	MA0	Voltage applied on port P3
0	0	0 to 0.1 V_{CC}
0	1	always valid
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6	V
V_1	charge-pump output voltage	−0.3	V_{CC}	V
V_2	crystal (Q1) input voltage	−0.3	V_{CC}	V
V_4	serial data input/output	−0.3	6	V
V_5	serial clock input	−0.3	6	V
V_{6-13}	P7 to P1 I/O voltage	−0.3	+16	V
V_{15}	prescaler input	−0.3	V_{CC}	V
V_{18}	drive output voltage	−0.3	V_{CC}	V
I_6	P7 to P0 output current (open collector)	−1	15	mA
I_4	SDA output current (open collector)	−1	5	mA
T_{stg}	storage temperature range (IC)	−40	+150	°C
T_j	maximum junction temperature	−	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air (DIL18)	−	80	K/W
	from junction to ambient in free air (SO16)	−	110	K/W
	from junction to ambient in free air (SO20)	−	80	K/W
	from junction to ambient in free air (SSOP20)	−	120	K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified
All pin numbers refer to DIL 18 version

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Functional range						
V_{CC}	supply voltage range		4.5	–	5.5	V
T_{amb}	operating ambient temperature range		–10	–	80	°C
f_{CLK}	clock input frequency		64	–	1300	MHz
N	divider		256	–	32767	
I_{CC}	supply current		25	35	50	mA
f_{XTAL}	crystal oscillator		3.2	4	4.48	MHz
Z_I	input impedance (pin 2)		–480	–400	–320	Ω
	input level	V_{CC} = 4.5 V to 5.5 V; T_{amb} = –10 to 80 °C; see typical sensitivity curve in Fig.5.				
	f = 80 to 150 MHz		12/–25	–	300/2.6	mV/dBm
	f = 150 to 1000 MHz		9/–28	–	300/2.6	mV/dBm
	f = 1000 to 1300 MHz		40/–15	–	300/2.6	mV/dBm
R_I	prescaler input resistance see SMITH chart in Fig.6		–	50	–	Ω
Output ports (open collector) P0-P7 (see note 1)						
I_{LO}	leakage current	V_{13} = 13.5 V	–	–	10	µA
V_{OL}	output voltage LOW	I_{13} = 5 mA; note 2	–	–	0.7	V
Input P3						
I_{OH}	input current HIGH	V_{OH} = 13.5 V	–	–	10	µA
I_{OL}	input current LOW	V_{OL} = 0 V	–10	–	–	µA
Input ports P4-5, P7						
V_{IL}	input voltage LOW		–	–	0.8	V
V_{IH}	input voltage HIGH		2.7	–	–	V
I_{IH}	input current HIGH	V_6 = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_6 = 0 V	–10	–	–	µA
Input port P6						
I_{IH}	input current HIGH	V_7 = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_7 = 0 V	–10	–	–	µA
SCL and SDA inputs						
V_{IH}	input voltage HIGH		3.0	–	5.5	V
V_{IL}	input voltage LOW		–	–	1.5	V
I_{IH}	input current HIGH	V_5 = 5 V, V_{CC} = 0 V; V_5 = 5 V, V_{CC} = 5 V	– –	– –	10 10	µA µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	input current LOW	V_5 = 0 V, V_{CC} = 0 V; V_5 = 0 V, V_{CC} = 5 V	−10 −10	– –	– –	µA µA
Output SDA (open collector)						
I_{LO}	leakage current	V_4 = 5.5 V	–	–	10	µA
V_4	output voltage	I_4 = 3 mA	–	–	0.4	V
Charge-pump output PD						
I_{IH}	input current HIGH (absolute value)	CP = 1	90	220	300	µA
I_{IL}	input current LOW (absolute value)	CP = 0	22	50	75	µA
V_O	output voltage	in-lock	1.5	–	2.5	V
I_{1leak}	off-state leakage current	T0 = 1	−5	–	5	nA
Operational amplifier output UD (test mode: T0 = 1)						
V_{18}	output voltage	V_{IL} = 0 V	–	–	100	mV
V_{18}	output voltage when switched-off	OS = 1; V_{IL} = 2 V	–	–	200	mV
G	operational amplifier current gain; $I_{18}/(I_1 - I_{1leak})$	OS = 0; V_{1L} = 2 V; I_{18} = 10 µA	2000	–	–	

Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with all open-collector ports active.

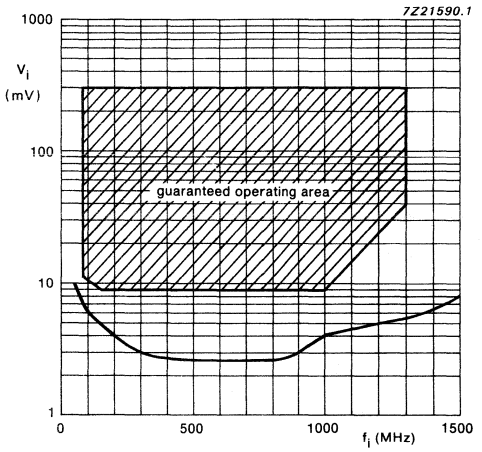


Fig.5 Prescaler typical input sensitivity curve; V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to +80 °C.

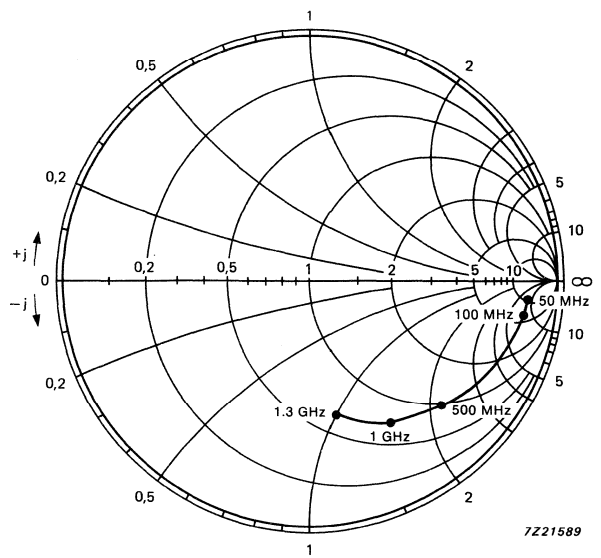


Fig.6 Prescaler Smith chart of typical input impedance; V_{CC} = 5 V; reference value = 50 Ω.

FLOCK FLAG DEFINITION FL

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm (K_{VCO} / K_O) \times I_{CP} \times (C1 + C2)/(C1 \times C2)$$

where:

K_{VCO}	=	oscillator slope (Hz/V)
I_{CP}	=	charge-pump current (A)
K_O	=	4 x 10E6
C1 and C2	=	loop filter capacitors

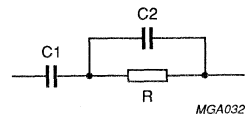


Fig.7 Loop filter.

FLOCK FLAG APPLICATION

- K_{VCO} = 16 MHz/V (UHF band)
- I_{CP} = 220 μA
- C1 = 180 nF
- C2 = 39 nF
- Δf = ± 27.5 kHz

Table 5 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	μs
Time span between the loop losing lock and FL-flag resetting	0	128	μs

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

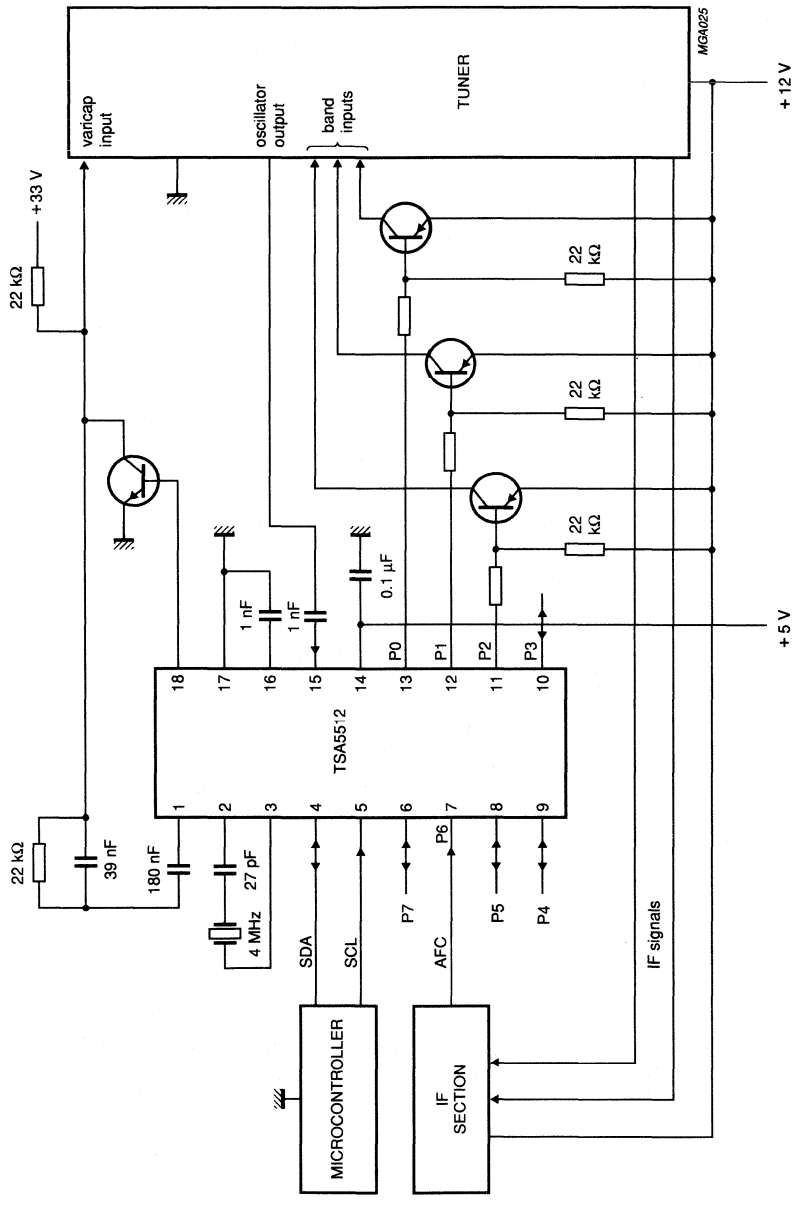


Fig.8 Typical application (DIL18).

1.3 GHz bi-directional I²C-bus controlled synthesizer

TSA5515T

GENERAL DESCRIPTION

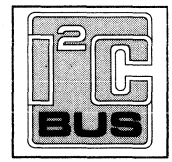
The TSA5515T is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the three output ports and set the charge-pump current. A flag is set when the loop is "in-lock". Another flag is set when a power dip occurs on the supply line. These flags are read out of the TSA5515T on SDA line (one status byte) during a READ operation. The device has 4 programmable addresses, programmed by applying a specific voltage on the AS pin. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

FEATURES

- Complete 1.3 GHz single-chip system
- Low power 5 V, 35 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner, etc.
- 3 bus-controlled output ports
- Power-down flag
- Available in SOT108A package

APPLICATIONS

- TV tuners
- VCR tuners



QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δf	frequency range	64	–	1300	MHz
$V_{I\ (RMS)}$	input voltage level (RMS value)				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator	3.2	4	4.48	MHz
I_O	open–collector output current				
	P7	–	–	5	mA
	P1, P2	–	–	20	mA
T_{amb}	operating ambient temperature range	–10	–	80	°C
T_{stg}	storage temperature range	–40	–	125	°C
$R_{th\ j\text{-}a}$	thermal resistance	–	110	–	K/W

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5515T	14	SO	plastic	SOT108A

1.3 GHz bi-directional I²C-bus controlled synthesizer

TSA5515T

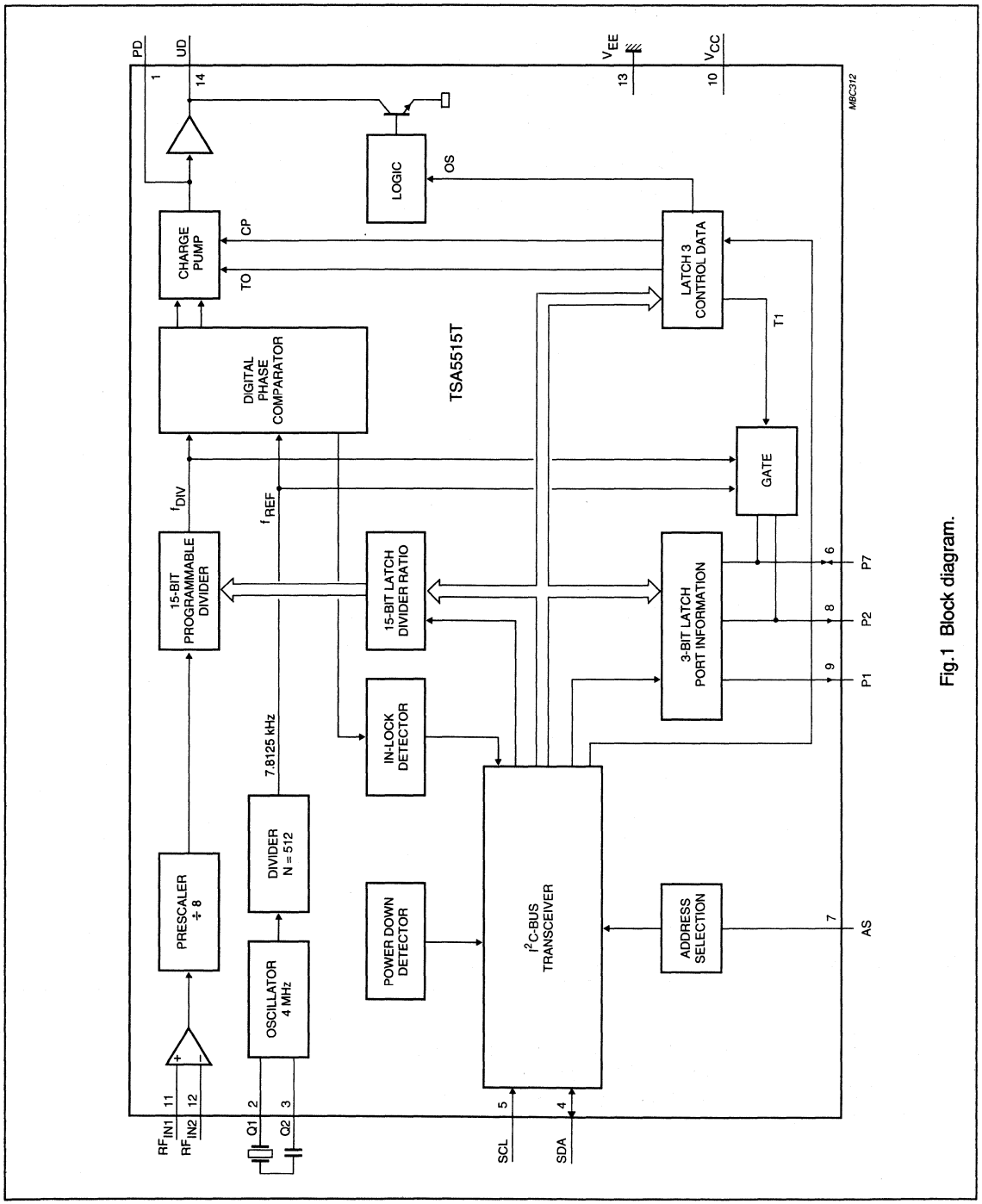


Fig.1 Block diagram.

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6	V
V_{P1}	charge-pump output voltage	−0.3	V_{CC}	V
V_{P2}	crystal (Q1) input voltage	−0.3	V_{CC}	V
V_{P4}	serial data input/output	−0.3	6	V
V_{P5}	serial clock input	−0.3	6	V
V_{P7}	address selection	−0.3	6	V
V_{P6}	output ports P7, P2, P1	−0.3	16	V
V_{P11}	prescaler inputs	−0.3	2.5	V
V_{P14}	drive output	−0.3	V_{CC}	V
I_{6L}	output port P7 (open collector)	−1	10	mA
I_{8L}	output port P2, P1 (open collector)	−1	25	mA
I_{4L}	SDA output (open collector)	−1	5	mA
T_{stg}	storage temperature range	−40	125	°C
T_j	junction temperature	−	125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	110 K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C, category A (> 1500 V).

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

1.3 GHz bi-directional I²C-bus controlled synthesizer

TSA5515T

PINNING

SYMBOL	PIN	DESCRIPTION
PD	1	charge-pump output
Q1	2	crystal oscillator input 1
Q2	3	crystal oscillator input 2
SDA	4	serial data input/output
SCL	5	serial clock input
P7	6	port output
AS	7	input for address selection
P2	8	port output
P1	9	port output
V_{CC}	10	voltage supply
RF_{IN1}	11	UHF/VHF signal input 1
RF_{IN2}	12	UHF/VHF signal input 2 (decoupled)
GND	13	ground
UD	14	drive output

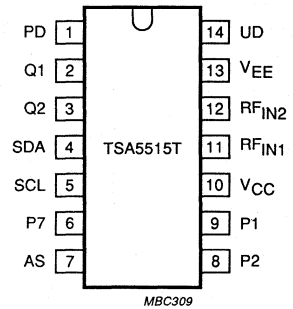


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TSA5515T is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode :
R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the TSA5515T. The bus transceiver has an auto-increment facility, which permits the programming of the TSA5515T within one single transmission (address + 4 data bytes).

The TSA5515T can also be partly programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning. At power-on, the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of the UHF/VHF signal is first divided by 8, the step size is 62.5 kHz. A 3.2 MHz crystal can offer a step size of 50 kHz.

Table 1 Write data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	X	X	X	OS	A	byte 4
Output ports control bits	P7	X	X	X	X	P2	P1	X	A	byte 5

MA1, MA0 programmable address bits (see Table 3)

A acknowledge bit

N14 to N0 programmable divider bits

$N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + N0$

CP charge-pump current

CP = 0 50 µA

CP = 1 220 µA

P7, P2, P1 = 1 open-collector outputs are active

P7, P2, P1 = 0 outputs are in high impedance state

T1, T0, OS = 0 0 0 normal operation

T1 = 1 P2 = f_{ref}, P7 = f_{DIV}

T0 = 1 3-state charge-pump

OS = 1 operational amplifier output is switched off (varicap drive disable)

X don't care.

READ mode :
R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5515T by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5515T generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.

A second data byte can be read out of the TSA5515T if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs.The TSA5515T will then release the data line to allow the processor to generate a STOP condition.

The POR flag (power-on-reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5515T (end of a READ sequence). Control of the loop is made possible with the in-lock flag FL, which indicates (FL = 1) when the loop is phase-locked.

Table 2 Read data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	1	1	1	1	1	1	–	byte 2

POR power-on-reset flag. (POR = 1 on power-on)

FL in-lock flag (FL = 1 when the loop is phase-locked).

MSB is transmitted first.

Address selection (see Table 3)

The module address contains programmable address bits (MA1 and MA0), which offer the possibility of having several synthesizers (up to 4) in one system. The relationship between MA1 and MA0 and the input voltage on AS input is given in Table 3.

Table 3 Address selection

MA1	MA0	Voltage applied on AS pin
0	0	0 to 0.1 V_{CC}
0	1	open
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to V_{CC}

1.3 GHz bi-directional I²C-bus controlled synthesizer

TSA5515T

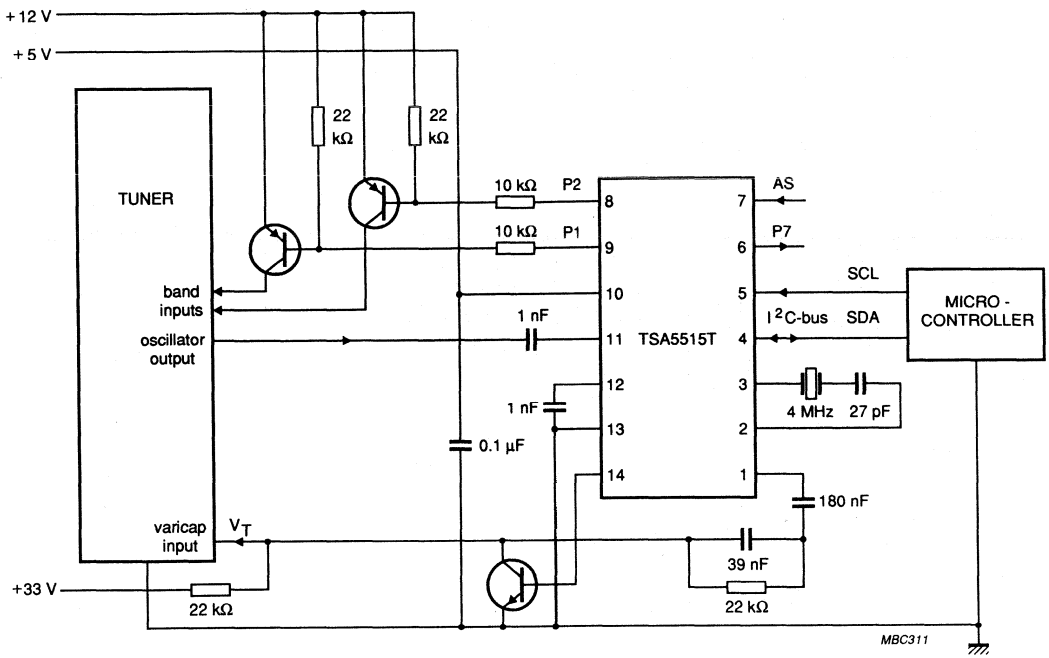


Fig.3 Typical application diagram.

CHARACTERISTICS

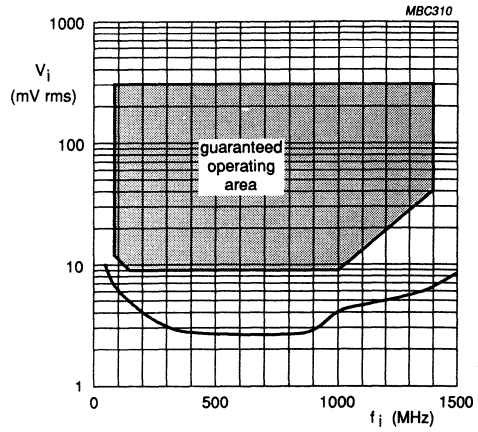
V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage range		4.5	–	5.5	V
T_{amb}	operating ambient temperature range		−10	–	80	°C
f_{CLK}	clock input frequency range		64	–	1300	MHz
N	divider		256	–	32767	
I_{CC}	supply current		25	35	50	mA
f_{XTAL}	crystal oscillator frequency		3.2	4	4.48	MHz
Z_I	input impedance (pin 2)		−480	−400	−320	Ω
$V_{I\ (RMS)}$	input voltage level (RMS value)	V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to 80 °C see typical sensitivity curve in Fig. 4				
	f = 80 to 150 MHz		12	–	300/2.6	mV
	f = 150 to 1000 MHz		9	–	300/2.6	mV
	f = 1000 to 1300 MHz		40	–	300/2.6	mV
R_I	prescaler input impedance	see Smith chart in Fig. 5	–	50	–	Ω
C_I	input capacitance		–	2	–	pF
Output ports (open collector) (see note 1)						
I_{LO}	leakage current	V_{6H} = 13.5 V	–	–	10	µA
V_{OL}	output voltage LOW (P7)	I_{6L} = 5 mA note 2	–	–	0.5	V
	output voltage LOW (P2, P1)	I_{8L} = 20 mA note 2	–	–	0.5	V
Address selection input (AS)						
I_{IH}	input current HIGH	V_{7H} = 5 V	–	–	20	µA
I_{IL}	input current LOW	V_{7L} = 0	−20	–	–	µA
Bus inputs SCL, SDA						
V_{IH}	input voltage HIGH		3	–	5.5	V
V_{IL}	input voltage LOW		–	–	1.5	V
I_{IH}	input current HIGH	V_{5H} = 5 V; V_{CC} = 0	–	–	10	µA
		V_{5H} = 5 V; V_{CC} = 5 V	–	–	10	µA
I_{IL}	input current LOW	V_{5L} = 0; V_{CC} = 0	−10	–	–	µA
		V_{5L} = 0; V_{CC} = 5 V	−10	–	–	µA
Output SDA (open collector)						
I_{LO}	leakage current	V_{4H} = 5.5 V	–	–	10	µA
V_{4L}	output voltage	I_{4L} = 3 mA	–	–	0.4	V
V_{14}	output voltage	V_{1L} = 0	–	–	100	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge-pump output PD						
I_{IH}	input current HIGH (absolute value)	CP = 1	90	220	300	µA
I_{IL}	input current LOW (absolute value)	CP = 0	22	50	75	µA
V_O	output voltage	in-lock	1.5	–	2.5	V
I_{1leak}	off-state leakage current	T0 = 1	–5	–	5	nA
Operational amplifier output UD (test mode: T0 = 1)						
V_{14}	output voltage	V_{1L} = 0	–	–	100	mV
	output voltage when switched off	T0 = 1; OS = 1; V_{1L} = 2 V	–	–	200	mV
h_{FE}	operational amplifier current gain $I_{14}/(I_1 - I_{1leak})$	T0 = 1; OS = 0; V_{1L} = 2 V; I_{14} = 10 µA	2000	–	–	

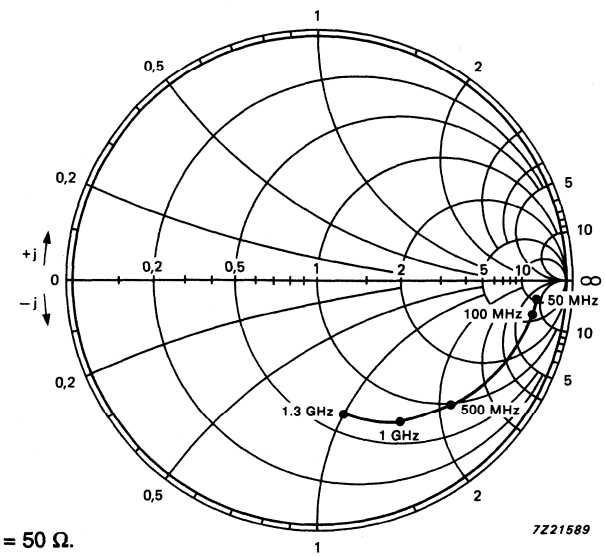
Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. A maximum of 1 port at the same time may sink 5 or 20 mA, to guarantee V_O = 0.5 V.



V_{CC} = 4.5 to 5.5 V; T_{amb} = −10 to 80 °C.

Fig.4 Prescaler typical input sensitivity curve.



V_{CC} = 5 V; reference value = 50 Ω.

Fig.5 Prescaler Smith chart of typical input impedance.

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm (K_{VCO} / K_O) \times I_{CP} \times (C1 + C2)/(C1 \times C2)$$

where:

K_{VCO} = oscillator slope (Hz/V)
I_{CP} = charge-pump current (A)
K_O = 4 x 10^6
C1 and C2 = loop filter capacitors.

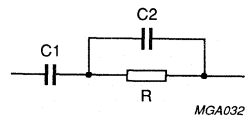


Fig.6 Loop filter.

FLOCK FLAG APPLICATION

- K_{VCO} = 16 MHz/V (UHF band)
- I_{CP} = 220 μA
- C1 = 180 nF
- C2 = 39 nF
- Δf = ±27.5 kHz.

Table 4 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	μs
Time span between the loop losing lock and FL-flag resetting	0	128	μs

Differential video amplifier — μA733/733C

DESCRIPTION

The 733 is a monolithic differential input, differential output, wide-band video amplifier. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth, and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter-follower outputs to the inputs of the second stage. The emitter-follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high-performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

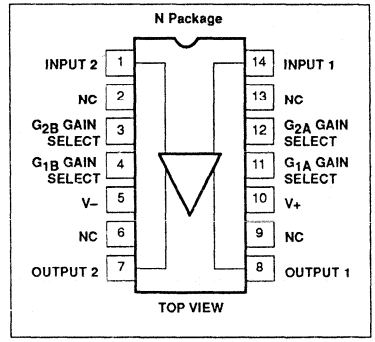
FEATURES

- 120MHz bandwidth
- 250kΩ input resistance
- Selectable gains of 10, 100, and 400
- No frequency compensation required
- MIL-STD-883A, B, C available

APPLICATIONS

- Video amplifier
- Pulse amplifier in communications
- Magnetic memories
- Video recorder systems

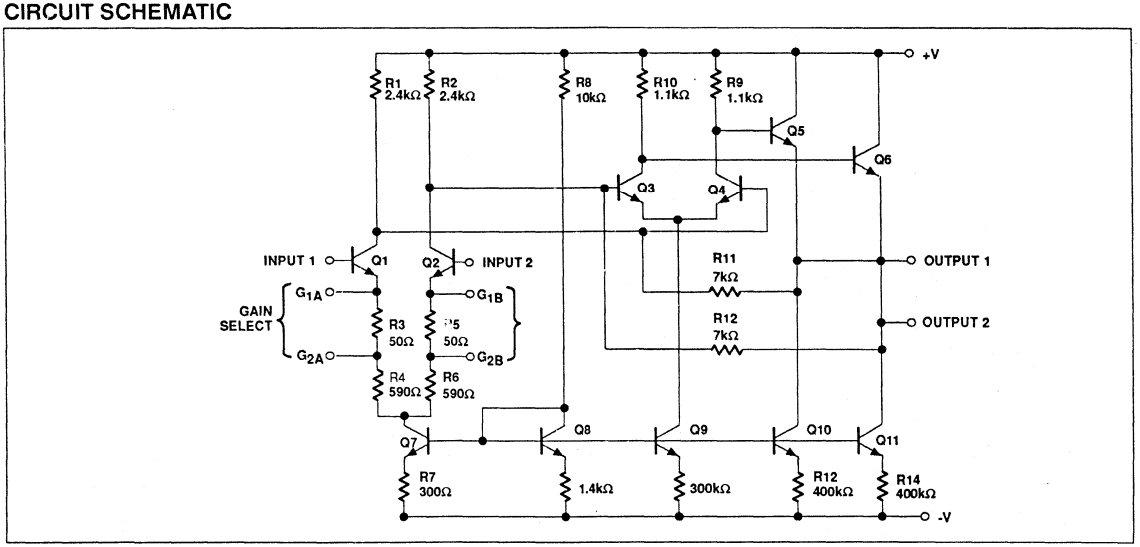
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE
14-Pin Plastic DIP	-55°C to +125°C	μA733N
14-Pin Plastic DIP	0 to +70°C	μA733CN

CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DIFF}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
V_{CC}	Supply voltage	±8	V
I_{OUT}	Output current	10	mA
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range		
	µA733C	0 to +70	°C
	µA733	-55 to +125	°C
$P_{D\ MAX}$	Maximum power dissipation, 25°C ambient temperature (still-air)[1]	1420	mW

NOTE:
1. The following derating factors should be applied 25°C:
   N package at 11.4mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C, V_S=±6V, V_{CM}=0, unless otherwisespecified. Recommended operating supply voltages V_S=±6.0V.

SYMBOL	PARAMETER	TEST CONDITIONS	µA733C			µA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Differential voltage gain	R_l = 2kΩ, V_{OUT} = $3V_{P-P}$							
	Gain 1[2]		250	400	600	300	400	500	V/V
	Gain 2[2]		80	100	120	90	100	110	V/V
	Gain 3[3]		8	10	12	9	10	11	V/V
BW									
	Gain 1[1]			40			40		MHz
	Gain 2[2]			90			90		MHz
	Gain 3[3]			120			120		MHz
t_R		V_{OUT} = $1V_{P-P}$							
	Gain 1[1]			10.5			10.5		ns
	Gain 2[2]			4.5	12		4.5	10	ns
	Gain 3[3]			2.5			2.5		ns
t_{PD}		V_{OUT} = $1V_{P-P}$							
	Gain 1[1]			7.5			7.5		ns
	Gain 2[2]			6.0	10		6.0	10	ns
	Gain 3[3]			3.6			3.6		ns
R_{IN}									
	Gain 1[2]			4.0			4.0		kΩ
	Gain 2[2]		10	30		20	30		kΩ
	Gain 3[3]			250			250		kΩ
	Input capacitance[2]	Gain 2		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	µA
I_{BIAS}	Input bias current			9.0	30		9.0	20	µA
V_{NOISE}	Input noise voltage	BW=1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR									
	Gain 2	V_{CM}=±1V, f≤100kHz	60	86		60	86		dB
	Gain 2	V_{CM}=±1V, f=5MHz		60			60		dB

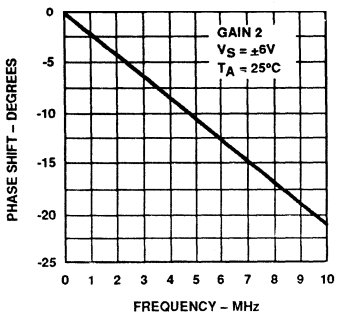
DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	µA733C			µA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
SVRR	Supply voltage rejection ratio Gain 2	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
	Output offset voltage	$R_L = \infty$							
	Gain 1[1]			0.6	1.5		0.6	1.5	V
	Gain 2 and 3[2, 3]			0.35	1.5		0.35	1.0	V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
	Output voltage swing, differential	R_L=2kΩ	3.0	4.0		3.0	4.0		V_{P-P}
I_{SINK}	Output sink current		2.5	3.6		2.5	3.6		mA
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER TEMPERATURE			**0°C ≤ T_A ≤ 70°C**			**-55°C ≤ T_A ≤ 125°C**			
	Differential voltage gain	R_l = 2kΩ, V_{OUT} = $3V_{P-P}$							
	Gain 1[1]		250		600	200		600	V/V
	Gain 2[2]		80		120	80		120	V/V
	Gain[3]		8		12	8		12	V/V
R_{IN}	Input resistance								
	Gain 2[2]		8			8			kΩ
I_{OS}	Input offset current				6			5	µA
I_{BIAS}	Input bias current				40			40	µA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2	V_{CM}=±V, F≤100kHz	50			50			dB
SVRR	Supply voltage rejection ratio								
	Gain 2	ΔV_S=±0.5V	50			50			dB
V_{OS}	Output offset voltage	$R_L = \infty$							
	Gain 1[1]				1.5			1.5	V
	Gain 2 and 3[2, 3]				1.5			1.2	V
V_{DIFF}	Output voltage swing, differential	R_L = 2kΩ	2.8			2.5			V_{P-P}
I_{SINK}	Output sink current		2.5			2.2			mA
I_{CC}	Power supply current	$R_L \pm \infty$			27			27	mA

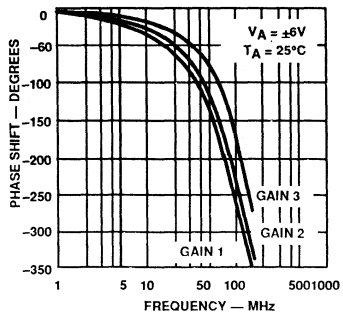
NOTES:
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

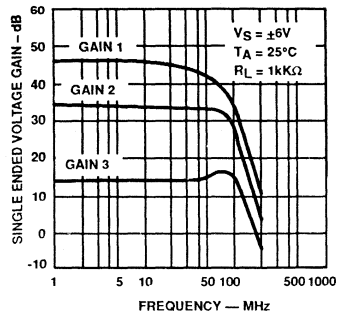
Phase Shift as a Function of Frequency



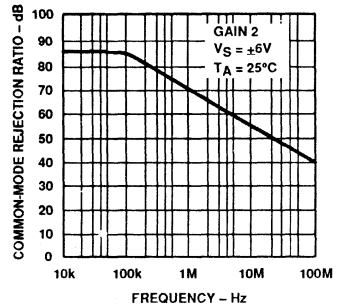
Phase Shift as a Function of Frequency



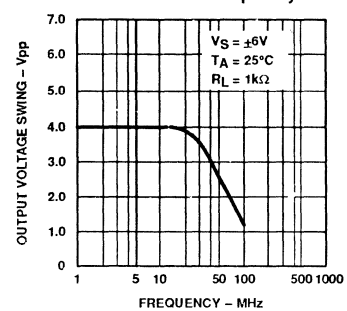
Voltage Gain as a Function of Temperature



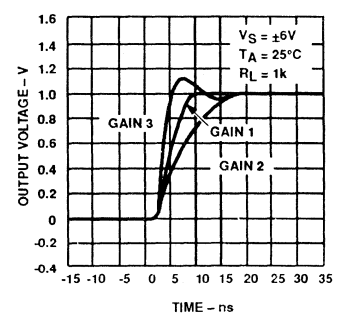
Common-Mode Rejection Ratio as a Function of Frequency



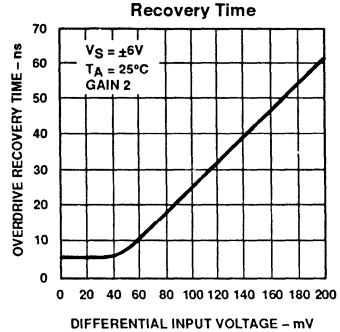
Output Voltage Swing as a Function of Frequency



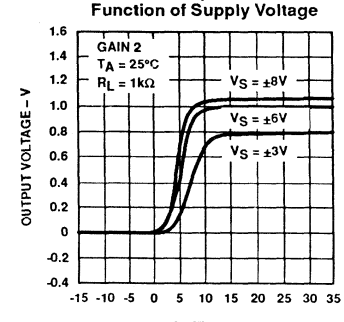
Pulse Response



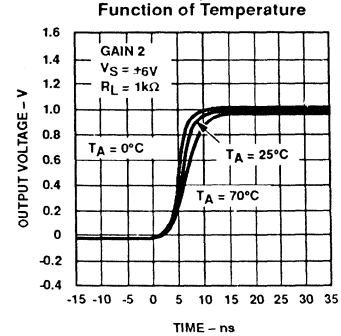
Differential Overdrive Recovery Time



Pulse Response as a Function of Supply Voltage

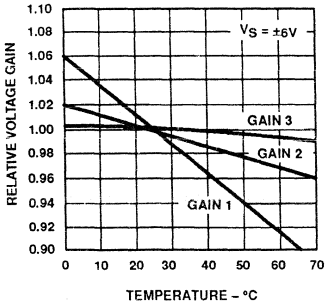


Pulse Response as a Function of Temperature

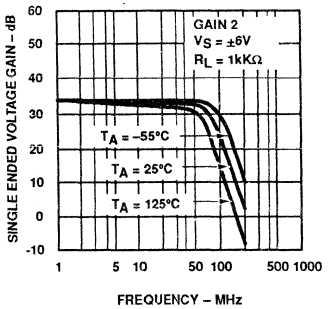


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

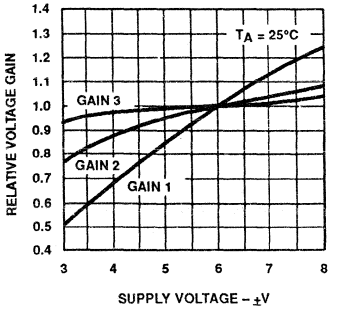
Voltage Gain as a Function of Temperature



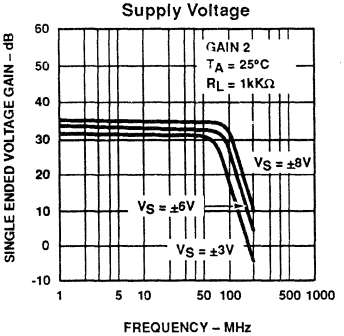
Gain vs. Frequency as a Function of Temperature



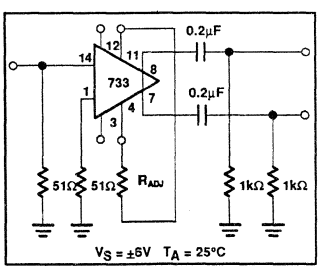
Voltage Gain as a Function of Supply Voltage



Gain vs. Frequency as a Function of Supply Voltage

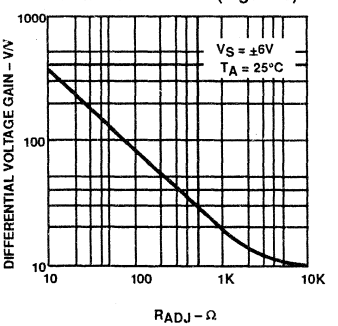


Voltage Gain Adjust Circuit

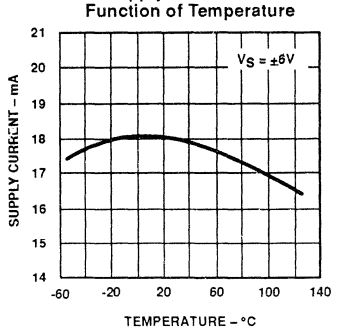


(Pin numbers apply to K Package)

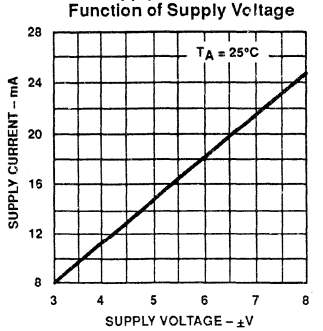
Voltage Gain as a Function of RADJ (Figure 3)



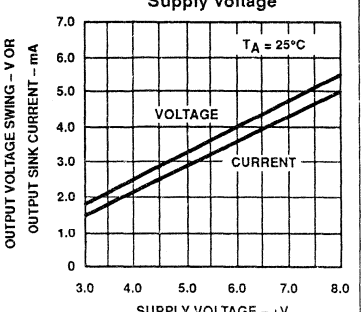
Supply Current as a Function of Temperature



Supply Current as a Function of Supply Voltage

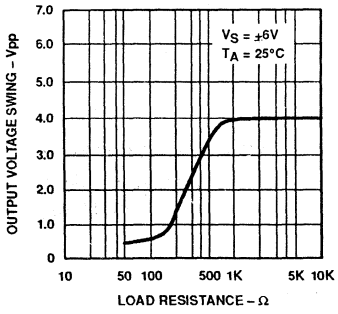


Output Voltage and Current Swing as a Function of Supply Voltage

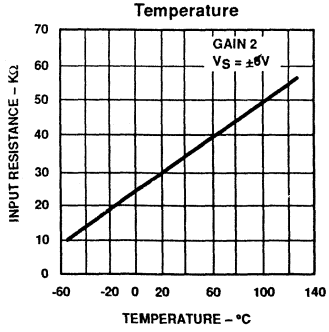


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

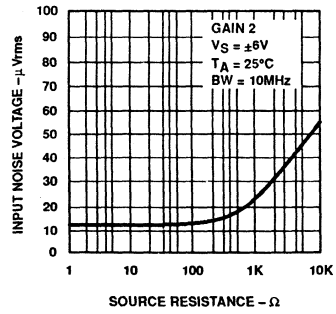
Output Voltage Swing as a Function of Load Resistance



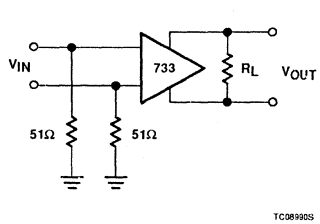
Input Resistance as a Function of Temperature

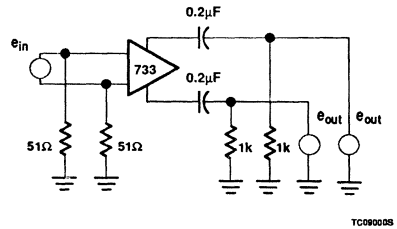


Input Noise Voltage as a Function of Source Resistance



TEST CIRCUITS T_A=25°C, unless otherwise specified.

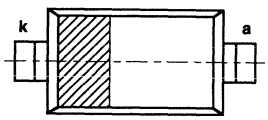




PACKAGE INFORMATION
Package outlines
Soldering

Package outlines IC02

PACKAGE OUTLINES



MSB045

MBB206

Fig.1 SOD123.

Package outlines IC02

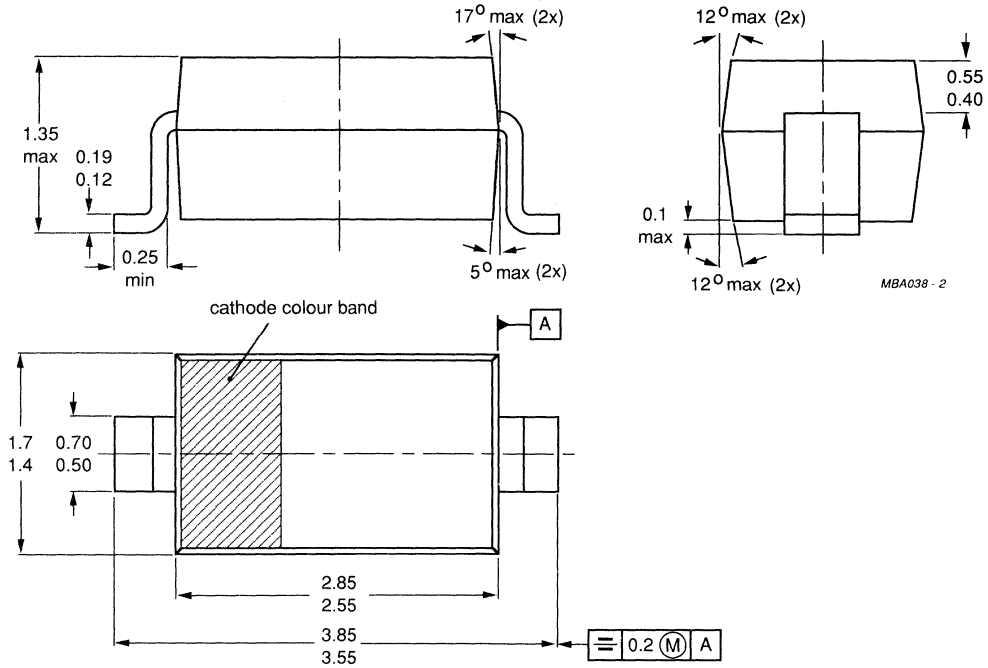
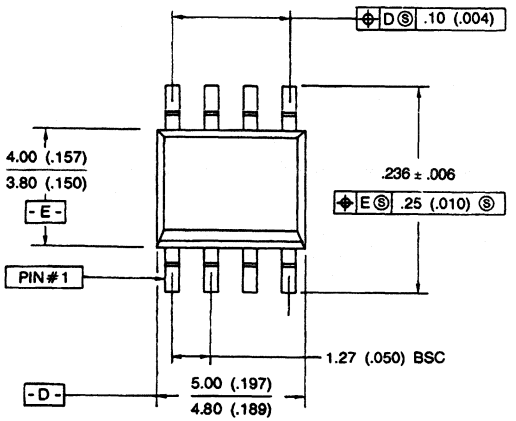
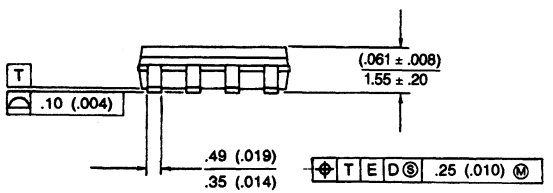
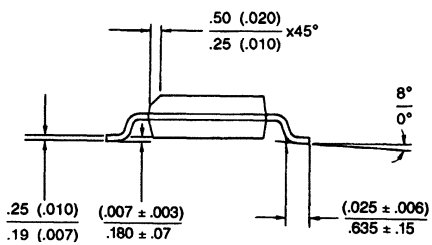


Fig.2 SOD323.

Package outlines IC02







853-0174 88070

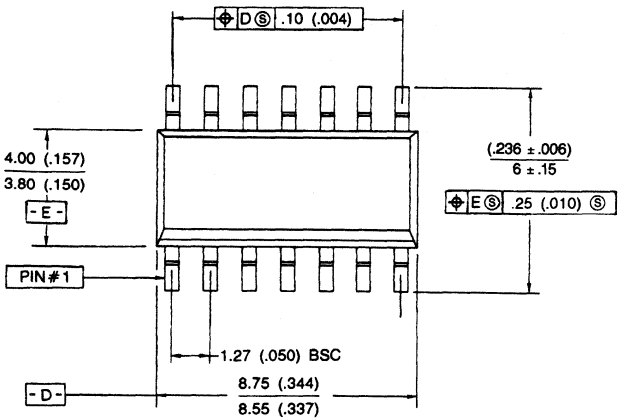
PO00273S

NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

Fig.3 8-pin plastic SO (D package).

Package outlines IC02



NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

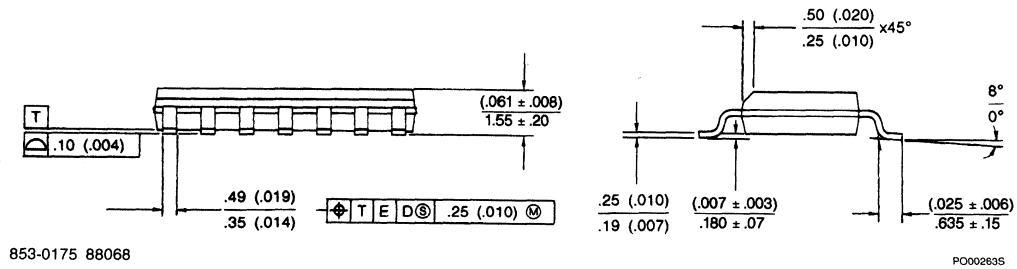
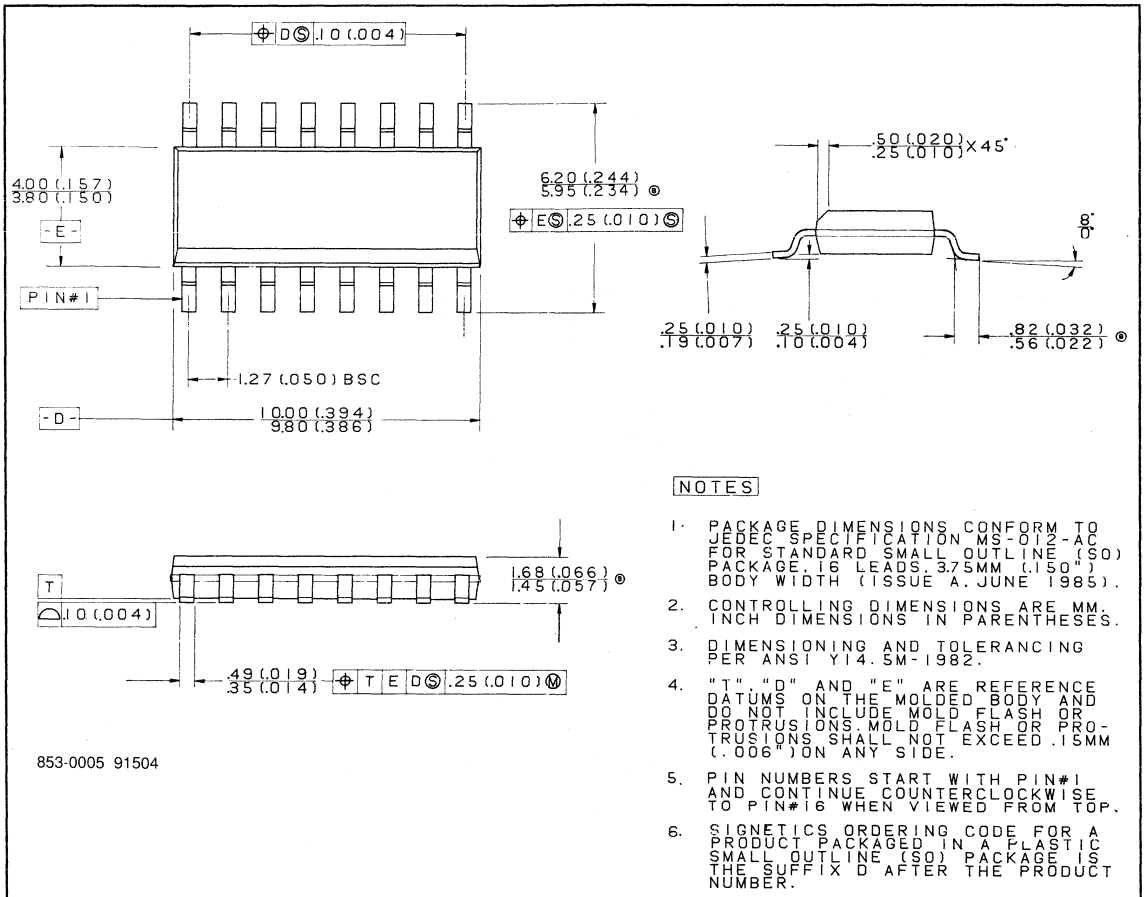


Fig.4 14-pin plastic SO (D package).

Package outlines IC02



NOTES

1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-012-AC FOR STANDARD SMALL OUTLINE (SO) PACKAGE, 16 LEADS, 3.75MM (.150") BODY WIDTH (ISSUE A, JUNE 1985).
2. CONTROLLING DIMENSIONS ARE MM. INCH DIMENSIONS IN PARENTHESES.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T", "D" AND "E" ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15MM (.006") ON ANY SIDE.
5. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#16 WHEN VIEWED FROM TOP.
6. SIGNETICS ORDERING CODE FOR A PRODUCT PACKAGED IN A PLASTIC SMALL OUTLINE (SO) PACKAGE IS THE SUFFIX D AFTER THE PRODUCT NUMBER.

Fig.5 16-pin plastic SO (D package).

Package outlines IC02

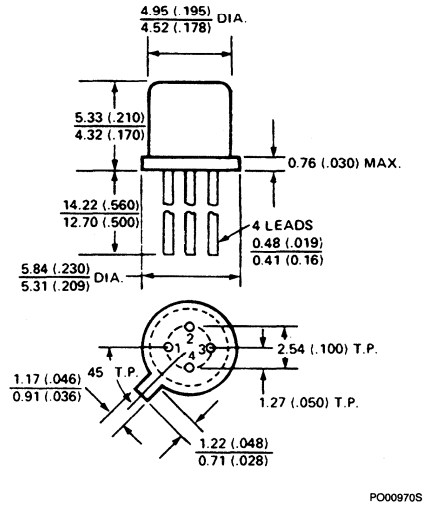
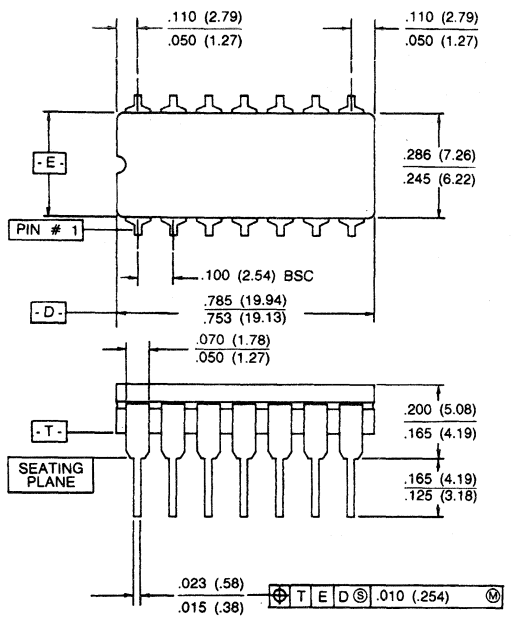


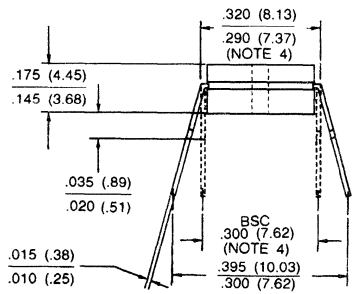
Fig.6 4-pin hermetic TO-72 header (E package).

Package outlines IC02



NOTES:

1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

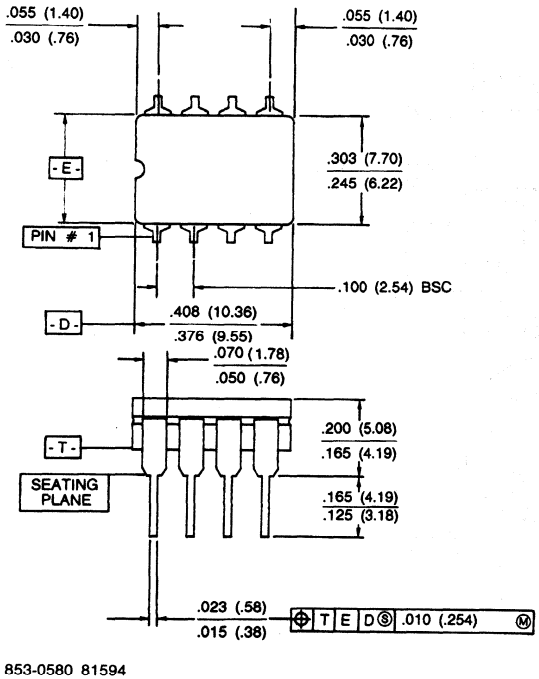


853-0581 81594

PO00440S

Fig.7 14-pin cerdip (F package).

Package outlines IC02



NOTES:

1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

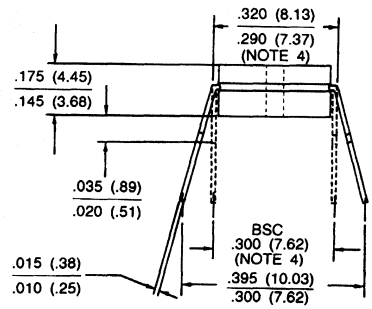


Fig.8 8-pin cerdip (FE package).

Package outlines IC02

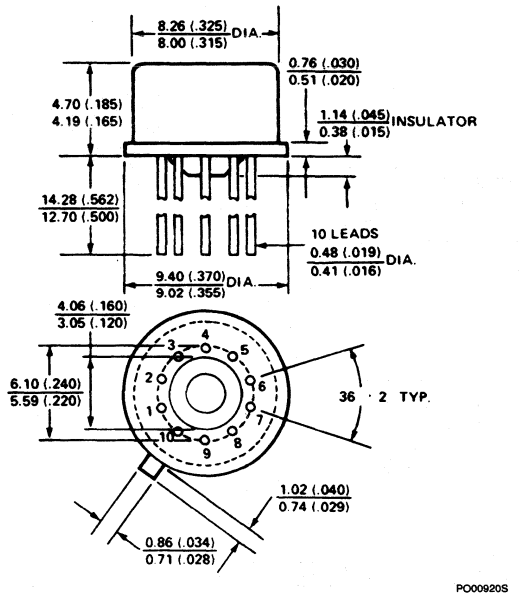


Fig.9 10-pin hermetic TO-5/100 header short can (H package).

Package outlines IC02

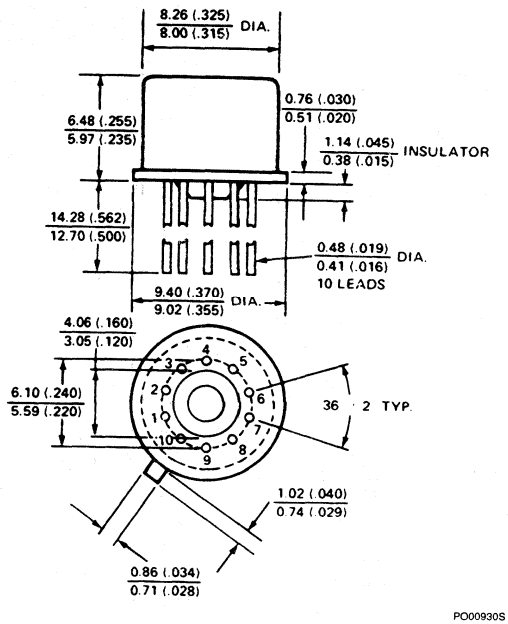
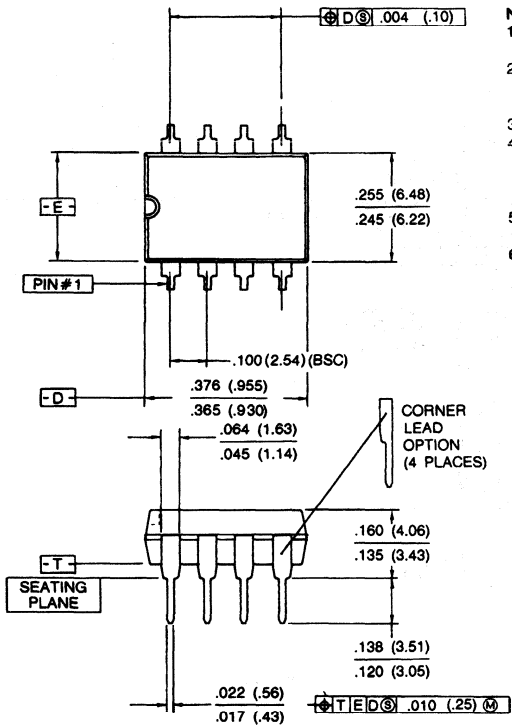
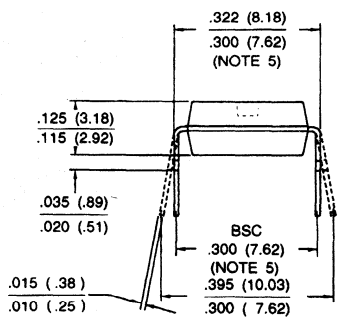


Fig.10 10-pin hermetic TO-5/100 header tall can (H package).

Package outlines IC02





853-0404 81230

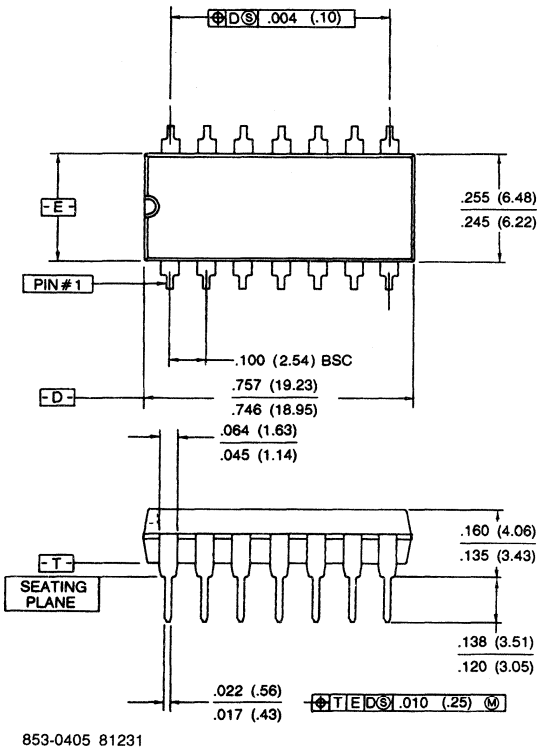
PO00312S

NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

Fig.11 8-pin plastic PDIP (N package).

Package outlines IC02



NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

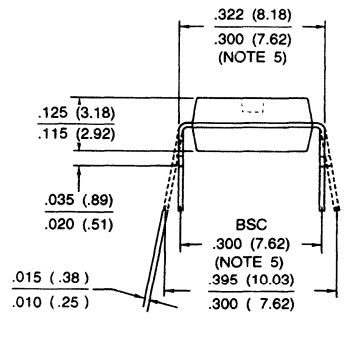
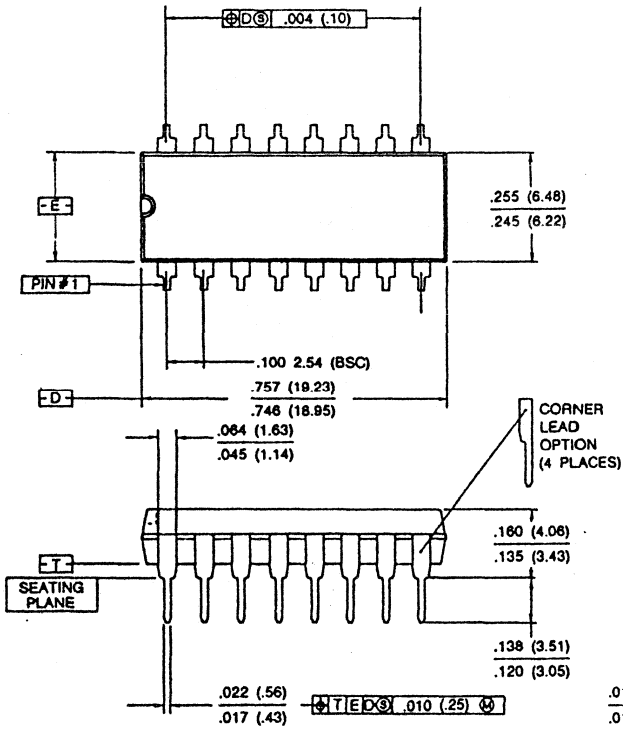


Fig.12 14-pin plastic DIP (N package).

Package outlines IC02

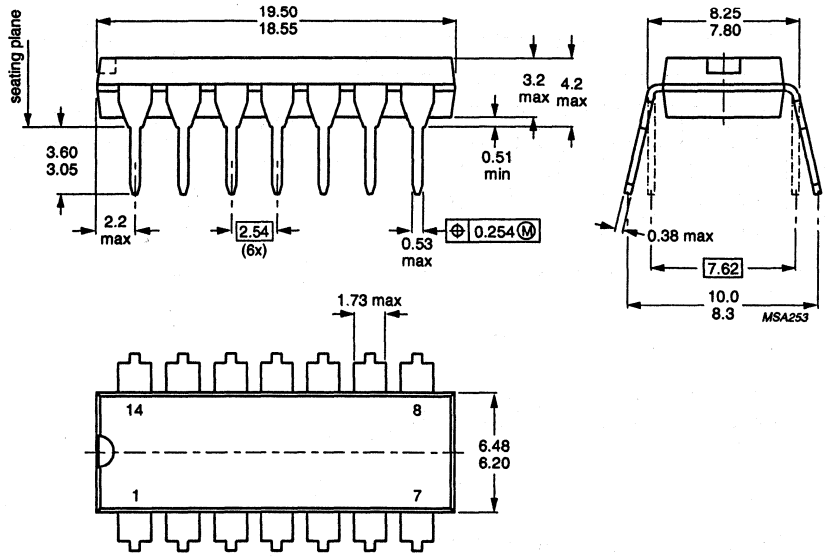


NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

Fig.13 NJ1 16-pin plastic PDIP.

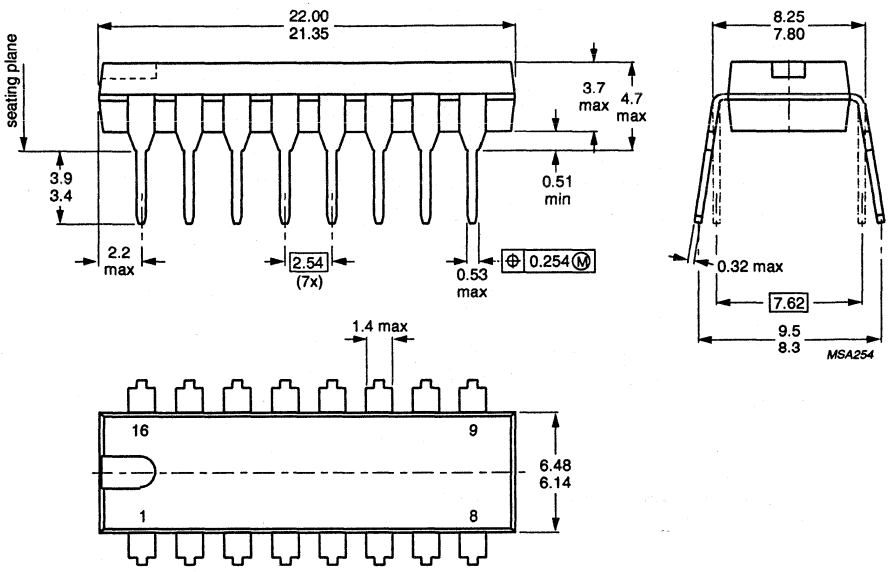
Package outlines IC02



Dimensions in mm.

Fig.14 plastic DIL, 14-pin (DIL14) (SOT27MF).

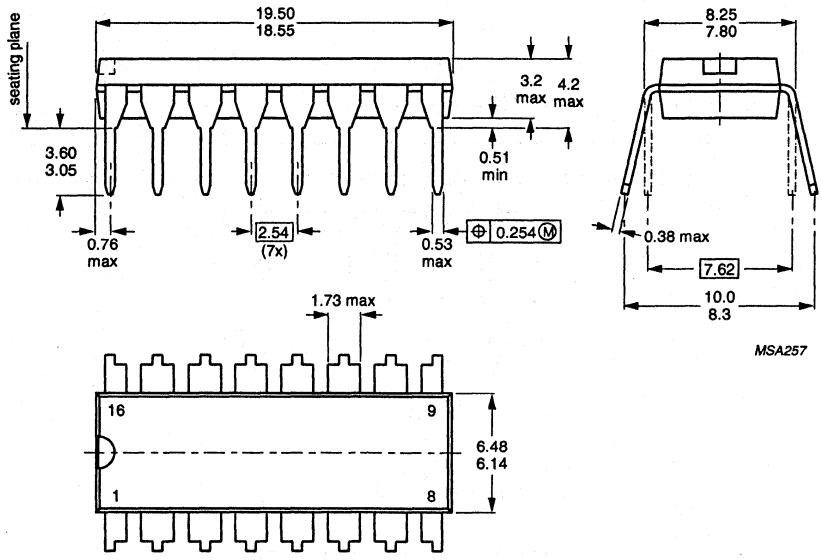
Package outlines IC02



Dimensions in mm.

Fig.15 Dual in-line, 16-pin (DIL-1) (SOT38GE, GG).

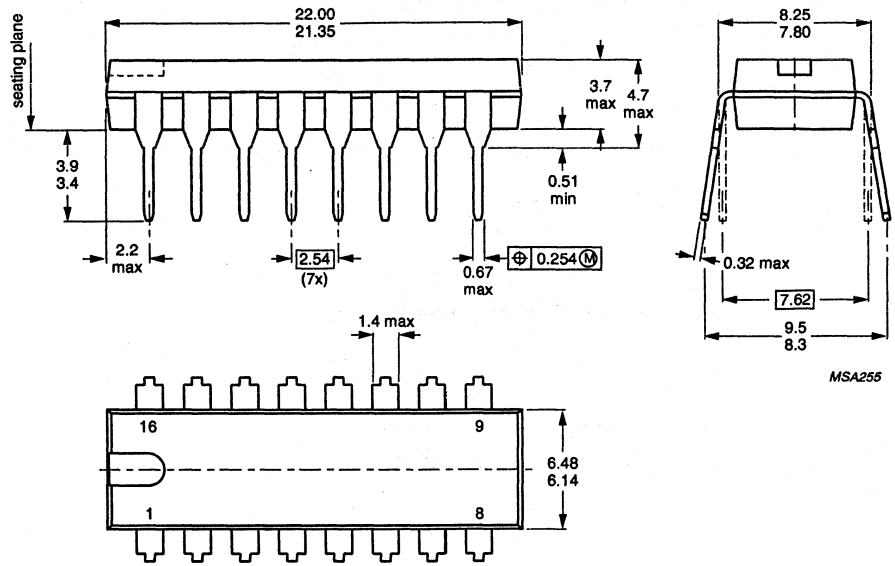
Package outlines IC02



Dimensions in mm.

Fig.16 Dual in-line, 16-pin (DIL) (SOT38DF).

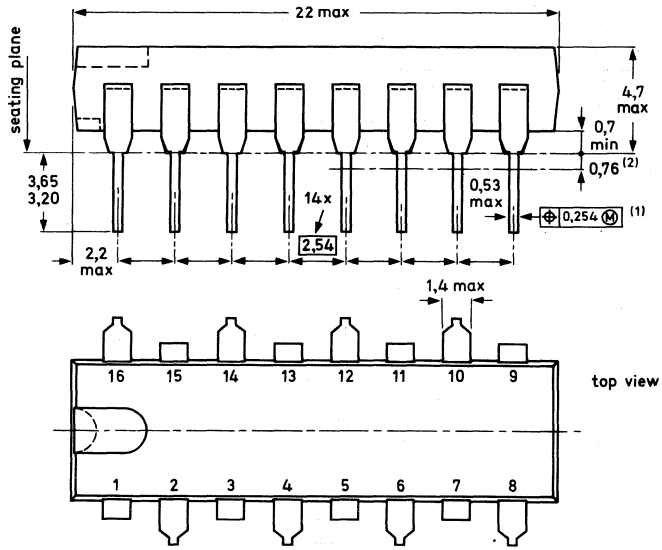
Package outlines IC02

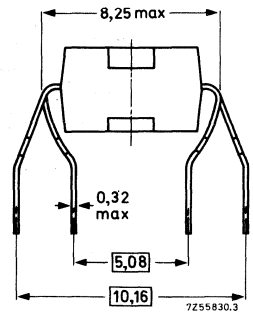


Dimensions in mm.

Fig.17 Dual in-line, 16-pin (DIL-3) (SOT38AG).

Package outlines IC02





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

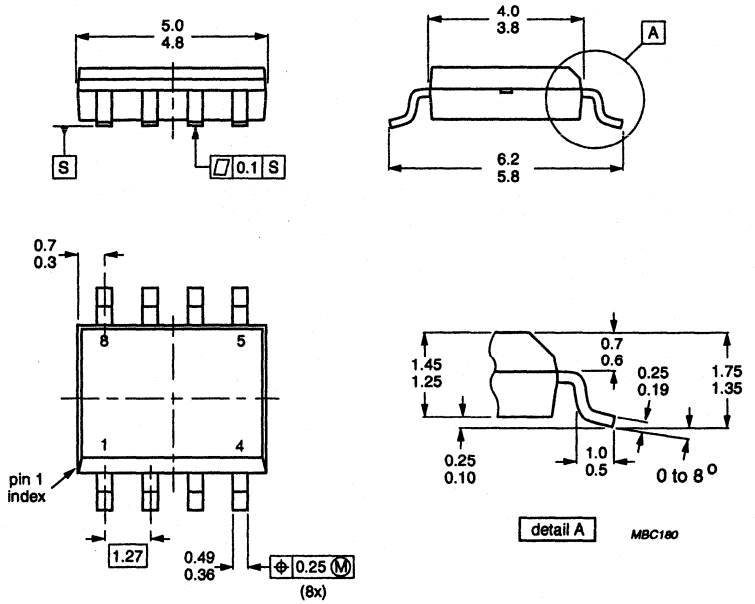
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm.

Fig.18 Quadruple in-line, plastic 16-pin (SOT58).

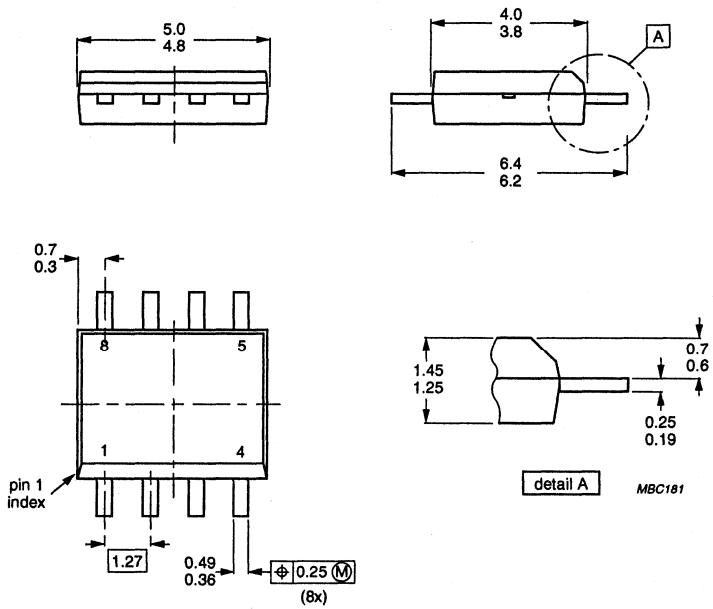
Package outlines IC02



Dimensions in mm.

Fig.19 SO, plastic, 8-pin (SO8) (SOT96A).

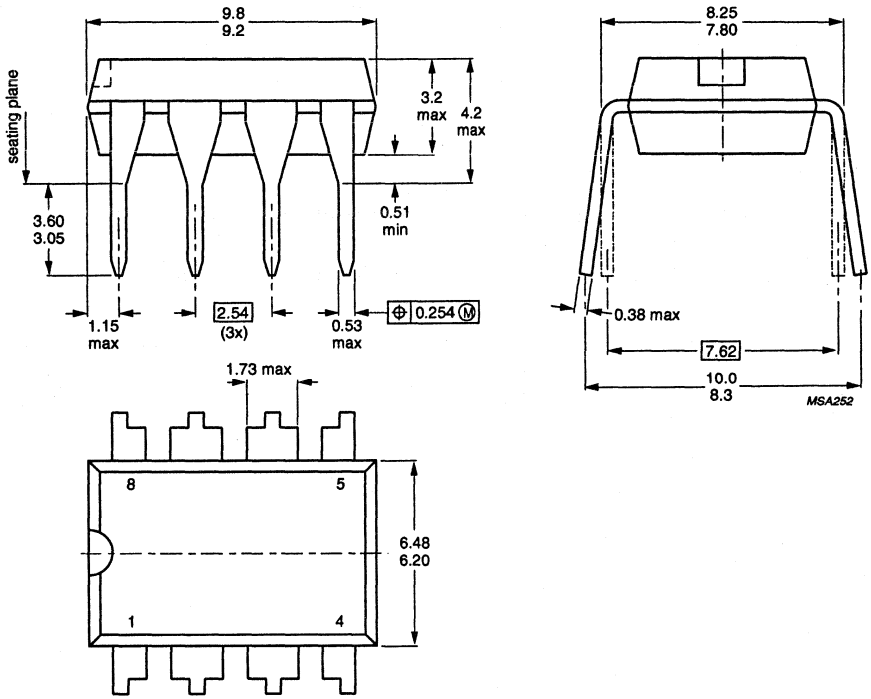
Package outlines IC02



Dimensions in mm.

Fig.20 SO, plastic, 8-pin (straight) (SO8S) (SOT96C).

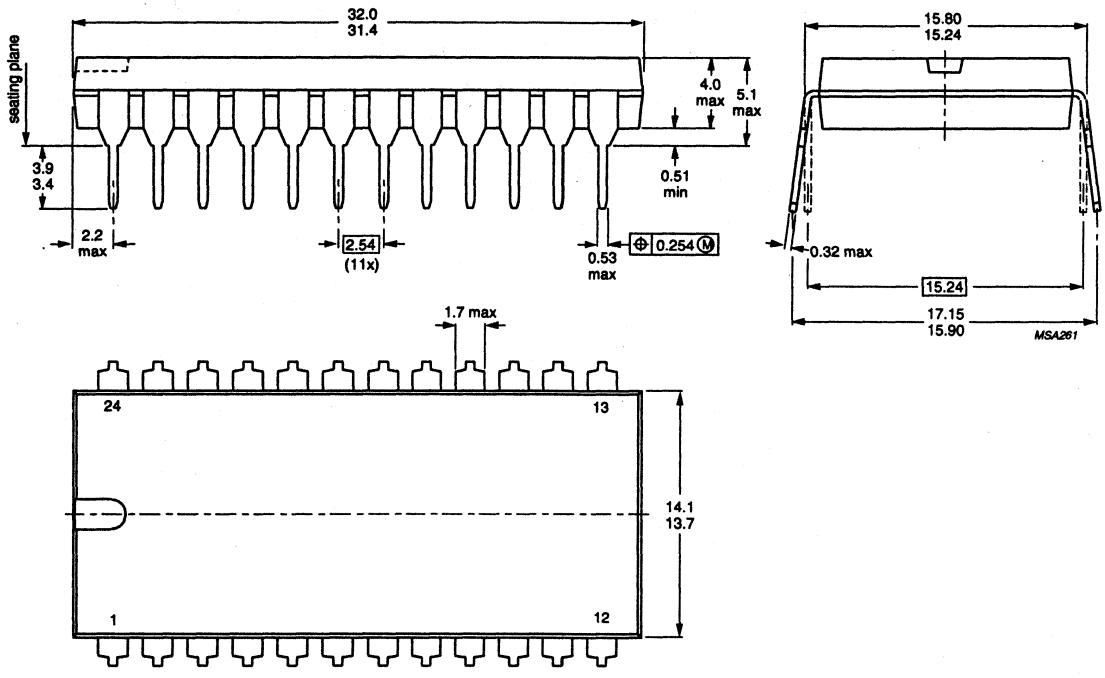
Package outlines IC02



Dimensions in mm.

Fig.21 DIL-bent-SIL, plastic, 8-pin (DIL8) (SOT97DE, DJ, GG).

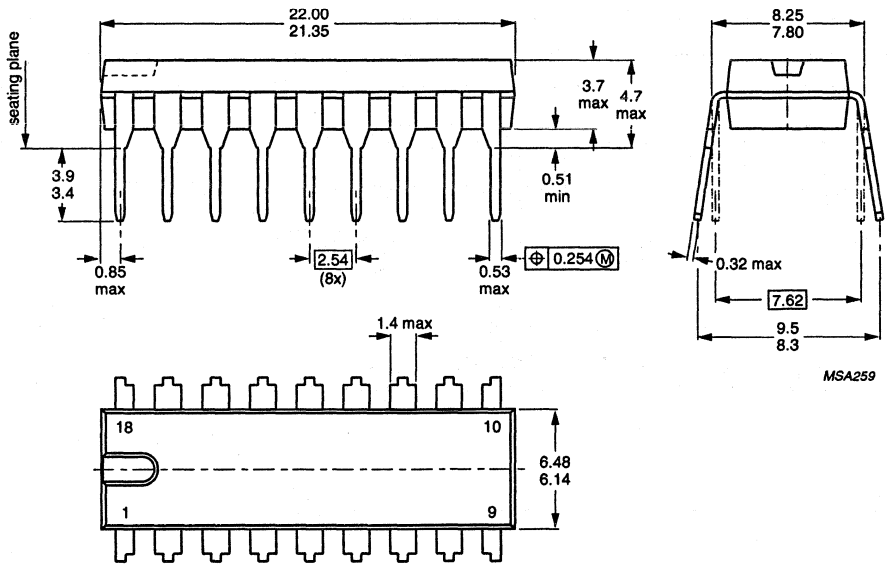
Package outlines IC02



Dimensions in mm.

Fig.22 Dual in-line, plastic, 24-pin (DIL24) (SOT101AG, FE, LE, LG).

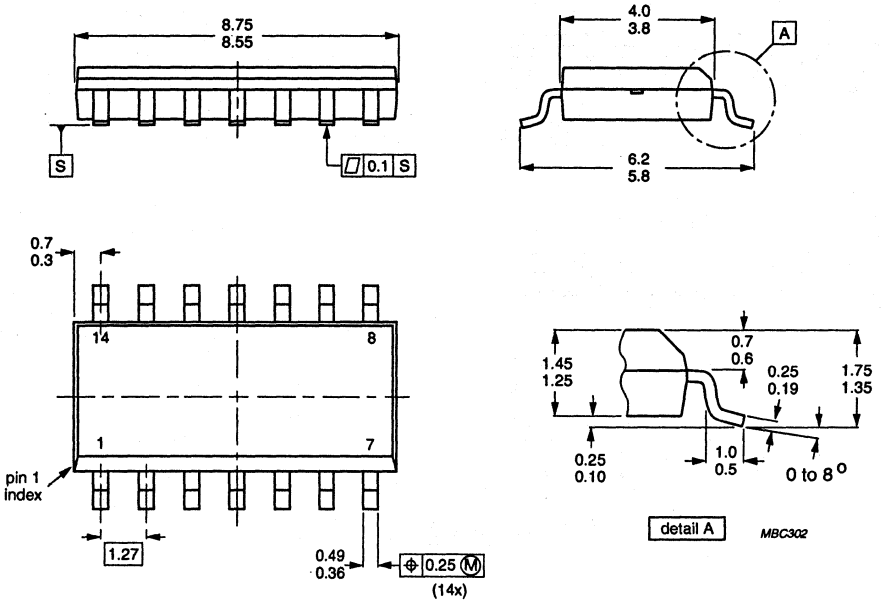
Package outlines IC02



Dimensions in mm.

Fig.23 Dual in-line, plastic, 18-pin (DIL18) (SOT102RG, RE, MG).

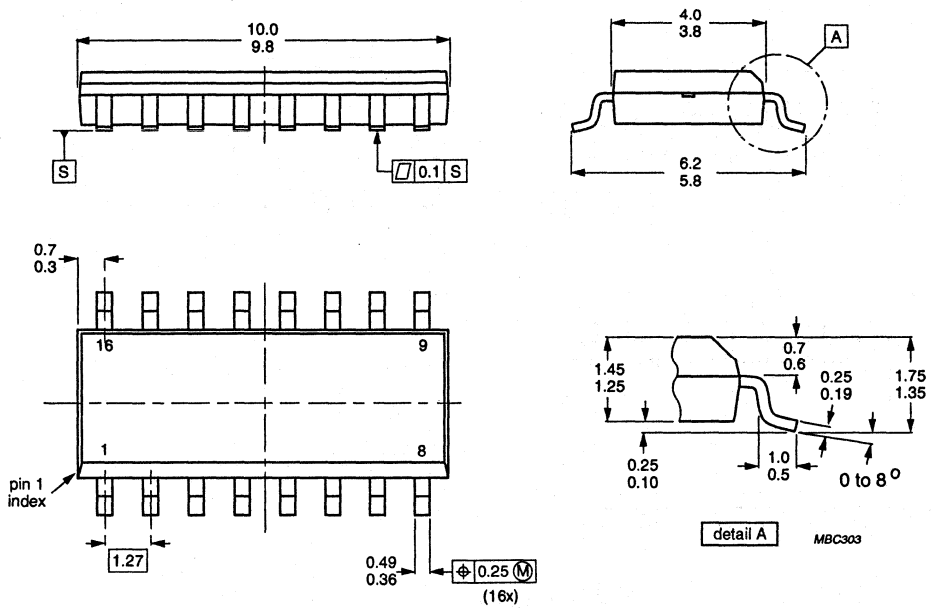
Package outlines IC02



Dimensions in mm.

Fig.24 plastic SO, 14-pin (SO14) (SOT108AG,AH).

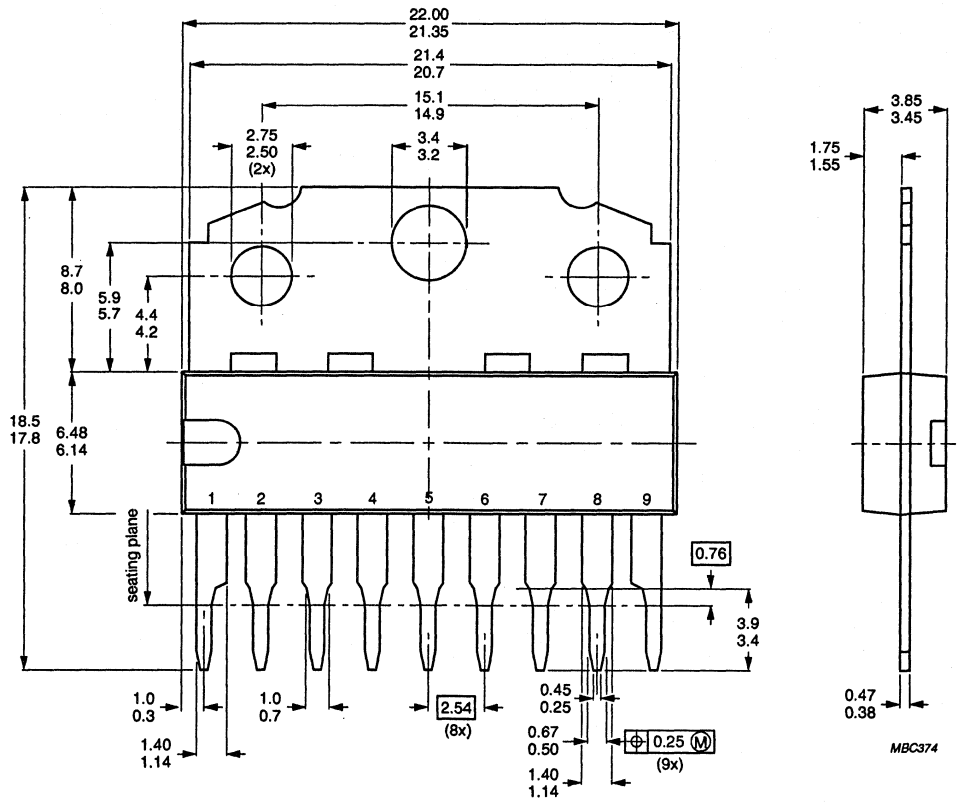
Package outlines IC02



Dimensions in mm.

Fig.25 plastic SO, 16-pin (SO16) (SOT109AG,DG).

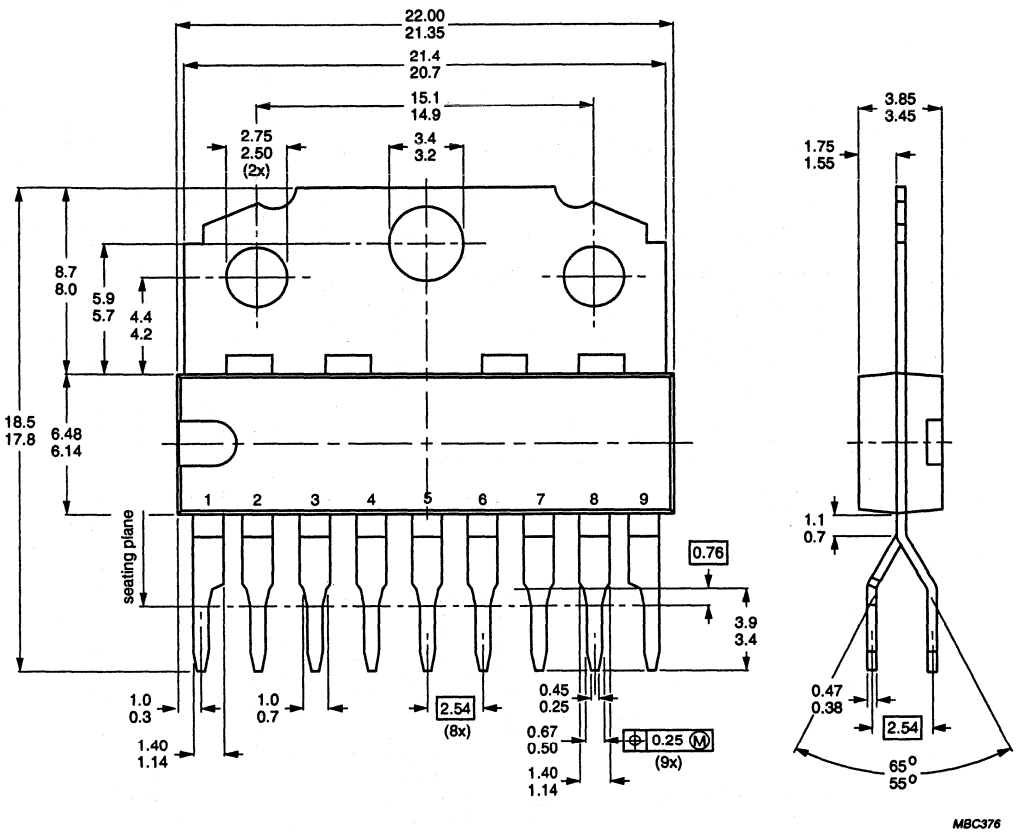
Package outlines IC02



Dimensions in mm.

Fig.26 Single in-line, plastic, medium power with fin, 9-pin (SIL9MPF) (SOT110BE).

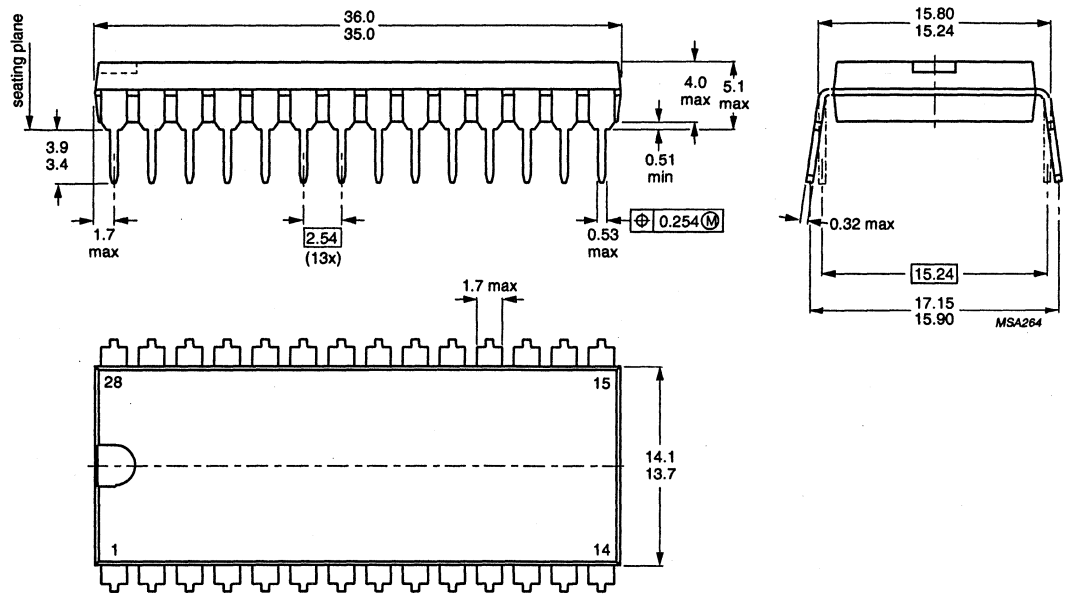
Package outlines IC02



Dimensions in mm.

Fig.27 plastic DIL-bent-SIL, medium power with fin, 9-pin (DBS9MPF) (SOT111BE).

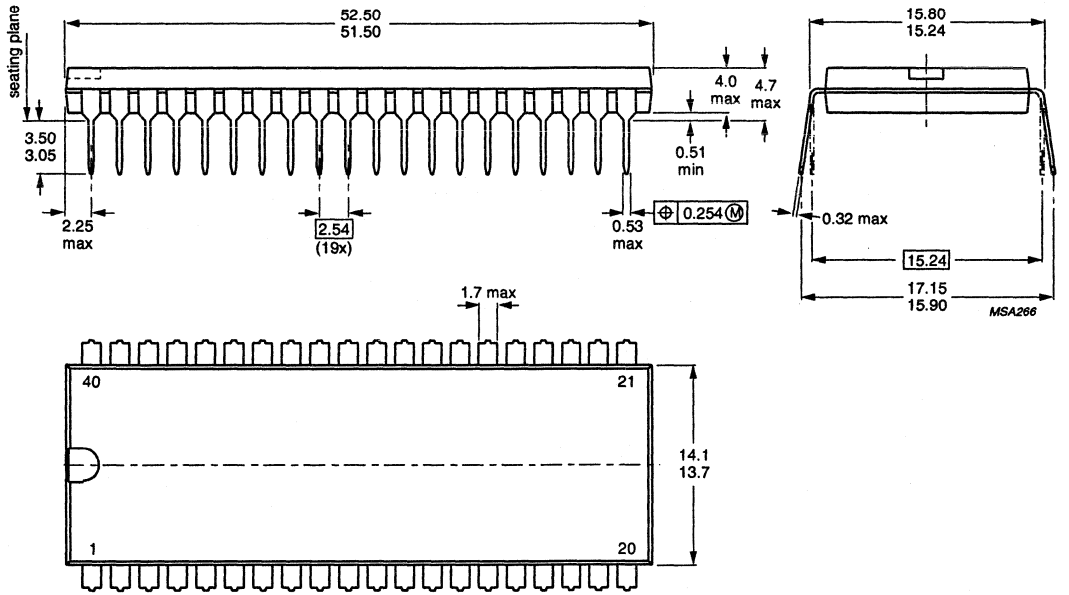
Package outlines IC02



Dimensions in mm.

Fig.28 Dual in-line, plastic, 28-pin (DIL28) (SOT117BE, NE, NG).

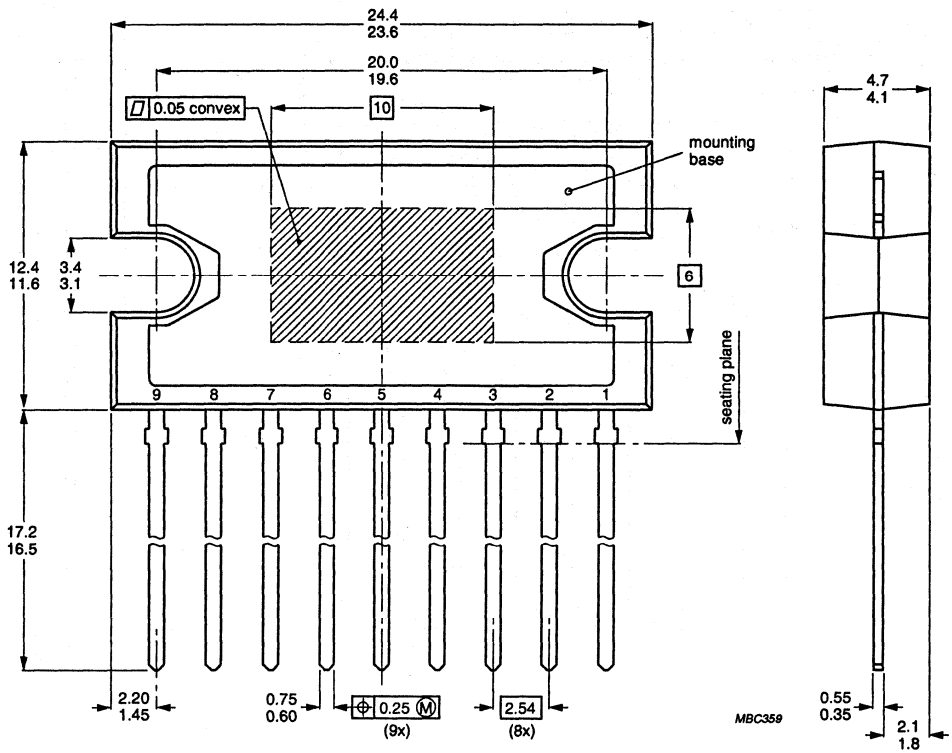
Package outlines IC02



Dimensions in mm.

Fig.29 Dual in-line, plastic, 40-pin (DIL40) (SOT129AE, AG, DE, DG, DH, FE, FG, FH).

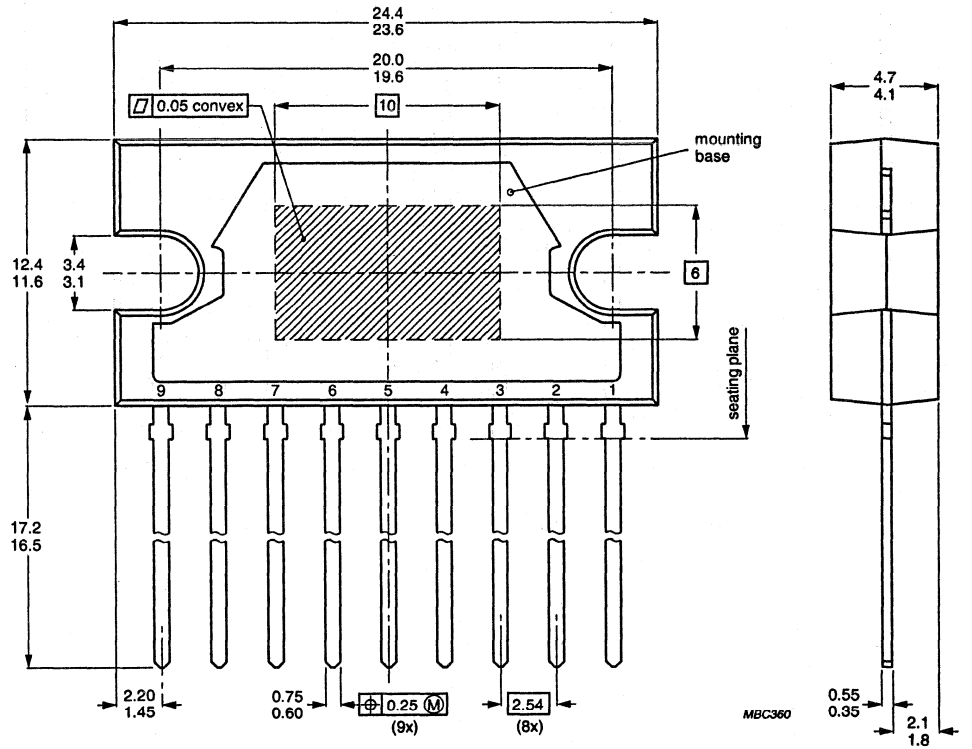
Package outlines IC02



Dimensions in mm.

Fig.30 Single in-line, plastic, power, 9-pin (SIL9P) (SOT131A, BE, CE).

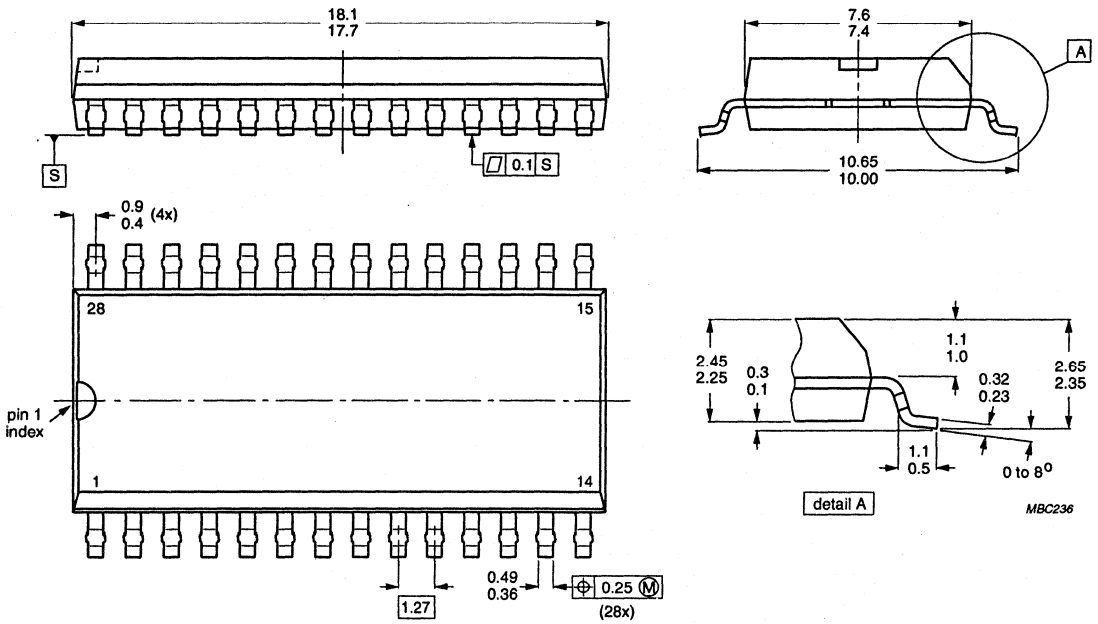
Package outlines IC02



Dimensions in mm.

Fig.31 Single in-line, plastic, power, 9-pin (SIL9P) (SOT131RA, RBE, RDG, RFG, RG).

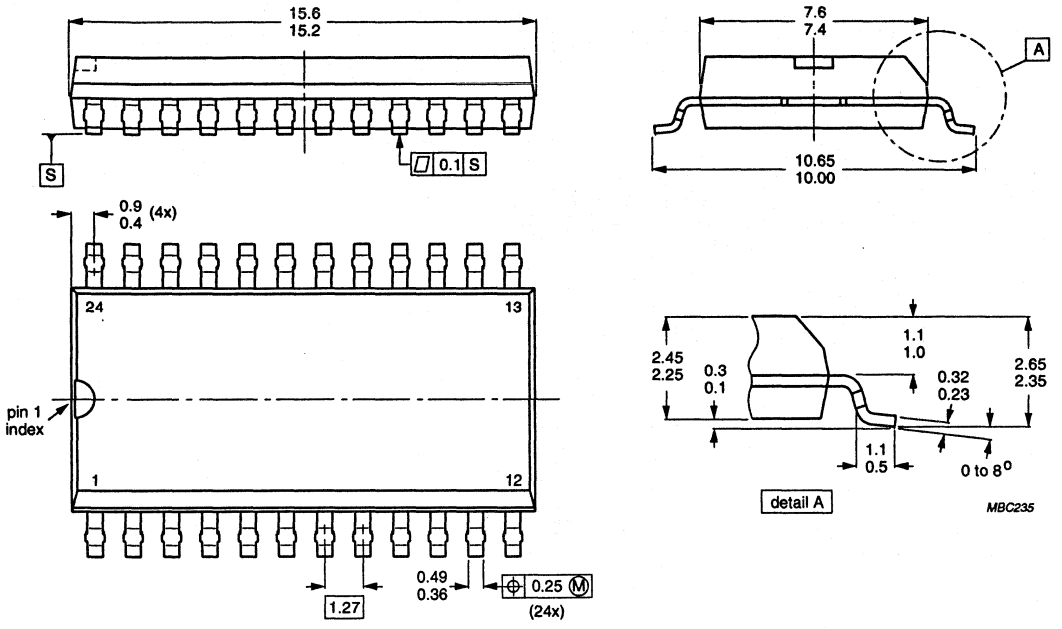
Package outlines IC02



Dimensions in mm.

Fig.32 SOL, plastic, 28-pin (SO28L) (SOT136AG, AH).

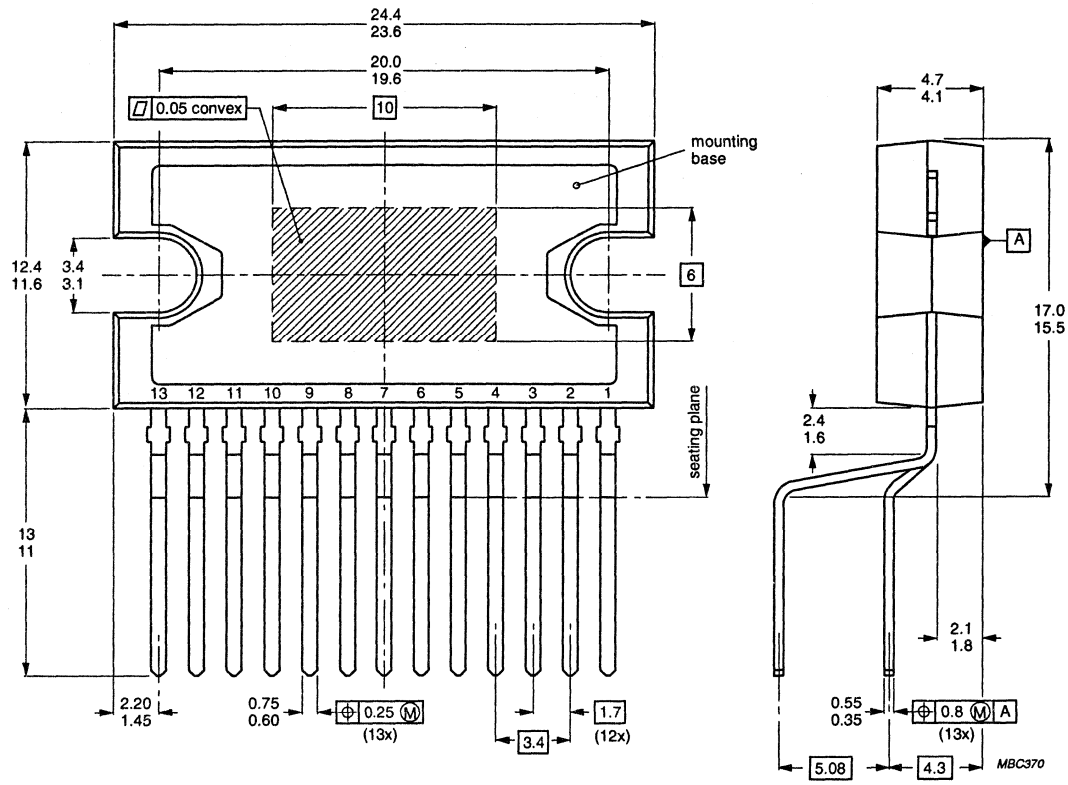
Package outlines IC02



Dimensions in mm.

Fig.33 SOL, plastic, 24-pin (SO24L) (SOT137AG, AH).

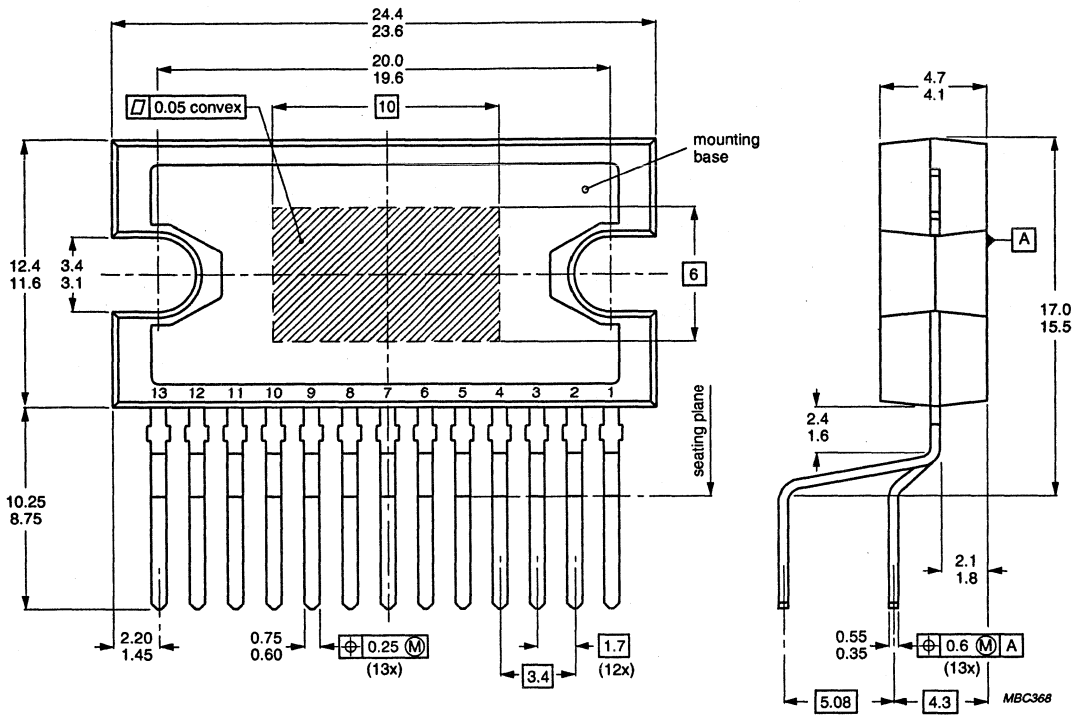
Package outlines IC02



Dimensions in mm.

Fig.34 DIL-bent-SIL, plastic, power, 13-pin (DBS13P) (SOT141BEA, CEA).

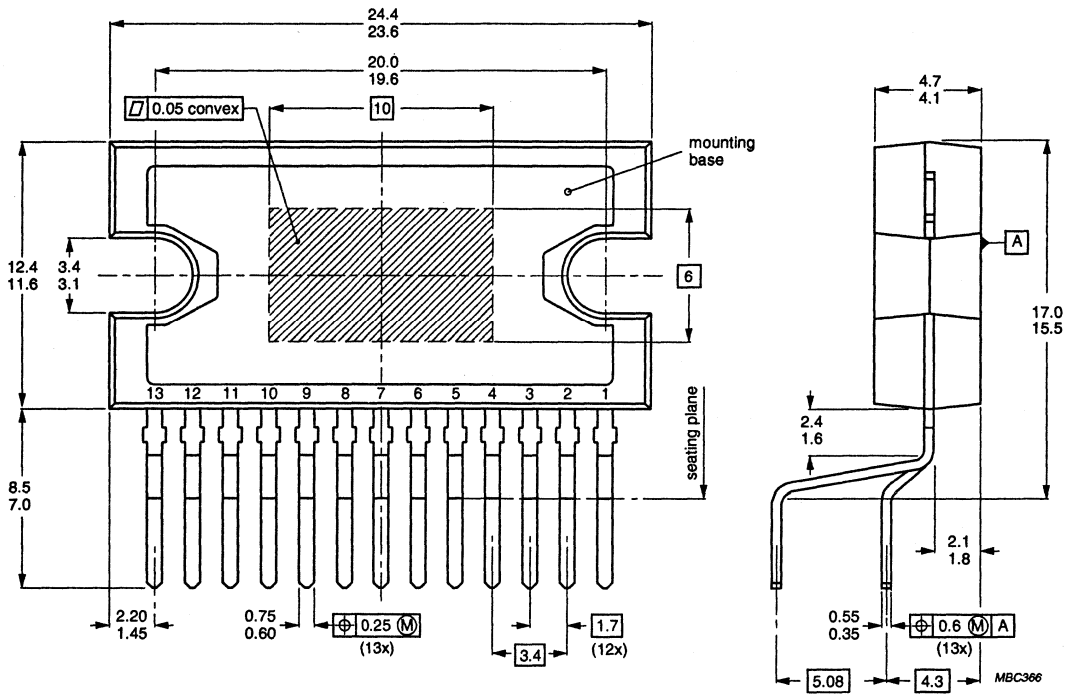
Package outlines IC02



Dimensions in mm.

Fig.35 DIL-bent-SIL, plastic, power, 13-pin (DBS13P) (SOT141BEB, CEB).

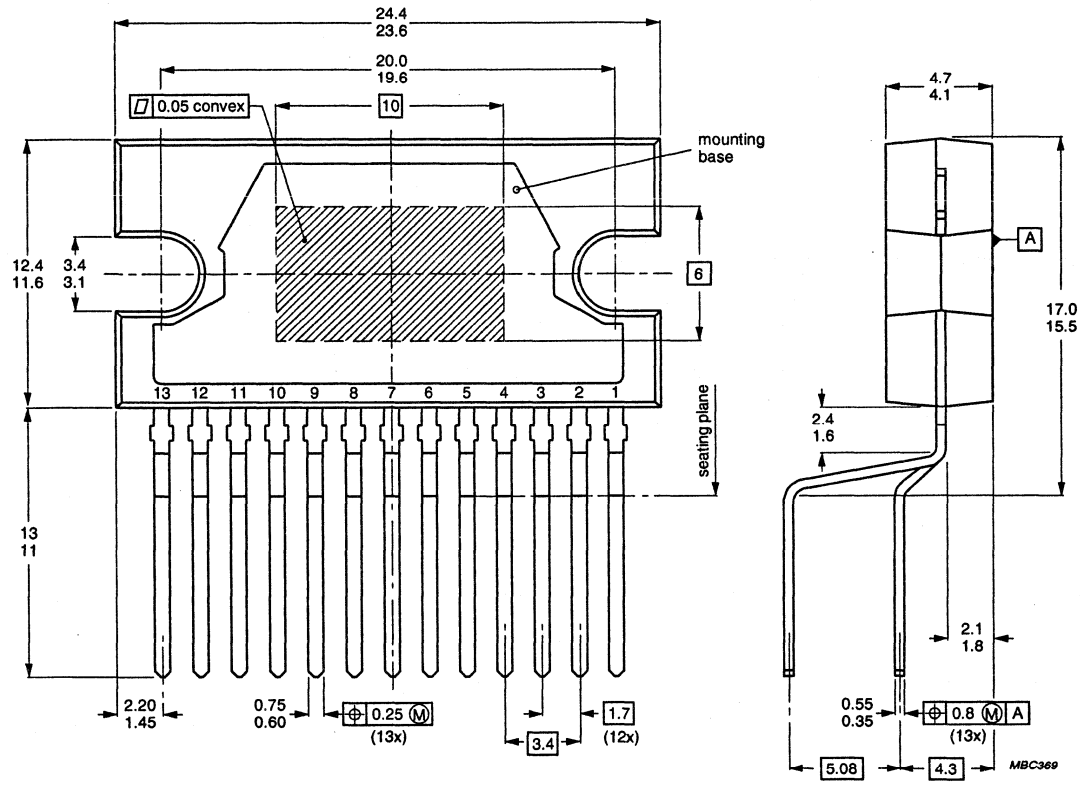
Package outlines IC02



Dimensions in mm.

Fig.36 DIL-bent-SIL, plastic, power, 13-pin (DBS13P) (SOT141BEC, CEC).

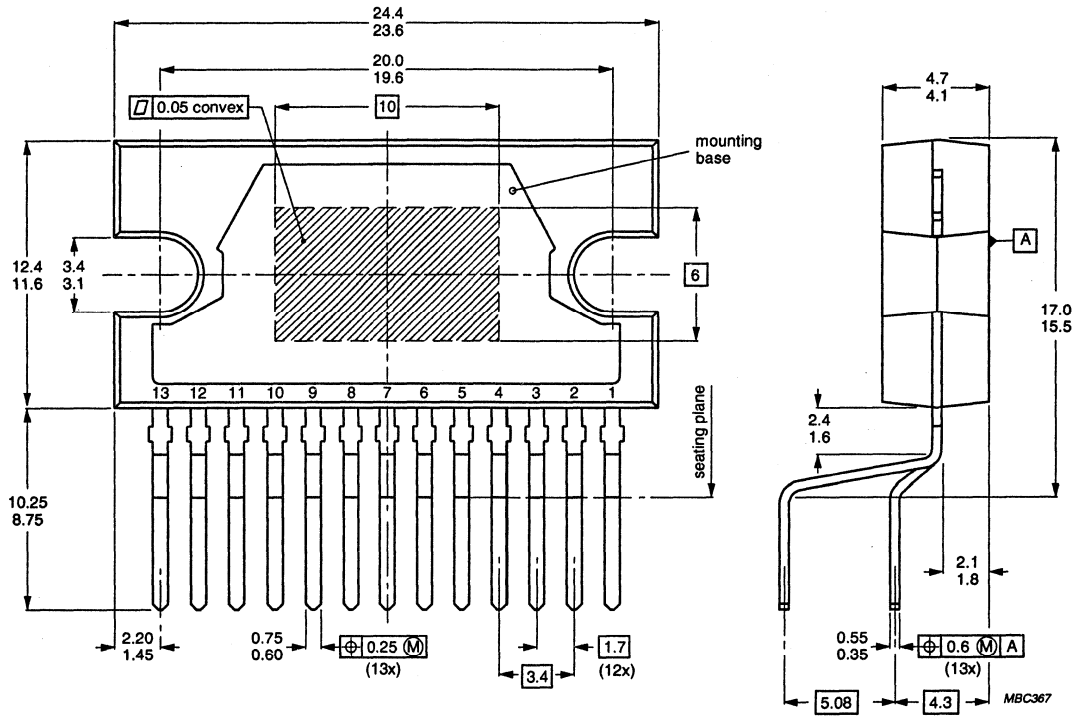
Package outlines IC02



Dimensions in mm.

Fig.37 DIL-bent-SIL, plastic, power, 13-pin (DBS13P) (SOT141RAA, RBEA, RDGA, RFGA, RGA).

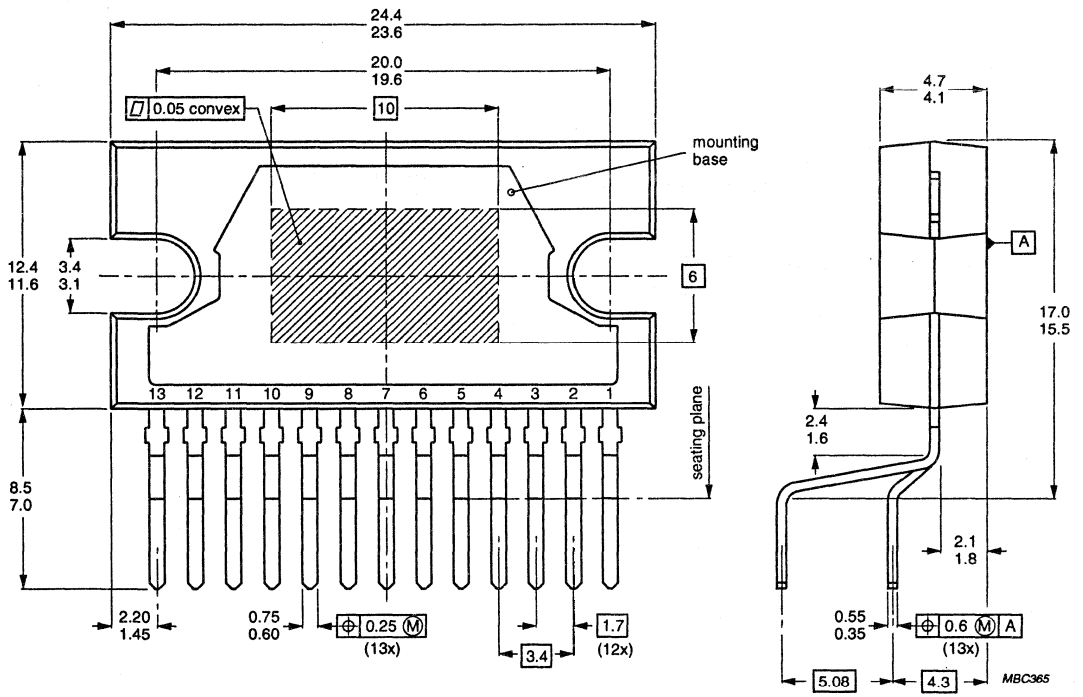
Package outlines IC02



Dimensions in mm.

Fig.38 DIL-bent-SIL, plastic, power, 13-pin (DBS13P) (SOT141RAB, RBEB).

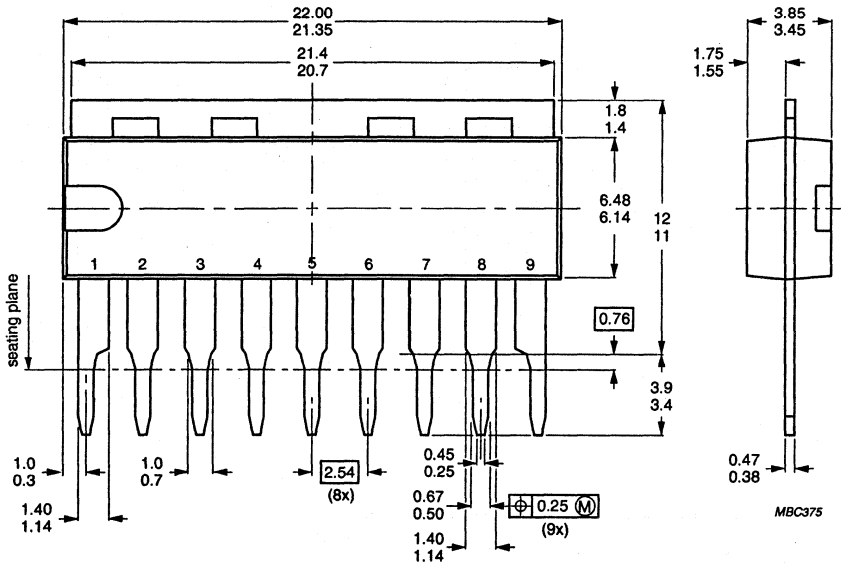
Package outlines IC02



Dimensions in mm.

Fig.39 DIL-bent-SIL, plastic, power, 13-pin (DBS13P) (SOT141RAC, RBEC, RDGC, RFGC, RGC).

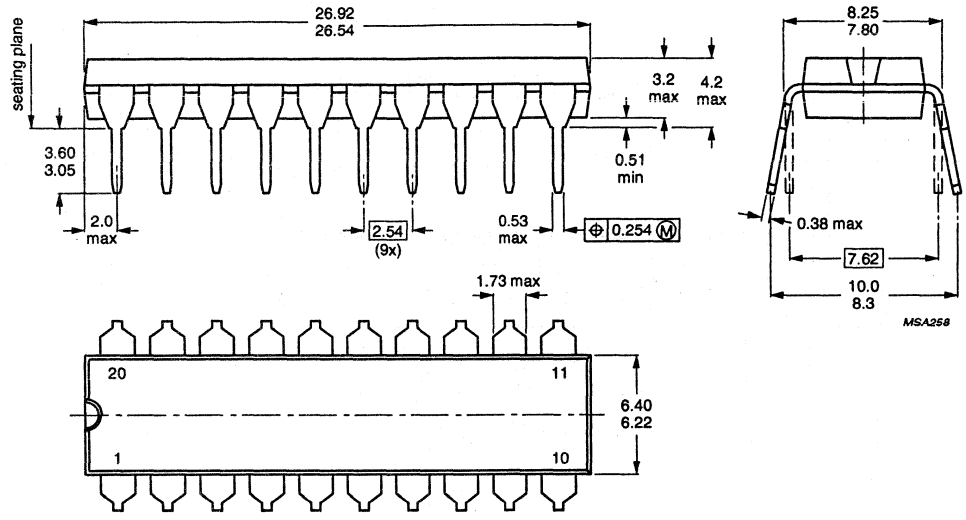
Package outlines IC02



Dimensions in mm.

Fig.40 Single in-line, plastic, medium power, 9-pin (SIL9MP) (SOT142BE).

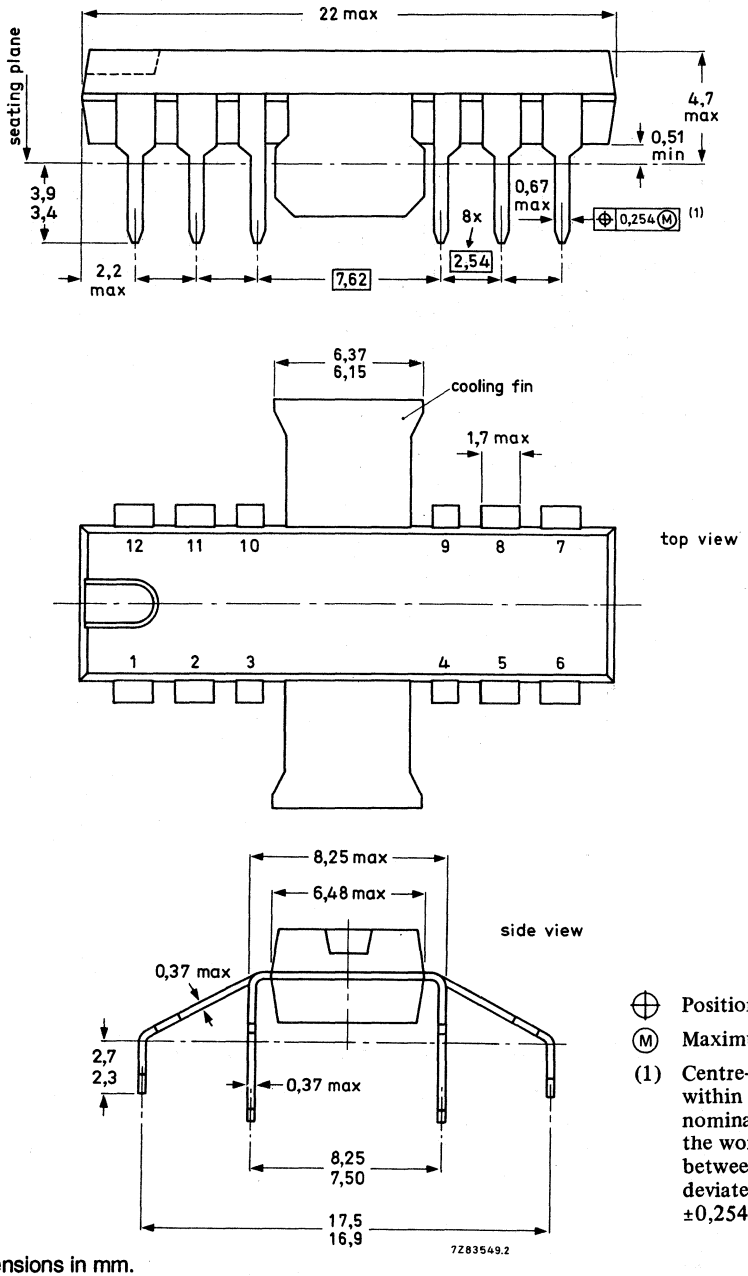
Package outlines IC02



Dimensions in mm.

Fig.41 Dual in-line, plastic, 20-pin (DIL20) (SOT146EF, EG, FE).

Package outlines IC02



⊕ Positional accuracy.

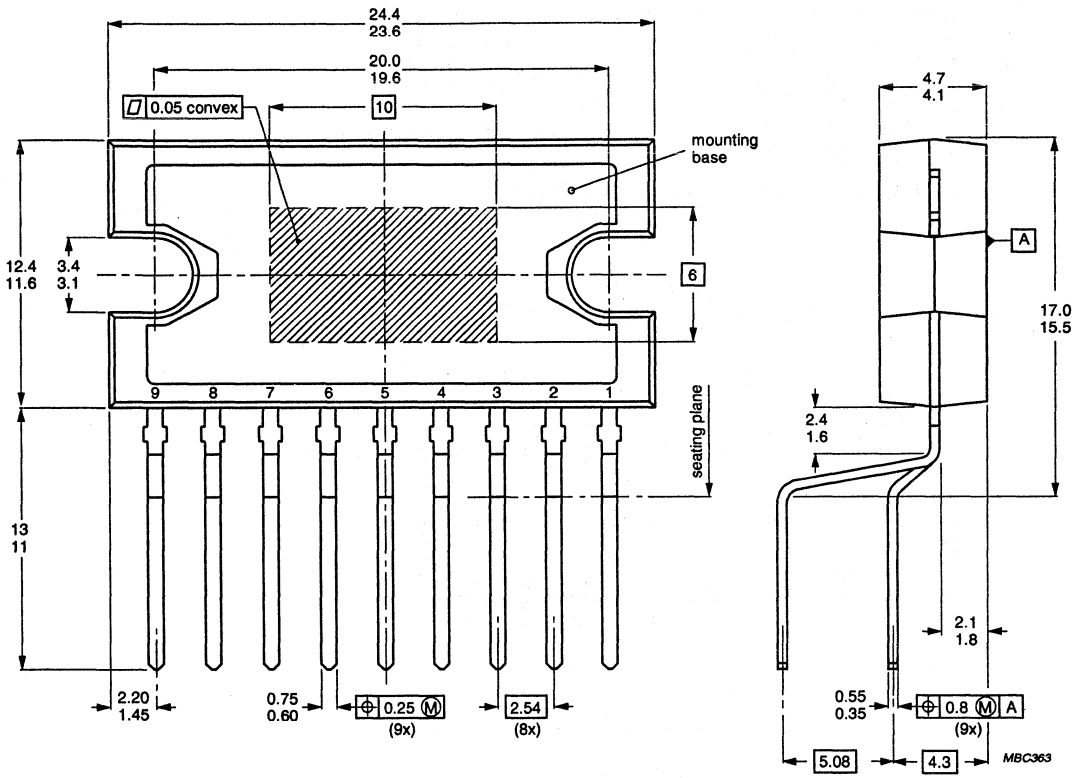
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

Dimensions in mm.

Fig.42 12-lead dual in-line, plastic with metal cooling fin (SOT150).

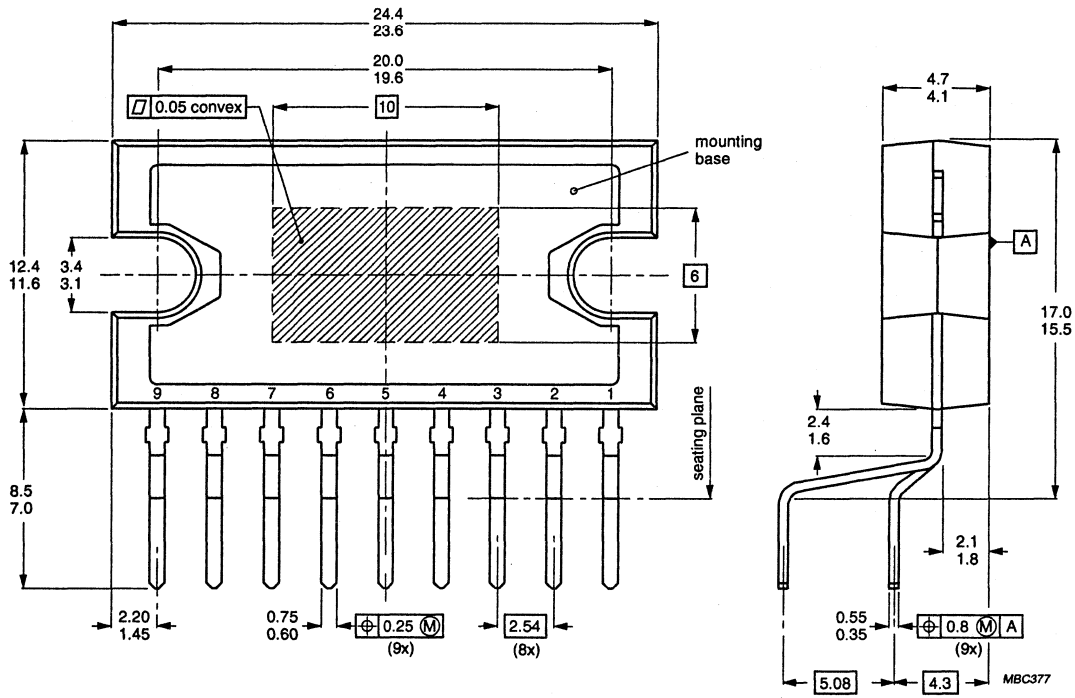
Package outlines IC02



Dimensions in mm.

Fig.43 DIL-bent-SIL, plastic, power, 9-pin (DBS9P) (SOT157A, BE, CE).

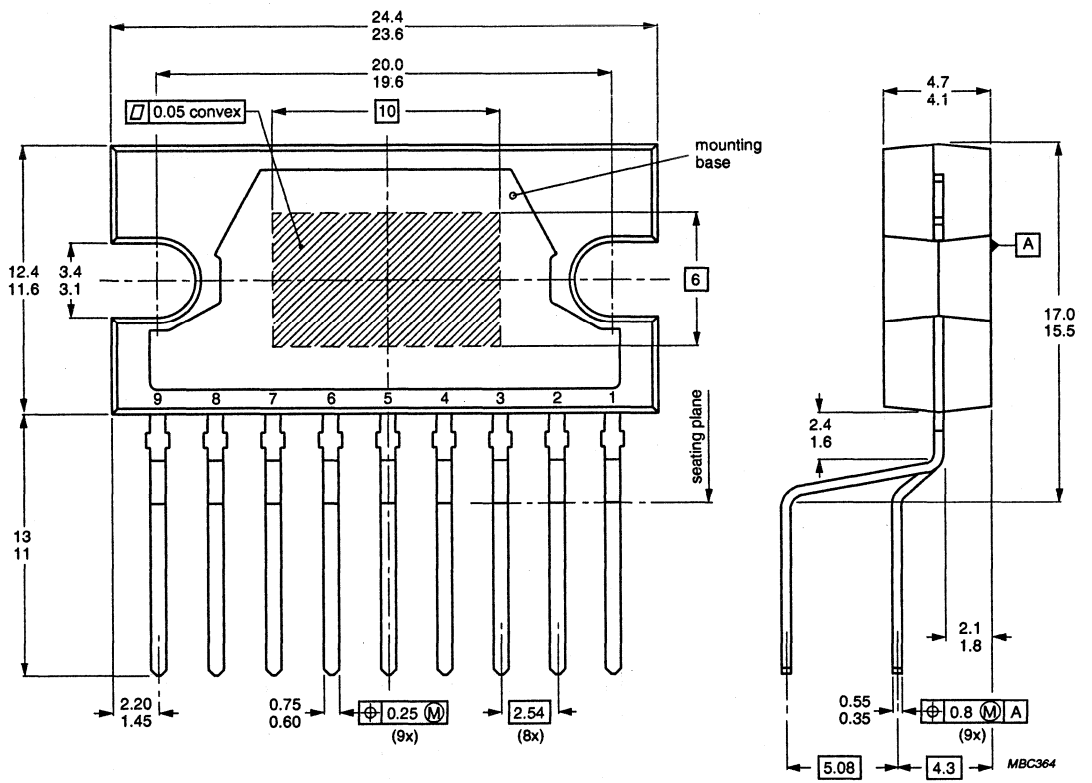
Package outlines IC02



Dimensions in mm.

Fig.44 DIL-bent-SIL, plastic, power, 9-pin (DBS9P) (SOT157AC, BEC, CEC).

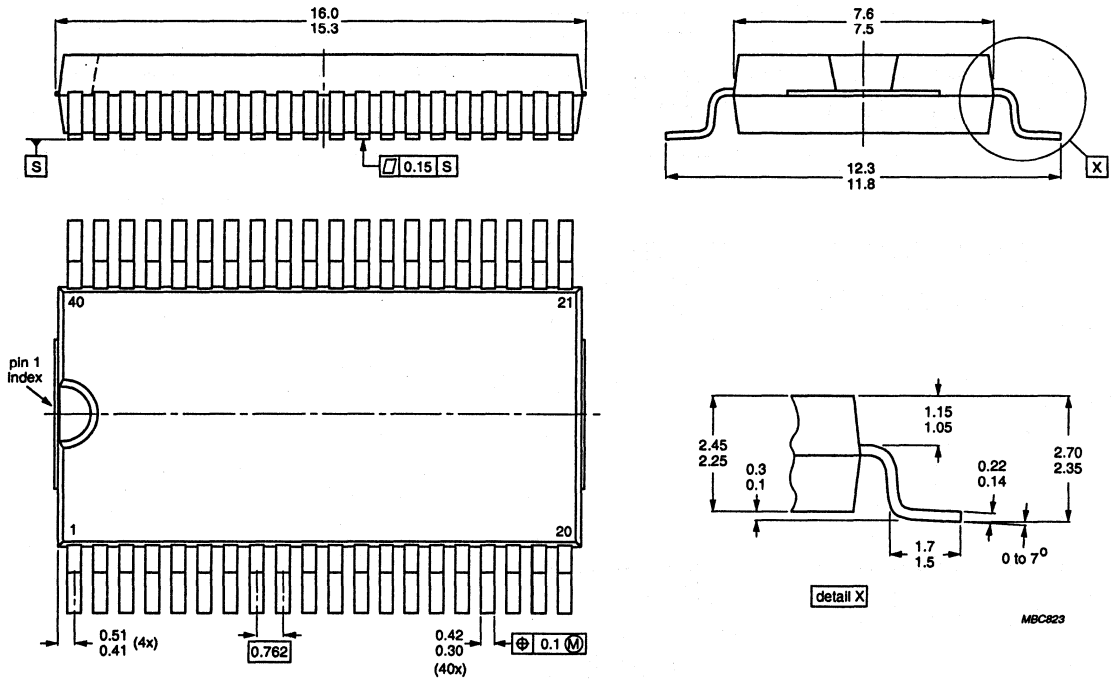
Package outlines IC02



Dimensions in mm.

Fig.45 DIL-bent-SIL, plastic, power, 9-pin (DBS9P) (SOT157RA, RBE, RCE, RDGA, RDGC, RFGA, RFGC, RGA).

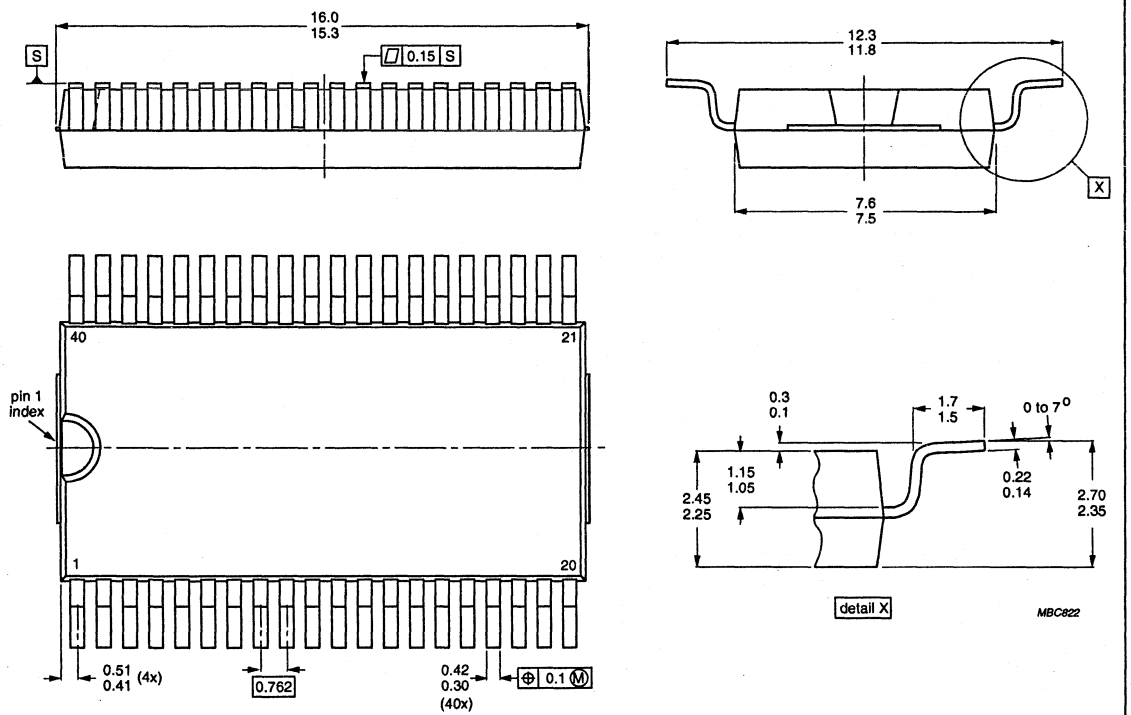
Package outlines IC02



Dimensions in mm.

Fig.46 VSO, plastic, 40-pin (VSO40) (SOT158AJ).

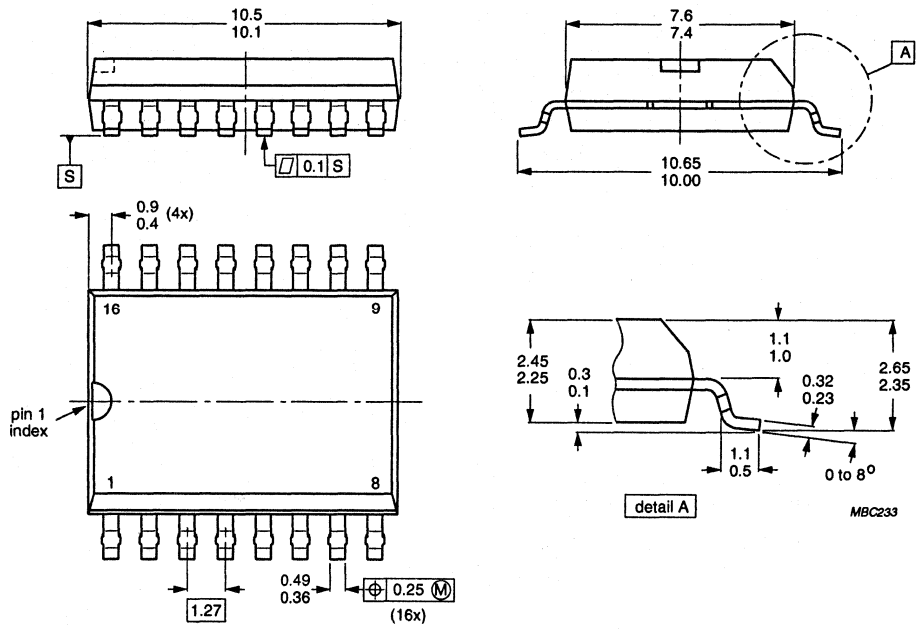
Package outlines IC02



Dimensions in mm.

Fig.47 VSO, plastic, 40-pin, face down (VSO40FD) (SOT158BJ).

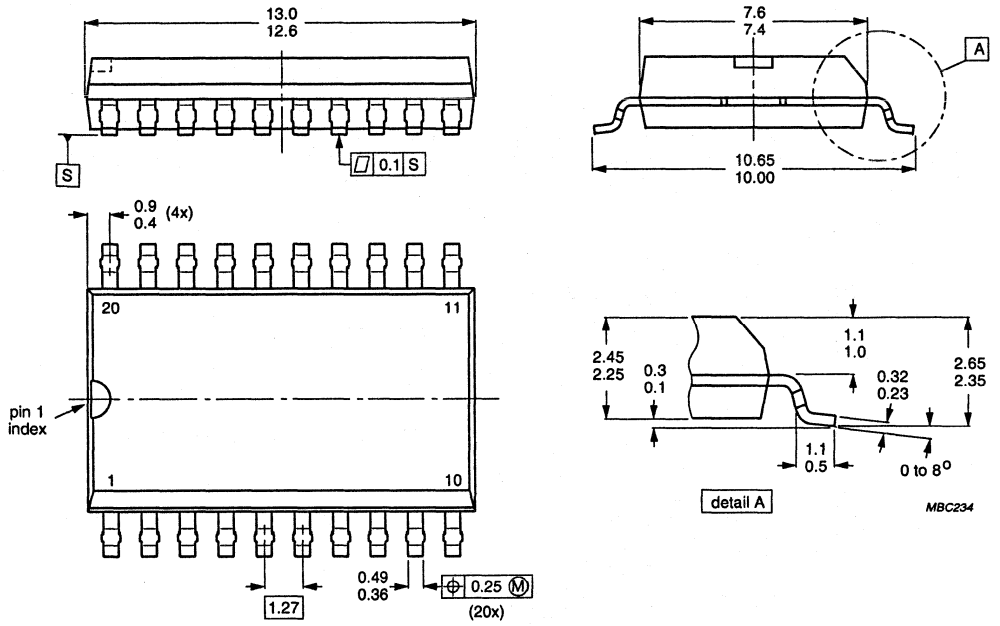
Package outlines IC02



Dimensions in mm.

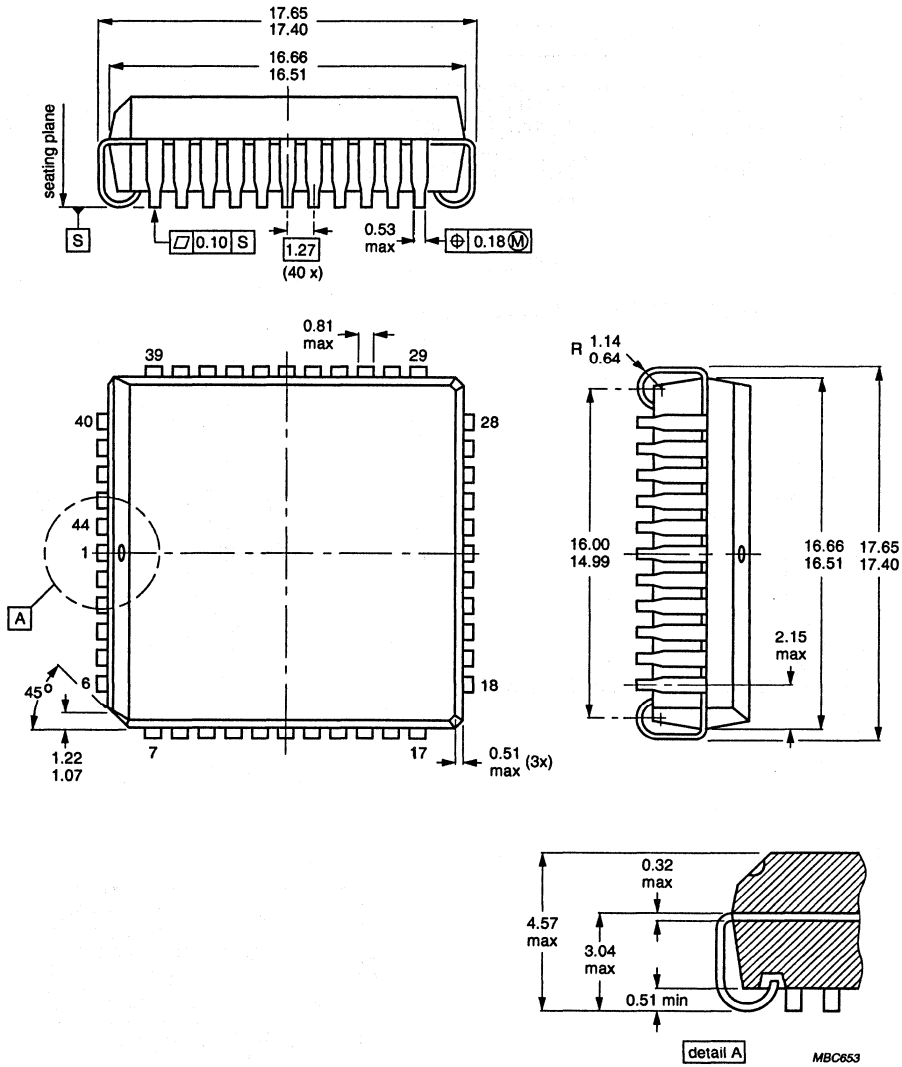
Fig.48 SOL, plastic, 16-pin (SO16L) (SOT162AG, AH).

Package outlines IC02



Dimensions in mm.

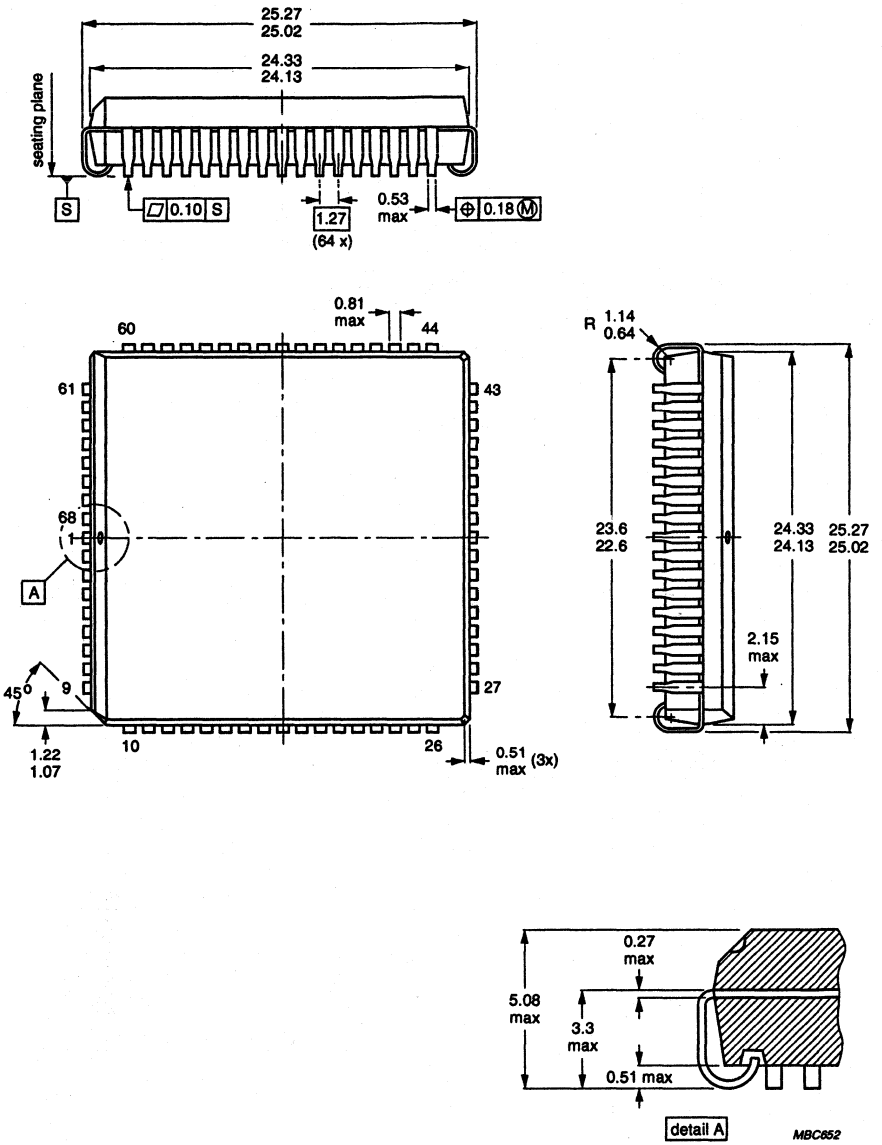
Fig.49 SOL, plastic, 20-pin (SO20L) (SOT163AG, AH).



Dimensions in mm.

Fig.50 Plastic leaded chip carrier, 44-lead (PLCC44) (SOT187CG).

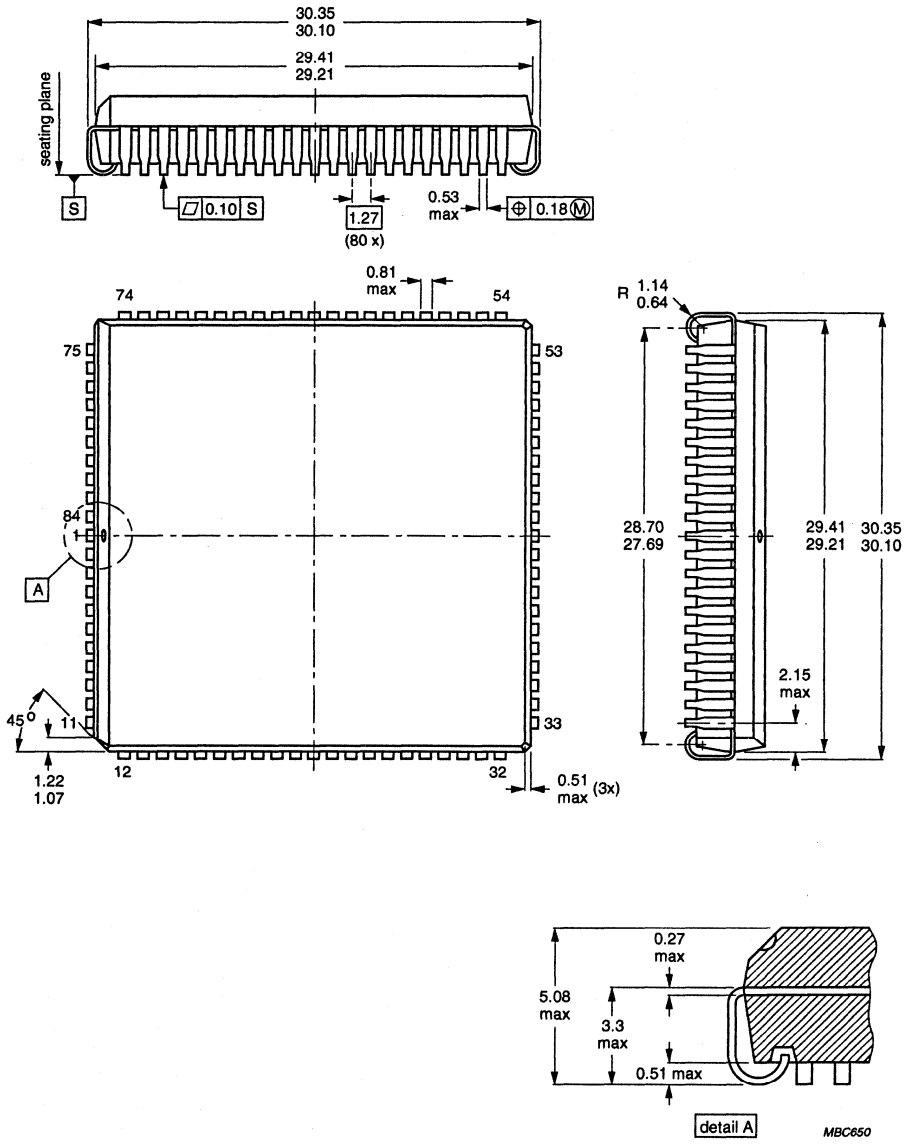
Package outlines IC02



Dimensions in mm.

Fig.51 Plastic leaded chip carrier, 68-lead (PLCC68) (SOT188CG).

Package outlines IC02



Dimensions in mm.

Fig.52 Plastic leaded chip carrier, 84-lead (PLCC84) (SOT189CG).

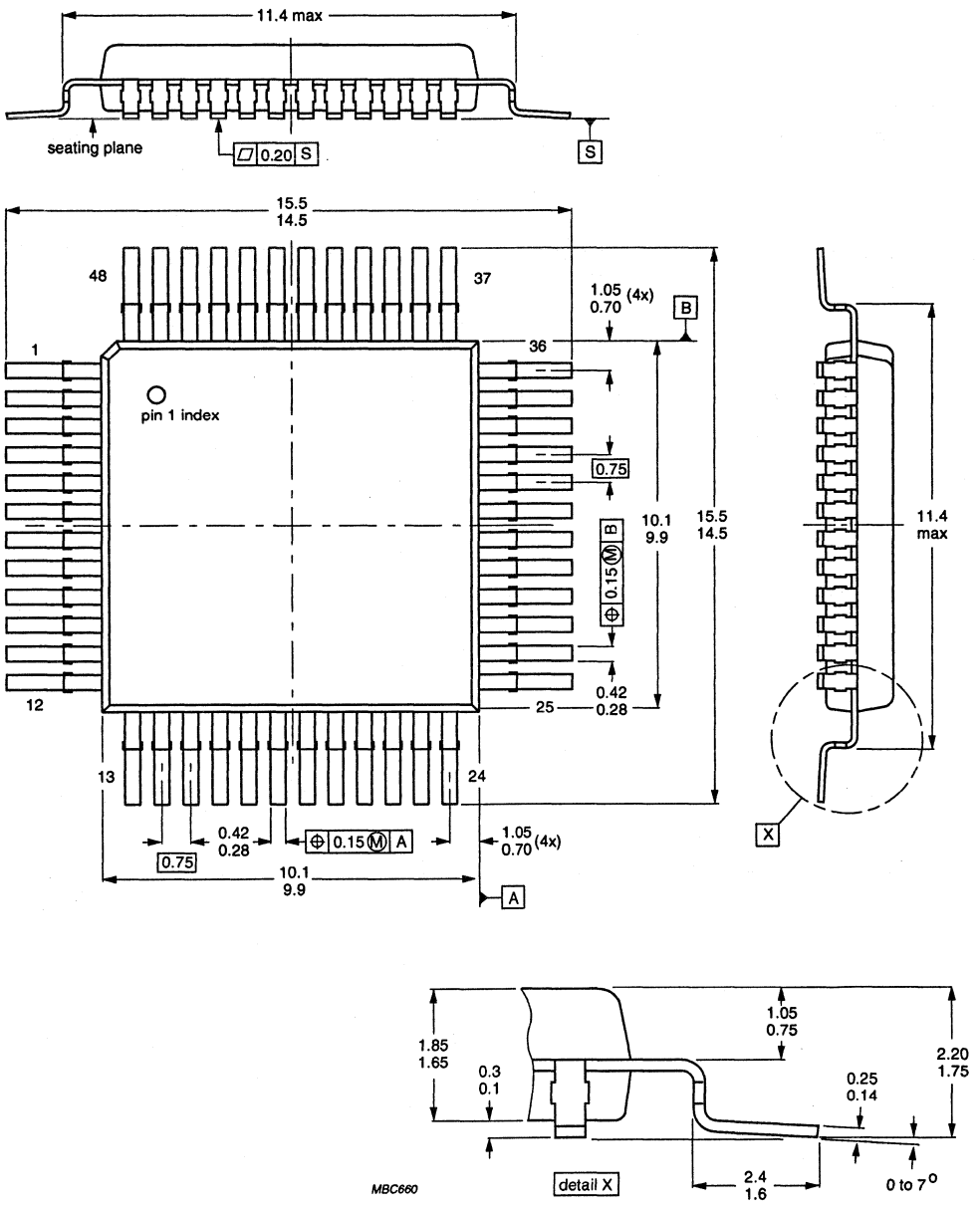


Fig.53 Quad flat-pack, plastic, 48-pin, 10 mm square (QFP48S10) (SOT196AG).

Package outlines IC02

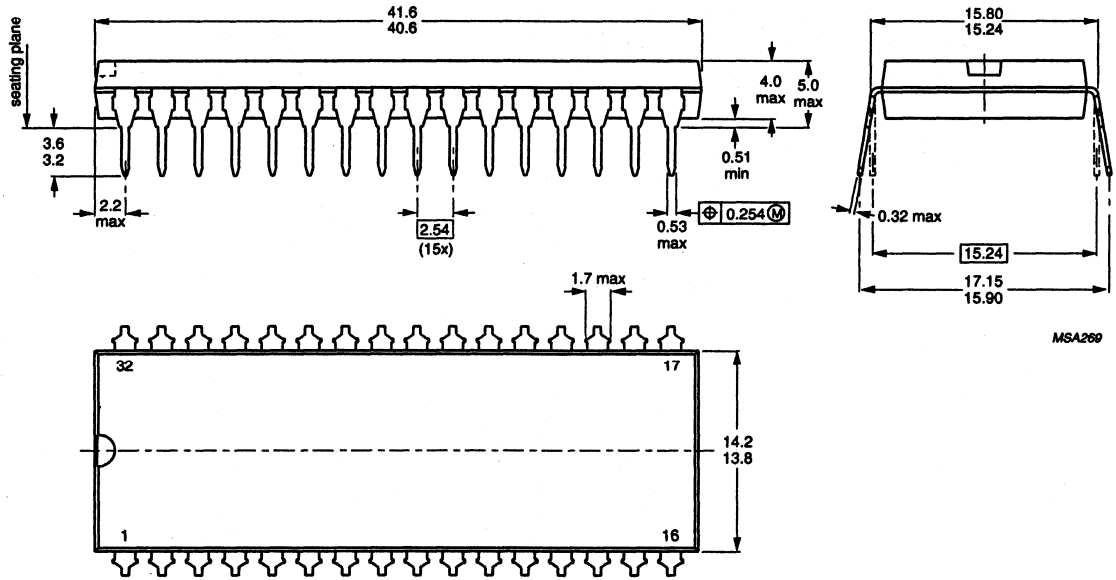
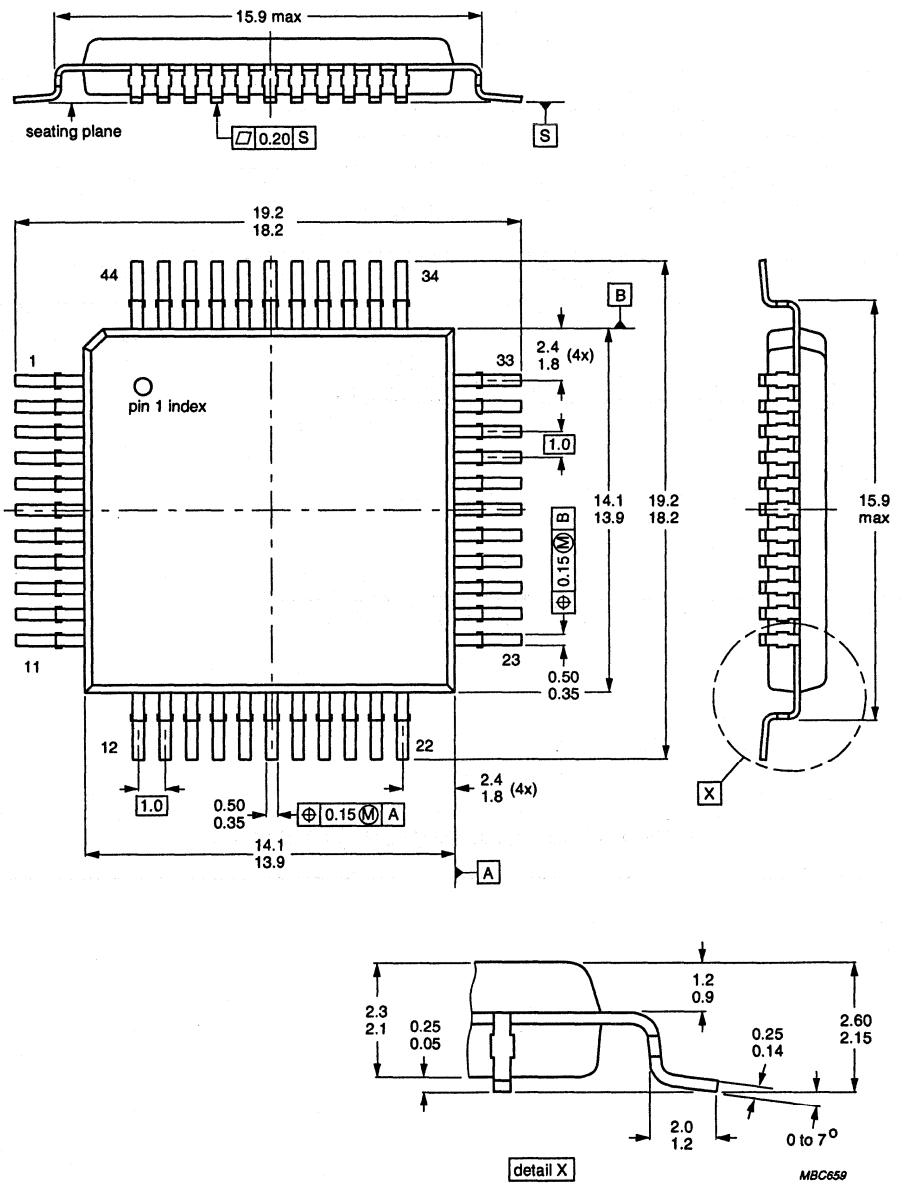


Fig.54 plastic DIL, 32-pin (DIL32) (SOT201A,AJ).

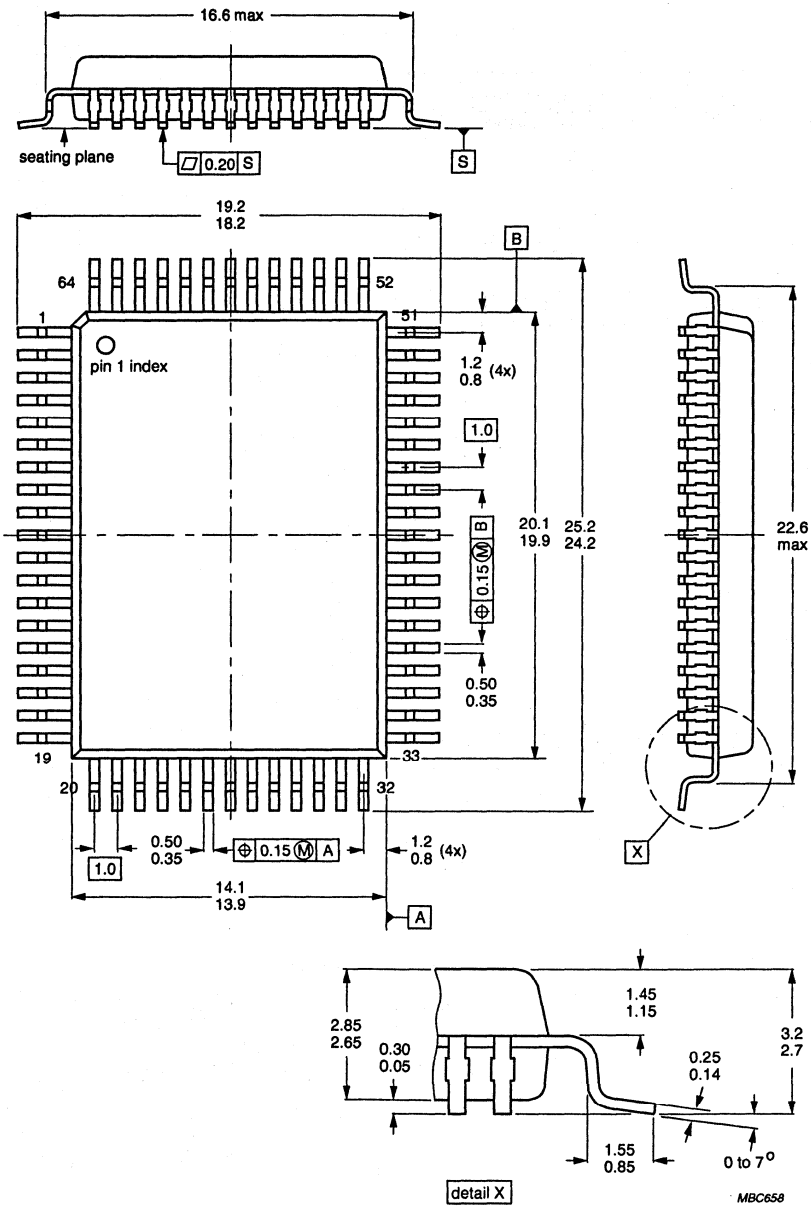
Package outlines IC02



Dimensions in mm.

Fig.55 44-lead quad flat-pack, plastic (SOT205AG).

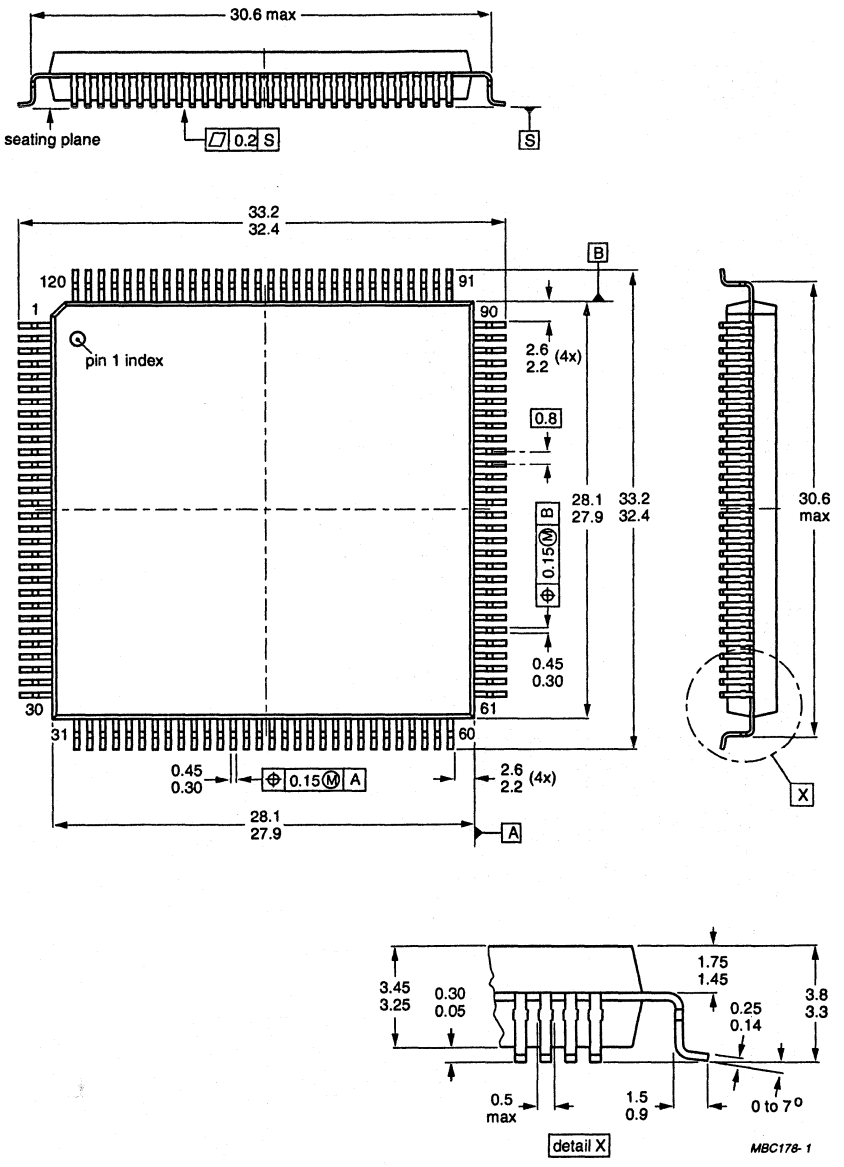
Package outlines IC02



Dimensions in mm.

Fig.56 Quad flat-pack, plastic, 64-pin, rectangular (QFP64REC) (SOT208A).

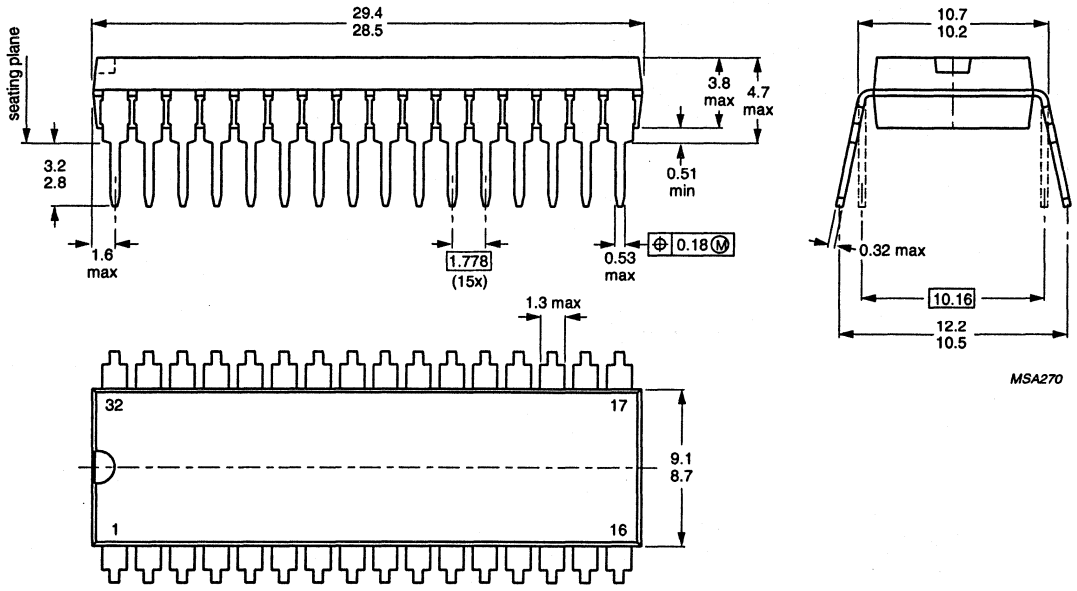
Package outlines IC02



Dimensions in mm.

Fig.57 Quad flat-pack, plastic, 120-pin (QFP120) (SOT220A).

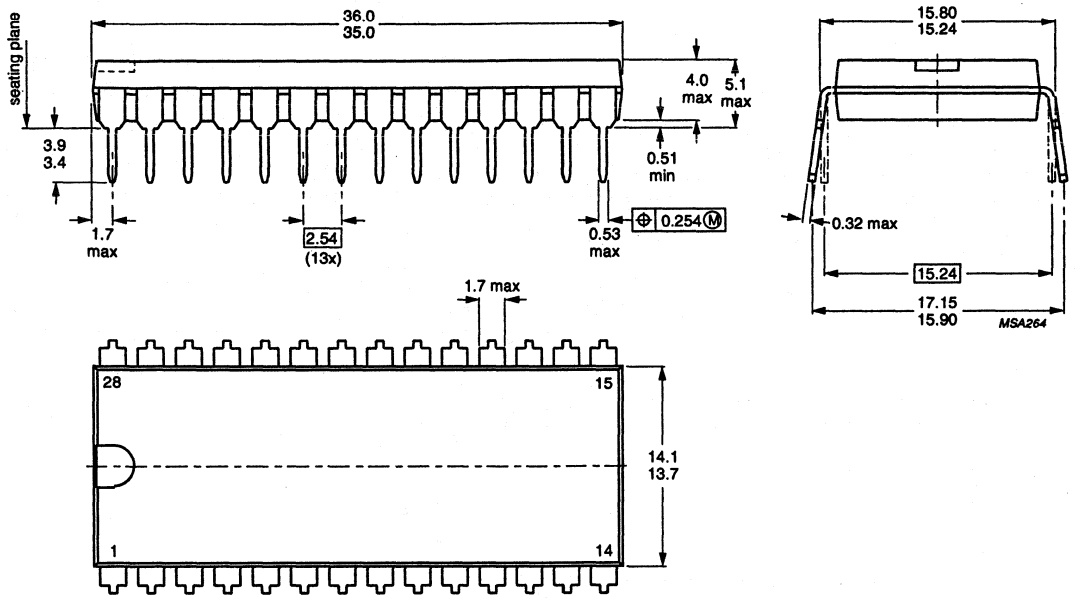
Package outlines IC02



Dimensions in mm.

Fig.58 Shrink dual in-line, plastic, 32-pin (DIL32SHR) (SOT232AG).

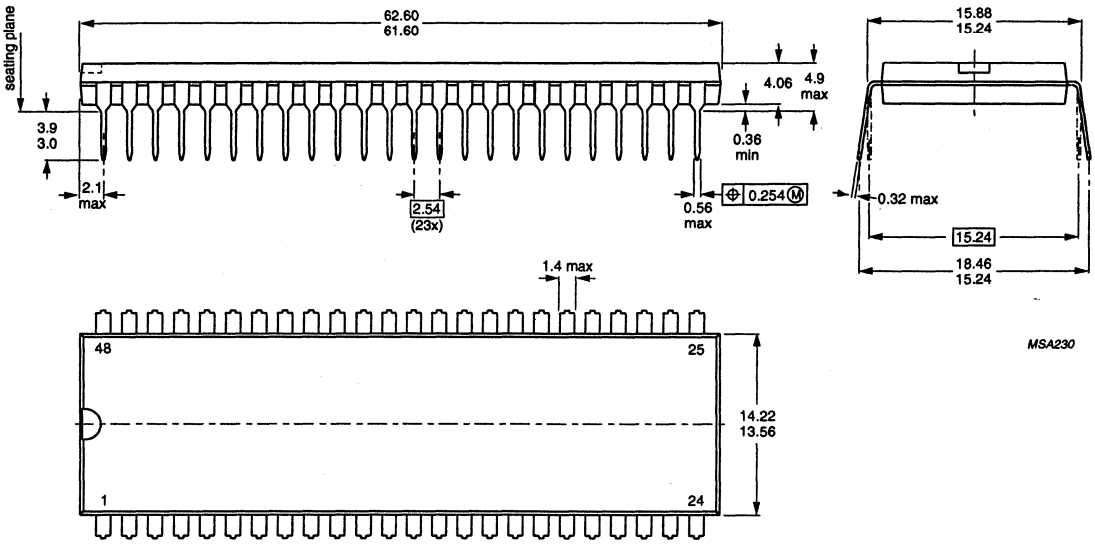
Package outlines IC02



Dimensions in mm.

Fig.59 Shrink dual in-line, plastic, 24-pin (DIL24SHR) (SOT234AG).

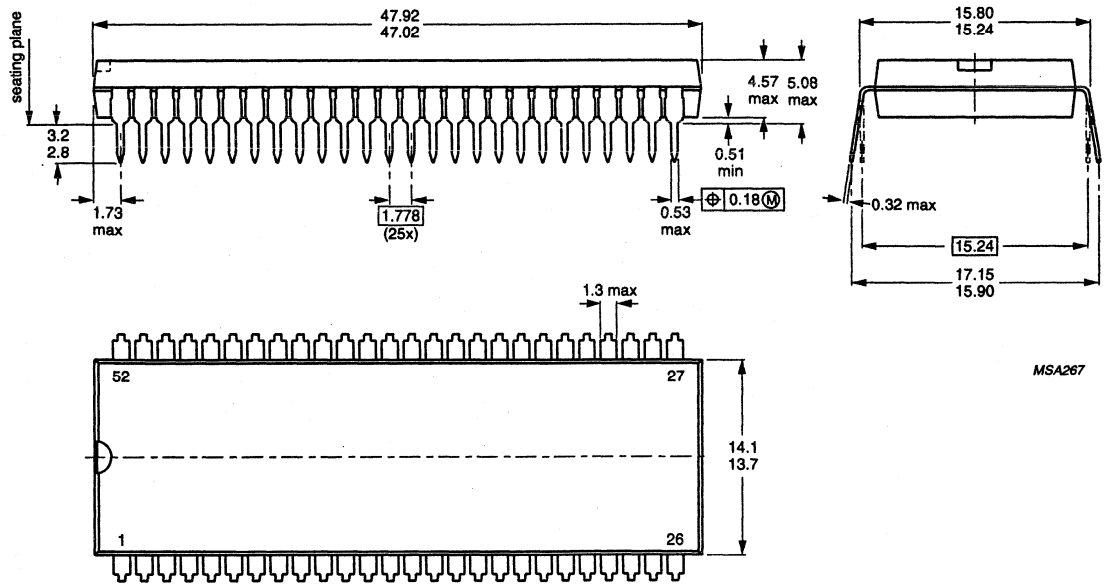
Package outlines IC02



Dimensions in mm.

Fig.60 plastic DIL, 48-pin (DIL48) (SOT240A).

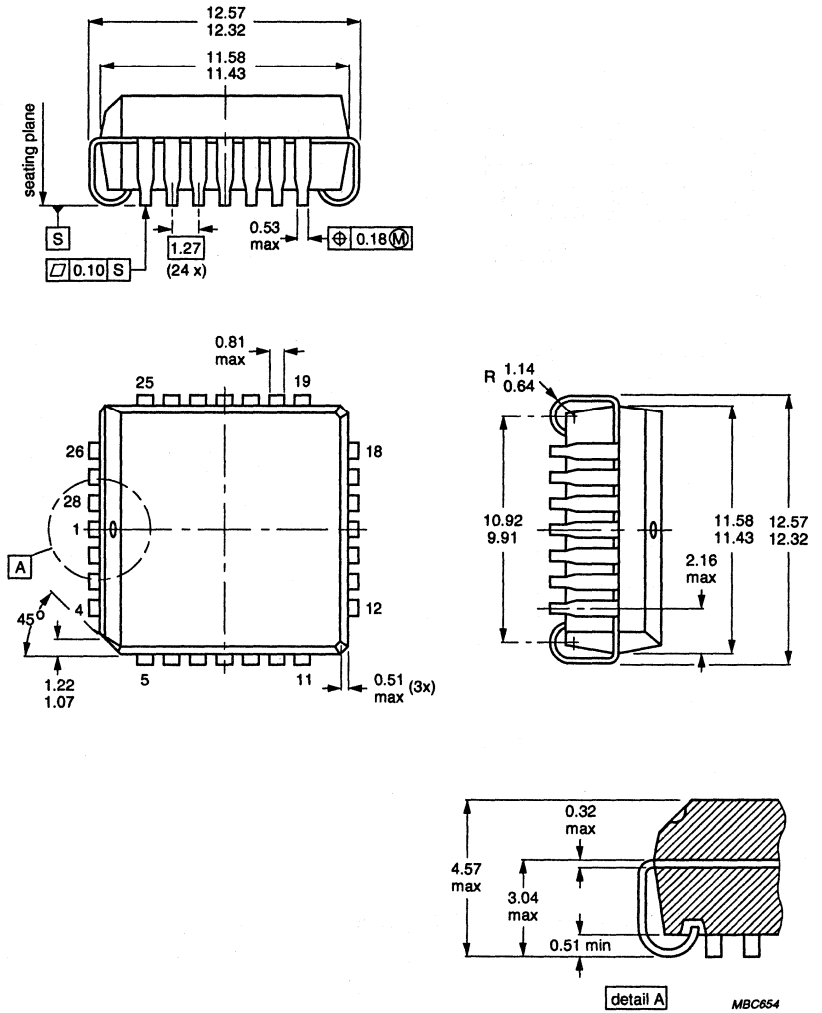
Package outlines IC02



Dimensions in mm.

Fig.61 plastic shrink DIL, 52-pin (DIL52SHR) (SOT247AG).

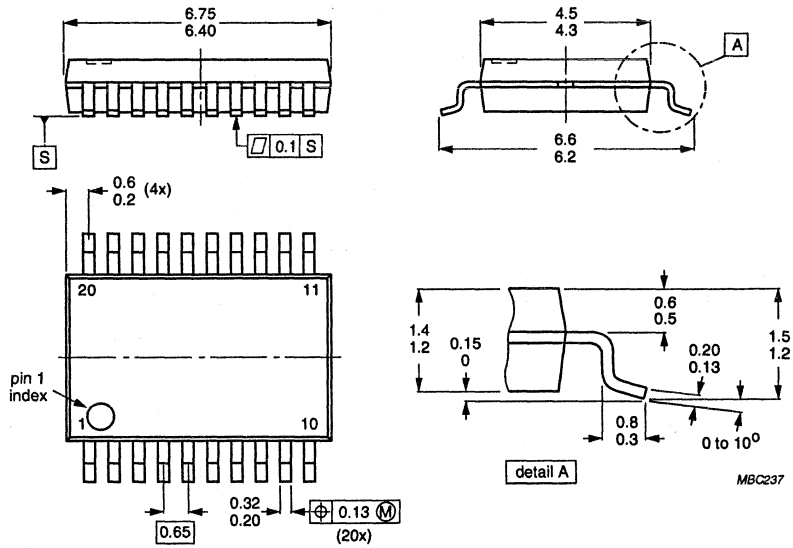
Package outlines IC02



Dimensions in mm.

Fig.62 Plastic leaded chip carrier, 28-lead (PLCC28) (SOT261CG).

Package outlines IC02



Dimensions in mm.

Fig.63 plastic shrink SO, 20-pin (SSOP20) (SOT266AG).

SOLDERING

Plastic mini-packs, PLCC and QFP

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

SOLDERING

Tab modules

FLUXING

Use a flux that does not have to be removed, or a water-soluble flux.

SOLDERING

The reflow soldering method using a pulse-heated tool is usually suitable. Limit the soldering operation to 3 s at 250 °C at the leads.

CLEANING

Avoid cleaning if possible. If cleaning is necessary, use cold or hot water. A detergent may be added to the water. Finally rinse with de-ionized water.

Do **not** use ultrasonic cleaning methods as these may damage the inner or outer leads.

Do **not** use solvents.

NOTES

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DATA HANDBOOK SYSTEM

Data handbook system

INTRODUCTION

Our data handbook system comprises more than 65 books with subjects including electronic components, subassemblies and magnetic products. The handbooks are classified into seven series:

INTEGRATED CIRCUITS;

DISCRETE SEMICONDUCTORS;

DISPLAY COMPONENTS;

PASSIVE COMPONENTS;

PROFESSIONAL COMPONENTS;

MAGNETIC PRODUCTS;

LIQUID CRYSTAL DISPLAYS.

Data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogues are available for selected product ranges (some catalogues are also on floppy discs).

For more information about data handbooks, catalogues and subscriptions, contact one of the organizations listed on the back cover of this handbook. Product specialists are at your service and enquiries are answered promptly.

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IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Telecom Systems
IC04	CMOS HE4000B Logic Family
IC05	Advanced Low-power Schottky (ALS) Logic Series
IC06	High-speed CMOS Logic Family
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IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
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IC19	Semiconductors for Datacom: LANs, UARTs, Multi-Protocol Controllers and Fibre Optics
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IC24	Low Voltage CMOS Logic

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SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small Signal Transistors
SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
SC06	High-voltage and Switching Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10	Surface Mounted Semiconductors
SC12	Optocouplers
SC13	PowerMOS Transistors
SC14	Wideband Transistors and Wideband Hybrid IC Modules
SC15	Microwave Transistors
SC16	Wideband Hybrid IC Modules
SC17	Semiconductor Sensors

DISPLAY COMPONENTS

DC01 Colour Display Components
Colour TV Picture Tubes and Assemblies
Colour Monitor Tube Assemblies

DC02 Monochrome Monitor Tubes and Deflection Units

DC03 Television Tuners, Coaxial Aerial Input Assemblies

DC04 Loudspeakers

DC05 Flyback Transformers, Mains Transformers and General-purpose FXC Assemblies

PASSIVE COMPONENTS

PA01 Electrolytic Capacitors

PA02 Varistors, Thermistors and Sensors

PA03 Potentiometers and Switches

PA04 Variable Capacitors

PA05 Film Capacitors

PA06 Ceramic Capacitors

PA07 Quartz Crystals for Special and Industrial Applications

PA08 Fixed Resistors

PA10 Quartz Crystals for Automotive and Standard Applications

PA11 Quartz Oscillators

PROFESSIONAL COMPONENTS

PC01 High-power Klystrons and Accessories

PC02 Cathode-ray Tubes

PC03 Geiger-Müller Tubes

PC04 Photo Multipliers

PC05 Plumbicon Camera Tubes and Accessories

PC06 Circulators and Isolators

PC07 Vidicon and Newvicon Camera Tubes and Deflection Units

PC08 Image Intensifiers

PC09 Dry-reed Switches

PC11 Solid-state Image Sensors and Peripheral Integrated Circuits

PC12 Electron Multipliers

MAGNETIC PRODUCTS

MA01 Soft Ferrites

MA02 Permanent Magnets

MA03 Piezoelectric Ceramics
Specialty Ferrites

LIQUID CRYSTAL DISPLAYS

LCD01 Liquid Crystal Displays and Driver ICs for LCDs

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